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A Ku-Band Fractional- N Frequency Synthesizer with Adaptive Loop Bandwidth Control

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Abstract: This paper presents a Ku-band fractional- N frequency synthesizer with adaptive loop bandwidth control (ALBC) to speed up the lock settling process and meanwhile ensure better phase noise and spur performance. The theoretical analysis and circuits implementation are discussed in detail. Other key modules of the frequency synthesizer such as broadband voltage-controlled oscillator (VCO) with auto frequency calibration (AFC) and programable frequency divider/charge pump/loop filter are designed for integrity and flexible configuration. The proposed frequency synthesizer is fabricated in 0.13 μm CMOS technology occupying $1.14 \times 1.18 \text{ mm}^2$ area including ESD/IOs and pads, and the area of the ALBC is only $55 \times 76 \mu\text{m}^2$. The out frequency can cover from 11.37 GHz to 14.8 GHz with a frequency tuning range (FTR) of 26.2%. The phase noise is -112.5 dBc/Hz @ 1 MHz and -122.4 dBc/Hz @ 3 MHz at 13 GHz carrier frequency. Thanks to the proposed ALBC, the lock-time can be shortened by about 30% from about 36 μs to 24 μs . The chip area and power consumption of the proposed ALBC technology are slight, but the beneficial effect is significant.



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Keywords: fractional- N frequency synthesizer; phase-locked loop (PLL); adaptive loop bandwidth control (ALBC); VCO; auto frequency calibration (AFC); loop filter

1. Introduction

In radio frequency integrated circuits (RFIC), the design of frequency synthesizers has been intensively discussed over the past few decades [1,2]. As the most common frequency synthesis technology, Phase-locked loop (PLL) frequency synthesizer is widely used in wireless communication, instruments, radar/navigation and other fields [3,4]. Based on the closed-loop feedback characteristic, the oscillator's frequency is divided, and the phase of the output signal compares with the phase of the input reference signal to generate feedback and control the oscillator's frequency, resulting in a gradualness elimination of the phase error, and finally locking the oscillator's output frequency [5].

The PLL based frequency synthesizer has lots of performance advantages such as wide bandwidth, agile frequency hopping, high-frequency stability, and suitable for multi-mode multi-standard, etc. However, due to its feedback (inert) characteristics, the PLL based frequency synthesizer needs a long time to stabilize the output frequency during the frequency switching process. The transient process of the typical charge pump (CP) PLL is a damping process, to speed up the locking, it is necessary to increase the loop bandwidth. However, from the steady-state analysis, to suppress the phase noise and spur, the loop bandwidth should be reduced. It is difficult for the PLL to satisfy both requirements. So, it is of great significance to speed up the locking process and shorten the locking time without affecting the noise performance [6].

To accelerate the locking speed, there are three main technologies namely dynamic loop bandwidth [7–12], fractional- N frequency division [6,13–15], feed-forward preset [16–18], and the emerging all-digital PLL (AD-PLL) [15,19]. Fractional- N technology can increase the reference frequency so that the loop bandwidth is no longer limited by the channel bandwidth and can be a larger value, and has been widely used. The feedforward preset technology presets the tuning voltage or frequency words of the voltage-controlled oscillator (VCO) and directly oscillates near the desired synthesized frequency. The VCO suitable for presets is the key to circuit design. Since the VCO needs possess the increased function, the phase noise will inevitably deteriorate. The dynamic loop bandwidth technology has proved to be simple and easy to implement as well as low cost, achieving fast locking without affecting the phase noise. Prior state-of-the-art, such as digital frequency detector with switchable bandwidth [11], auxiliary phase detector [9] and double loop filter [8] etc., all require circuit modification of the phase-frequency detector (PFD), CP or other analog modules with a potential risk of phase noise deterioration.

This work addresses the design of a fractional- N frequency synthesizer with adaptive loop bandwidth control (ALBC). By only adding a very compact, low power digital circuit without changing any key module design of the PFD, CP, and VCO, etc., we can speed up the lock process of about 30%. Along with many well-designed key modules, the fully-integrated frequency synthesizer is fabricated in $0.13\ \mu\text{m}$ CMOS technology occupying $1.14 \times 1.18\ \text{mm}^2$ area including ESD/I/Os and pads, and the area of the ALBC is only $55 \times 76\ \mu\text{m}^2$. The rest of the paper goes as follows: Section 2 presents the architecture of the proposed frequency synthesizer, Section 3 focuses on the theoretical analysis, building blocks design and presetting number setting of the proposed ALBC, Section 4 demonstrates other key modules design of the frequency synthesizer, Section 5 reports the experimental results; finally, some conclusions are drawn in Section 6.

2. Architecture

The structure diagram of the frequency synthesizer designed in this paper is shown in Figure 1, which also had been integrated into the transceiver in Reference [4]. The frequency synthesizer is a fractional frequency synthesizer, including a PFD, a programmable CP, a programmable on-chip loop filter, a VCO, a high-speed high-speed divider-by-2, a programmable frequency divider, a Σ - Δ modulator (SDM), an AFC block, an ALBC, buffers and digital control interface (SPI) etc. An external active crystal oscillator was used as a reference frequency of the frequency synthesizer. In order to speed up the AFC, the working clock of the AFC was set at 80 MHz, while the reference clock of the PFD is 20 MHz so that the frequency division ratio is not too small and also to avoid the chip area of the on-chip loop filter from being too large.

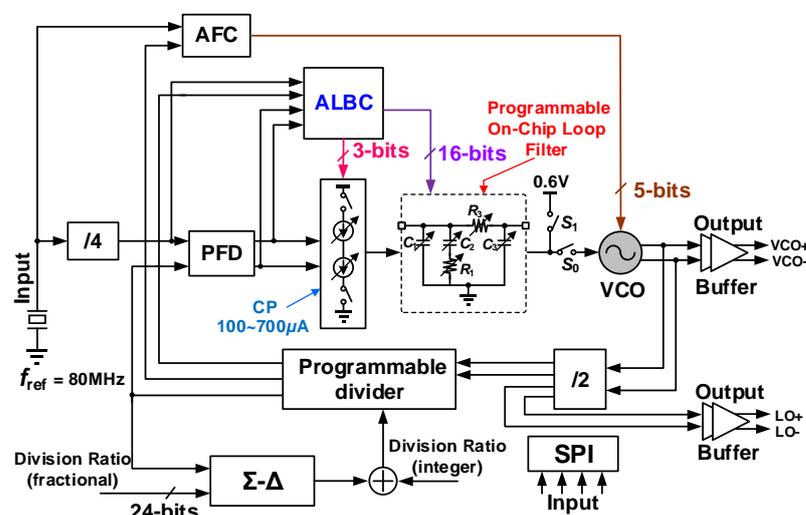


Figure 1. The block diagram of the frequency synthesizer in this paper.

The working procedure of the frequency synthesizer is disconnecting the loop filter, turning on the AFC, automatically selecting the best frequency tuning sub-band from the 32 sub-bands of the VCO, then disconnecting the AFC loop and open the PLL loop, monitoring the PLL lock state, adaptively adjust the loop bandwidth, and finally reaching the locked state.

Since the frequency synthesizer requires a large frequency range, the frequency division ratio (N) and K_{VCO} both have a relatively large changing range. However, the lock time should be changing slightly when jumping to each oscillator frequency. That means we must stabilize the loop bandwidth when the frequency synthesizer is locked at a different frequency. So, the output current of the CP and the parameters of the loop filter are programmable with a digitally-controlled set of current sources, capacitance and resistance, respectively.

Conflicts are inevitable in the loop parameters design. Large loop bandwidth can fibrilate locking quickly, while small loop bandwidth can suppress out-of-band phase noise to ensure better phase noise and spur performance after locked. To solve this contradiction, an ALBC module is designed in this paper without changing any key module such as PFD, CP, and VCO, etc. The proposed module can monitor the locking status of the frequency synthesizer. When the frequency synthesizer is far from the locked state, the CP and loop filter will be controlled by the module to set a large loop bandwidth to accelerate locking, while the frequency synthesizer is close to the locked state, the loop bandwidth is adjusted to a lower value to obtain better phase noise and spur performance.

3. Adaptive Loop Bandwidth Control

Detailed introduction of the ALBC such as theoretical analysis, circuits and algorithm implementation are present. Occupying only $55 \times 76 \mu\text{m}^2$, the ALBC unit can automatically control the loop bandwidth jump from a higher one to a lower one, resulting in a shortened locking time while ensuring better phase noise and spur performance.

3.1. Theoretical Analysis of Speed up the Locking Process with ALBC

The transfer function of the third-ordered loop filter in this paper can be expressed as

$$Z(s) = \frac{1}{s} \cdot \frac{(1 + R_1 C_1 s)}{R_1 R_3 C_1 C_2 C_3 s^2 + [R_1 C_1 (C_2 + C_3) + R_3 C_3 (C_1 + C_2)]s + (C_1 + C_2 + C_3)} \quad (1)$$

C_1 – C_3 are capacitors in the Loop filter that with digital controlled set of capacitance, while R_1 and R_3 are potentiometers with digital controlled set of resistance in Figure 1. The open-loop transfer function of the frequency synthesizer is

$$H_{open}(s) = K_{cp} \cdot Z(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} = \frac{I_{cp}}{2\pi} \cdot Z(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N}, \quad (2)$$

where K_{cp} and K_{VCO} are the gain of CP and the tuning gain of VCO respectively, I_{cp} is the output current of the CP, N is the frequency division ratio supplying by the divider-by-2 and programmable frequency divider.

The closed-loop transfer function of the frequency synthesizer is

$$\begin{aligned} H_{close}(s) &= \frac{N \cdot H_{open}(s)}{1 + H_{open}(s)} = \frac{N I_{cp} K_{VCO} Z(s)}{2\pi N s + I_{cp} K_{VCO} Z(s)} \\ &= \frac{N I_{cp} K_{VCO} (1 + R_1 C_1 s)}{2\pi N [R_1 R_3 C_1 C_2 C_3 s^4 + [R_1 C_1 (C_2 + C_3) + R_3 C_3 (C_1 + C_2)]s^3 + (C_1 + C_2 + C_3)s^2] + I_{cp} K_{VCO} (1 + R_1 C_1 s)}. \end{aligned} \quad (3)$$

Ignoring the third-order and fourth-order terms in the formula which have little effect on lock time, so Formula (3) can be simplified as

$$H_{close}(s) = \frac{\frac{I_{cp}}{2\pi} \frac{K_{VCO}}{(C_1 + C_2 + C_3)} (1 + R_1 C_1 s)}{s^2 + \frac{1}{N} \frac{I_{cp}}{2\pi} \frac{K_{VCO}}{(C_1 + C_2 + C_3)} R_1 C_1 s + \frac{1}{N} \frac{I_{cp}}{2\pi} \frac{K_{VCO}}{(C_1 + C_2 + C_3)}}. \quad (4)$$

Equation (4) is a typical second-order system, which can be written as

$$H_{close}(s) = \frac{N(2\zeta\omega_n s + \omega_n^2)}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{5}$$

where ω_n is the natural frequency, ζ is the damping coefficient. Both of them can be written as

$$\omega_n = \sqrt{\frac{I_{cp}K_{VCO}}{2\pi(C_1 + C_2 + C_3)N}} \approx \sqrt{\frac{I_{cp}K_{VCO}}{2\pi C_1 N}} \tag{6}$$

$$\zeta = \frac{R_1 C_1}{2} \sqrt{\frac{I_{cp}K_{VCO}}{2\pi(C_1 + C_2 + C_3)N}} \approx \frac{R_1}{2} \sqrt{\frac{I_{cp}K_{VCO}}{2\pi C_1 N}}. \tag{7}$$

When the frequency synthesizer jumps from the lock frequency f_1 to the lock frequency f_2

$$f_2 = (N + \Delta N)f_{ref,PFD} = f_1 + \Delta f = Nf_{ref,PFD} + \Delta f = N(f_{ref,PFD} + \frac{\Delta f}{N}) \tag{8}$$

It can be seen from (8), the frequency division ratio jump ΔN is equivalent to the reference frequency jump of the PFD. It is worth noting that although the frequency division ratio changes, the corresponding loop bandwidth will also change. Under normal circumstances, ΔN is much less than N , so the equivalent is acceptable. The relationship between the input phase of the frequency synthesizer (the phase of the reference frequency of the PFD) and the output phase (the phase of the VCO output frequency), which can be expressed as $\theta_{VCO}(s) = H_{close}(s) \cdot \theta_{ref,PFD}(s)$, so

$$\Delta F_{VCO}(s) = s \cdot \theta_{VCO}(s) = H_{close}(s) \cdot s \cdot \theta_{ref,PFD}(s) = H_{close}(s) \cdot \Delta F_{ref,PFD}(s). \tag{9}$$

The reference frequency jump $\Delta f/N$, can be regarded as adding a frequency step signal $\Delta f/N$ to the input of the frequency synthesizer. $\Delta F_{ref,PFD}(s)$ in Equation (9) can be written as the Laplace transform of the frequency step signal

$$\Delta F_{ref,PFD}(s) = \frac{\Delta f}{N \cdot s}. \tag{10}$$

From Equations (5), (9) and (10), the step response of frequency locking can be obtained as

$$\varepsilon(t) = \begin{cases} -e^{-\zeta\omega_n t} \left[\cos(\omega_n t \sqrt{1-\zeta^2}) - \frac{\zeta}{\sqrt{1-\zeta^2}} \sin(\omega_n t \sqrt{1-\zeta^2}) \right] & (0 < \zeta < 1) \\ e^{-\omega_n t} (1 - \omega_n t) & (\zeta = 1) \\ -e^{-\zeta\omega_n t} \left[\cos(\omega_n t \sqrt{\zeta^2-1}) - \frac{\zeta}{\sqrt{\zeta^2-1}} \sin(\omega_n t \sqrt{\zeta^2-1}) \right] & (\zeta > 1) \end{cases}, \tag{11}$$

$\varepsilon(t)$ is defined as the instantaneous frequency variation. Since PLL is usually a damped system, $0 < \zeta < 1$, when ε reaches an acceptable frequency error, the lock time can be expressed as

$$T_{lock} = \frac{\ln\left(\frac{\Delta f}{\varepsilon\sqrt{1-\zeta^2}}\right)}{\zeta \cdot \omega_n}. \tag{12}$$

From Equation (5), the loop bandwidth can be expressed as $\omega_c = 2 \cdot \zeta \cdot \omega_n$, so the lock time can be further expressed as

$$T_{lock} = \frac{2 \cdot \ln\left(\frac{\Delta f}{\varepsilon\sqrt{1-\zeta^2}}\right)}{\omega_c}, \tag{13}$$

where the loop bandwidth $\omega_c = \frac{I_{cp} \cdot K_{VCO} \cdot R_1 \cdot C_1}{2\pi \cdot N \cdot (C_1 + C_2 + C_3)}$.

According to Equation (13), the ALBC module designed in this paper automatically controls I_{cp} and RC in the loop filter to set the loop bandwidth to a higher value when the PLL is far away from the locked state to speed up the locking process, while lower the loop bandwidth when the PLL is close to the locked state to obtain better phase noise performance.

3.2. Building Blocks of the ALBC

Figure 2 shows the block diagram of the ALBC module. The specific circuit logic is that the output of the PFD up and down are done OR operation and used as the counting window of Counter1. The clock of Counter1 is obtained by the VCO through the high-speed divider-by-2, and then through the 16/17 dual-mode divider with a frequency of about $f_{VCO}/32$. When the maximum pulse width of up or down is less than $N1$ clock cycle, Counter2 is enabled and starts counting with f_{ref} as the clock. When Counter2 continuously counts to $N2$, the state of the state machine switches and adjusts the CP current and the RC in the on-chip loop filter, so that the loop bandwidth is switched from a wide bandwidth to a narrow bandwidth.

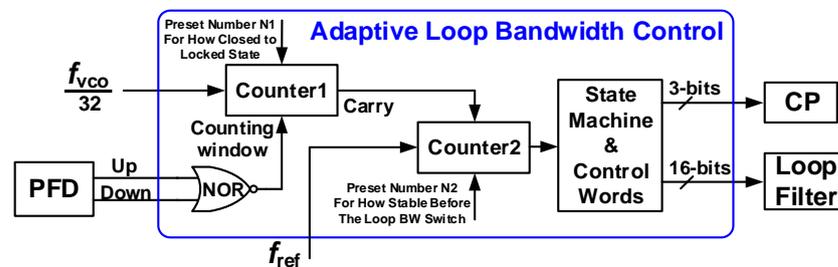


Figure 2. Block diagram of the adaptive loop bandwidth control (adaptive loop bandwidth control (ALBC)) module.

$N1$ and $N2$ are both preset numbers, which respectively represent how close to the locked state and the degree of stability required before the loop bandwidth is switched, and can be preset automatically according to the desired locked frequency.

3.3. $N1$ and $N2$ Presetting

Then, we analyze how to determine the values of the preset numbers $N1$ and $N2$ in Figure 2 based on the relationship between locking time, loop filter parameters and loop bandwidth, etc. According to the structure of the programmable frequency divider in this paper, we have the following formula

$$f_{ref,PFD} = \frac{f_{ref}}{4} = \frac{f_{VCO}}{2 \cdot [(16P + S) + F/(2^{24} - 1)]}. \tag{14}$$

When the PLL is close to the locked state, the PFD's Up and Down signal do OR operation with a narrow pulse output signal lasting for multiple $f_{ref,PFD}$ cycles, and the pulse width of the narrow pulse becomes smaller and smaller. When the PLL is far away from the locked state, after the OR operation, the output signal is not a continuous narrow pulse signal.

Suppose that after continuous M narrow pulses with a pulse width less than $\eta / f_{ref,PFD}$, the loop bandwidth ω_c changes from $2\omega_c^{set}$ to ω_c^{set} . $\eta / f_{ref,PFD}$ which can be regarded as the preset counting window of counter1 in ALBC, then

$$\frac{\eta}{f_{ref,PFD}} = \frac{N1}{f_{VCO}/32}. \tag{15}$$

From Equations (14) and (15), we can get

$$N1 = \frac{(16P + S) + F / (2^{24} - 1)}{16} \cdot \eta. \tag{16}$$

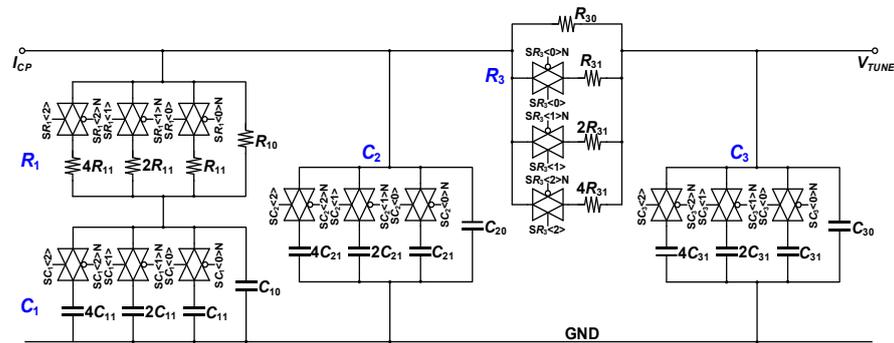
So, $N1$ is related to the selection of η . If η is too small, the preset counting window time is too short, and the counting error is relatively large. That may cause the failure to continuously output M pulses with pulse width less than $\eta / f_{ref, PFD}$, resulting in the loop bandwidth unable to switch. If η is too large, it means that the loop bandwidth is switched when it is still far away from the locked state, and the lock time will not be significantly reduced. According to the limited simulation and test results, it is estimated approximately to choose η of 5%~10%. Behavior-level modeling to speed up the simulation will make a further study to facilitate a more explicit relationship between η and locking time reduction.

The selection of $N2$ determines the required stability before the loop bandwidth is switched. The duration of M pulses with a pulse width less than $\eta / f_{ref, PFD}$ should be at least greater than one period of the natural frequency ω_n . We make $N2 / f_{ref} = 1 / \omega_n$, then

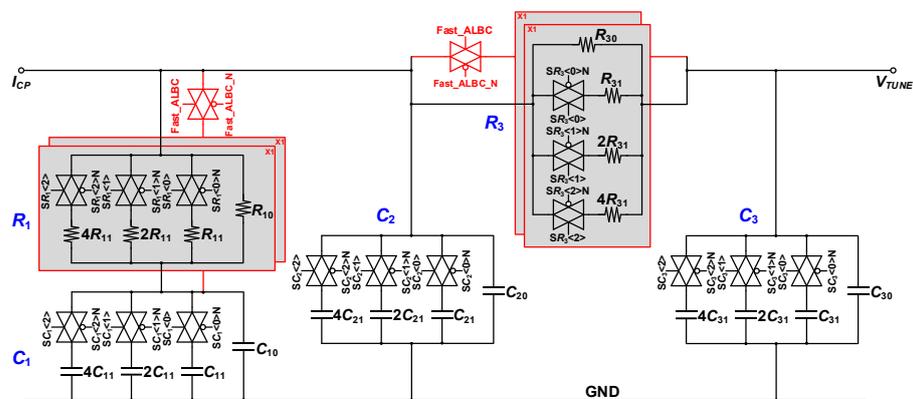
$$N2 = f_{ref} \cdot \sqrt{\frac{2\pi C_1}{I_{cp} K_{VCO}} 2 \cdot [(16P + S) + F / (2^{24} - 1)]}. \tag{17}$$

3.4. Circuits Implementation of the Loop Filter

The control range of I_{cp} is from 100 μA to 700 μA . Figure 3a shows the circuit schematic of the programmable loop filter. The resistance and capacitance are all controlled by the transmission gate to adjust the parameter value actually connected to the PLL loop. Each resistance and capacitance is controlled by a 3-bit control word.



(a)



(b)

Figure 3. (a) The schematic of the programmable loop filter, (b) the programmable loop filter adding fast loop bandwidth switch by ALBC.

In order to speed up locking more significantly, we hope that the loop bandwidth ω_c changes at least from $2\omega_c^{set}$ to ω_c^{set} controlled by ALBC. This paper adds a control word to the programmable loop filter for fast loop bandwidth switch. The schematic of the final loop filter is shown in Figure 3b.

Here we change the loop bandwidth by controlling the charge pump current and the resistors rather than the capacitors in the loop filter. That is because the capacitor is an energy storage element. In the PLL loop locking process, if we control the capacitors connecting to the loop, the capacitors would be charged, which takes time and affects the response process of the locking. If we control the capacitors disconnecting to the loop, the capacitors would be discharged, when the capacitors are connected to the loop again, it is equivalent to a step signal for the loop, which may cause a greater impact to the loop state.

In the ALBC process, the loop bandwidth ω_c is changed from $2\omega_c^{set}$ to ω_c^{set} . According to Formula (13), the I_{cp} should be changed from $4I_{cp0}$ to I_{cp0} , and R_1 should be tuned and reduced by half from R_1^{set} to $R_1^{set}/2$. In order to maintain the loop's phase margin, R_3 should be changed from R_3^{set} to $R_3^{set}/2$. In the ALBC process, the damping coefficient ζ remains unchanged, while the natural frequency ω_n becomes half of the initial state. This also shows from another perspective that the PLL can maintain stability and speed up the lock during the entire ALBC process.

4. Other Key Modules Design of the Frequency Synthesizer

4.1. Broadband VCO

A LC-VCO with a structure of all NMOS is adopted in this paper to meet the requirements of low voltage and high operating frequency. The detailed circuit schematic is shown in Figure 4. A 1-bit varactor and 4-bit capacitor arrays are used to achieve coarse frequency adjustment and a pair of varactors biased at $V_{DD}/2$ are used to achieve fine frequency adjustment [20]. Large capacitor C_{tail} , inductor L_{tail} and a low-pass filter at the mirror current source are used to optimize the phase noise of the LC-VCO. A two-stage output buffer is used to enhance the output drive capability to drive the following mixer, divider-by-2 and test pads. A self-biased structure is adopted at the first-stage output buffer to obtain higher linearity while the second-stage buffer is used to match 50 ohms.

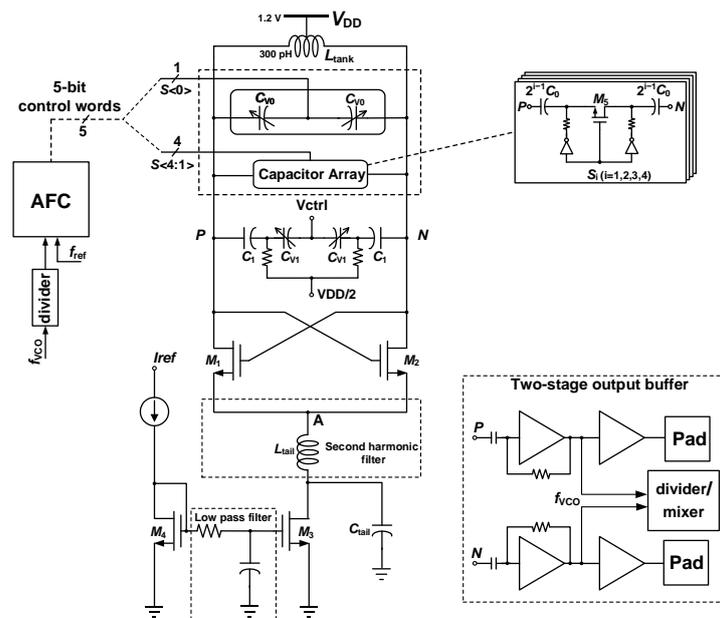


Figure 4. Schematic of the broadband LC voltage-controlled-oscillator (VCO).

Due to the higher operating frequency of the VCO, the parasitic capacitance from the switched capacitor array has a more serious impact on its oscillation frequency. To mitigate the tradeoff between the maximum oscillation frequency and the frequency tuning range, a

1-bit varactor and a 4-bit capacitor arrays is used to replace the traditional 5-bit capacitor arrays for coarse frequency adjustment. The 1-bit varactor is controlled by two voltage states of 1.2 V and 0 V. The 5-bit control word divides the VCO oscillation frequency curve into 32 sub-bands. The 5-bit control word is automatically searched and generated by the AFC according to the target frequency.

4.2. Programmable Frequency Divider

The output frequency of the frequency synthesizer is set by changing the programmable frequency divider’s division ratio. In this paper, we adopt the pulse swallowing structure to facilitate the circuits. A dual-mode frequency divider of 16/17 frequency division is used. Since the working frequency of the dual-mode frequency divider is relatively high, reaching about 7 GHz, special attention need to be paid to the circuit design. For example, it is necessary to ensure simulation results under each process corner meeting the indicator.

As shown in Figure 5, the 16/17 dual-mode frequency divider consists of three parts, a synchronous 4/5 frequency division, an asynchronous 4 frequency division, and control logic circuits. Considering that the synchronous 4/5 frequency divider with the highest operating frequency is the front stage of the 16/17 dual-mode frequency divider, the CML structure is adopted to implement it. The working frequency of the asynchronous divide-by-4 is below 2 GHz, so the TSPC structure is adopted to achieve minimizing the power consumption. Insert a logic conversion circuit between synchronous 4/5 frequency division and asynchronous four-frequency division to convert CML logic to TSPC logic.

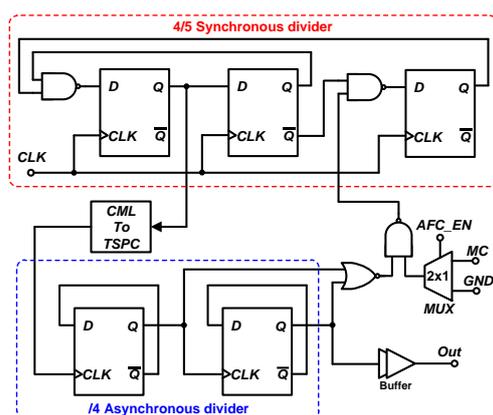


Figure 5. Schematic of the 16/17 dual-mode frequency divider.

The maximum operating frequency of the synchronous 4/5 frequency divider determines that of the 16/17 dual-mode frequency divider. Pseudo-differential CML structure is adopted for the three-D flip-flops in Figure 5, which promotes the operation frequency as well as increases the output swing. As shown in Figure 6, to reduce the time delay and further increase the operating frequency, the NAND gate is embedded into the CML logic D flip-flop. The clock and signal lines in the circuit are connected in differential form, which can effectively suppress common-mode interference signals and prevent logic mistakes.

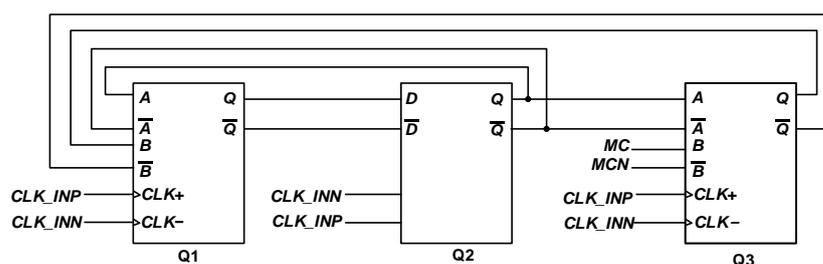


Figure 6. Schematic of the synchronous 4/5 frequency divider.

The P/S counter in the programmable divider is realized by an 8-bit synchronous counter as shown in Figure 7. The output data is edge-synchronized to avoid glitches and logic mistakes in the subsequent logic operations. On the other hand, compared with the asynchronous counter, although the structure of the synchronous counter is complex, there is no delay accumulation during asynchronous carry, so the operating frequency is higher. The combinational logic circuit in the synchronous counter restricts the maximum operation frequency and needs to be specially optimized during circuit design to reduce the delay as much as possible.

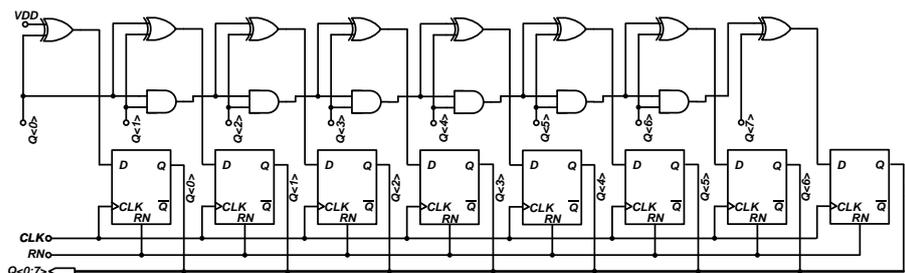


Figure 7. Eight-bit synchronous counter.

4.3. Phase Frequency Detector and Charge Pump

The PFD in this frequency synthesizer adopts the TSPC edge-triggered PFD, as shown in Figure 8. The output buffer circuit uses transmission gates and inverters as well as two cross-connected inverters at the same time to reduce the inconsistency and phase error of the differential output.

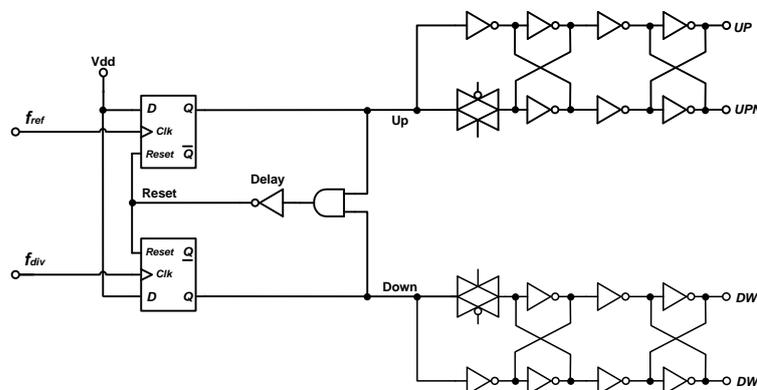


Figure 8. Schematic of the phase-frequency detector (PFD).

Due to the large output frequency range of the frequency synthesizer, the K_{VCO} of the VCO has a great change. To maintain the loop stability and facilitate the fast lock mode by ALBC, the output current of the CP is designed as a programmable parameter with a digital controlled set of current sources from 100 μ A to 700 μ A, and the adjustment step is 100 μ A. The schematic of the CP is shown in Figure 9.

The CP adopts a source switch structure to reduce the current charge sharing and injection as well as clock feed-through. The CP current is programmable of three-bit by controlling the transmission gate in the mirror path of the current mirror. The gates of the transistors in the mirror currents are affected by the up and down clock signals, and large capacitors needs to be added to stabilize the gate voltage. This large capacitor is implemented with MOS capacitors for compact chip area. Furthermore, we also draw paralleled mom capacitors above the MOS capacitors' layout.

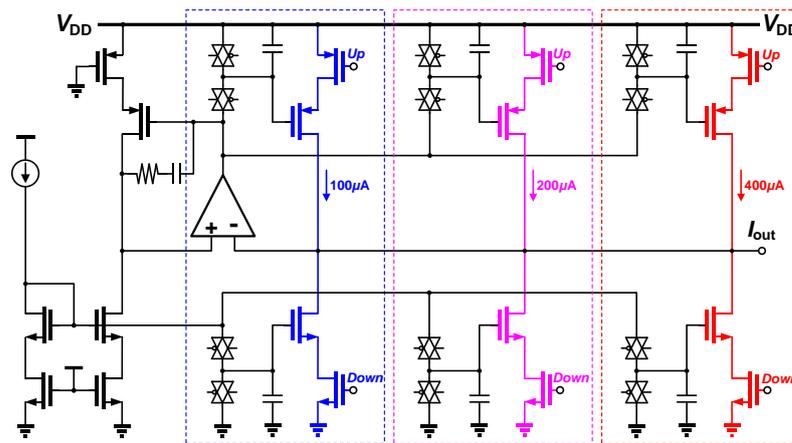


Figure 9. Schematic of the programmable charge pump (CP).

4.4. Auto Frequency Calibration

Figure 10 illustrate the detail circuit level diagram of the AFC using in Reference [20]. The counters are designed by an analog circuit design flow, while the other circuits are designed by EDA synthesizing. Due to the uncertainty of the window, the clock edge of the counter and the jitter of the clock, there is bound to be an error in the counting. To reduce the counting error, we use two counters (counter1 and counter2) counting the rising edge and the falling edge respectively, and the theoretical counting error would reduce by half.

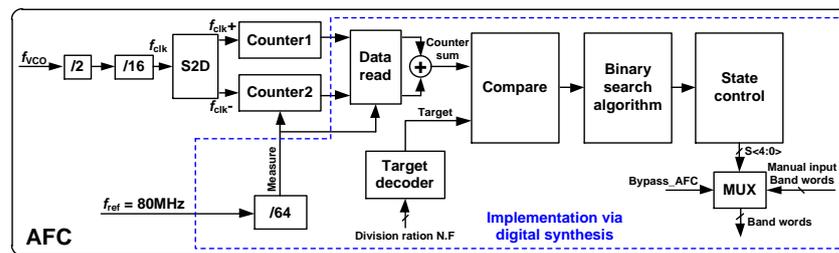


Figure 10. Structure of the proposed auto frequency calibration (AFC).

When the AFC is active, the voltage of V_{TUNE} should be fixed at $V_{DD}/2$. The $V_{DD}/2$ voltage is not suitable to be provided by a bandgap source, that is because the output of the bandgap reference source cannot have a very low impedance, resulting in common-mode noise being generated during VCO oscillation, which in turn affects the VCO, CP, frequency divider and other modules that require the bandgap to provide reference current. Even if after the end of the AFC process and the bandgap disconnecting with the V_{TUNE} of the VCO, there will still be common-mode noise entering the bandgap through the switch, and cause the deterioration of the phase noise.

We use a PMOS and two resistor to generate $V_{DD}/2$ voltage as shown in Figure 11. When the AFC works, PMOS is turned on and $V_{DD}/2$ is connected to V_{TUNE} . After the end of the AFC process, the PMOS is turned off and the connection with the V_{TUNE} is disconnected at the same time. The I_{cp} of the CP is connected to the V_{TUNE} by flowing past the entire loop filter. The $V_{DD}/2$ generating circuit is placed after the first stage filtering R_1 and C_1 of the loop filter, and before the second and third stage filtering C_2, R_3, C_3 . In this way, the noise of the $V_{DD}/2$ generating circuit will be filtered by the second-order low-pass filter.

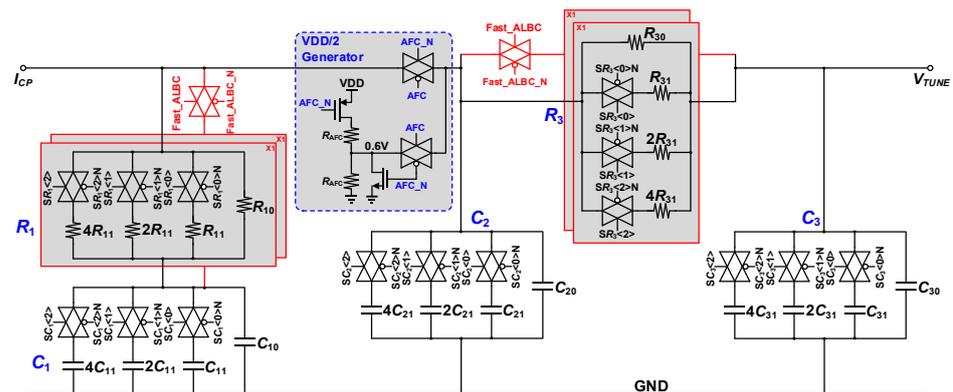


Figure 11. Programmable loop filter with embedded VDD/2 generation circuit.

5. Experimental Results

The frequency synthesizer with ALBC is prototyped in 0.13 μm CMOS technology, and the chip microphotograph is shown in Figure 12. The frequency synthesizer occupying $1.14 \times 1.18 \text{ mm}^2$ area including ESD/I/Os and pads, and the area of the ALBC is only $55 \times 76 \mu\text{m}^2$. A printed circuit board (PCB) is designed and fabricated. The chip is wire bonded and mounted on the PCB for all measurements.

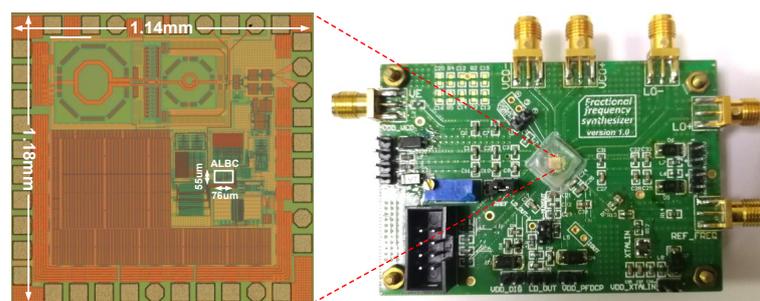


Figure 12. Chip micrograph and printed circuit board (PCB) test bench of the frequency synthesizer.

The frequency range and phase noise of the frequency synthesizer were conducted using an Agilent spectrum analyzer E4440A. The frequency covers from 11.37 GHz to 14.8 GHz with a frequency tuning range (FTR) of 26.2%. Figure 13a shows the spectrum of the frequency synthesizer at about 11.7 GHz with a power of -8.39 dBm . Figure 13b shows the spectrum at about 14.7 GHz with a power of -10.69 dBm . The power degradation is mainly caused by the loss of PCB transmission line. Figure 14 depicts that the phase noise performance of the frequency synthesizer is -112.5 dBc/Hz @ 1 MHz and -122.4 dBc/Hz @ 3 MHz at the carrier frequency of 13 GHz.

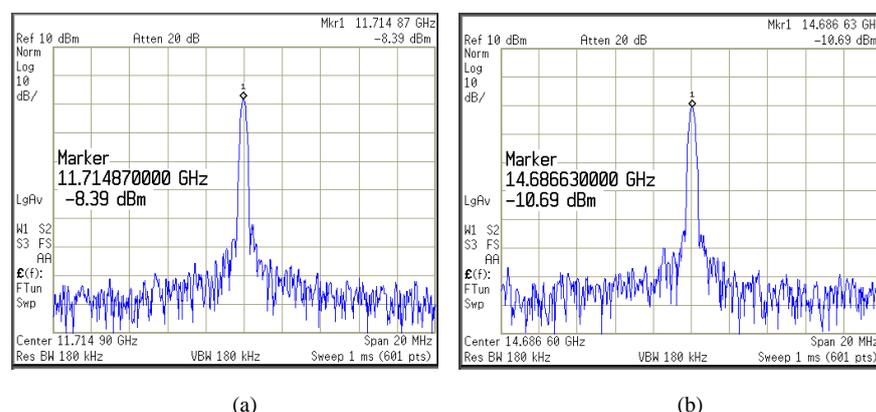


Figure 13. Measured spectrum of the frequency synthesizer (a) at about 11.7 GHz, and (b) at about 14.7 GHz.

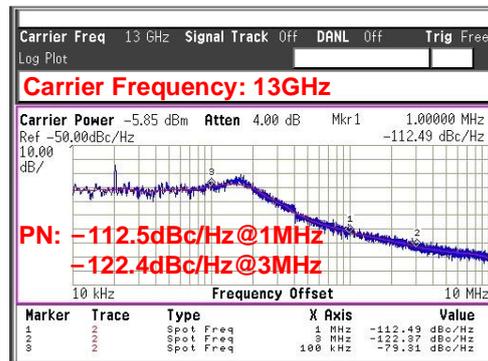


Figure 14. Measured phase noise @ 13GHz of the frequency synthesizer.

The transient behavior of the frequency synthesizer shown in Figure 15 with the VCO output frequency hopping from 12.6 GHz to 12.7 GHz in one of the 32 VCO frequency sub-bands. We can see the control voltage of the VCO is set to 0.6 V during frequency-search time, and the AFC is operating to choose an optimum sub-band with sustaining about 6 μ s. Then, the control voltage begins to fluctuate and settles to a steady-state finally. The ALBC is tuned on to automatically control the loop bandwidth from about 300 KHz when the PLL is far away from the locked state, to about 150 KHz when approaching the locked state. Figure 15 depicts that the lock-time can be shortened by about 30% from 36 μ s to 24 μ s, with the ALBC off and on respectively.

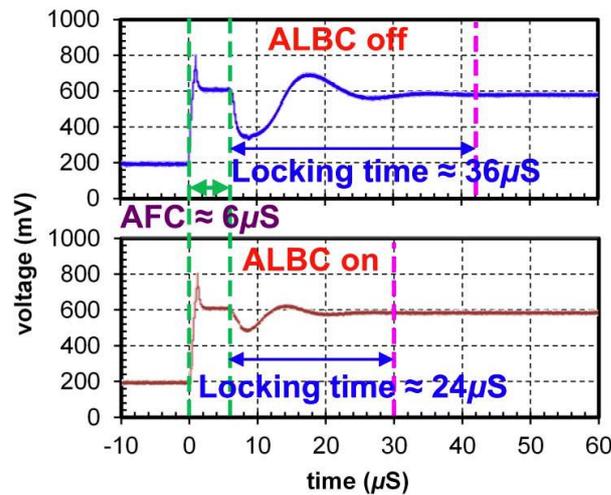


Figure 15. Measured lock-time comparison when the ALBC off/on.

A summary of the performance of the proposed frequency synthesizer and comparison with other state-of-the-arts is presented in Table 1, exhibiting high frequency, wide tuning range, low phase noise, fast locking time with slight chip area and power cost.

Table 1. Summary and compare of measurement performance of these frequency synthesizers.

	Process	Frequency (GHz)	Phase Noise (dBc/Hz)	Total Area (mm ²)	Locking Time (μs)	Improvement of Locking Time	Chip Area Cost (μm ²)
This work	0.13 μm	11.37–14.8	−112.5 @ 1 MHz −122.4 @ 3 MHz	1.14 × 1.18	24	30%	55 × 76
[6]	0.18 μm	2.368–2.469	−113.0 @ 1 MHz	1.6 × 1.3	20	75%	N/A Add 3 modules
[12]	0.18 μm	0.001–0.016	−105 @ 0.1 MHz	0.25 × 0.45	53.22	24.7%	N/A
[15]	40 nm	2.25–2.7	−109.4 @ 1 MHz −111.2 @ 30 MHz	0.0104	30	N/A	N/A
[18]	0.35 μm	0.56–0.82	−85 @ 10 KHz	0.4 (Core)	10	>90%	N/A
[19]	65 nm	1.8	−73 @ 0.4 MHz	0.35	N/A	A few μs	N/A

6. Conclusions

In this paper, a Ku-Band Fractional- N frequency synthesizer with ALBC is proposed. The ALBC unit is used to automatically control the loop bandwidth jump from a higher one when the PLL is far away from the locked state, to a lower one when the PLL approaching the locked state. As a result, we can speed up the lock settling process while ensuring better phase noise and spur performance. Theoretical analysis, building blocks of the proposed ALBC, preset number ($N1$ and $N2$) setting, and the corresponding loop filter circuits are discussed in detail. In addition, we have designed VCO, programmable frequency divider, PFD/CP, AFC and other key modules to constitute a complete frequency synthesizer. The frequency synthesizer is fabricated in 0.13 μm CMOS technology occupying $1.14 \times 1.18 \text{ mm}^2$ area including ESD/IOs and pads, and the area of the ALBC is only $55 \times 76 \text{ μm}^2$. Experimental results showed a frequency covering from 11.37 GHz to 14.8 GHz with a frequency tuning range (FTR) of 26.2%. while a phase noise of $-112.5 \text{ dBc/Hz @ 1 MHz}$ and $-122.4 \text{ dBc/Hz @ 3 MHz}$ at 13 GHz carrier frequency. By only adding a very compact, low power digital circuit without changing any other module design, the locking time, benefitting by the proposed ALBC, can be shortened by about 30% from 36 μs to 24 μs. These results demonstrated that the proposed frequency synthesizer achieves a very competitive overall performance for Ku-Band applications.

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