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Body-Effect-Free OLED-on-Silicon Pixel Circuit Based on Capacitive Division to Extend Data Voltage Range

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Abstract: This paper proposes an OLED pixel compensation circuit that copes with threshold voltage variation, narrow data voltage range, and body effect on a backplane of silicon-based transistors. It consists of six PMOS transistors and two capacitors. The data voltage range is extended by the capacitor division with two capacitors, and the connection of both source and gate nodes to the supply voltage makes the driving transistor free from the body effect. In addition, the reference voltage is used to initialize the gate node voltage of the driving transistor as well as to adjust the data voltage region. By the SPICE simulation, it is verified that the current error over the threshold voltage variations of ±10 mV is reduced to be −1.200% to 0.964% at the maximum current range of around 8 nA, and the data voltage range is extended to 3.4 V, compared to the large current error range from −21.46% to 27.36% and the data voltage range of 0.41 V in the basic 2T1C circuit. In addition, the body-effect-free circuit outperforms the latest 4T1C circuit of the current error range from −3.279% to 3.388%.

Keywords: OLEDoS; pixel compensation; threshold voltage variation; data voltage range; body effect

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1. Introduction

Recently, augmented reality and virtual reality (AR/VR) have been attracting much attention in various areas such as games [1], education [2], business [3], surgery [4], imaging [5], and tourism [6] due to their immersion and interaction [7]. These AR/VR devices consist of display, sensors, and controllers. The display shows the visual information and the virtual images; sensors including cameras, gyroscope, accelerometer, and magnetometer track the motion of the head, eyes, and hands; and controllers provide the user interface. Because the main purposes of AR/VR are to enrich the real world by overlaying virtual objects and to offer an immersive environment, a promising AR/VR set requires a high quality head-mounted display (HMD) with high resolution, high frame rate, small form factor, and high dynamic range [8]. To meet these requirements of the near-eye displays for HMD headsets, micro organic light emitting diode (OLED) displays have been widely studied and developed on a backplane of silicon-based transistors. This OLED on silicon (OLEDoS) approach can provide fast optical response, high contrast ratio, small form factor, and the full integration of display driving circuits.

On the other hand, OLEDoS displays have some challenges, including the issues of conventional active matrix OLED (AMOLED) displays on a thin film transistor (TFT) backplane [9–15]. First, because the pixels in the high resolution microdisplay of more than 3000 pixels per inch (ppi) occupy very small areas of several tens of μm^2, the current through an OLED flows at the narrow range of several nA. Therefore, the gate-source voltage (V_{gs}) of the transistor should be adjusted at a level lower than a threshold voltage (V_{th}), that is, the sub-threshold region where the current increases exponentially over V_{gs}. Due to this exponential characteristic as well as the high mobility of silicon-based transistors, the current range is covered by the substantially narrow range of the gate voltage that cannot be directly supported by the conventional digital to analog converter (DAC) in the source

driver. Second, even though the V_{th} variation of silicon-based transistors is controlled within several tens of mV, they lead to a large current difference. Therefore, even this small V_{th} variation should be compensated for. Third, whereas the silicon-based transistors are fabricated normally at the complementary metal oxide semiconductor (CMOS) backplane, the pixel circuit in the small area must be designed only with one-type transistors, n-type MOS (NMOS) transistors, or p-type MOS (PMOS) transistors due to the requirement of the additional well area for the CMOS implementation. In the end, unlike TFTs of three terminals, the CMOS transistors of four terminals experience the body effect, where the change of the source body voltage (V_{sb}) causes the V_{th} variation. Consequently, if V_{sb} is not kept at a constant level, the compensation operation cannot be accomplished perfectly.

To cope with the narrow data voltage range issue, OLEDoS pixel compensation circuits of source follower (SF) and capacitive division (CD) have been proposed. The SF architecture extends the data voltage range by a voltage gain close to 1 from the gate node to the source node [16,17], where an OLED or a diode-connected transistor is used as an active load. In addition, several diode-connected transistors are placed as an active load to scale down the effect of the data voltage by a factor of the number of stacked transistors including a driving transistor [18]. The CD method uses two capacitors to enlarge the data voltage range [19–21], where a capacitor is integrated by the metal-insulator-metal (MIM) one, and the other is implemented by the parasitic gate capacitor of the driving transistor. However, these previous approaches do not address the body effect issue. Their driving transistors have different source voltage levels at compensation and emission periods, causing the increased current error.

This paper proposes a pixel compensation circuit based on the CD scheme for a high resolution OLEDoS microdisplay. The proposed circuit extends the data voltage range and compensates for the V_{th} variation without the body effect.

2. Proposed OLEDoS Pixel Circuit

The proposed OLEDoS pixel circuit consists of six PMOS transistors (T_1, T_2, T_3, T_4, T_5, T_D) and two MIM capacitors (C_1, C_2) as shown in Figure 1a. Because the lower mobility transistors need a larger gate voltage range for a given current range, PMOS transistors are used in the proposed circuit. While T_D is a driving transistor which adjusts the current through an OLED, other transistors are used as switching transistors. There are five control signals of two previous scanning pulses ($SCAN[n-2]$, $SCAN[n-1]$), a current scanning pulse ($SCAN[n]$), and two additional ones ($COMP[n]$, $EM[n]$) with one reference voltage (V_{REF}). The timing diagram for the pixel programming is presented in Figure 1b. $ELVDD$ and $ELVSS$ are the highest and lowest supply voltages. All bodies of PMOS transistors are connected to $ELVDD$, enabling the integration in the same N-well for a small pixel area. In addition, because source and body terminals of T_D are tied to $ELVDD$, the proposed pixel circuit is free from the body effect that changes V_{th}. V_{REF} is given in between $ELVDD$ and $ELVSS$ to initialize the gate voltage of T_D via T_3 and $SCAN[n-2]$ and to adjust the region of the data voltage (V_{DATA}) driven by the source drivers via T_2 and $COMP[n]$. T_4 enables the diode connection on T_D for V_{th} compensation, and T_5 controls the connection between the drain of T_D and the anode of the OLED. Finally, C_1 and C_2 are employed to expand the range of V_{DATA} up to a supportable one by the conventional DACs of the source drivers.

The overall operation of the proposed circuit can be explained by four phases, such as initializing, V_{th}-sampling, data programming, and emitting. To secure enough time for each phase, the whole line time is allocated by using three scanning pulses as control signals.

In the initializing phase of Figure 2a, $COMP[n]$ and $SCAN[n-2]$ turn T_2 and T_3, while the other switching transistors stay in the off state. Therefore, the gate voltage of T_D and the terminals of C_2 are charged to V_{REF}. This turns T_D on as well because V_{REF} is given to be lower than $ELVDD$.

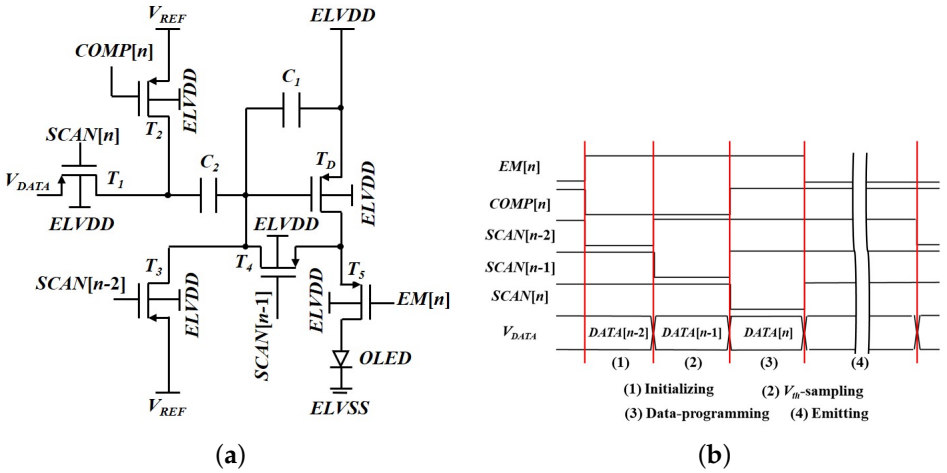

Figure 1. Proposed OLEDoS pixel circuit. (**a**) Schematic. (**b**) Timing diagram.

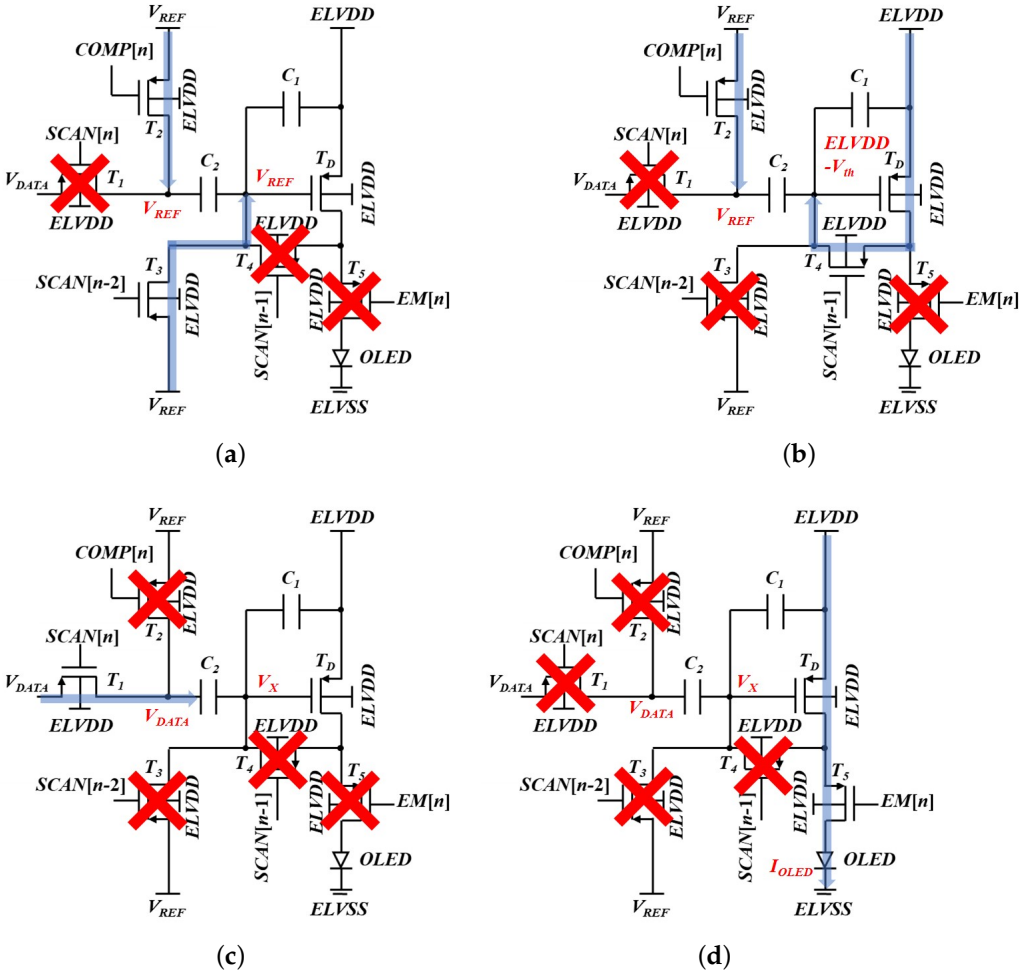

Figure 2. Operation phases of the proposed pixel circuit. (**a**) Initializing. (**b**) V_{th}-sampling. (**c**) Data programming. (**d**) Emitting.

In the V_{th}-sampling phase of Figure 2b, while T_1, T_3, and T_5 are turned off, T_2 and T_4 are turned on to hold the voltage of V_{REF} on one terminal of C_2 and to set the diode connection on T_D. Consequently, the gate voltage of T_D becomes $ELVDD - |V_{th}|$, and the voltages across C_1 and C_2 change to $|V_{th}|$ and $ELVDD - |V_{th}| - V_{REF}$. While TFTs show different threshold voltages according to operation regions, CMOS transistors have a

common threshold voltage. Therefore, the V_{th} sampled at the saturation region can be used to compensate for the variation at the sub-threshold region. The total amount of charges on C_1 and C_2 (Q_1) is described at the gate node of T_D similar to Equation (1).

$$Q_1 = -C_1 \cdot |V_{th}| + C_2(ELVDD - |V_{th}| - V_{REF}) \tag{1}$$

In the data programming phase of Figure 2c, only T_1 is turned on to charge C_2 with V_{DATA}. Because the gate node of T_D becomes a floating node without any current paths from itself, the amount of charges (Q_2) should be equal to Q_1 as shown in Equation (2), where V_X is the gate voltage of T_D. As a result, V_X is decided by the difference of V_{DATA} and V_{REF} multiplied with the ratio of C_1 and C_2 as presented in Equation (3).

$$Q_2 = C_1(V_X - ELVDD) + C_2(V_X - V_{DATA}) = Q_1 \tag{2}$$

$$V_X = ELVDD - |V_{th}| + \frac{C_2}{C_1 + C_2}(V_{DATA} - V_{REF}) \tag{3}$$

In the final emitting phase of Figure 2d, T_5 enables the programmed current to flow through the OLED as described in Equation (4), where T_D operates at the sub-threshold region in the exponential relationship between the drain current and the gate-source voltage. V_T is the thermal voltage, n is a sub-threshold slope factor between 1 and 1.5, and I_0 is a sub-threshold current. The resultant current (I_{OLED}) is independent of the variations on Vth and $ELVDD$. In addition, the voltage region of V_{DATA} is adjusted by V_{REF} to support the given range of I_{OLED}. Because the V_{DATA} is scaled by the ratio of $C_2/(C_1 + C_2)$, the smaller ratio leads to the larger V_{DATA} range over the required I_{OLED} range. Furthermore, since source and body nodes of T_D are maintained at $ELVDD$ for V_{th}-sampling and emitting phases, the V_{th} variation can be successfully addressed.

$$\begin{aligned} I_{OLED} &= I_0 \exp\left(\frac{ELVDD - V_X - |V_{th}|}{nV_T}\right) \\ &= I_0 \exp\left(\frac{C_2}{C_1 + C_2}\frac{V_{REF} - V_{DATA}}{nV_T}\right) \end{aligned} \tag{4}$$

3. Simulation Results

V_{th}, I_0, and n of PMOS transistors are -0.7688 V, 4.02×10^{-14} A, and 1.42 at a 110 nm high voltage CMOS process technology. The channel lengths and widths of T_1 to T_5 and T_D are assigned to the minimum values of 0.65 µm and 0.4 µm, respectively. The transfer curve of a PMOS transistor is presented in Figure 3. C_1 and C_2 are 26 fF and 4 fF. While $ELVDD$ and $ELVSS$ are set to 7 V and 0 V, V_{REF} is assigned to 4 V. The pixel circuit simulation is conducted over an FHD (1920 × 1080) display at a 60 Hz frame rate by the simulation program with integrated circuit emphasis (SPICE). The maximum I_{OLED} is assumed to be around 8 nA to support a luminance of up to 2000 cd/m^2 in a blue OLED presented in Figure 4, where the sub-pixel area is assumed to be 3 µm × 9 µm. These simulation parameters and target display specifications are summarized in Table 1.

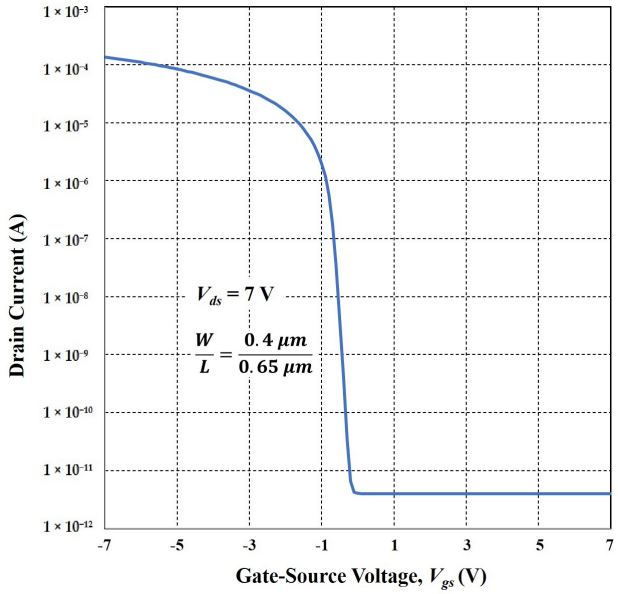

Figure 3. Transfer curve of a PMOS transistor used in the simulation.

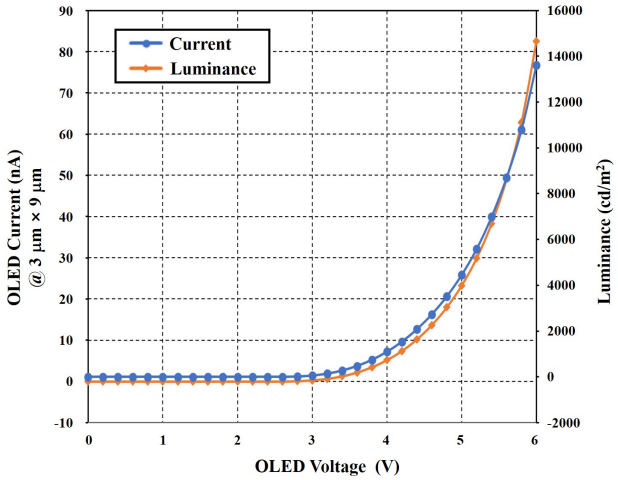

Figure 4. Current and luminance plots of a blue OLED at the sub-pixel area of 3 μm × 9 μm.

Table 1. Simulation parameters.

Simulation Parameters	Value
V_{th}	−0.7688 V
n @ sub-threshold	1.42
I_0 @ sub-threshold	4.02×10^{-14} A
Channel Length	0.65 μm
Channel Width	0.4 μm
C_1	26 fF
C_2	4 fF
$ELVDD/ELVSS$	7 V/0 V
V_{REF}	4 V
Maximum I_{OLED}	8 nA
Frame Rate	60 Hz @ FHD

The proposed pixel circuit is compared with a basic pixel circuit of a switching transistor, a driving transistor, and a capacitor (2T1C) as well as the latest CD circuit of three switching transistors, one driving transistor, and one capacitor (4T1C) [21]. Because the

previous 4T1C circuit was implemented by NMOS transistors, we have modified it into a PMOS version with C_1 of 30 fF to compare the performance as shown in Figure 5, where *ELVDD* and *ELVSS* are 7 V and 0 V. In addition, one more supply voltage (*VDD*) of 4 V is connected to body terminals of all PMOS transistors in the 4T1C circuit similar to its NMOS transistor version, in which all body terminals of transistors are connected to the ground of the voltage higher than the lowest negative supply voltage. W/L of all transistors is fixed at 0.4 µm/0.65 µm. While the proposed pixel circuit assigns the separate full line times to initializing, sampling, and programming, the 4T1C scheme should finish them within a line time. Therefore, the proposed 6T1C can secure enough charging time for each operation step. However, more transistors in the proposed one lead to a larger circuit area than the 4T1C circuit. The simulation has been conducted at a condition in which the maximum I_{OLED} is around 8 nA, and the gamma of a display is 2.2. The differences between V_{DATA} and its maximum are depicted in Figure 6 for three pixel circuits. The V_{DATA} ranges of the proposed and latest ones are substantially extended to 3.4 V and 3.6 V, compared to 0.41 V of 2T1C.

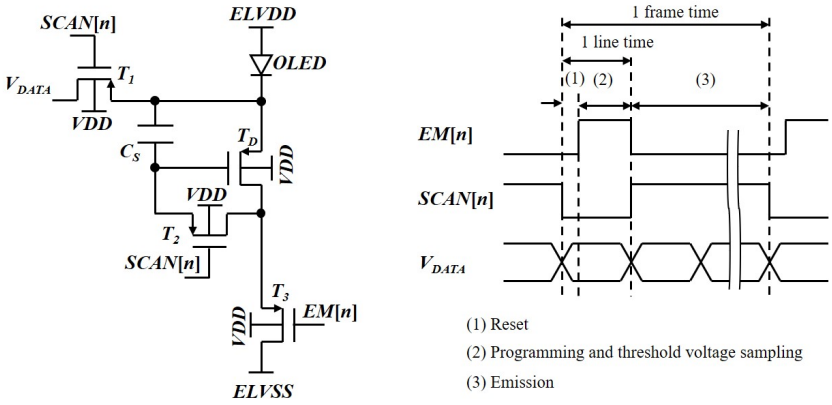

Figure 5. PMOS transistor version of 4T1C pixel circuit and timing diagram.

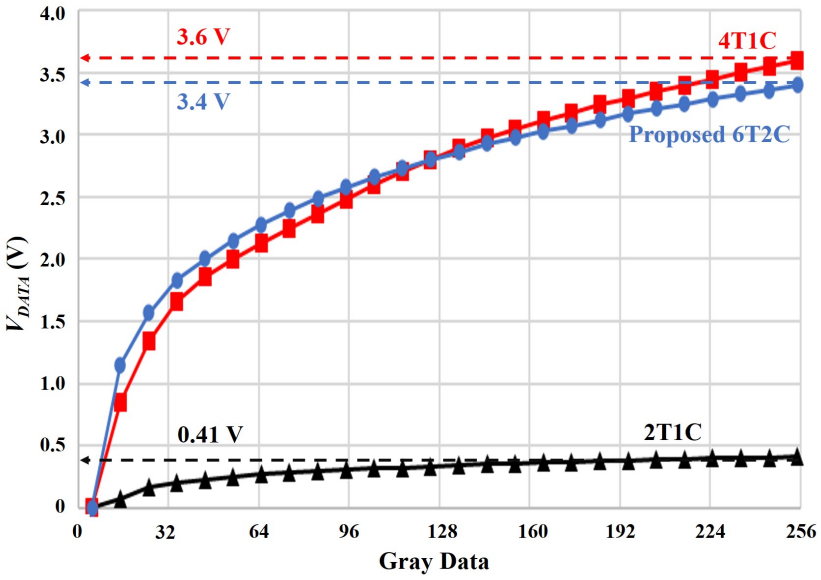

Figure 6. Extended V_{DATA} ranges of 6T2C and 4T1C circuits, compared to the narrow one of the 2T1C circuit.

In addition to the extended V_{DATA} range, the compensation performances over the V_{th} variation (ΔV_{th}) of ±10 mV are evaluated for 2T1C, 4T1C, and the proposed 6T2C circuits. While the 2T1C circuit shows large current errors between −21.46% and 27.36%,

as illustrated in Figure 7a, the 4T1C circuit achieves reduced errors between −3.279% and 3.388%, as shown in Figure 7b. Furthermore, the proposed 6T2C pixel circuit reduces the errors into a much smaller range between −1.200% and 0.964%, as presented in Figure 7c. Table 2 compares the performances of previous OLEDoS pixel circuits along with the proposed one. By sacrificing the pixel circuit area due to the large number of transistors, the proposed circuit shows a small current error as well as a wide V_{DATA} range without the body effect, along with the assignment of the full line time to all initializing, sampling, and programming.

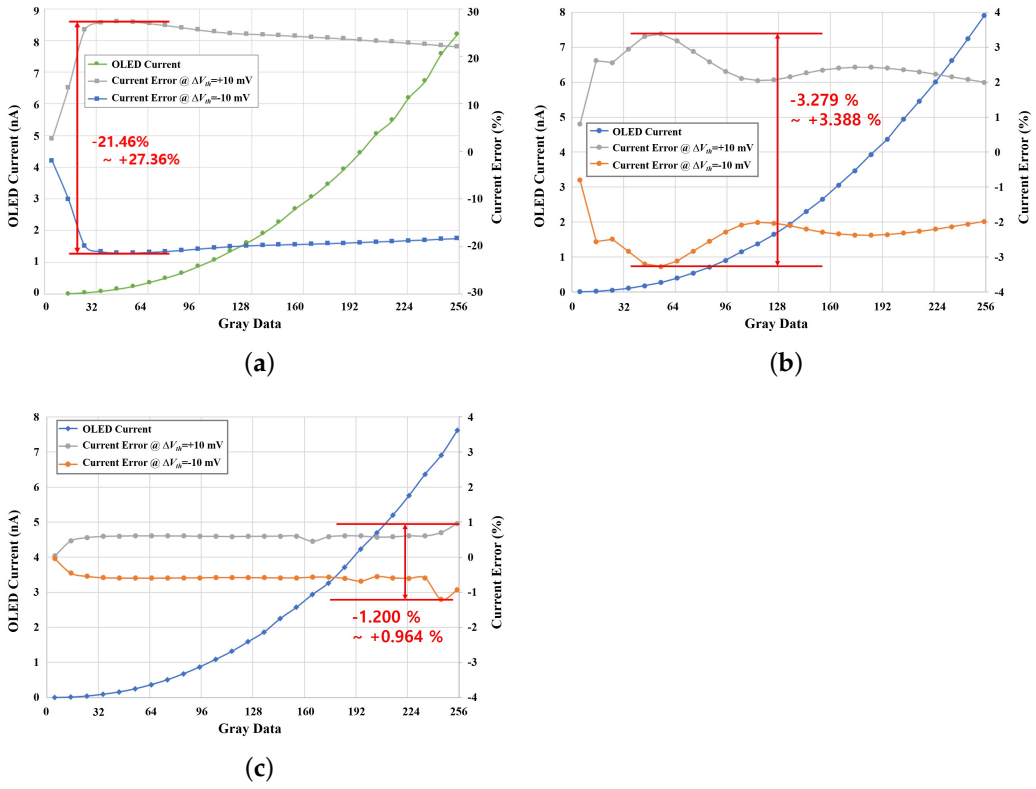

Figure 7. OLED currents and current errors over gray data. (**a**) 2T1C circuit. (**b**) 4T1C circuit. (**c**) Proposed 6T2C circuit.

Table 2. Performance summary and comparison. All pixel circuits have been designed with PMOS transistors of 0.4 µm/0.65 µm and re-simulated with the same SPICE model parameters.

	2T1C	4T1C [21]	This Work (6T2C)
V_{DATA} Range	0.41 V	3.6 V	3.4 V
V_{DATA} Region Control	Not Applicable	Not Applicable	Separate V_{REF}
I_{OLED} Error	−21.46% to 27.36%	−3.279% to 3.388%	−1.200% to 0.964%
Body Effect	No	Yes	No

4. Conclusions

We demonstrate a body-effect-free OLEDoS pixel circuit for high resolution HMDs that compensates for V_{th} variations and extends the V_{DATA} range. The V_{DATA} range is adjusted by the ratio of two MIM capacitors, C_1 and C_2, and the separate V_{REF} is applied to control the V_{DATA} region. The proposed 6T2C circuit achieves a smaller current error range from −1.200% to 0.964% at the V_{th} variations of ±10 mV in comparison to the range from −21.46% to 27.36% of the basic 2T1C circuit. Furthermore, the proposed body-effect-free structure outperforms the latest 4T1C circuit of the current error range from −3.279% to 3.388%. The V_{DATA} range is also enlarged to 3.4 V, which is similar to 3.6 V of the 4T1C

circuit, compared to 0.41 V of the basic 2T1C circuit. Consequently, the proposed OLEDoS pixel circuit can contribute to realizing high resolution HMDs for immersive and high quality AR/VR applications sooner.

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