# High-Speed Column Driver IC Having Buffer Amplifier with Embedded Isolation Switch and Compact Adaptive Biasing for Flat-Panel Displays 

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Citation: Kim, H.-R.; An, C.-H.; Kong, B.-S. High-Speed Column Driver IC Having Buffer Amplifier with Embedded Isolation Switch and Compact Adaptive Biasing for Flat-Panel Displays. Electronics 2021, 10, 2309. https://doi.org/10.3390/ electronics10182309

Academic Editor: Anna Richelli

Received: 8 August 2021
Accepted: 17 September 2021
Published: 20 September 2021

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#### Abstract

A high-speed column driver IC with an area-efficient high-slew-rate buffer amplifier is proposed for use in a large-sized, high-resolution TFT-LCD panel application. In the proposed architecture, explicit isolation switches have been embedded into the buffer amplifier resulting in a fast settling response. The amplifier also has a structure that adjusts the tail current of the input stage using a very compact adaptive biasing. The proposed column driver IC, having the proposed buffer amplifier for driving a 55 -inch 4 K ultra-high-definition (UHD) TV panel, was fabricated in a $0.18-\mu \mathrm{m} 1.8-\mathrm{V}$ low-voltage, $1.2-\mu \mathrm{m} 9-\mathrm{V}$ medium-voltage, and $1.6-\mu \mathrm{m} 18-\mathrm{V}$ high-voltage CMOS process. The performance evaluation results indicated that $90 \%$ and $99.9 \%$ falling settling times were improved from $1.947 \mu \mathrm{~s}$ to $0.710 \mu \mathrm{~s}(63.5 \%$ improvement) and $4.131 \mu \mathrm{~s}$ to $2.406 \mu \mathrm{~s}$ ( $41.7 \%$ improvement), respectively. They also indicated that the layout size of the proposed buffer amplifier was reduced from $5580 \mu \mathrm{~m}^{2}$ to $4402 \mu \mathrm{~m}^{2}$ ( $21.1 \%$ reduction).


Keywords: high-slew-rate; high-speed; settling time; low-power; buffer amplifier; adaptive biasing; column driver; source driver; flat-panel display (FPD)

## 1. Introduction

Large-sized, high-resolution, flat-panel display (FPD) monitors and TVs require lowpower, small-area, high-slew-rate amplifiers as column (data or source) drivers [1-10]. As display panels are becoming larger and require higher resolution, driving an FPD will be challenged because the driver has to drive heavy R and C panel loads more effectively, with a faster settling time, less power, and smaller area. The R and C panel loads driven by a buffer amplifier are ever increasing with the advancement of FPD technology, whereas the constraint on settling time is becoming tighter. A column driver for a large FPD typically requires receiver comparators, data registers, and shift registers, which are composed of low-voltage transistors, gamma reference voltages and digital-toanalog converters (DACs), which are composed of middle-voltage transistors, level shifters and output buffers with output-polarity switches, which are composed of high-voltage transistors [1-14]. Recently, the column driver may include a delay-locked loop (DLL) or phase-locked loop (PLL) for high-frequency operation, analog-to-digital converters (ADCs) for compensating the organic light-emitting diode (OLED) display degradation, and a temperature sensor for monitoring the ambient temperature. The driver sub-system can use either an analog $[1-12,14]$ or a digital [13] approach as its driving scheme. The thin-film transistor liquid-crystal displays (TFT-LCDs) adopt inversion driving methods (column, frame, line, dot, and 2-dot inversions) to alternate the polarities of liquid crystal (LC) cells in regard to common electrode voltage $\left(\mathrm{V}_{\mathrm{COM}}\right)$. Among various inversion methods to prevent
the deterioration of the liquid crystal material in a TFT-LCD, the dot inversion is popularly used in high-resolution displays since it can provide a high image quality. However, this type of inversion method can have higher power consumption than other methods because twice as high a driving voltage is required for reliable operation. The power consumption of the FPD column driver has been reduced by using the charge recycling (charge sharing) of adjacent odd and even output channels [15-18]. Moreover, the dot inversion method typically requires explicit components such as polarity multiplexer switches to alternate the LC polarity, which can degrade the panel driving speed. Actually, in the FPD column driver, the time for panel driving is critical since it must not exceed the horizontal scanning pattern time [19-26].

To satisfy these requirements, class AB or B amplifiers [18-26] have been widely used as output buffer amplifiers in FPDs. In this case, there can be numerous issues concerning explicit switch on-resistance, high-slew-rate amplifier design, adaptive biasing circuit design, and the resulting overheads in terms of area and power consumption. Let us describe these issues and conventional approaches to address them in more detail. As mentioned earlier, to provide high image quality, the dot inversion method requires explicit polarity multiplexer switches at buffer outputs as shown in Figure 1a. In this case, the settling time of the buffer amplifier increases due to the ON-resistance of these switches. To overcome this problem [23], proposed a driving scheme using embedded polarity multiplexer switches instead of explicit polarity multiplexer switches. In this scheme, the settling time can be enhanced but requires so many transistors for embedding the switches, resulting in an area increase. Moreover, in case of using charge recycling to reduce the power consumption [15-17], as mentioned earlier, another type of switch is required at the output of the buffer amplifiers, resulting in a settling time degradation. The class AB amplifier in [18] has been traditionally used as a buffer amplifier for FPD column drivers. Since the slew-rate of the buffer amplifier increases in proportion to the input bias current, the bias current at the input should be increased to provide a high-slew-rate operation. The authors of [24], having an interpolation structure where several input stages collectively work as a group, also adopted the buffer amplifier, performing the same operation as in [18]. This uses a 3- or 4-bit DAC-embedded operational amplifier with $\mathrm{gm}_{\mathrm{m}}$ modulation of multiple differential input stages for voltage interpolation, and implements a 10-bit DAC with buffer-reusing. A rail-to-rail class B output buffer with comparator stage was proposed in [25]. The buffer amplifier with comparator structure consumes a lot of static current in static driving such as the black (TV) or white (Note-PC) pattern of an FPD. For the buffer amplifiers in [23-25], the class AB or B configuration has its slew-rate proportional to the bias current at the input. Thus, the power consumption increases as the bias current increases to provide a higher slew-rate. The class AB amplifiers with various adaptive biasing schemes have been proposed to improve the slew-rate without having a large input bias current [21,22,26]. In [21,22], the settling time is reduced but the circuit for implementing the adaptive biasing requires so many transistors, resulting in increased power consumption and chip area. In [26], the number of transistors for implementing the adaptive biasing has been reduced from 26 to 10 as compared to [22]. However, the area overhead is not small enough since there are still many current mirror transistors used. Consequently, a high-slew-rate low-power buffer amplifier with small active area is still required for use in FPD column driver ICs.

In this paper, to address the issues mentioned above, an adaptively biased high-slewrate output buffer amplifier and a high-speed column-line driving method are proposed. We present a new driving scheme in which there are no explicit switches at the output of the buffer amplifiers to reduce the settling time and minimize the layout area. We also present a novel buffer amplifier with embedded isolation switches and a very compact adaptive biasing circuit to improve the settling time and reduce overheads in terms of chip area and power consumption. The rest of this paper is structured as follows. Section 2 presents the architecture and operation of the proposed driving scheme and buffer amplifier. Section 3
demonstrates performance comparison and evaluation results. Finally, conclusions are drawn in Section 4.


Figure 1. Conventional column driver IC with output buffer amplifiers having polarity multiplexer switches (PMUXs) and charge-sharing switches (CSSWs): (a) with output-polarity multiplexer switches (OPMUXs) and (b) with input-polarity multiplexer switches (IPMUXs) and output-isolation switches (OISWs) [2].

## 2. Proposed Driving Method and Buffer Amplifier

As shown in Figure 1a, the conventional column driver having $n$-bit R-string digital-to-analog converters (R-DACs) with multiple gamma reference voltages comprises data resisters (DRs), shift registers (SRs), data multiplexer switches (DMUXs), data latches (DLs), level shifters (LSs), positive- and negative-polarity DACs (PDACs and NDACs), positiveand negative-polarity buffer amplifiers (PAMPs and NAMPs), output-polarity multiplexer switches (OPMUXs), and charge-sharing switches (CSSWs) [16]. The OPMUXs are located at the rear of the buffer amplifiers. In [23], to avoid the ON-resistance of the OPMUXs, they have been embedded into the output stages of the buffer amplifiers. By this approach, the settling time can be improved but requires so many additional transistors (as many as 14), resulting in an area overhead. As shown in Figure 1b, the polarity multiplexer switches can be located in front of the buffer amplifiers for the same purpose [2]. The resulting inputpolarity multiplexer switches (IPMUXs) can be designed to be small without degrading the settling time, leading to an area reduction. However, as seen in Figure 1b, there is
still the need for switches after the buffer amplifiers, which are called output-isolation switches (OISWs), to prevent the sourcing and sinking of the current through the driver transistors during the charge recycling by CSSWs. Since OISWs can cause a non-negligible ON-resistance at buffer outputs in the same way as OPMUXs, the settling time cannot be improved as expected.

The schematic diagram of the proposed $n$-bit fully RDAC-based column driver is shown in Figure 2. As compared to the conventional design shown in Figure 1b, the proposed column driver has no explicit OISWs, letting the ON-resistance at buffer outputs be zero. As a result, the time constant governing the settling time at the output of the buffer amplifier will be reduced leading to a substantial improvement in the settling behaviour. Actually, the role of OISWs is embedded into the proposed buffer amplifier as will be explained later. Embedding OISWs into the buffer amplifiers in our driving scheme can also lead to an area reduction since the embedded switches can have a smaller size. The polarity multiplexer switches (PMUXs) at the outputs of the buffer amplifiers in Figure 1a are also moved to the inputs of the buffer amplifiers as in [2]. Placing PMUXs at the inputs of the buffers does not cause any degradation of the input settling behaviour since the input capacitance of the buffers is relatively small. The size of the input-polarity multiplexer switches (IPMUXs) can also be made to be small, leading to an area reduction.


Figure 2. Architecture of the proposed column driver IC with input-polarity multiplexer switches (IPMUXs) and isolation switch-embedded buffer amplifiers.

The structure of the proposed class $A B$ buffer amplifier is shown in Figure 3. As described above, the proposed driving scheme shown in Figure 2 has no explicit outputisolation switches (OSIWs) at the outputs of buffer amplifiers. Then, to allow for the output channels to perform charge recycling and not fight against the buffer output stages even without OISWs, the proposed buffer amplifier has a pair of embedded isolation switches (EISWs), MPISW and MNISW. When these switches are off, driver transistors MPD1 and MND1 are enabled and work as a normal buffer output stage. When they are on, Pup and $P d n$ are at $V D D 2$ and GND, respectively, letting the driver transistors be fully off. Note that bias voltages $V_{B P 3}$ and $V_{B N 4}$ must also be disabled during the period in which these switches are on. The EISWs can also be used for measuring the leakage of the driver transistors. On top of these merits, having no explicit isolation switches at the outputs of the buffer amplifiers can provide another important advantage of allowing bulky adaptive biasing circuits in the conventional designs to be replaced with a very compact circuit.

To see this aspect in more detail, let us consider a pair of auxiliary current sources MPT1A and MNT1A of the conventional buffer amplifier in Figure 4 [26], which provide an adaptive bias current to the input differential pair for slew-rate enhancement. Another pair of auxiliary current mirrors composed of MN7A, MP8A, MP9A, MP10A and MP7A, MN8A, MN9A, and MN10A perform the same role for the opposite type of input differential pair.

As is well known, the slew-rate improvement provided by adaptive biasing is effective while the buffer amplifier is slewing. It should be noted here that the proposed driving scheme, having no explicit series switches at buffer outputs, can provide a very high-slewrate so that the $0 \sim 90 \%$ output transition (slewing) period is much shorter than the $90 \sim 100 \%$ transition (settling) period (see the waveform referred to as 'proposed' in Figure 7). This fact implies that there is no need to use a bulky adaptive biasing circuit as conventional designs do. For example, in a conventional design [22], a very bulky adaptive biasing circuit composed of 26 transistors was used. In another conventional design [26], the number of transistors for the same purpose was reduced but still summed up to 10. Meanwhile, as shown in Figure 3, the proposed buffer amplifier uses only two auxiliary current source transistors (MPT1A and MNT1A) for enhancing the slew-rate. The bulky auxiliary current mirror circuits (MN7A, MP8A, MP9A, MP10A and MP7A, MN8A, MN9A, and MN10A) in the conventional buffer amplifier in Figure 4 are all eliminated. By this approach, the slewrate of the proposed buffer amplifier may be somewhat less than that of the conventional buffer, but the overall settling behaviour of the proposed driver IC will be even better due to there being no explicit series switches at the output of the buffer amplifier. For the conventional buffer amplifier in Figure 4, the bulky auxiliary current source circuits will be required to compensate the settling time degradation due to non-negligible ON-resistance caused by the explicit series switches at the output of the buffer.


Figure 3. Proposed class AB buffer amplifier having embedded isolation switches (EISWs) and a very compact adaptive biasing circuit.

In the proposed output buffer amplifier in Figure 3, the voltage levels of Pup and Pdn driving output transistors MPD1 and MND1 and auxiliary current sources MPT1A and MNT1A, respectively, are adjusted for a push-pull operation of the driver in conjunction with the capacitive load at the output. The greater the output capacitive $\left(\mathrm{C}_{\mathrm{L}}\right)$ load is, the larger the amount of voltage change at Pup and $P d n$ occurs. Hence, the slew-rate of the proposed output buffer amplifier becomes larger as the output capacitive $\left(\mathrm{C}_{\mathrm{L}}\right)$ load becomes heavier since the buffer uses main and auxiliary current sources (MPT1/MNT1 and MPT1A/MNT1A) to generate an adaptive input bias current. The size of MPT1A (MNT1A) is about 40 times smaller than that of MPD1 (MND1) as in [26]. The threshold voltage of MPT1A (MNT1A) is also higher than that of MPD1 (MND1). This results in an auxiliary bias current of about 5 nA for MPT1A (MNT1A), which is negligibly small as compared to the bias currents of MPT1 (MNT1) ( 1.6 uA ), MP4 (MP6) and MN4 (MN6) $(2.1 \mathrm{uA})$, and MPD1 (MND1) ( 5.6 uA ). This causes almost no increase in the static power consumption of the buffer amplifier in the steady state. When there is either a large voltage
step at the input or a heavy capacitive load at the output of the buffer, the voltage of Pup (Pdn) changes from its nominal value to near GND (VDD2). Then, the amount of current flowing through the auxiliary current source MPT1A (MNT1A) increases considerably resulting in a substantial increase in the slew-rate. When the incoming input voltage swing is small, Pup ( $P d n$ ) will have a small voltage change, resulting in a small or no current through MPT1A (MNT1A).


Figure 4. Conventional slew-rate-enhanced buffer amplifier with adaptive biasing [26].
Considering the theoretical point of view, the rising and falling slew-rates of the proposed buffer amplifier can be written as

$$
\begin{align*}
& \frac{d V_{\text {out_rise }}}{d t}=\frac{\mathrm{I}_{\mathrm{MPT1}}+\mathrm{I}_{\mathrm{MPT1A}}}{\mathrm{C}_{\mathrm{C}}}  \tag{1}\\
& \frac{\mathrm{dV}_{\text {out_fall }}}{\mathrm{dt}}=\frac{\mathrm{I}_{\mathrm{MNT1}}+\mathrm{I}_{\mathrm{MNT1A}}}{\mathrm{C}_{\mathrm{C}}} \tag{2}
\end{align*}
$$

where $\mathrm{I}_{\text {MPT1 }}$ and $\mathrm{I}_{\mathrm{MNT1}}$ are the base tail currents, $\mathrm{I}_{\mathrm{MPT1A}}$ and $\mathrm{I}_{\text {MNT1A }}$ are the auxiliary tail currents, and $C_{C}$ is the compensation capacitor. As described earlier, when a large voltage change occurs at the input, either $\mathrm{I}_{\text {MPT1A }}$ or $\mathrm{I}_{\mathrm{MNT1A}}$ increases fast, resulting in a substantially increased slew-rate. The settling time at the output of the buffer amplifier can be expressed as

$$
\begin{equation*}
\mathrm{V}_{\text {out }}(\mathrm{t})=\mathrm{V}_{\mathrm{ip}}\left(1-\mathrm{e}^{-\frac{\mathrm{t}}{\tau}}\right) \tag{3}
\end{equation*}
$$

where $V_{i p}$ is the step-input voltage and $\tau$ is the time constant of the network. In the conventional schemes shown in Figure 1, $\tau$ will be (RON-DRIVER + RON-SWITCH + RESD).CLOAD where RON-DRIVER is the ON-resistance of a driver transistor in the buffer amplifier, RON_SWITCH is the ON-resistance of an explicit switch at buffer output, RESD is the electrostatic discharge (ESD) protection resistor, and CLOAD is the capacitive load at the pad. On the other hand, the settling time for the proposed scheme shown in Figure 2 is determined by a time constant $(\tau)$ of (RON-DRIVER + RESD).CLOAD. Considering that the ON-resistance of the explicit switch has a substantial portion of the total resistance value, having no explicit switches at buffer outputs is important for speeding up the settling time.

In summary, the proposed column-line driving scheme can provide an improved settling behaviour by having no explicit series switches at the outputs of the buffer am-
plifiers. This feature has been achieved by having embedded isolation switches (EISWs) in the proposed buffer amplifier and by moving OPMUXs to the inputs of the buffer. By doing so, the active area can also be reduced since the size of these switches can be made to be smaller. On top of having EISWs, the proposed output buffer amplifier has an area-efficient adaptive biasing circuit composed of just two extra transistors for enhancing the slew-rate. As mentioned earlier, the conventional designs in $[22,26]$ used as many as 26 and 10 extra transistors, respectively, for the same purpose. The compact design of the proposed buffer amplifier allows our driving scheme to be more area- and energy-efficient with substantially improved settling performance.

## 3. Experimental Results

A column driver IC, having the proposed driving scheme and output buffer amplifier, was fabricated in a $0.18-\mu \mathrm{m} 1.8-\mathrm{V}$ low-voltage, $1.2-\mu \mathrm{m} 9-\mathrm{V}$ medium-voltage, and $1.6-\mu \mathrm{m} 18-\mathrm{V}$ high-voltage CMOS process. Figure 5 shows a chip photograph of the column driver IC and a layout picture of a pair of the proposed buffer amplifiers, which occupy areas of $17,368 \times$ $888 \mu \mathrm{~m}^{2}$ and $142 \times 31 \mu \mathrm{~m}^{2}$, respectively. Figure 6 shows measured output buffer waveforms for a full-swing white pattern in dot inversion with charge recycling to verify the fast settling response of the proposed scheme. The driving condition for the measurement has used 8.5-K $\Omega$ and $300-\mathrm{pF}$ load of a 4 K ultra-high-definition (UHD) 55-inch TFT-LCD panel having a voltage swing of $16.6 \mathrm{~V}(0.2-16.8 \mathrm{~V})$. There is some noise in the measured waveforms due to the high sampling rate of the oscilloscope used in the measurement.


Figure 5. Chip photograph of the proposed column driver IC and layout picture of a pair of output buffer amplifiers.


Figure 6. Measured waveforms of the proposed column driver IC with charge recycling.
The simulated single-cycle transition waveforms for conventional $[18,23,26]$ and proposed output buffer amplifiers without charge recycling are comparatively shown in Figure 7. The reason for having waveforms without charge recycling is to clearly compare the settling behaviour of the buffer amplifiers. As seen in Figure 7, the settling time for the rising and falling transient responses ( $90 \%$ and $99.9 \%$ ) of the proposed output buffer amplifier is the fastest. Table 1 summarizes important performance matrices such as the static and dynamic currents, settling times ( $90 \%$ and $99.9 \%$ ), slew-rates ( $90 \%$ and $99.9 \%$ ) and active area of the conventional $[18,23,26]$ and proposed buffer amplifiers, which are obtained by a simulation in the same process technology to compare the performance in the same conditions. Measurement results are also included for the proposed design, which indicates that the measured and simulated performance are well matched to each other. As seen in Table 1, although the static and dynamic currents of the output buffer amplifier in [18] are similar to those of the proposed buffer amplifier, the setting time and slew-rate are much slower, and the active area is larger. In the case of [18], having the PMUXs at the rear of the buffer amplifier requires larger switch transistors to reduce the ON-resistance to obtain a fast transient response. The buffer amplifier in [23] has a somewhat improved settling time and slew-rate than that in [18] by embedding the PMUXs into the buffer amplifier. However, since it does not use any adaptive biasing, the settling time and slew-rate are slower than the proposed buffer. Adapting the adaptive biasing in the buffer amplifier in [26] improved the settling time and slew-rate as compared to [18,23]. The proposed buffer amplifier consumes static and dynamic currents similar to those of the buffer amplifier in [26], but due to there being no explicit switches at the output of the buffer amplifier, the settling time and slew-rate are substantially improved. The active area of the proposed buffer amplifier, having a very compact adaptive biasing circuit, is about $4402 \mu^{2}$ achieving up to $21.1 \%$ reduction as compared to conventional designs.


Figure 7. Simulated single-cycle output transition waveforms of conventional and proposed buffer amplifiers.

Table 1. Simulated and measured performance comparison of buffer amplifiers in the same process.

| Items | [18] | [23] | [26] | This work |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1994 | 2015 | 2020 |  |  |
|  | Simulated | Simulated | Simulated | Simulated | Measured |
| CMOS Process ( $\mu \mathrm{m}$ ) (Poly/Metal) | 0.18 (1P/3M) | 0.18 (1P/3M) | 0.18 (1P/3M) | 0.18 (1P/3M) | 0.18 (1P/3M) |
| Supply Voltage (V) | 1.8/9/18 | 1.8/9/18 | 1.8/9/18 | 1.8/9/18 | 1.8/9/18 |
| $\begin{gathered} \text { DC (Static) current } \\ (\mu \mathrm{A}, \mathrm{DC} 8.5 \mathrm{~V} @ 17 \mathrm{~V}) \end{gathered}$ | 11.42 | 11.43 | 11.45 | 11.44 | 11.4 |
| Operating (Dynamic) current ( $\mu \mathrm{A}, 0.2-16.8 \mathrm{~V} @ 17 \mathrm{~V}$ ) | 376.4 | 393.4 | 389.4 | 399 | 380 |
| 90\% Settling time ( $\mu \mathrm{s}$, rising/falling) | 1.817/1.947 | 1.651/1.814 | 0.989/0.991 | 0.669/0.710 | 0.59/0.62 |
| 99.9\% Settling time ( $\mu \mathrm{s}$, rising $/$ falling) | 3.943/4.131 | $3.111 / 3.081$ | 3.404/3.305 | 2.534/2.406 | 2.33/2.24 |
| 90\% Slew-rate ( $\mathrm{V} / \mu \mathrm{s}$, rising /falling) | 8.222/7.673 | 9.049/8.235 | 15.106/15.075 | 22.331/21.042 | 25.322/24.096 |
| 99.9\% Slew-rate ( $\mathrm{V} / \mu \mathrm{s}$, rising/falling) | 4.205/4.014 | 5.330/5.382 | 4.871/5.017 | 6.544/6.892 | 7.117/7.403 |
| Height area $(\mu \mathrm{m}$, cell pitch $=31 \mu \mathrm{~m})$ | 180 | 158 | 160 | 142 | 142 |
| Panel loads | $\mathrm{R}=8.5 \mathrm{~K}^{1}, \mathrm{C}=300 \mathrm{pF}^{1}$ |  |  |  |  |
| Conditions | VDD2 $=17 \mathrm{~V}, \mathrm{VSS}=0 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$, Period $=7.4 \mathrm{\mu s}^{2}$, Driving range $=0.2-16.8 \mathrm{~V}$ |  |  |  |  |

[^0]Table 2 compares the experimentally measured performance for the conventional [18,23-26] and proposed buffer amplifiers. Although the buffer having a DAC-embedded op-amp with $\mathrm{g}_{\mathrm{m}}$-modulation [24] used a driving voltage higher by 1-V (6\%) than others and a resistive load ( $3.5-\mathrm{K} \Omega$ ) smaller by $41.2 \%$ than ours, it has a slower settling time than the
proposed design. The output buffer amplifier in [25] has a slower settling time ( $99.9 \%$ rising) than the proposed buffer, even though the R and C panel loads are much smaller and the operating voltage is lower. Although the proposed output buffer amplifier consumes static and dynamic currents similar to those of the buffer amplifier in [26], due to it having no switches at buffer outputs, the $90 \%$ rising and $99.9 \%$ falling settling times are improved from $0.91 \mu \mathrm{~s}$ to $0.59 \mu \mathrm{~s}(35.1 \%$ improvement $)$ and $3.04 \mu \mathrm{~s}$ to $2.24 \mu \mathrm{~s}(26.3 \%$ improvement), respectively. As compared to the buffer amplifier in [18] widely used in the industry, the enhancements are as much as $63.5 \%$ ( $90 \%$ falling) and $41.7 \%$ ( $99.9 \%$ falling). Table 3 summarizes the corner simulation results of the proposed buffer amplifier at FF $\left(-30^{\circ} \mathrm{C}\right), \mathrm{NN}\left(25^{\circ} \mathrm{C}\right)$, and SS $\left(125^{\circ} \mathrm{C}\right)$ with 18 -V high-voltage $\mathrm{p} / \mathrm{n}$ MOSFET transistors to verify the operation robustness of the proposed scheme. Table 4 summarizes the metal-oxide-semiconductor field-effect transistor (MOSFET) device-related parameters used in our design. Figure 8 depicts the experimental setup to obtain the simulated waveforms and measured data. The top figure shows the block diagram of on-chip connectivity, and the figures in the middle and bottom show the configurations at board level, where a fivesegment distributed RC network was used for simulation and a real panel was attached for measurement.

Table 2. Measured performance of buffer amplifiers.

| Items | [18] | [23] | [24] | [25] | [26] | This work |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1994 | 2015 | 2019 | 2020 | 2020 |  |
|  | Measured |  |  |  |  |  |
| $\begin{gathered} \text { CMOS Process } \\ (\mu \mathrm{m}) \\ \text { (Poly/Metal) } \end{gathered}$ | - | $\begin{gathered} 0.18 \\ (1 \mathrm{P} / 3 \mathrm{M}) \end{gathered}$ | $\begin{gathered} 0.18 \\ (1 \mathrm{P} / 4 \mathrm{M}) \end{gathered}$ | $\begin{gathered} 0.35 \\ (2 \mathrm{P} / 3 \mathrm{M}) \end{gathered}$ | $\begin{gathered} 0.18 \\ (1 \mathrm{P} / 3 \mathrm{M}) \end{gathered}$ | $\begin{gathered} 0.18 \\ (1 \mathrm{P} / 3 \mathrm{M}) \end{gathered}$ |
| Supply Voltage <br> (V) | 2.5~6 | 1.8/7/13.5 | 1.8/9/18 | 3.3/5 | 1.8/9/18 | 1.8/9/18 |
| Number of bits | - | 8 | 10 | 10 | 8 | 8 |
| $\begin{aligned} & \text { DC (Static) } \\ & \text { current }(\mu \mathrm{A}) \end{aligned}$ | 180 | - | $7^{1}$ | - | 11.40 | 11.40 |
| Operating voltage <br> (V) | 3.3 | 10.36 | $9 / 18^{2}$ | 5 | DC 8.5 @17 | DC 8.5 @17 |
| Operating (Dynamic) current ( $\mu \mathrm{A}$ ) | - | 247 | - | - | 371 | 380 |
| 90\% Settling time ( $\mu \mathrm{s}$, rising) | - | 1.47 | - | - | 0.91 | 0.59 |
| 90\% Settling time ( $\mu \mathrm{s}$, falling) | - | 1.38 | - | - | 0.95 | 0.62 |
| 99.9\% Settling time ( $\mu \mathrm{s}$, rising) | - | $2.61{ }^{3}$ | $5.6{ }^{4,5}$ | 5.6 | 3.11 | 2.33 |
| 99.9\% Settling time ( $\mu \mathrm{s}$, falling) | - | $2.53{ }^{3}$ | - | - | 3.04 | 2.24 |
| Area ( $\mu \mathrm{m}^{2}$ ) | 4000 | $31 \times 158{ }^{6}$ | $23 \times 510$ | - | $31 \times 160{ }^{6}$ | $31 \times 142{ }^{6}$ |
| Panel loads | $\underset{\mathrm{pF}}{\mathrm{R}=10 \mathrm{~K} \Omega, \mathrm{C}=10}$ | $\begin{gathered} \mathrm{R}=3.29 \mathrm{~K} \Omega, \\ \mathrm{C}=364 \mathrm{pF} \end{gathered}$ | $\begin{aligned} \mathrm{R}= & 5 \mathrm{~K} \Omega^{5}, \mathrm{C}= \\ & 300 \mathrm{pF}^{5} \end{aligned}$ | $\begin{aligned} \mathrm{R}= & 1.5 \mathrm{~K} \Omega, \mathrm{C}= \\ & 100 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & \mathrm{R}=8.5 \mathrm{~K} \Omega, \\ & \mathrm{C}=300 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & \mathrm{R}=8.5 \mathrm{~K} \Omega, \\ & \mathrm{C}=300 \mathrm{pF} \end{aligned}$ |
| Conditions | $\begin{gathered} \mathrm{VDD}=3.3 \mathrm{~V} \\ \mathrm{~T}=27^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} \text { VDD }=10.36 \mathrm{~V} \\ \mathrm{~T}=25^{\circ} \mathrm{C}, \\ \text { Period }=7.4 \mu \mathrm{~s}^{7} \\ 0.2-10.16 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & \text { VDD }=18 \mathrm{~V} \\ & 0.2 \sim 17.8 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \mathrm{VDD}=5 \mathrm{~V} \\ & 0 \sim 4.995 \mathrm{~V} \end{aligned}$ | $\begin{gathered} \text { VDD }=17 \mathrm{~V}, \\ \mathrm{~T}=25^{\circ} \mathrm{C} \text { Period } \\ =7.4 \mu \mathrm{~s} 7 \\ 0.2-16.8 \mathrm{~V} \end{gathered}$ | $\begin{gathered} \mathrm{VDD}=17 \mathrm{~V}, \\ \mathrm{~T}=25^{\circ} \mathrm{C} \text { Period } \\ =7.4 \mu \mathrm{~s} 7 \\ 0.2-16.8 \mathrm{~V} \end{gathered}$ |

[^1]Table 3. Corner simulation results of the proposed buffer amplifier.

|  | CMOS Process Parameter <br> (High-Voltage p/n MOSFET) | Best <br> $(\mathrm{FF})$ | Typical <br> $(\mathrm{NN})$ |
| :---: | :---: | :---: | :---: |

${ }^{1}$ Period for one-line horizontal operation.
Table 4. Device parameters used in the proposed column driver IC.

| CMOS Process Parameter | LV MOSFET | MV MOSFET | HV MOSFET ${ }^{\mathbf{1}}$ |
| :---: | :---: | :---: | :---: |
| Supply voltage | 1.8 V | 9 V | 18 V |
| Transistor type | Low voltage | Medium voltage | High voltage |
| Minimum length | LVP/LVN | MVP/MVN | HVP/HVN |
|  | $0.18 \mu \mathrm{~m}$ | $1.2 \mu \mathrm{~m}$ | $1.6 \mu \mathrm{~m}$ |
| Application block | Receiver (Comparator), DRs | R-DACs | Output Buffers |
|  | (Deserializers), DLL, SRs, | (PDACs, NDACs) | (PAMPs, NAMPs) |
|  | DMUXs, DLs |  | AMP Bias, LSs, IPMUXs |

${ }^{1}$ MOSFET applied to the proposed output buffer amplifiers and IPMUXs.


Figure 8. Experimental setup for simulation and measurement.

The improved performance of the proposed design in terms of settling time, active area, and power consumption comes from the fact that the proposed buffer amplifier uses a smaller number of transistors for incorporating the adaptive biasing, and the polarity and isolation switches at the output of the buffer amplifier are moved either in front of or into the buffer amplifier. From the experimental evaluation results presented above, it can be implied that the proposed scheme is suitable for applications requiring a very high-speed operation, especially as a buffer amplifier for driving large-size high-definition FPDs.

## 4. Conclusions

A column driver with a high-speed driving scheme and an area-efficient high-slewrate buffer amplifier for FPD applications is proposed in this paper. To obtain a fast settling response with reduced active area and power consumption, the proposed driving scheme has eliminated all series switches in front of the output channels by moving them either to the buffer amplifier inputs or into buffer output stages. The proposed buffer amplifier also has a very compact adaptive biasing circuit composed of just two transistors that can draw a large amount of bias current during the transient period. The performance of the proposed driving scheme and buffer amplifier has been proven by an experimental chip fabrication, which indicates that the proposed approach is well suited for a high-speed column driver design in a large-sized high-resolution TFT-LCD. Other possible application areas for our design are quantum-dot LCDs (QD-LCDs), organic light-emitting diodes (OLEDs), quantum-dot LEDs (QLEDs), and a variety of other flat-panel displays with large capacitive loads.

Author Contributions: H.-R.K. and C.-H.A. designed the circuits, performed the simulation and implementation, analyzed the measurement data, and wrote the manuscript. C.-H.A. and B.-S.K. reviewed, wrote, and edited the manuscript. All authors have read and agreed to the published version of the manuscript.
Funding: This research received no external funding.
Acknowledgments: This work was supported by the NRF grant (2019R1A2C1011155); by the MOTIE and KEIT grant (20010560); by the NRF grant (2020M3H2A1076786); by the KIAT grant (P0012451); by the IITP grant (2019-0-00421); by the NRF grant (NRF-2020M3F3A2A01082301). The EDA tools were supported by the IC Design Education Center (IDEC) at KAIST.

Conflicts of Interest: The authors declare no conflict of interest.

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[^0]:    ${ }^{1} \mathrm{R}$ and C : five-order distributed RC network, ${ }^{2}$ Period for one-line horizontal operation.

[^1]:    ${ }^{1}$ Simulated data. ${ }^{2} 9 \mathrm{~V}(0-9 \mathrm{~V}), 18 \mathrm{~V}(9-18 \mathrm{~V}) .{ }^{3} 2.61 \mu \mathrm{~s}, 2.53 \mu \mathrm{~s}$ at $99 \%$ rising/falling settling time. ${ }^{4}$ Target voltage- $10 \mathrm{mV}(0.2-17.8$ V@VDD2 $=18 \mathrm{~V}) .{ }^{5} \mathrm{R}$ and C: five-order distributed RC network. ${ }^{6}$ Buffer area with input-polarity multiplexer switches or output-polarity multiplexer switches. ${ }^{7}$ Period for one-line horizontal operation.

