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Influence of Parasitic Resistances on the Input Resistance of Buck and Boost Converters in Maximum Power Point Tracking (MPPT) Systems

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Abstract: DC/DC converters are widely used in photovoltaic (PV) systems to maximize the power drained from solar panels. As the power generated by a PV panel depends on the temperature and irradiance level, a converter needs to constantly modify its input resistance to remain at the maximum power point (MPP). The input resistance of a converter can be described by a simple equation that includes the converter load resistance and the duty cycle of the switching signal. The equation is sufficient for an ideal converter but can lead to incorrect results for a real converter, which naturally features some parasitic resistances. The goal of this study is to evaluate how the parasitic resistances of a converter influence its input resistance and if they are relevant in terms of MPPT system operation.

Keywords: buck converter; boost converter; parasitic resistances; static characteristics; maximum power point tracking (MPPT)

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1. Introduction

The efficiency of photovoltaic (PV) panels is relatively small compared with other energy sources; monocrystalline panels convert up to 20% of the solar energy that reaches their surface into electric current. The output power of a PV panel depends not only on the irradiance level but also on the panel temperature and load resistance. If the resistance does not match a specific value, then the PV system does not generate the maximum power available at the moment. Hence, there is a need for DC/DC converters, which can regulate their input resistance and act as a part of maximum power point tracking (MPPT) systems (Figure 1) [1–4].

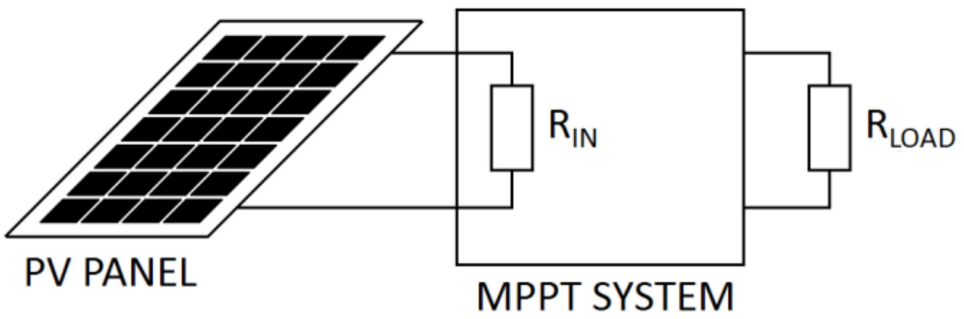

Figure 1. The structure of an MPPT system.

To reach the maximum power point of a PV panel, the MPPT system needs to set its input resistance value R_{IN} to be equal to the internal resistance of the panel. When an MPPT system features a DC/DC converter, the input resistance is modified by the duty

cycle of the PWM signal. However, since the internal resistance of a PV panel changes with the temperature and irradiance level, the MPPT system needs to constantly monitor the output power of the PV panel and modify the duty cycle of the converter in order to drain the maximum amount of energy [5].

Searching for the maximum power point may be achieved by different strategies, from simple ones such as open voltage (OV) [6,7], perturb and observe (P&O), and incremental conductance (IC) algorithms [3,7–12] to more complex strategies that use artificial intelligence [4]. More algorithms can be found in the literature [13–15], but since tracking algorithms were not within the scope of this study, they are not analyzed here.

An MPPT system can be basically built with any type of DC/DC converter, but the most common are buck (Figure 2a) and BOOST (Figure 2b) converters operating in continuous conduction mode (CCM) [1,12,16,17]. Those two types of converters are popular mostly because of their simplicity and high efficiency (above 90%) [17,18].

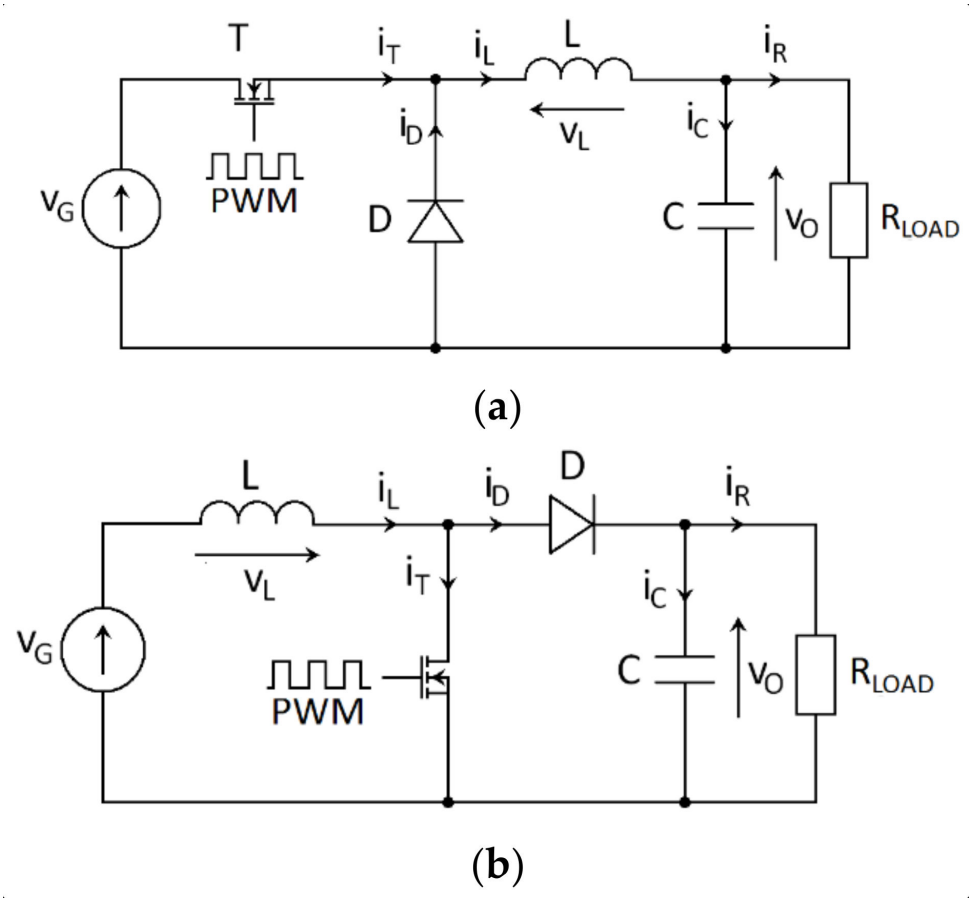

Figure 2. DC/DC converters commonly used for MPPT systems: (**a**) buck and (**b**) boost.

The selection of a converter depends on the application, because each type of converter has different features. Simplifying the input resistance R_{IN} of buck and boost converters involves a function of their load resistance R_{LOAD} and the duty cycle D_A as shown in Equations (1) and (2) [5]:

$$R_{IN(BUCK\_CCM)} = \frac{R_{LOAD}}{D_A^2}, \quad (1)$$

$$R_{IN(BOOST\_CCM)} = R_{LOAD}\,(1 - D_A)^2. \quad (2)$$

According to Equation (1), the input resistance of a buck converter is always larger than its load resistance ($R_{IN} > R_{LOAD}$). A similar statement exists for boost converters, except that its input resistance is always smaller than its load resistance ($R_{IN} < R_{LOAD}$).

This implies some restrictions regarding the implementation of these converters, which were previously explained and discussed in detail [5].

It was shown that some parasitic effects, such as equivalent series resistances (ESRs) of converter components, can affect the converter's characteristics [19]. The question that needs to be answered is if and how the parasitic resistances affect the input resistance of a converter. Therefore, equations similar to Equations (1) and (2), including all relevant parasitic resistances, should be derived and evaluated. To the best of our knowledge, the model of a converter input resistance, including the parasitic resistances of the components, has not yet been presented in terms of the issues related to a maximum power point tracking system. Therefore, the goal of this study is to provide an extended model of the input resistance (including the parasitic resistances) and verify it with experimental data.

2. Parasitic Resistances in DC/DC Converters and Their Impact on Converter Input Resistance

As was mentioned in the previous section, the input resistance of a converter should be equal to the internal resistance of a PV panel to acquire the maximum power from the panel. To calculate the input resistance of a non-ideal buck or boost converter operating in CCM, Equations (3) and (4) can be used, which include all relevant parasitic resistances. The equations were derived using models presented in [20]. The parasitic resistances included in Equations (3) and (4) are depicted in Figure 3.

$$R_{IN(BUCK\_CCM\_PAR)} = \frac{R_{LOAD} + R_Z}{D_A^2}, \tag{3}$$

$$R_{IN(BOOST\_CCM\_PAR)} = R_{LOAD}(1 - D_A)^2 + R_Z, \tag{4}$$

$$R_Z = D_A(R_T - R_D) + R_D + R_L, \tag{5}$$

where R_L is the ESR of an inductor, R_D is the static resistance of a diode, and R_T is the ON resistance of a transistor.

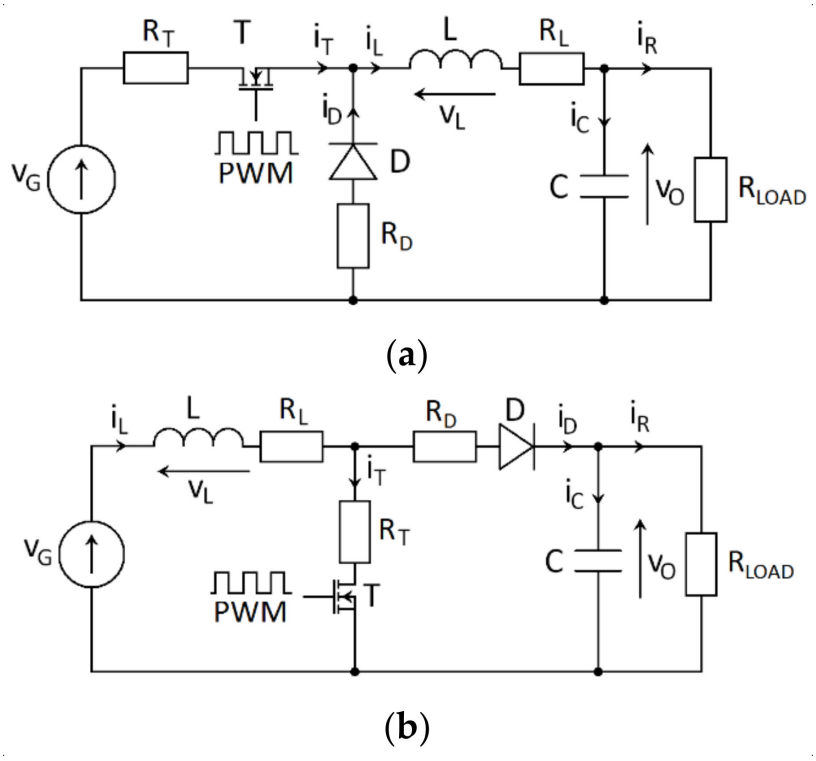

Figure 3. Converters with parasitic resistances: (**a**) buck and (**b**) boost.

The ESR value of the output capacitor is not shown in Figure 3 because it is irrelevant in terms of the converter input resistance. According to Equation (3), the strength of the influence of parasitic resistances on the input resistance of a converter R_{IN} depends on the relation between the load resistance R_{LOAD} and the value R_Z, described in Equation (5). Since the parasitic resistances should be kept relatively small to achieve high converter efficiency, their influence on the converter input resistance is negligible in most cases. However, for heavy loads, the influence might be noticeable.

To visualize the relation between the parasitic resistances, duty cycle, and the input resistance of a buck converter, the following parameters were used in Equations (1) and (3): L = 1000 µH, C = 330 µF, R_L = 1 Ω, R_D = 0.141 Ω, R_T = 0.012 Ω, and R_{LOAD} = 10 Ω. The parasitic values were chosen based on the measurement of the real components using an RLC bridge PM6306 (Fluke Corporation, Everett, WA, USA). To minimize the influence of any additional resistance, the PCB layout incorporated relatively wide and short traces. The results of the calculations are presented in Figure 4a.

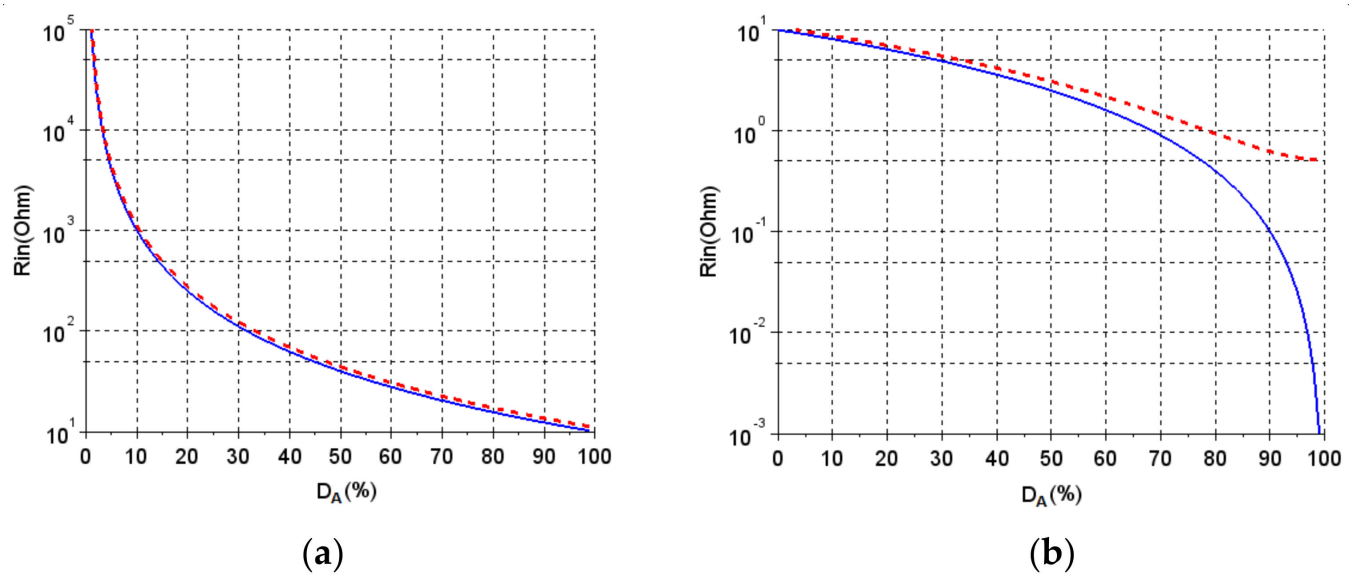

Figure 4. Input resistance of the (**a**) buck and (**b**) boost converters as a function of the duty cycle. The solid line is the ideal model, and the dashed line is the model with parasitic resistances.

A similar analysis was performed for a boost converter. According to Equation (4), the input resistance of a boost converter contains an offset, which means that the minimum achievable value of the input resistance is increased by the parasitic resistances. This situation is depicted in Figure 4b, where the input resistance of a boost converter was calculated using Equations (2) and (4) for different duty cycles. The simulated converter featured the following parameters: L = 500 µH, C = 330 µF, R_L = 0.5 Ω, R_D = 0.141 Ω, R_T = 0.012 Ω, and R_{LOAD} = 10 Ω. All of the parameters are visualized in Figure 4b.

Figure 4a shows that the influence of the parasitic resistances on the input resistance of a buck converter is relatively constant and basically depends on the ratio between the parasitic resistances and the load resistance. At first, when examining Figure 4a, the difference between the input resistances seems to be small (almost negligible) due to the relatively large load resistance and the logarithmic scale. However, the parasitic resistances led to differences of about 10% between the input resistances (calculated for an ideal Equation (1) and non-ideal Equation (3) converter).

A detailed analysis of the influence of a specific parasitic resistance on the input resistance of the buck and boost converters is provided in Appendix A.

As for the boost converter, the influence of the parasitic resistances on the input resistance changes with the duty cycle. Whereas the differences between the input resistance equations of the ideal and non-ideal buck converter are relatively constant over a wide

range of duty cycles, the differences in the boost converter vary and become significant for high duty cycle values. The reason for this is that, according to Equation (4), the parasitic resistances create an offset that prevents the input resistance from reaching infinitely small values. This can play a significant role in the designing process of the converter, as additional offset in the input resistance can prevent the MPPT system from reaching the maximum power point, especially when the panel temperature increases, leading to further reductions in the maximum power point resistance value R_{MPP}. An example of a panel maximum power point resistance change caused by temperature fluctuations is provided in Figure A3. The provided example shows a 30% drop in the R_{MPP} over a 60 °C change in temperature which, combined with the influence of the parasitic resistances, can lead to a less efficient MPPT system.

3. Materials and Methods

To evaluate the influence of the parasitic resistances on the input resistance of a buck converter, a dedicated measurement system was designed and built. The system consisted of a PIC32MZ microcontroller (Microchip Technology Inc., Chandler, AZ, USA) that generated a PWM signal, measuring the voltage, current, and temperature of a PV panel and sending the acquired data to a computer via a USB port (Figure 5).

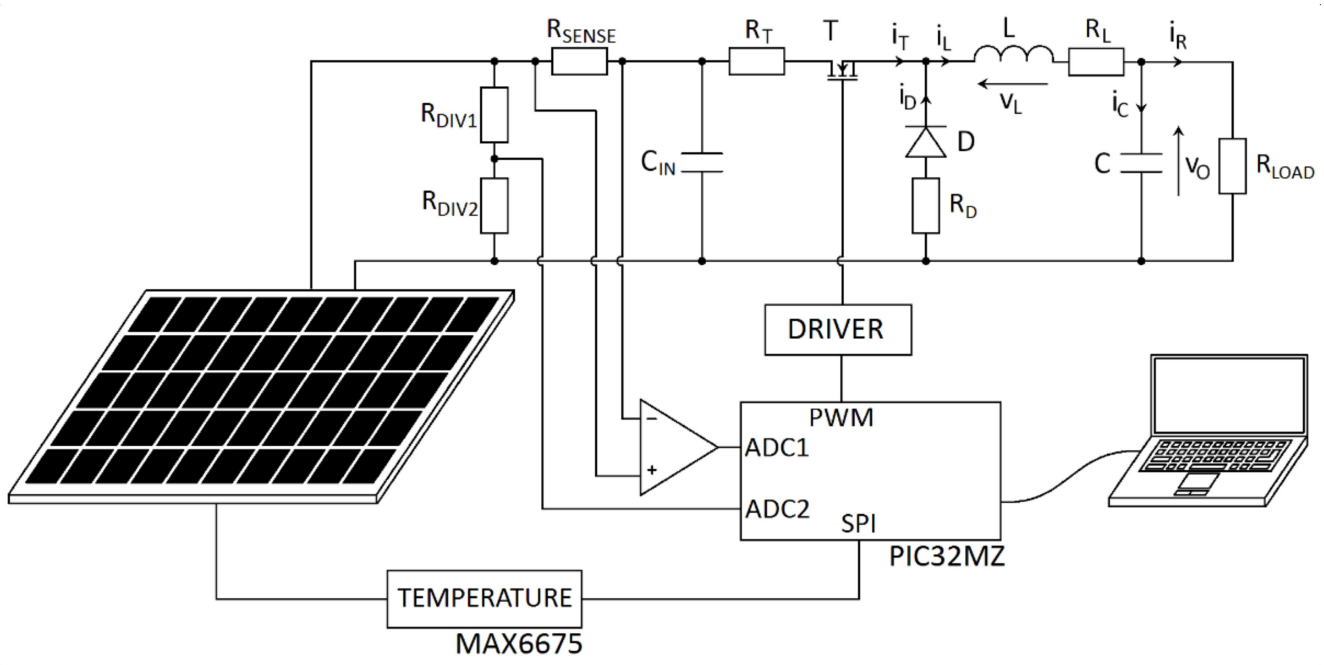

Figure 5. A dedicated system for the measurement of the I-V characteristics of a photovoltaic panel and searching for the maximum power point resistance.

The current was measured with a 0.1 Ω sense resistor and a differential amplifier (INA180A1). Additionally, the differential amplifier featured a low-pass input filter (Figure 6) to suppress any high-frequency noise from the converter (i.e., the chopped input current). The cut-off frequency of the filter was set to 79.5 kHz. The gain error of the differential amplifier, caused by the 1 Ω resistors of the input filter, was less than 0.1%, which was a satisfactory value. The system enabled measurement of a maximum of 1.5 A and 25 V with a theoretical accuracy of 0.4 mA and 6.2 mV, respectively.

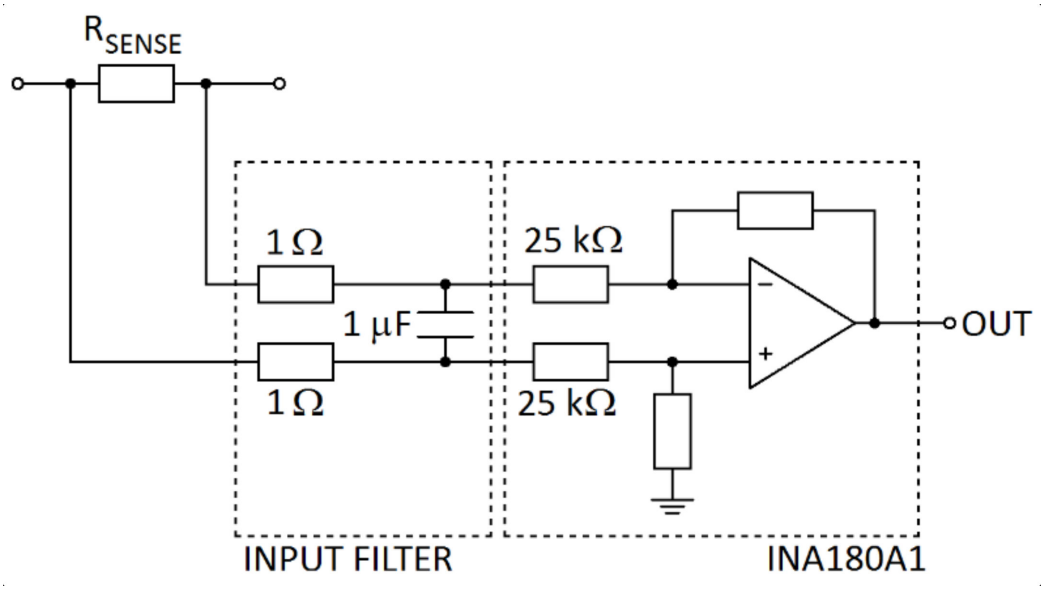

Figure 6. Input filter of the differential amplifier.

The panel temperature was measured using a thermocouple and a MAX6675 IC (Maxim Integrated, San Jose, CA), which featured a resolution of 0.25 °C. The simplified algorithm of the measurement is shown in Figure 7. The panel was illuminated for a short period of time (5 s) using halogen lamps. The short exposure time was required to maintain the temperature of the panel at a constant level of 25 °C. A longer exposure time could lead to additional errors due to the influence of the temperature on the panel characteristics. The heating curve of the PV panel illuminated with the halogen lamps is depicted in Figure A4.

During the exposure time, the I-V characteristic was measured by changing the pulse duration in the PWM signal. The duty cycle was changed with a step size of 0.005 (i.e., 0.5%). After each step change, the controller waited for about 25 ms to minimize the influence of transient oscillations. After that, a series of 10 measurements of the input voltage and current (one measurement per switching cycle) was performed, followed by temperature measurement of the PV panel. Next, the values were averaged and sent to a computer via a USB port. The whole measurement process was repeated for various irradiance levels.

The buck converter used during the measurement featured the following parameters: f_{PWM} = 100 kHz, L = 1000 µH, C_{IN} = 100 µF, C = 330 µF, R_L = 0.9 Ω, R_{SENSE} = 0.1 Ω, R_D = 0.141 Ω, R_T = 0.012 Ω, an MBRS340T3 diode (ON Semiconductor®, Phoenix, AZ, USA), and an NVD5867NLT4GT transistor (ON Semiconductor®, Phoenix, AZ, USA). Each parameter is visualized in Figure 5.

The proposed system was built and used to acquire the experimental data presented in Section 4. Both the measurement system and the halogen lamps used to illuminate the tested panels are depicted in Appendix B (Figures A5 and A6, respectively).

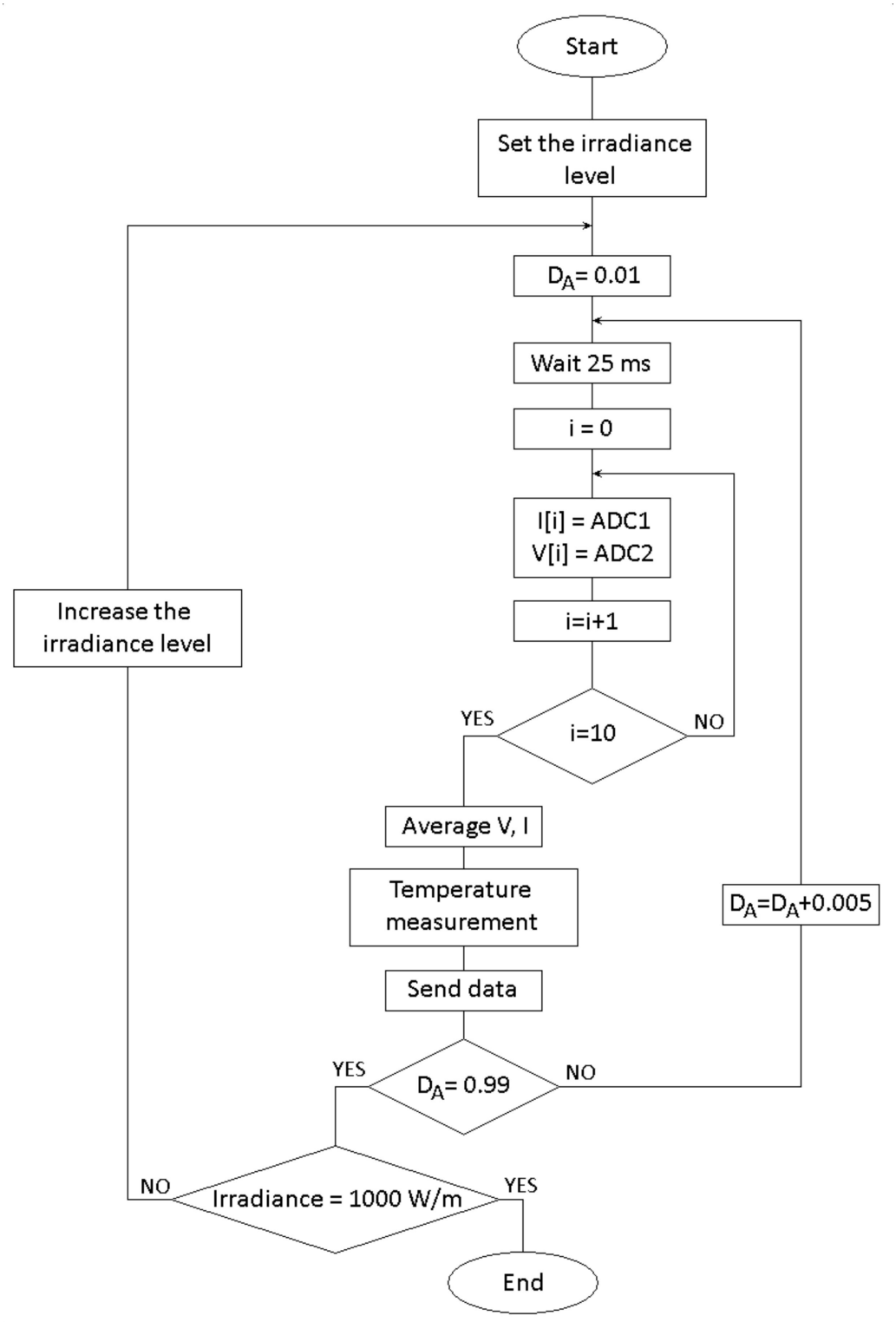

Figure 7. The algorithm for the measurement.

4. Results

The measurements recorded with the system described in the previous section led to the characteristics presented in Figure 8. The dots in the figure represent the values of the input resistance that were determined based on experimental data as a ratio between the input voltages and currents. The voltages and currents were determined with respect to the measured I-V characteristics at a maximum power point and for a specific irradiance level. All the other curves were calculated based on the duty cycle at a maximum power

point; therefore, to simplify the notation, the duty cycle corresponding to the maximum power point is denoted as D_{AMPP} hereafter. The solid lines represent the input resistances that were calculated for an ideal converter using the equation that did not include parasitic resistances (Equation (1)). The D_A value in the equation was equal to the duty cycle at the maximum power point D_{AMPP}, as mentioned above. The same duty cycle was used to calculate the input resistance of a non-ideal converter (including the parasitic resistances), which was described in Equation (3). The calculations for the non-ideal converter are indicated in Figure 8 by the dashed lines. The curves were measured and calculated for two PV panels (5 W and 10 W) and two load resistances (5 Ω and 10 Ω). More details can be found in the caption to Figure 8. Detailed parameters of the PV panels are provided in the Appendix A (Tables A1 and A2).

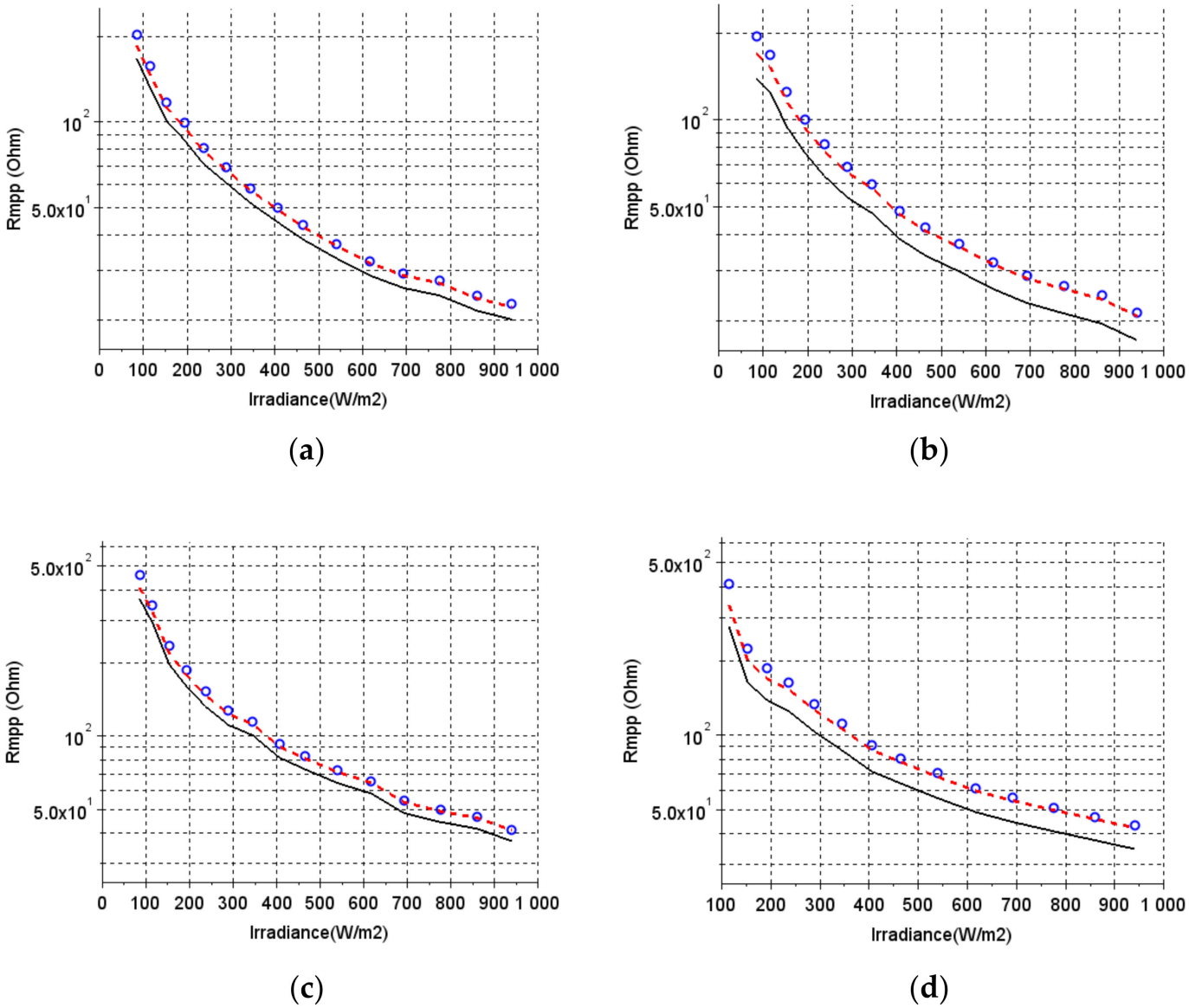

Figure 8. Input resistance of a buck converter at the maximum power point for different irradiance levels: (**a**) PV 10 W, R_{LOAD} = 10 Ω; (**b**) PV 10 W, R_{LOAD} = 5 Ω; (**c**) PV 5 W, R_{LOAD} = 10 Ω; and (**d**) PV 5 W, R_{LOAD} = 5 Ω. The solid line is the ideal model, the dashed lines are the model with parasitic resistances, and the dots represent the experimental data (measurements).

5. Discussion

The results of the measurements are presented in Figure 8. In all cases, the figures showed good consistency between the measurements and the model of a non-ideal buck converter that included the parasitic resistances (Equation (3)). Inconsistencies between the measurements and the model of an ideal converter were not substantial, but they were noticeable. The inductor resistance was relatively high, which had a substantial impact on the final results. Nevertheless, the presented figures show that the models featuring the parasitic resistances could be used to accurately calculate the input resistance.

The curves of the ideal converter moved toward the lower values, which is in agreement with the theory since parasitic resistances can only add up to the final value of the input resistance. As predicted, the discrepancies were more significant for higher loads (in this case, 5 Ω), which proved that for relatively high loads, the parasitic resistances should be included in the model.

Notably, for lower values of irradiance, even the model of a non-ideal converter, including the parasitic resistances, showed less consistency in comparison with the measurements. The differences started to accumulate slowly. For higher irradiance levels, the accuracy varied from 1% to 2% in comparison with the measured value (Figure 9), whereas for the lowest irradiance, the discrepancies reached up to 18% (the difference between the measurement and non-ideal model for the 5 W panel and 5 Ω resistance).

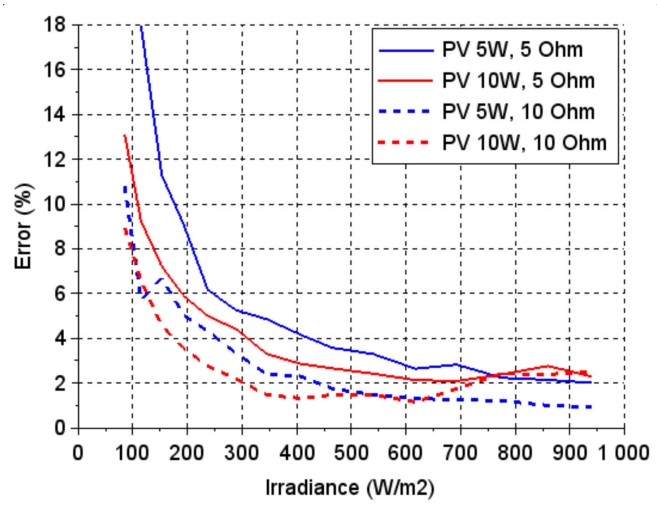

Figure 9. Errors between the input resistance calculated with Equation (3) and the measurements.

Another factor that seems to influence the accuracy is the load resistance. The analysis of the results showed higher discrepancies for the 5 Ω resistance (in both the 5 Ω and 10 W panels) than when a 10 Ω resistor was connected to the load of the converter. A detailed analysis of the errors is provided in the Appendix C (Tables A3 and A4). We found that the irradiance level and the load resistance were not directly responsible for the differences between the measurement and the model of a non-ideal converter. When the irradiance level decreased, the internal resistance of the PV panel rose. To maintain the panel at the maximum power point, the input resistance of a converter needs to be increased (i.e., the duty cycle needs to be reduced). If the value of the load resistance additionally decreases, the duty cycle has to decrease even more. In that case, if the duty cycle D_{MPP} experiences an error caused by wrong identification of the maximum power point, it would influence the accuracy and cause differences between the values of the input resistance. The differences would be observed between the values calculated with Equations (1–4) and in the ratio between the measured values of the voltage and current. A more detailed description of this problem is provided in Appendix C.

For the values calculated for an ideal buck converter, the curves shown in Figure 8 differ from the measured values by 10.5–19% with a 10 Ω resistor and 19.5–39% with a 5 Ω

resistor. The differences are beyond the accuracy of the measurement system. Even if the additional errors located at low irradiance levels were considered, the results would still show large discrepancies between the model and the measurements. For higher duty cycle values (when the accuracy was high), the differences between the model (Equation (1)) and the measured values matched the values of the parasitic resistances and could be predicted with Equation (3).

Despite the impact of the duty cycle differences on the input resistance calculations, (especially with low D_{MPP} values), the accuracy of the measurements was acceptable, and they could be used for evaluation of the presented models.

6. Conclusions

Maximum power point tracking systems are widely used for maximizing the power drawn from photovoltaic panels. The choice of the appropriate converter depends on the application, since every converter type has its own specifications and restrictions regarding its usage. The goal of this study was to evaluate if and how parasitic resistances of a converter influence its input resistance. A dedicated system was designed and used to measure the I-V characteristics of a PV panel under a stable temperature and for various irradiance levels. The measurements were performed in short intervals to avoid heating of the panel. Mathematical models of buck and boost converter input resistance containing parasitic resistances were presented and used for simulation in this paper. The results presented in Section 4 showed that the model containing parasitic resistances was in good agreement with the measurements and could therefore be used to calculate precise values of input resistance. Some discrepancies were observed at low irradiance levels due to the duty cycle error, which was explained and discussed in Section 5 and Appendix C. It was shown that the parasitic resistances could have a noticeable effect on the input resistance of a buck or boost converter if the load resistance value was comparable to the parasitic resistances. However, for a boost converter, the influence of the parasitic resistances changed significantly with the duty cycle of a PWM signal, as was shown in Section 2 (Figure 4b). In general, the parasitic resistances changed the input resistance of the converter; in the buck converter, the change was proportional to the load resistance, and in the boost converter, the resistances created an offset that influenced the operating point and, in some cases, might have prevented the MPPT system from reaching the maximum power point.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The curves presented in Figure A1 represent the percentage error between the ideal and non-ideal input resistance of a buck converter. The error was calculated using Equation (A1):

$$\delta = \frac{|R_{in-i} - R_{in-ni}|}{R_{in-ni}}, \tag{A1}$$

where $R_{in\text{-}i}$ is the theoretical value of the input resistance calculated with Equations (1) or (3) and where $R_{in\text{-}ni}$ is the theoretical value of the input resistance calculated with Equations (2) or (4).

Figure A1a shows how the inductor equivalent series resistance influences the input resistance, with reference to the ideal case described with Equation (1) for different values of the duty cycle D_A. The curves were drawn for various ratios (from 0.001 to 0.1) between a parasitic resistance and the load resistance of the converter. Similar calculations were performed for the transistor and diode resistances (Figure A1b,c, respectively). The figures show that the influence of the inductor resistance on the input resistance does not change with the duty cycle, and it depends only on the ratio between the parasitic resistance and the load resistance of the converter. As for the other parasitic resistances, the influence depends on the duty cycle. It seems that the transistor resistance does not have much of an impact on the input resistance of a converter for lower duty cycle values, whereas the diode resistance has less influence for higher values of D_A. Nevertheless, the total error between the input resistances calculated with and without the parasitic resistances does not exceed the ratio between R_Z, calculated with Equation (5), and the load resistance R_{LOAD}. The analysis shows that if the parasitic resistances of a buck converter are relatively small (i.e., below 1% of the load resistance), then their impact on the input resistance of the buck converter is also small for all duty cycle values. In such cases, the parasitic resistances can be omitted in Equation (3).

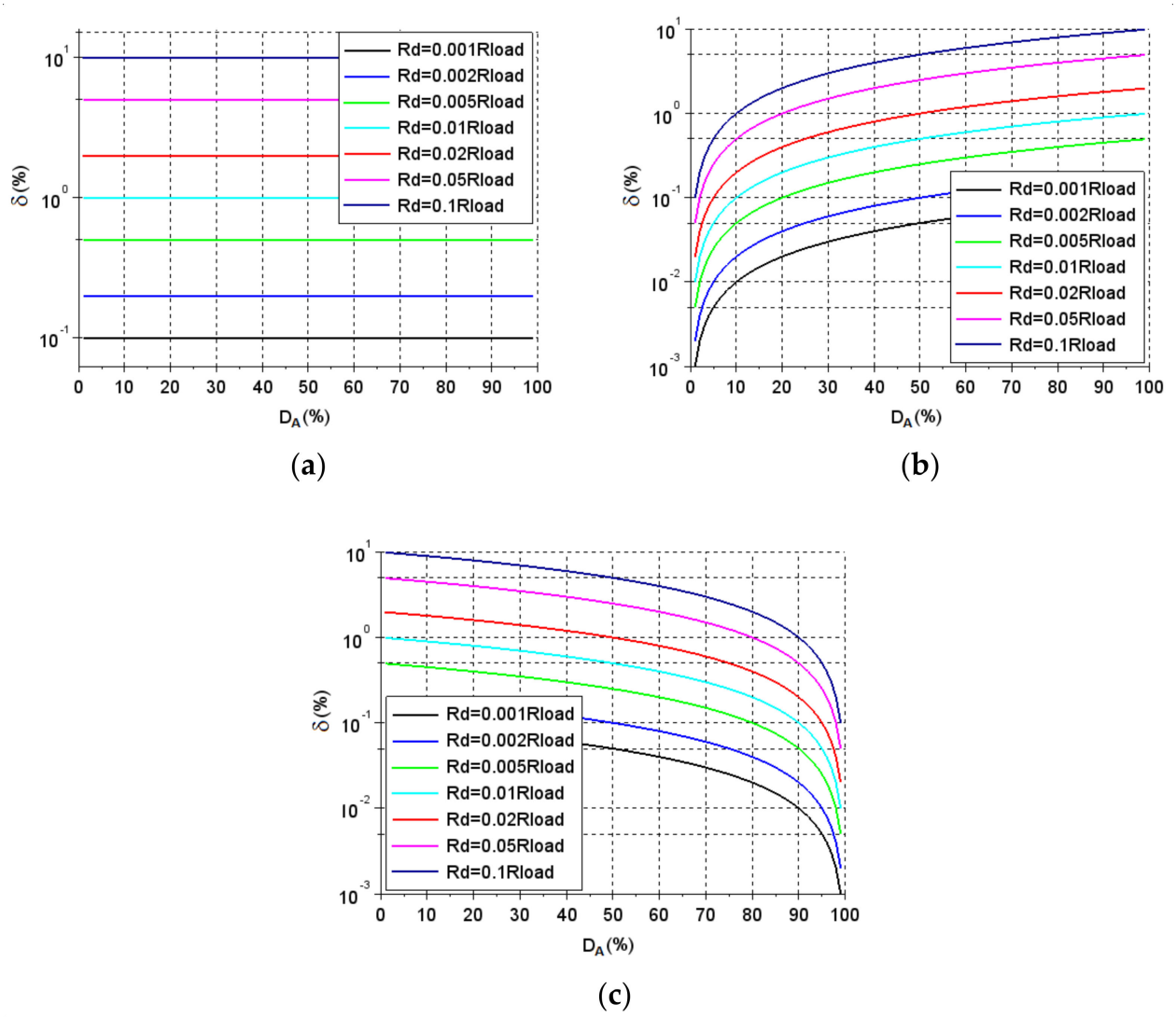

Figure A1. Influence of a specific parasitic resistance on the input resistance of a buck converter, for different duty cycle values. The figures represent a percentage error calculated with Equation (A1) for different values of: (**a**) inductor resistance R_L; (**b**) transistor resistance R_T; (**c**) diode resistance R_D.

A similar analysis was performed for a boost converter. Figure A2a–c shows the influence of a single parasitic resistance on the input resistance of a boost converter for different values of the duty cycle and for different ratios between the parasitic resistance and the load resistance of the converter. For the boost converter, the impact of a parasitic resistance on the input resistance of the converter can be larger than the ratio between the parasitic resistance and the load resistance. According to Figure A2a–c, even if a parasitic resistance value constitutes only 1% of the load resistance, then for a duty cycle of 50%, its influence on the load resistance can reach 2–4%. For D_A = 75%, it can reach up to 16%. This indicates that boost converters are more sensitive to parasitic resistances than buck converters. The influence of the parasitic resistances on the input resistances of a boost converter is noticeable for higher duty cycles even if the parasitic resistances are relatively small.

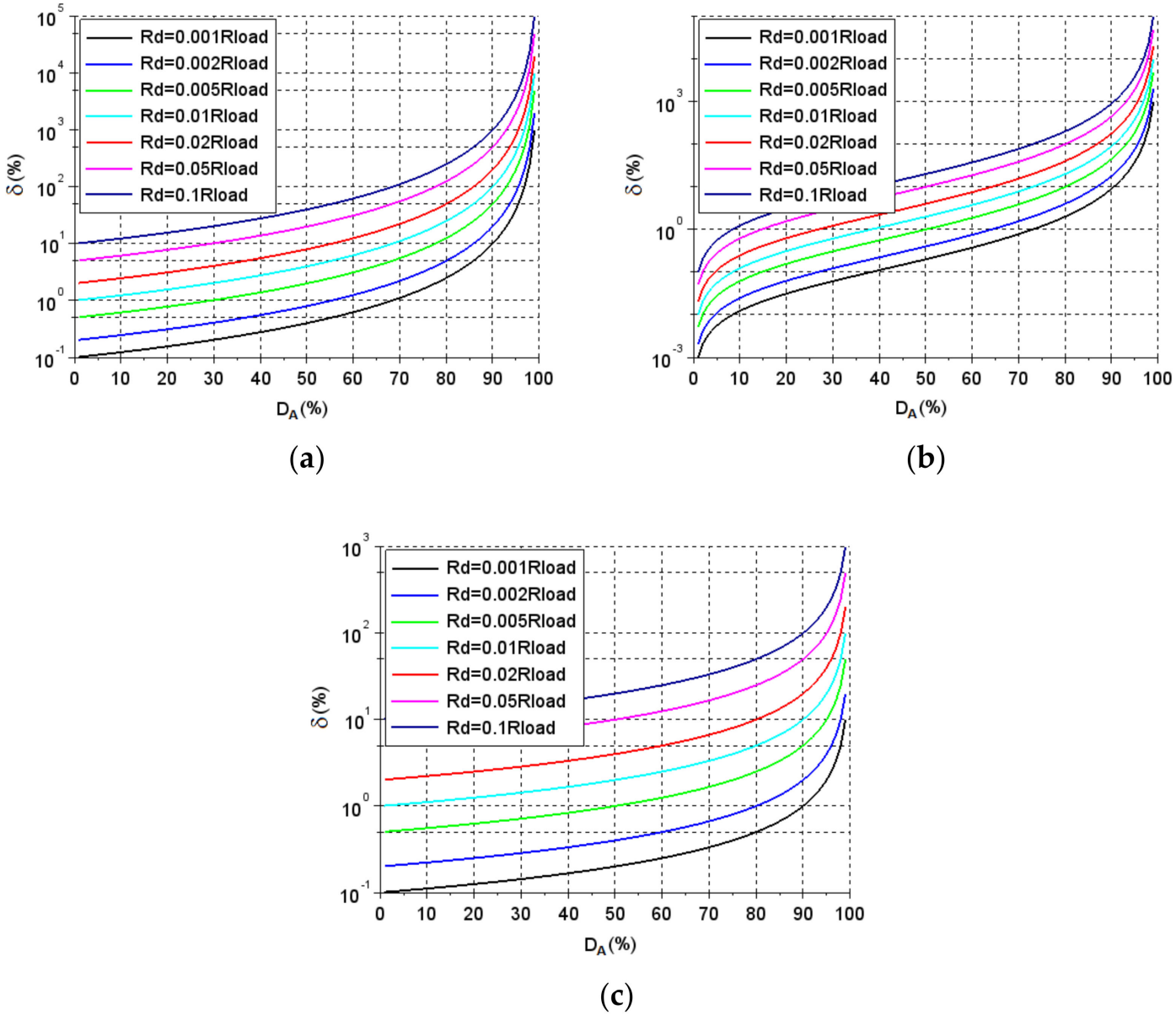

Figure A2. Influence of a specific parasitic resistance on the input resistance of a boost converter, for different duty cycle values. The figures represent a percentage error calculated with Equation (A1) for different values of: (**a**) inductor resistance R_L; (**b**) transistor resistance R_T; (**c**) diode resistance R_D.

Figure A3 shows the changes in the maximum power point resistance vs. the temperature of the panel, which explains why the panel characteristics must be measured in stable temperature conditions. Figure A4 shows how the temperature of the panel changed over time while illuminated. The curve shows that short periods of exposure enabled measurement in stable temperature conditions.

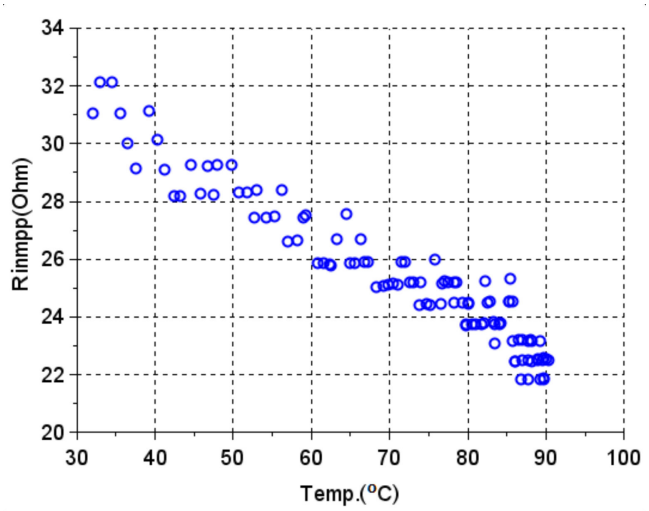

Figure A3. Change in the panel's maximum power point resistance caused by temperature (measured for a 10 W panel).

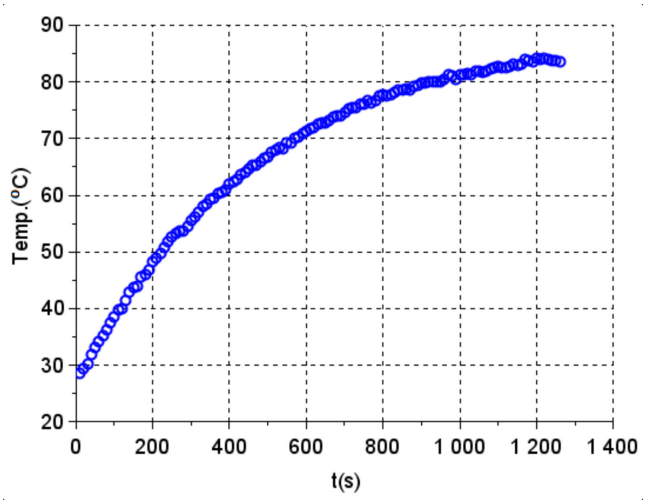

Figure A4. The heating curve of a 10 W PV panel illuminated with halogen lamps (1000 W/m^2).

Table A1. Detailed parameters of the 10 W PV panel under standard test conditions.

Name	Symbol	Value	Unit
Dimension	W × L	290 × 330	mm
Peak power	P_{max}	10	W
Maximum power current	I_{mp}	0.57	A
Maximum power voltage	V_{mp}	17.49	V
Short circuit current	I_{sc}	0.61	A
Open circuit voltage	V_{oc}	21.67	V

Table A2. Detailed parameters of the 5 W PV panel under standard test conditions.

Name	Symbol	Value	Unit
Dimension	W × L	231 × 186	mm
Peak power	P_{max}	5	W
Maximum power current	I_{mp}	0.30	A
Maximum power voltage	V_{mp}	16.5	V
Short circuit current	I_{sc}	0.34	A
Open circuit voltage	V_{oc}	21.0	V

Appendix B

The experimental data were acquired with the system presented in Figure A5. The PV panels were illuminated with 150 halogen lamps (12 V, 50 W each) and placed next to each other as shown in Figure A6. The lamps were connected in series and parallel to create a string powered with 60 V (30 strings connected in parallel, where each string consisted of 5 lamps connected in series). The lamps were powered with DC voltage to avoid irradiance fluctuations. All the bulbs created an illumination area of 640 mm × 680 mm (width × height). The irradiance level of 1000 W/m^2 was achieved at 70% of the bulbs' maximum power and a distance of 55 cm from the light source.

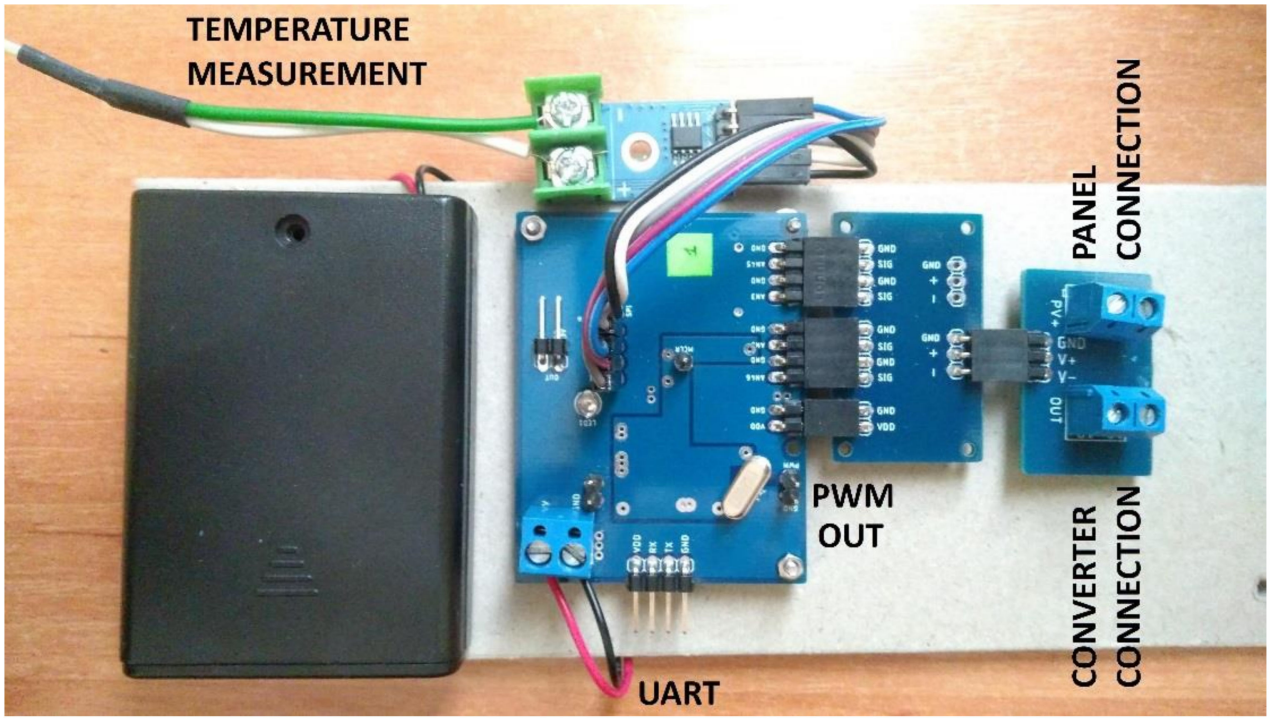

Figure A5. A measuring system incorporating a PIC32MZ microcontroller, used to control the buck converter and measure the input current, input voltage, and temperature of the panel.

Figure A6. Halogen lamps used to illuminate the measured panels.

Appendix C Analysis of the Errors

Tables A3 and A4 list the errors between the measurements and calculations presented in Figure 8. The errors are marked as follows:

- $\delta_{m\text{-}i}$: error between the measurement results and the model of an ideal converter (Equation (1));
- $\delta_{m\text{-}ni}$: error between the measurement results and the model of a non-ideal converter (Equation (3)).

The errors were calculated with reference to the measured value according to the following:

$$\delta = \frac{|R_{th} - R_m|}{R_m}, \tag{A2}$$

where R_{th} is the theoretical value of input resistance calculated with Equations (1) or (3) and R_m is the input resistance calculated as the ratio between the measured values of the voltage and the current.

The system was capable of measuring a maximum of 1.5 A and 25 V with a theoretical accuracy of 0.4 mA and 6.2 mV, respectively. This means that if the measured current is relatively small (e.g., 28 mA, which corresponds to the current of the 5 W PV panel at the lowest irradiance level set during the experiment), the measurement error can reach up to ±1.4%. For higher currents (i.e., irradiance levels), the error decreases, and for the maximum irradiance level, it drops to 0.13%.

Table A3. Differences between measured and calculated values for a 10 W PV panel.

Irradiance W/m^2	5 Ω Load Resistance		10 Ω Load Resistance	
	$\delta_{m\text{-}i}$ %	$\delta_{m\text{-}ni}$ %	$\delta_{m\text{-}i}$ %	$\delta_{m\text{-}ni}$ %
85	-	-	19.8	10.8
115	33	17.9	15.2	5.71
153	27.5	11.3	16	6.69
193	25.7	9.08	14.5	5.04
237	23.3	6.16	13.8	4.32
289	22.5	5.25	12.9	3.33
345	22.1	4.85	12.1	2.4
406	21.5	4.17	12	2.31
465	21	3.57	11.4	1.75
540	20.8	3.3	11.2	1.47
617	20.2	2.64	11	1.30
692	20.3	2.82	10.9	1.26
776	19.8	2.23	10.8	1.20
860	19.7	2.14	10.6	0.995
940	19.6	2.01	10.5	0.908

Table A4. Differences between measured and calculated values for a 5 W PV panel.

Irradiance W/m^2	5 Ω Load Resistance		10 Ω Load Resistance	
	$\delta_{m\text{-}i}$ %	$\delta_{m\text{-}ni}$ %	$\delta_{m\text{-}i}$ %	$\delta_{m\text{-}ni}$ %
85	29	13.1	18	8.95
115	25.8	9.22	15.9	6.56
153	24.1	7.22	14	4.57
193	23	5.89	13.1	3.56
237	22.2	5	12.3	2.76
289	21.7	4.41	11.8	2.19
345	20.7	3.31	11.1	1.46
406	20.3	2.86	10.9	1.32
465	20.1	2.66	11	1.48
540	19.9	2.42	11	1.47
617	19.6	2.13	10.7	1.15
692	19.5	2.08	11.2	1.74
776	19.7	2.39	11.8	2.42
860	20	2.76	11.7	2.38
940	19.5	2.29	11.8	2.52

Appendix D

If a small fluctuation appears in the current or voltage measurement, the power curve has an additional bump (Figure A7a), which can cause misidentification of the duty cycle at the maximum power point (i.e., instead of the true D_{MPP} (Figure A7b), an adjacent duty cycle (Figure A7c) can be taken as the maximum power point value). If the duty cycle has a relatively large value, the error caused by the input resistance miscalculation is not significant. However, if the duty cycle is low, then a wrong D_{MPP} value can cause large differences between the measured and calculated input resistances.

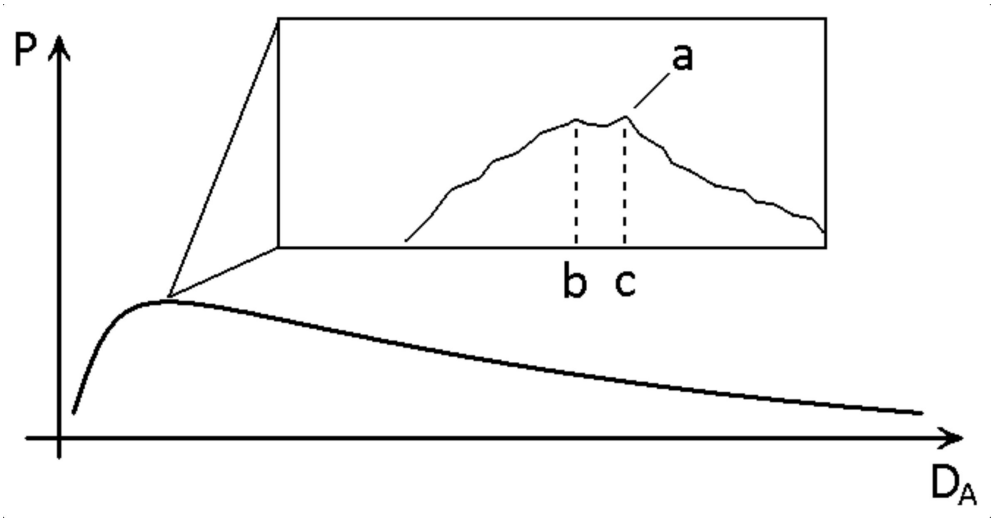

Figure A7. Impact of fluctuations in the power curve on the identification of the duty cycle at the maximum power point. (**a**) A power fluctuation. (**b**) Duty cycle at the actual maximum power point. (**c**) Duty cycle at the fluctuation.

To visualize the effect of the power fluctuation on the duty cycle and thus the input resistance of a buck converter, a simulation was performed. The input resistance was calculated using (1). Next. the same resistance was calculated, but this time, the duty cycle was increased by 0.5%. Finally, the error between those two values was determined. The results of the simulation are presented in Figure A8. The results of the simulation show a correlation with the error curves presented in Figure 9, which means that the deviation in a duty cycle is one of the main reasons why the differences between the measurements and calculations appear in Figure 8 at a low irradiance level. The solution to this problem may be increasing the resolution of the PWM signal or better filtering of the measured signals.

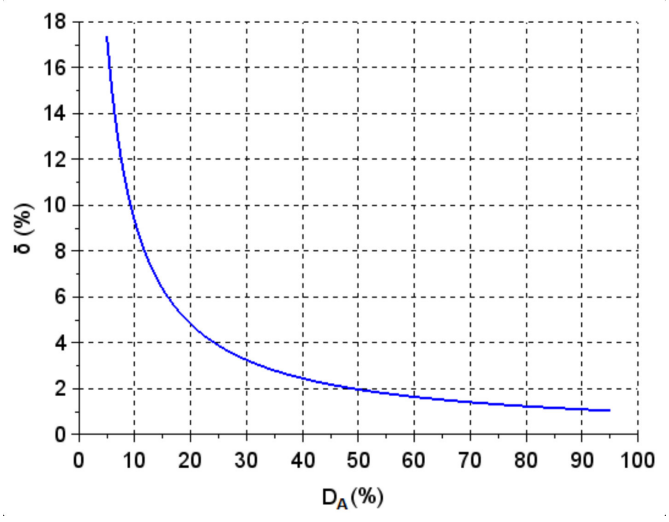

Figure A8. Influence of 0.5% deviation in the duty cycle on the input resistance calculations of a buck converter.

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