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A Novel Multilevel Controller

Hanying Gao [1,*], Xiangnan Liu [1], Mingjie Ren [2], Shuai Feng [1] and Zhiying Li [1]

[1] School of Electrical and Electronic Engineering, Harbin University of Science and Technology, Harbin 150080, China; 1920300072@stu.hrbust.edu.cn (X.L.); 1820300077@stu.hrbust.edu.cn (S.F.); 1820300063@stu.hrbust.edu.cn (Z.L.)

[2] School of Automation, Harbin University of Science and Technology, Harbin 150080, China; 1920510064@stu.hrbust.edu.cn

* Correspondence: ghy@hrbust.edu.cn; Tel.: +86-137-9666-8369

Abstract: Active power filter is an important means to improve power quality, and power topology is an important part of active power filter. Therefore, the research on power topology has important practical value. This paper proposes a simple-structure topology that employs eight switching power devices, two capacitors, and eight diodes to realize nine-level voltage output. The proposed topology can effectively reduce the volume and weight of the device and achieve multilevel output. Simultaneously, a compound control strategy, consisting of integrated phase voltage control and cell capacitance voltage control, is proposed for unit voltage equalization control. Finally, taking the three-phase active power filter as the research object, simulation and experimental verification are carried out with the proposed topology. The results show that the proposed topology and control scheme are feasible, and in the case of sudden load change, the fluctuation of capacitor voltage V_1 is less than 3 V, the fluctuation of capacitor voltage V_2 is less than 1 V, and the THD (Total Harmonic Distortion) of the phase current is well suppressed to 3.84%.

Keywords: active power filter; nine-level power topology structure; voltage sharing control

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1. Introduction

The rapid development of power conversion technology has led to a large number of applications of power electronic devices. On the one hand, this has made the transformation and application of electric energy convenient; on the other hand, serious power quality problems are caused. The active power filter (APF) will be one of the most important devices to improve the power quality in the future [1,2]. Compared with the passive power filter, the APF can achieve fast and flexible compensation, does not influence the system impedance, and does not produce resonance with the grid impedance. It can comprehensively solve power quality problems. Compared with the traditional two-level APF, a multilevel APF can improve the system capacity considerably; moreover, the compensation effect is better, and the system reliability is higher [3,4]. Switching frequency and high voltage put considerable stress on switch devices in traditional two-level APF topologies, so it is not suitable for high power and high voltage occasions [5]. The advantage of a multilevel topology is that the high voltage problem can be dealt with using low voltage modules in cascade and a conventional low voltage control strategy. The multilevel structure can significantly reduce the voltage stress of the unit module, the phase current harmonic component, and the switching loss [6,7]. In recent years, multilevel research has been gradually attracting the attention of many experts and scholars. It mainly focuses on two aspects: the multilevel topology and the optimization of the control strategy [8,9].

Regarding the multilevel topology, three main structures have been proposed: diode-clamped, flying capacitor, and cascade H-bridge multilevel converter [10,11]. However, when these topologies are extended to higher output levels, more switching devices and clamp devices are needed, resulting in a sharp increase in cost. To solve this problem,

a previous study [12] proposed a modified neutral point clamped (NPC) topology. Compared with the traditional NPC topology, it only needs four capacitors and eight switches to achieve nine-level output; however, capacitor voltage control is complex, the number of capacitors can be cut in half. Other studies [13] proposed an improved H-bridge topology in which each phase is composed of an H-bridge and a level conversion unit. Although fewer switching devices are used, the control of this structure is complex and the capacitor voltage balancing is difficult to achieve. Reference [14] proposed a topology that employs eight switching power devices, four diodes and four numbers of sources to realize nine-level voltage output. However, the nine-level topology has not been applied in practice and its applicability is unknown. One study [15] proposed a novel nine-level topology that each phase consists of a diode clamped inverter with a two-level H-bridge in series. However, the H-bridge can only provide active power. In addition, the inverter requires a complex nonlinear prediction model to stabilize the capacitor voltage. Another study [16] proposed a new H-bridge asymmetric structure. In this structure, although six unidirectional switches are used to achieve seven-level output, there is no method for extension to higher levels.

Regarding the optimization of the control strategy, reference [17] proposed a method to balance the capacitor voltage using a redundant switching state. However, this method is unfit for topologies without redundant states. Reference [18] proposed a method that employs a cosine function to replace the output current, therefore achieving capacitor voltage equalization. Although this method can reduce the number of current sensors, it is difficult to debug owing to its large number of parameters. References [19,20] proposed a carrier-stack modulation technology that can achieve power balance for each capacitor. However, the papers do not provide a specific voltage sharing control strategy.

This paper proposes a simple topology, which consists of eight switching power devices, two capacitors and eight diodes to realize nine levels voltage output. Compared with the traditional nine-level topologies, the new nine-level topology has the advantages of fewer switching devices, lower cost, and smaller volume. In addition, the topology has fewer switching devices and only needs two capacitors, which reduces the complexity of control and has higher practicability. Simultaneously, a compound control strategy, consisting of integrated phase voltage control and cell capacitance voltage control, is proposed for unit voltage equalization control. To verify the proposed nine-level control strategy, a three-phase APF was selected as the research object. The results demonstrate that the proposed control scheme is feasible and enables voltage sharing of the unit capacitor.

This paper proceeds as follows: Section 2 introduces the topology of the new nine-level active power filter and compares with other nine-level topologies. Section 3 mainly introduces the control strategy of the nine-level active power filter and gives the design scheme of LCL filter parameters. Simulation and experimental verification are given in Sections 4 and 5, respectively. In Section 6, the results of simulation and experiment are discussed. Finally, the conclusion and future research direction are given in Section 7.

2. Analysis of the Novel Nine-Level Topology

2.1. Presentation of the Novel Nine-Level Topology and Analysis of Its Working Mechanism

As shown in Figure 1, a novel APF based on a nine-level topology is proposed. The topology of each phase is same. Taking B-phase as an example, it includes eight switches (SW_{B1}, SW_{B2}, SW_{B3}, SW_{B4}, SW_{B5}, SW_{B6}, SW_{B7}, and SW_{B8}), two energy storage capacitors (C_{B1} and C_{B2}) and eight diodes (D_1, D_2, D_3, D_4, D_5, D_6, D_7 and D_8). As shown in Table 1, when SW_{B1} and SW_{B2} (or SW_{B5} and SW_{B6}) are switched on simultaneously, C_{B1} (or C_{B2}) short circuit; therefore, SW_{B1} and SW_{B2} (or SW_{B5} and SW_{B6}) must work in a complementary stat shows the nine working states of the novel topology; there are three switches in each working state. The C_{B1} voltage is V_1, and the C_{B2} voltage is V_2, where $V_1 = 3V_2$.

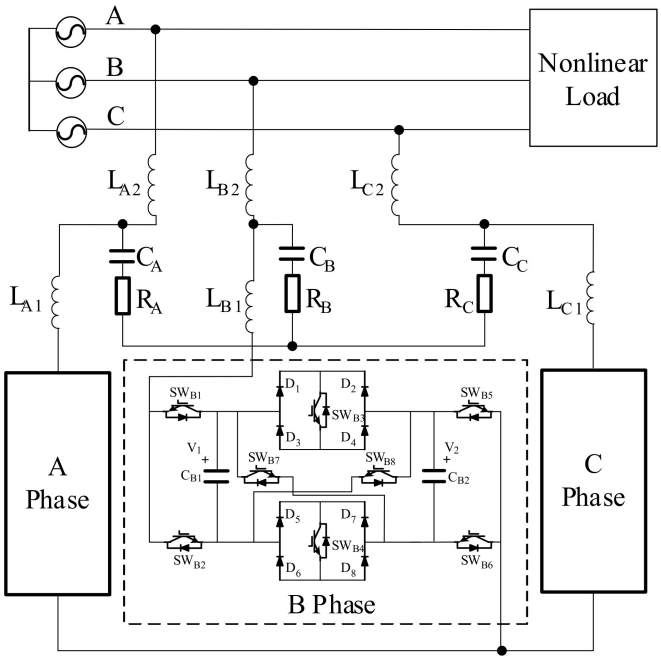


Figure 1. Main circuit of the nine-level active power filter.

Table 1. Output state of a new topology.

SW Status								Output State
SW_{B1}	SW_{B2}	SW_{B3}	SW_{B4}	SW_{B5}	SW_{B6}	SW_{B7}	SW_{B8}	
1	0	0	0	0	1	0	1	$V_1 + V_2 = 4V_2$
1	0	0	1	0	1	0	0	$+V_1 = 3V_2$
1	0	0	1	1	0	0	0	$V_1 - V_2 = 2V_2$
1	0	1	0	0	1	0	0	$+V_2$
1	0	1	0	1	0	0	0	0
0	1	0	1	1	0	0	0	$-V_2$
0	1	1	0	0	1	0	0	$-(V_1 - V_2) = -2V_2$
0	1	1	0	1	0	0	0	$-V_1 = -3V_2$
0	1	0	0	1	0	1	0	$-(V_1 + V_2) = -4V_2$

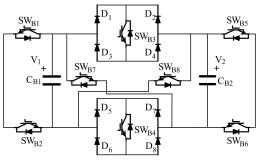
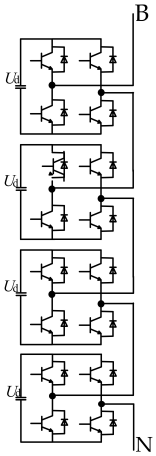
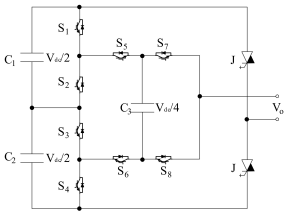
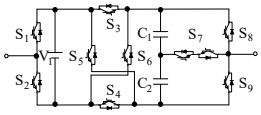
2.2. Comparison of Nine-Level Topology and Capacitance Voltage Control Strategy

2.2.1. Comparison of Nine-Level Topology

The new topology is compared with the other three nine-level topologies, as shown in Table 2. Traditional topology takes nine-level cascaded H-bridge topology as an example, each phase of cascaded H-bridge topology needs four H-bridge modules, namely 16 switches and 4 capacitors to realize nine levels output, and the capacitor voltage of each module should be considered, which increases the difficulty and cost of the system. The nine-level topologies mentioned in [21,22] need 10,9 switches and 3,2 capacitors respectively and [22] needs an additional voltage source. The number of switches is the most important part of the topology. The increase of their number will increase the cost, size, and control complexity of the circuit. From the size, cost and reliability of inverter, capacitor is also a very important part. Therefore, it is very important to reduce the number of switches and capacitors. The proposed topology only needs eight switches, two capacitors and eight diodes to realize nine levels output. Compared with two-level topology, the proposed topology reduces the voltage change rate and voltage stress of the switches. The comparison in Table 2 shows that the topology proposed in this paper uses fewer switching devices and only needs two capacitors, which reduces the complexity of control and has higher practicability. It also has the advantages of low cost and small volume. In addition, the topology proposed in this paper is asymmetric, the SW_{B5} and SW_{B6} only

need to withstand the V_2 rated voltage, the voltage stress is low, so MOSFET (300 V) with lower cost can be used to instead of IGBT (SW_{B5} and SW_{B6}) to further reduce the cost of active power filter. Considering the limitation of blocking voltage, it is mainly used in medium and low voltage applications. If IGCT is used as switching devices, the proposed topology can also be applied to high voltage applications.

Table 2. Comparison of nine-level topology.

Structure / Category	New Topology	Cascade H-Bridge Nine-Level	[21]	[22]
Topology				
Number of power switches	8	16	10	9
Number of capacitors	2	4	3	2

2.2.2. Comparison of Capacitance Voltage Control Strategy

At present, there are many kinds of capacitor voltage sharing control of multilevel active filter, for example, reference [23] proposed to select the optimal switching state sequence from the redundant switching states to balance the capacitor voltage. However, this method requires that there are many redundant states in the topology to select the optimal switching sequence. The topology proposed in this paper is asymmetric topology, and the redundant switch state is limited, this method cannot control the capacitor voltage well. In addition, model predictive control and neural network algorithm are proposed in reference [24,25] to realize voltage sharing control of capacitor voltage, but this kind of control strategy has a large amount of calculation, which leads to the decline of real-time performance, will affect the effect of harmonic compensation, and is difficult to achieve with high complexity. For some asymmetric topologies, it is not limited to the existing voltage stabilizing control strategy, so it should be flexible to adopt voltage stabilizing strategy. Aiming at the voltage stability of capacitor under the new nine-level topology, a two-stage voltage sharing control strategy is proposed, which is the overall control and the independent control respectively, which can better stabilize the capacitor voltage. The control strategy has the advantages of small computation, high real-time performance, and easy implementation.

3. Control Method of the APF System with the Novel Topology

3.1. Overall Control Strategy of the System

The APF system consists of four parts: harmonic detection, DC voltage stabilizing control, compensation current fast tracking, and carrier-stack PWM generation. The *id-iq* current detection method was applied in this study to achieve fast detection and compensation of the phase current. Considering the influence of capacitor charge and discharge on capacitor voltage stabilization, this paper proposed a voltage stabilizing control strat-

egy combining unit capacitor voltage control with phase voltage comprehensive control. For current tracking, a quasi-PR and a repetitive control strategy were used to track the given harmonic current accurately. In addition, this paper proposes a carrier-stack strategy to generate PWM and integrate it into the cell capacitor voltage control. Figure 2 presents the control system structure diagram of the APF. The phase capacitance voltage control output, u_{1Bf}, and the unit voltage control output, u_{2Bf}, are superimposed to obtain the composite capacitance control output (u_{Af}, $u_{Bf,}$ and u_{Cf}). Then, u_{Af}, u_{Bf}, and u_{Cf} are combined with the harmonic suppression unit to obtain the modulation wave (u_A, u_B, and u_C), and the PWM control signal is generated via the carrier-stack.

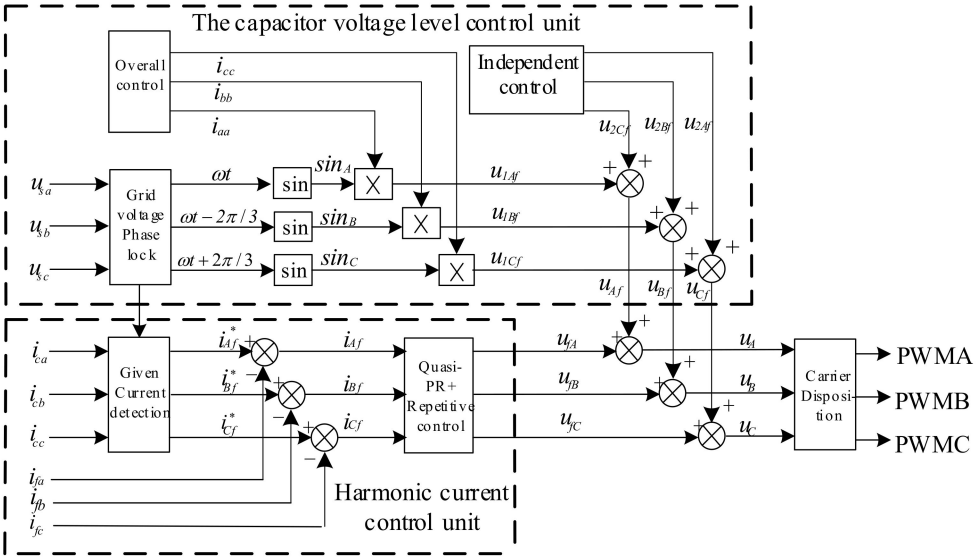


Figure 2. Global control strategy of the system.

3.1.1. The Reference Current Detection Unit

The reference current detection unit is shown in Figure 3, the three-phase fundamental active current is obtained by coordinate transformation, filtering, inverse transformation and other processing of the three-phase current, and the harmonic signal to be compensated, namely harmonic reference current, can be obtained by subtracting the three-phase fundamental active current from the total three-phase current.

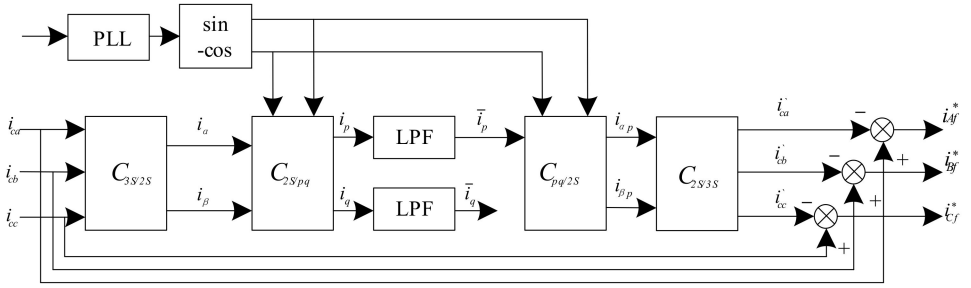


Figure 3. The reference current detection unit.

3.1.2. The Current Tracking Unit

Taking B-phase as an example, the error signal i_{Bf} is obtained by subtracting the feedback current i_{fb} from the reference current i_{Bf}*. Then, the error signal passes through the quasi-PR and repetitive controller to receive the output signal u_{fB}, as shown in Figure 4. Finally, the feedback signal can track the reference signal.

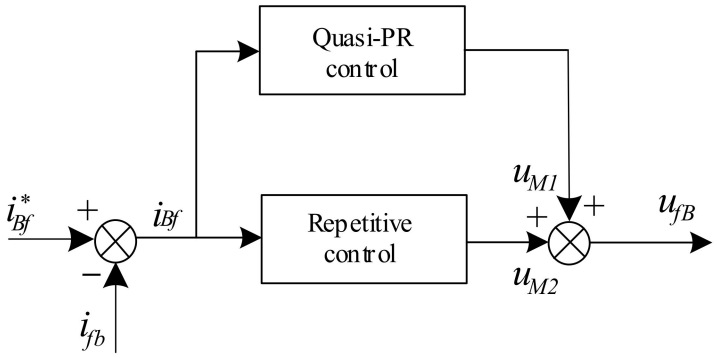


Figure 4. The current tracking unit.

The transfer function of quasi-PR controller is as follows:

$$G_{PR}(s) = K_p + \frac{2K_{in}\omega_c s}{s^2 + 2\omega_c + \omega_n^2}. \quad (1)$$

where ω_n is the resonant frequency of PR controller, K_p is the proportional coefficient of PR controller, and K_{in} is the resonant coefficient, which is the gain of resonant frequency.

It can be controlled by changing the ω_c to expand the bandwidth of resonance frequency, in the case of power grid frequency offset, it can also effectively control the signal, reduce the sensitivity of the system to the change of power grid frequency, and has good dynamic suppression performance.

Although the harmonic compensation of PR controller suppresses a certain number of harmonics, it increases the difficulty of implementation of the algorithm. Especially with the increase of the harmonic number, such as 7th, 9th, 11th, etc. When simultaneous compensation is needed, the computational complexity of the digital signal processor will increase greatly. Moreover, in order to ensure the stability of the current loop, the number of harmonics that can be suppressed by harmonic compensator is restrained by the bandwidth of current loop. Therefore, a repetitive control strategy is introduced, the principle is shown in Figure 5. The repetitive controller can compensate for the repeated periodic error by cycle integration, and then suppress the periodic interference, which has good steady-state control performance.

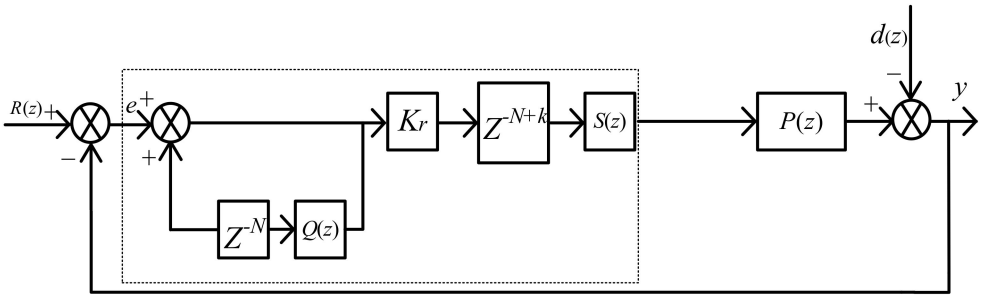


Figure 5. Block diagram of repetitive control principle.

where $R(z)$ is the given input, e is the error signal, $d(z)$ is the disturbance signal, Z^{-N} is the delay link, and N is the sampling times in a fundamental period; $P(z)$ is the control object and K_r is the gain of repetitive controller; Z_k is the leading compensation link; $S(z)$ is a combination of low-pass filter and notch filter. To improve the stability of the system, the attenuation filter $Q(z)$ is usually added to the internal mode positive feedback channel. According to the empirical value, $Q(z) = 0.95$ is often taken. The combination of repetitive control and quasi-PR control can realize the dynamic suppression of each harmonic and better tracking of command current.

3.1.3. The Grid Voltage Phase-Locked Unit

Shown in Figure 6 is the grid voltage phase-locked unit. The double second-order generalized integral phase-locked loop (DSOGI-PLL) and two second-order generalized integrators (SOGI) are used to extract the positive sequence components of three-phase grid voltage. Then, the PI controller makes the value of V_q 0, outputs the phase-locked frequency, and feeds back the phase-locked frequency to the previous coordinate transformation to form a closed-loop phase-locked.

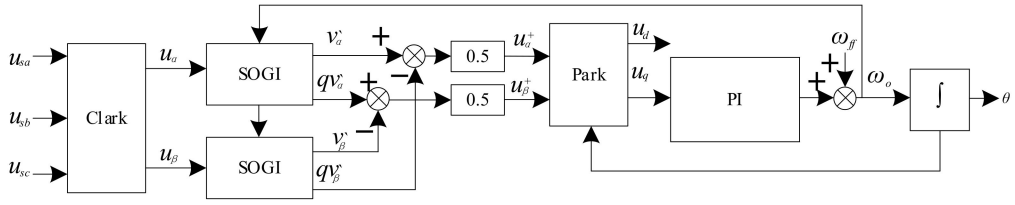


Figure 6. The grid voltage phase-locked unit.

3.1.4. The Carrier Disposition Unit

The carrier disposition unit is shown in Figure 7. Eight triangular carriers with the same frequency and phase are vertically and evenly distributed in the coordinate system. According to the principle of SPWM output waveform, when the modulation wave signal is higher than the carrier signal, the output level plus 1, when the modulation wave signal is lower than the carrier signal, the output level minus 1.

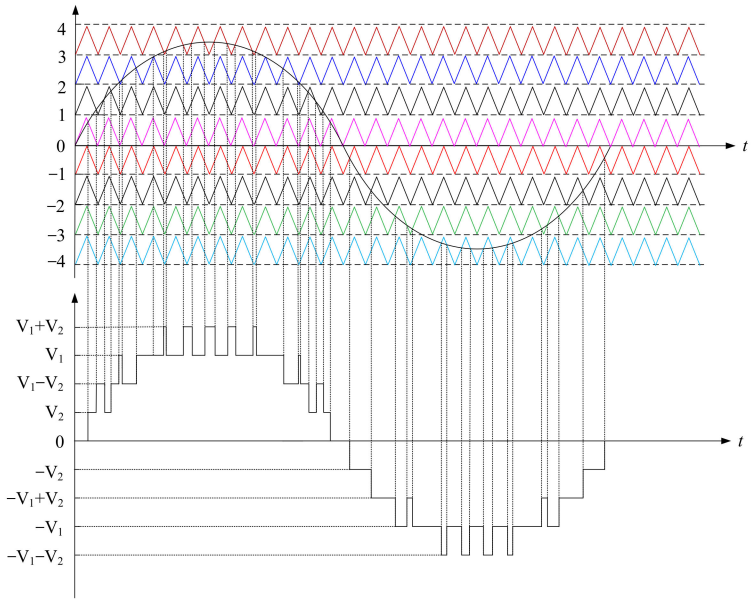


Figure 7. The carrier disposition unit.

3.2. Integrated Control Strategy of Phase Voltage

The first step is to control the sum of the capacitor voltage. The reference voltage (V_{ref1} + V_{ref2}) is compared with the actual capacitor voltage (V_{B1} + V_{B2}), and the modulation wave i_{bb} is obtained by PI regulation, as shown in Figure 8. Then, the phase of B-phase is multiplied by i_{bb} to obtain u_{1Bf}, thus, integrated control of the B-phase unit voltage, C_{B1} and C_{B2}, is achieved, and V_{ref1} + V_{ref2} = V_{B1} + V_{B1}.

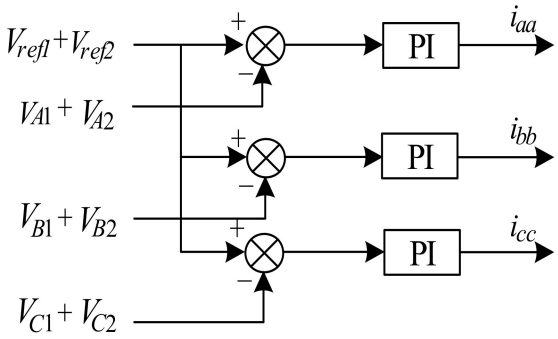


Figure 8. Integrated control strategy of phase voltage.

3.3. Control Strategy of the Cell Capacitance Voltage

Figure 9 presents the control strategy of the cell capacitance voltage of the C_{B1} and C_{B2} voltages; this strategy is composed of charge-discharge state determination and charge-discharge control, where sgn(i_B) is the sign function of i_B.

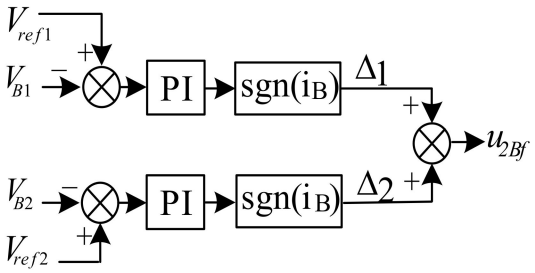


Figure 9. Control strategy of cell capacitance voltage.

3.3.1. Determination of the Charge-Discharge State

Table 3 shows the charging and discharging state judgment of C_{B1} and C_{B2}. Figure 10 shows the working order of the cell circuit when C_{B1} and C_{B2} of the B-phase are charged and discharged. First, according to the circuit output state and i_B flow path to determine which state the capacitors (C_{B1} and C_{B2}) is in. If C_{B1} and C_{B2} are charged and discharged at states 9, 7, 3 and 1 in Table 3 the unit output will change at this time. Simultaneously, C_{B1} and C_{B2} are suspended at state 5, therefore, charging and discharging do not require adjustment in this case. According to this analysis, the charging and discharging of capacitors C_{B1} and C_{B2} can only be performed at states 2, 4, 6, and 8.

Table 3. Determination of charge and discharge status of C_{B1} and C_{B2}.

Current / Output Level	$i_B > 0$	$i_B < 0$
9: $V_1 + V_2 = 4V_2$	-	-
8: $V_1 = 3V_2$	C_{B1} discharge, C_{B2} suspend	C_{B1} charge, C_{B2} suspend
7: $V_1 - V_2 = 2V_2$	-	-
6: V_2	C_{B2} discharge, C_{B1} suspend	C_{B2} charge, C_{B1} suspend
5: 0	-	-
4: $-V_2$	C_{B2} charge, C_{B1} suspend	C_{B2} discharge, C_{B1} suspend
3: $-(V_1 - V_2) = -2V_2$	-	-
2: $-V_1 = -3V_2$	C_{B1} charge, C_{B2} suspend	C_{B1} discharge, C_{B2} suspend
1: $-(V_1 + V_2) = -4V_2$	-	-

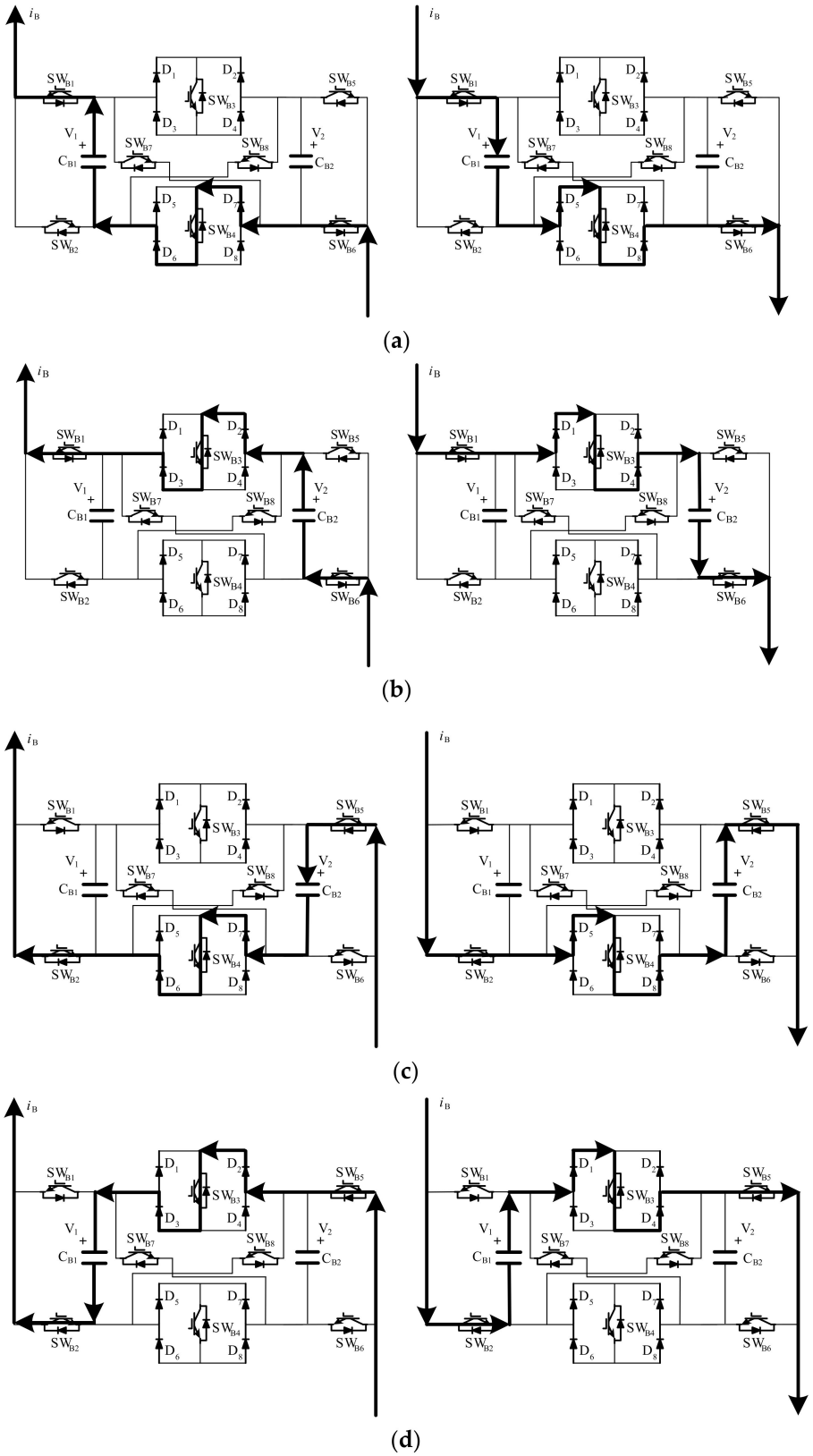


Figure 10. Circuit working state when C_{B1} and C_{B2} are charged and discharged: (**a**) level 8; (**b**) level 6; (**c**) level 4; (**d**) level 2.

3.3.2. Control Strategy of the Capacitor Voltage Regulation

As shown in Figure 9, C_{B1} and C_{B2} are charged and discharged, and the actual voltage values, V_{B1} and V_{B2}, of C_{B1} and C_{B2}, respectively, reference voltage V_{ref1} and V_{ref2}, are PI-adjusted. Δ_1 and Δ_2 are obtained using the sign function sgn(i_B), and their sum yields U_{2Bf}. Figure 11 shows the voltage stabilizing strategy of nine-level cell capacitor. Eight carriers are stacked to output the nine-level states from low to high, recorded as 1–9 levels, respectively. According to the principle of carrier cascade modulation, two levels can be output when the modulation wave is located in region 1 or 2 (corresponding to $-V_1$ in Table 3). Assuming that V_{B1} is greater than V_{ref1}, the V_{B1} output can be reduced by prolonging the discharge time or reducing the charging time of C_{B1}. In the discharge state of C_{B1}, if carrier 2 is compared with the modulation wave, then the output is either level 2 or level 3.

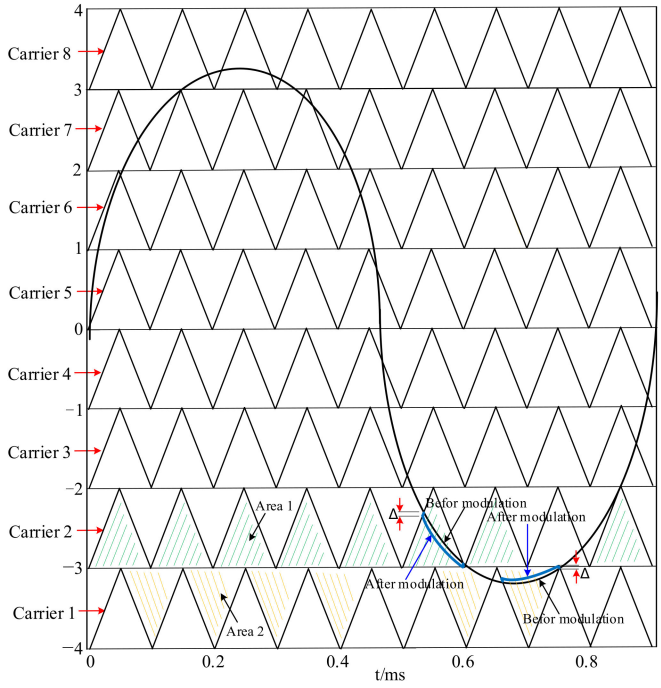


Figure 11. Schematic diagram of unit capacitor voltage stabilization.

At this time, the duration of C_{B1} discharge can be prolonged by reducing the amplitude of modulation wave, this increases the duration of level 2. If carrier 1 is compared with the modulation wave, the output is either level 2 or level 1. At this time, by reducing the amplitude of modulation wave, the charging time of C_{B1} can be prolonged, and then the output time of level 2 can be prolonged. For the same reason, to reduce the charging time of C_{B1}, the amplitude of the modulation wave can be changed when the C_{B1} is in the charging state. Therefore, the amplitude of the modulation wave can be adjusted to stabilize the capacitor. The stable voltage control of C_{B2} is consistent with that of $C_{B1.}$ To achieve the goal of stable capacitance voltage, we can change the amplitude of the modulation wave. Table 4 depicts the situation of the four levels of fine adjustment and the correction of the modulated waves, taking the actual voltage as an example.

Table 4. Fine tuning correction of the modulation wave.

Carrier / Output Level	State	8	7	6	5	4	3	2	1
		Up (↑) or Down (↓)							
8: $V_1 = 3V_2$	discharge	↓	↑	-	-	-	-	-	-
	charge	↑	↓	-	-	-	-	-	-
6: V_2	discharge	-	-	↓	↑	-	-	-	-
	charge	-	-	↑	↓	-	-	-	-
4: $-V_2$	discharge	-	-	-	-	↓	↑	-	-
	charge	-	-	-	-	↑	↓	-	-
2: $-V_1 = -3V_2$	discharge	-	-	-	-	-	-	↓	↑
	charge	-	-	-	-	-	-	↑	↓

3.4. Parameter Selection of the Passive Device

Because the compensation inductance determines the change rate di/dt of the inductance current, it also determines the dynamic compensation effect of the APF. Theoretically, in a certain range, the dynamic rate of the inductor current is greater; hence, the compensation effect will be better. The dynamic rate of the inductor current increases with the decrease in inductance, but when the inductance decreases, the ripple current in the compensation current increases, which affects the compensation effect. The stability of DC voltage is an indispensable condition for active power filter to achieve good harmonic compensation effect, and the compensation capacity and capacitance value of the APF determine the voltage and voltage ripple of the capacitor, it is necessary to select the capacitance voltage and voltage ripple reasonably.

3.4.1. Parameter Selection of LCL

1. Inductance parameter selection: It is assumed that the inductance relationship between the grid side and the inverter side is as follows:

$$L_1 = \lambda L_2. \tag{2}$$

where L_1 is the grid side inductor, L_2 is the inverter side inductor, λ is a constant.

The resonance frequency of LCL filter is:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}}. \tag{3}$$

where C_f is the capacitor value of LCL.

Then the resonant frequency of LCL can be written as follows:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{\lambda + 1}{\lambda L_2 C_f}}. \tag{4}$$

And the resonant frequency also needs to meet the following conditions:

$$10f \le f_{res} \le 0.5 f_{sw}, \tag{5}$$

where f is the power grid frequency, and f_{sw} is the switching frequency.

The total inductance L should not only restrain the harmonic but also track the reference current quickly. Similar to reference [6], the inductance should meet the following conditions:

$$\frac{V_{dc}}{8\sqrt{2}\Delta i_{max}\ f_{sw}} \le L < \frac{\sqrt{V_{dc}^2 - \frac{8}{3}E_m^2}}{\sqrt{2}\omega I_m}, \tag{6}$$

where V_{dc} is the dc bus voltage, $E_{m,}$ is the effective value of grid phase voltage, the switching period, $f_{SW,}$ is 10 kHz, I_m is the peak value of the inverter output current, Δi_{max} is the maximum ripple current, which is less than 20% I_m, so

$$0.625 \text{ mH } \leq L < 14.0 \text{ mH}. \tag{7}$$

According to Equation (7), the inductance, L, was selected as 3 mH.

L_2 should be selected to be as small as possible. If the inductance at the network side is too large, the dynamic performance of the system will be reduced. The calculation results need to satisfy that the current ripple attenuation of LCL filter is about 20%. The attenuation formula is as follows:

$$\frac{i_g(n_{sw})}{i(n_{sw})} = \frac{1}{1 + \left(1 - 4\pi^2 f_{sw}^2 L C_f\right)/\lambda}, \tag{8}$$

where $i(n_{sw})$ is the Nth harmonic current of the grid, $i_g(n_{sw})$ is the Nth harmonic current of the bridge arm. Here the value of λ is 2.

Therefore, the inverter side inductance L_1 = 2 mH, the grid side inductance L_2 = 1 mH.

2. Selection of capacitance parameters: The principle of capacitance selection is that the value of capacitance should be selected as small as possible to ensure that its impact can be completely ignored. The capacitance should be selected according to the rated power of APF. Generally, 5% of the rated power of APF is considered to be the threshold value of reactive power caused by the filter capacitor, and it is only necessary not to exceed the threshold value.

$$\text{C} \leq 0.05 \times \frac{P}{2\pi f E_{line}^2}, \tag{9}$$

where f is the frequency of the power network, P is the rated power of the system, and E_{line} is the effective value of the grid line voltage.

$$\text{C} \leq 8.82 \text{ μF}, \tag{10}$$

where the value of capacitance C is 8 μF.

3. Resistance selection: The selection of resistance has a great influence on the system. If the selected value is too small, the resonance cannot be suppressed and large loss will be produced. If the resistance is selected too large, the suppression ability of LCL to high frequency harmonic will be reduced. The resistance is generally taken as 0.3 to 0.4 times of the capacitance impedance at resonance frequency,

$$\text{R} \approx \frac{1}{3\omega_{res} C_f}, \tag{11}$$

where ω_{res} is the resonant frequency of the system, and C_f is the capacitance value in LCL. The value of R is taken as 4 Ω

3.4.2. Selection Guideline of the Capacitor

The selection of the DC side capacitance parameters, C_1 and C_2, is related to DC side voltage ripple γ_v, switching frequency f_{sw}, current peak I_m, and DC side voltage average value U_{avg}.

Voltage ripple of the DC side voltage can be expressed as follows:

$$\gamma_v = \frac{U_{\max} - U_{avg}}{U_{avg}} = \frac{U_{avg} - U_{\min}}{U_{avg}}, \tag{12}$$

where U_{min} and U_{max} are the minimum and maximum values of the DC side voltage, respectively.

According to (12), the following equation can be obtained:

$$U_{max} = U_{avg} + \gamma_v U_{avg}, \tag{13}$$

$$U_{min} = U_{avg} - \gamma_v U_{avg}. \tag{14}$$

Because $Q = it$ and $Q = CU$,

$$\Delta U_{\max} = U_{\max} - U_{avg} = \gamma_v U_{avg} = \frac{\Delta Q}{C} = \frac{1}{C} T_S I_m \tag{15}$$

According to Equation (14), the DC side capacitance, C, is

$$C = \frac{1}{\gamma_v U_{avg}} T_S I_m = \frac{1}{\gamma_v U_{avg} f_{SW}} I_m, \tag{16}$$

where γ_v is 0.8%, T_S is the switching period, f_{sw} is 10 kHz, U_{avg} is 400 V, I_m is 28.28 A, and thus C = 883.75 μF. Therefore, the DC side capacitances, C_1 and C_2, can be selected as 1000 μF.

4. Simulation Study

Based on the analysis of the nine-level topology, the following simulation studies were performed. The simulation parameters were as follows. The voltage, V_1, of C_1 was 300 V, the voltage, V_2, of C_2 was 100 V, f_{sw} was 10 kHz, the grid side voltage was 220 V, and the grid side frequency, f, was 50 Hz.

4.1. Balanced Load and Power Grid

As shown in Figures 12–14, the THD of the B-phase grid side current was reduced from 30.77% to 1.11% when the power grid and load were balanced, which highlights the advantages of harmonic suppression of the novel nine-level APF system. Simultaneously, to verify the real-time property of the APF system, the rapidity and reliability of the proposed compound capacitor voltage control strategy were evaluated. When the simulation time was 1.2–1.3 s, a nonlinear load of 30 Ω was connected in parallel and then cut off. It can be seen from Figure 14a, it can be observed that the grid side current was restored to steady state within 0.01 s. Figure 15 also shows that the capacitances can be well stabilized at approximately 300 V and 100 V, and that the voltage ripple does not exceed 1%.

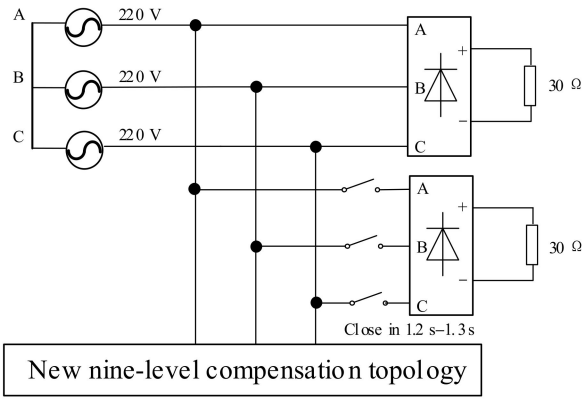
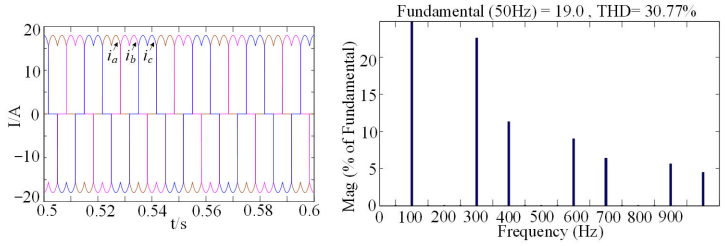
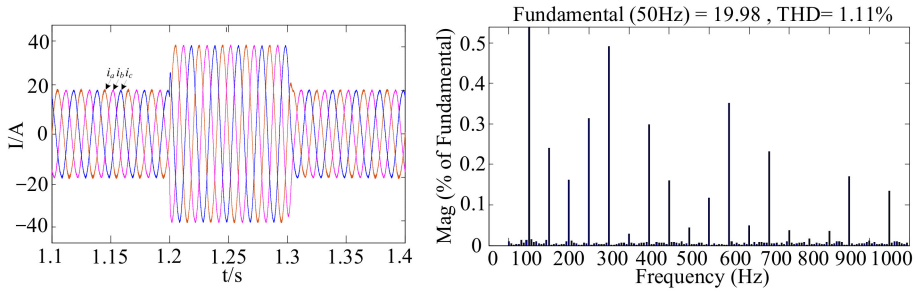


Figure 12. Balanced load topology.



(**a**) (**b**)

Figure 13. Uncompensated waveforms: (**a**) current of power grid; (**b**) THD of B-phase current.



(**a**) (**b**)

Figure 14. Compensated waveforms: (**a**) current of power grid; (**b**) THD of B-phase current.

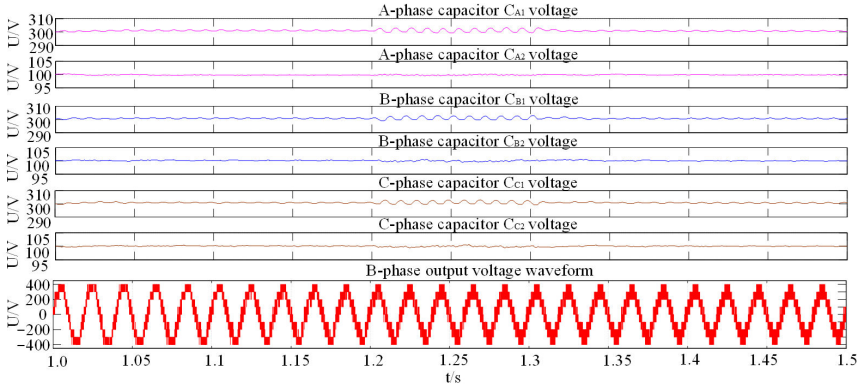


Figure 15. Capacitor voltage and B-phase output voltage waveforms.

4.2. Unbalanced Load and Power Grid

As shown in Figures 16–18, the THD of the B-phase grid side current was reduced from 31.50% to 2.91% under unbalanced grid and load conditions, therefore demonstrating that even under severe conditions, the proposed novel nine-level topology has great advantages and good adaptability in an APF harmonic suppression system. Simultaneously, the dynamic and static performance of the system under unbalanced load is verified, a nonlinear load of 30 Ω was connected to the system in parallel and then cut off at the simulation time of 1.2–1.3 s. As shown in Figure 18a, the grid side current was restored to steady state within 0.01 s. Figure 19 also shows that the capacitances can be well stabilized at approximately 300 V and 100 V, and that the voltage ripple does not exceed 1%.

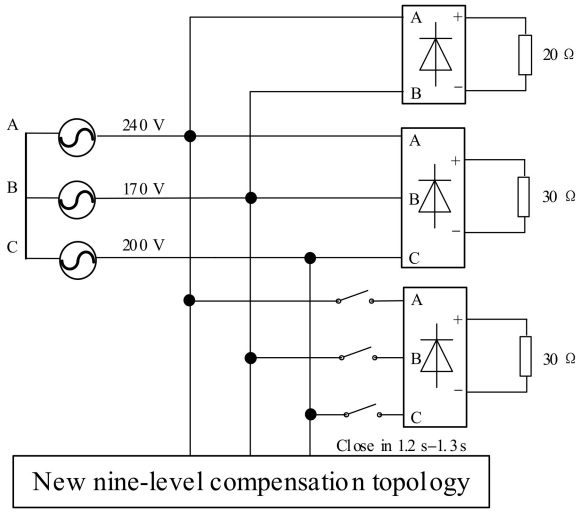
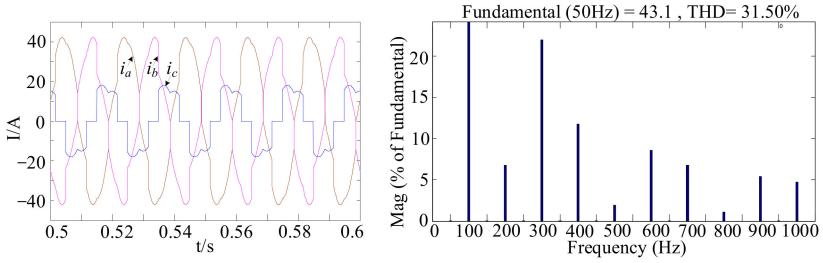
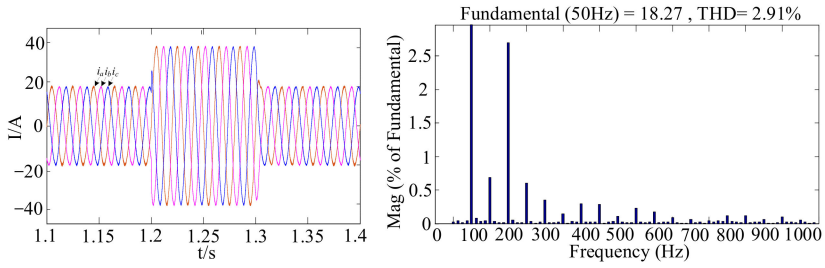


Figure 16. Topology of the unbalanced load.



(**a**) (**b**)

Figure 17. Uncompensated waveforms: (**a**) current of power grid; (**b**) THD of B-phase current.



(**a**) (**b**)

Figure 18. Compensated waveforms: (**a**) current of power grid; (**b**) THD of B-phase current.

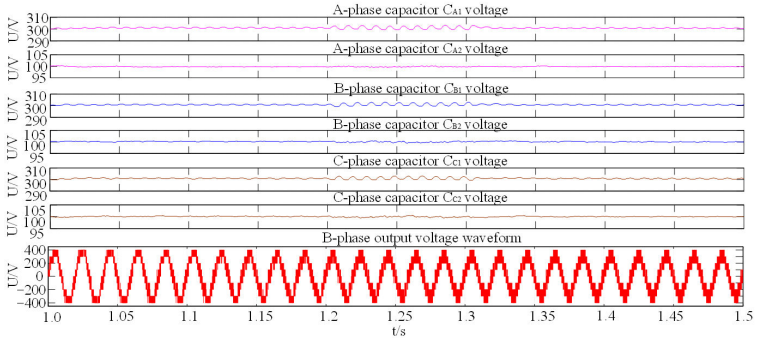


Figure 19. Waveform of capacitor voltage and B-phase output voltage.

5. Experimental Section

Based on the principle analysis and simulation research of nine-level topology, experiments were conducted. The topology proposed in this paper is asymmetric, the SW_{B1}, SW_{B2} need to withstand the $3V_2$ rated voltage, SW_{B3}, SW_{B4}, need to withstand the $2V_2$ rated voltage, SW_{B5}, SW_{B6}, only need to withstand the V_2 rated voltage, and the SW_{B7} and SW_{B8} only need to withstand the $2V_2$ rated voltage. For the convenience of the experiment, the switching devices used in this paper are all FF200R06KE3 (600 V, 200 A) (Infineon, Germany). The rise and fall time of the device is about 0.05 µs. Underrated conditions, the conduction voltage drop is 1.45 V, the conduction voltage drop is small, and the turn-on and turn-off time is short, so the switch device has good switching characteristics. Table 5 presents the key parameters of the APF system. Figure 20 shows the experimental platform of the system.

Table 5. Key parameters.

Parameters	Value
The voltage V_1	300 V
The voltage V_2	100 V
The capacitor C_1, C_2	1000 µF
The inductor L_1, L_2	2 mH, 1 mH
Three-phase balanced grid voltage	220 V, 220 V, 220 V
The balanced load R	30 Ω
Three-phase unbalanced grid voltage	240 V, 170 V, 200 V
Rectifier load R_{AB}	20 Ω

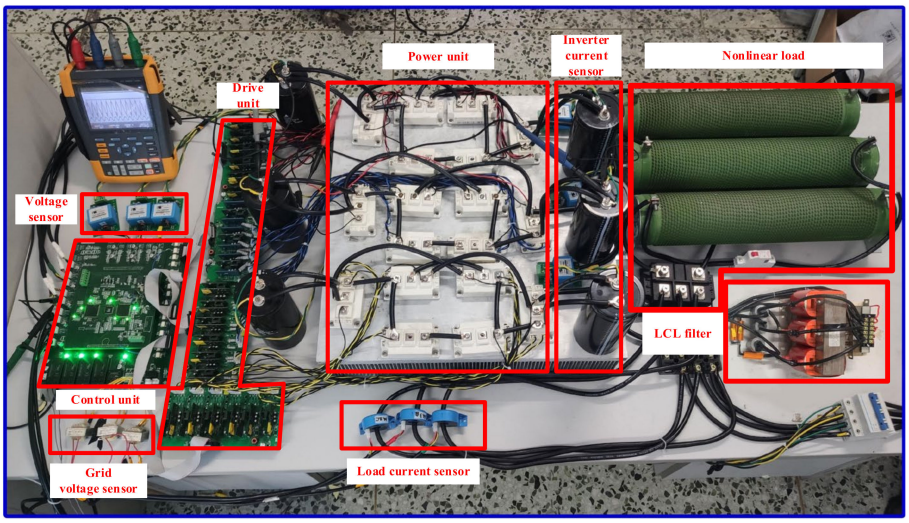


Figure 20. Experimental platform.

Figure 21 shows the start and stop process of the system. When the inverter is started, take A-phase as positive, and B-phase and C-phase as negative. Because the resistance of capacitor C_{A1} is three times that of capacitor C_{A2}, $V_{CA1} = 3V_{CA2}$, similarly, $V_{CB1} = 3V_{CB2}$, $V_{CC1} = 3V_{CC2}$, S_a, S_b, S_c switches are opened, nine-level inverter is started to establish capacitor voltage. After establishing capacitor voltage, S_a, S_b, S_c switches are closed, and the inverter is started. When the inverter is stopped, first, the grid connection switch is disconnected, then the control circuit switch is disconnected, and the voltage on the capacitor is discharged through the resistor until the capacitor voltage is zero, and the inverter stops.

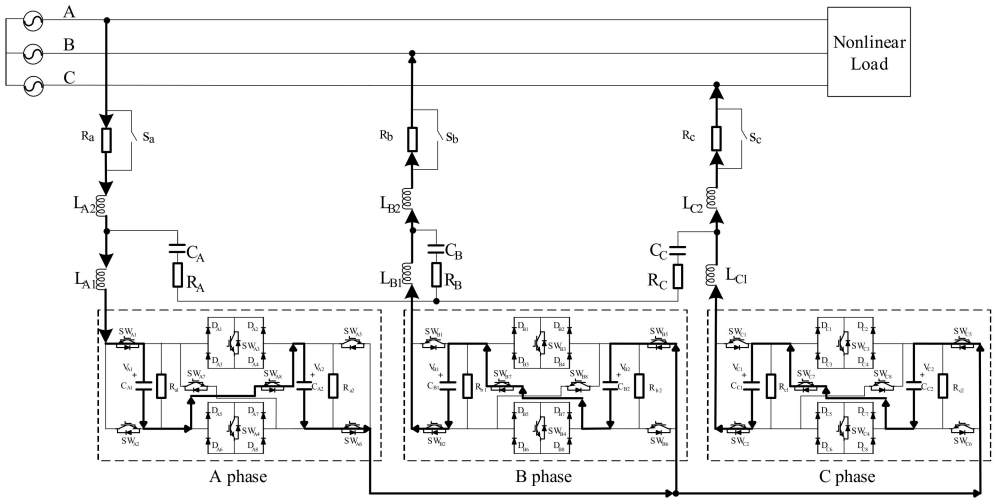
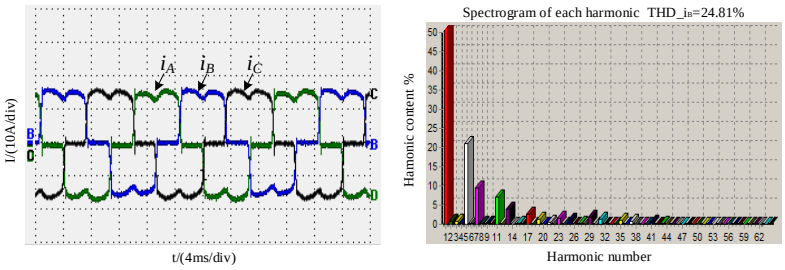


Figure 21. The start and stop process of the system.

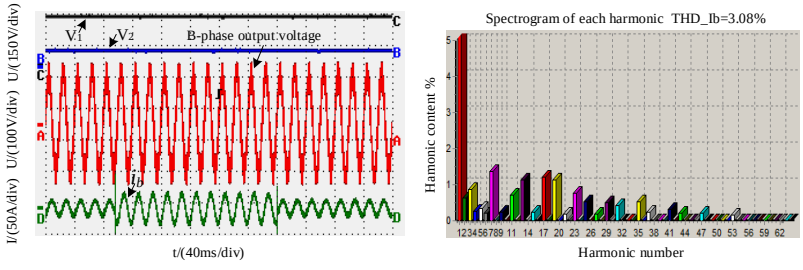
5.1. Balanced Load and Power Grid

As shown in Figures 22 and 23, the B-phase THD was reduced from 24.81% to 3.08% when both load and grid were balanced, which demonstrates that the novel nine-level system has a good harmonic suppression effect. Simultaneously, to verify the real-time property of the APF system, the rapidity and reliability of the proposed compound capacitor voltage control strategy were verified. According to the experimental parameters, a nonlinear load was connected in parallel for a short time and then cut off. Figure 23a illustrates that the grid side current can reach the steady state very quickly, and the capacitance voltage ripple is very small.



(**a**) (**b**)

Figure 22. Uncompensated waveforms: (**a**) current of power grid; (**b**) THD of B-phase current.



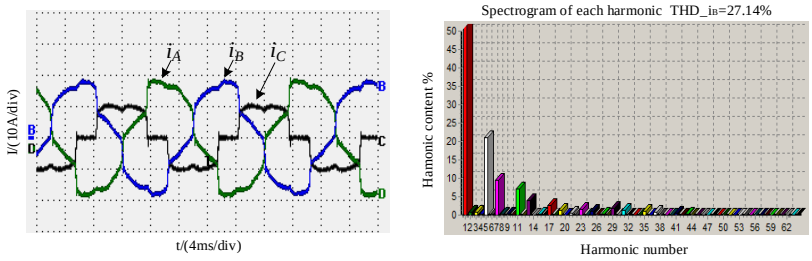
(**a**) (**b**)

Figure 23. Compensated waveforms: (**a**) current of power grid; capacitor voltage and output voltage, (**b**) THD of B-phase current.

5.2. Unbalanced Load and Power Grid

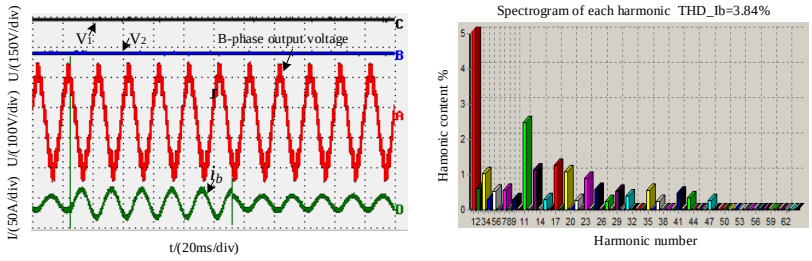
Figures 24a and 25a show the load and grid unbalance before and after the input of the three-phase current waveform APF system on the grid side. It can be observed that

before the compensation, the imbalance and harmonic content are very high, and after compensation, three-phase balance is achieved, and the B-phase THD is reduced from 27.14% to 3.84%. This indicates that harmonic suppression of the novel nine-level system is effective under unbalanced conditions. Furthermore, to verify the real-time property of the APF system, the rapidity and reliability of the proposed compound capacitor voltage control strategy were evaluated. According to the experimental parameters, a nonlinear load was put in parallel for a short time and then cut off, as shown in Figure 25a; the grid current was able to reach the steady state in a short time, and the capacitor voltage fluctuations were small.



(**a**) (**b**)

Figure 24. Uncompensated waveforms: (**a**) current of power grid; (**b**) THD of B-phase current.



(**a**) (**b**)

Figure 25. Compensated waveforms: (**a**) current of power grid; capacitor voltage and output voltage, (**b**) THD of B-phase current.

6. Discussion

In Section 4, the total harmonic distortion of B-phase current is reduced to 1.11% under the condition of grid balance, load balance, and load fluctuation. When the grid and load are unbalanced and the load fluctuates, the total harmonic distortion of B-phase current is reduced to 2.91%. It can be seen that the new nine-level active power filter proposed in this paper can still effectively suppress harmonics and the grid side current can return to a stable state in 0.1 s under bad grid conditions, which proves the rapidity and reliability of the composite control strategy. In Section 5, the total harmonic distortion of B-phase current is reduced to 3.08% under the condition of power grid and load balance fluctuation. When the power grid and load are unbalanced and the load fluctuates, the total harmonic distortion of B-phase current in the power grid is reduced to 3.84%. It is lower than the standard of harmonic content less than 5% in China's national power quality. The results show that the new nine-level active power filter has good harmonic suppression effect, and the load fluctuation is restored to a stable state in 0.1 s, which verifies the real-time performance, rapidity, and reliability of the new APF system.

7. Conclusions and Future Work

This paper proposes a novel nine-level power topology with only eight switching devices, two capacitors, and eight diodes. This topology not only increases the output level but also significantly reduces the THD of the output voltage. In addition, a compound control strategy, consisting of integrated phase voltage control and cell capacitance voltage

control, is proposed to ensure sharing voltage control of the capacitor voltage in the APF system. To verify the feasibility of the novel topology, simulations, and experimental studies were conducted. The results reveal that the capacitor voltages, V_1 and V_2, can be maintained stably at the reference value, respectively, under a balanced and unbalanced power grid. Moreover, the fluctuation of capacitor voltage V_1 is less than 3 V, and the fluctuation of capacitor voltage V_2 is less than 1 V after sudden changes in load, and the THD of the phase current is well suppressed to 3.84%. The proposed nine-level topology reduces the number of switches, further reduces the cost of the system and the complexity of control, achieves better nine levels output and achieves better control effect in the proposed control strategy. The experimental results are basically consistent with the theoretical simulation results, and the harmonic content meets the national standard. The future research work is to increase the number of output levels by optimizing the power topology to reduce the volume and cost of the device. At the same time, the capacitor voltage sharing and harmonic compensation control strategy are optimized to improve the practicability and reliability of the control device.

Author Contributions: Conceptualization, H.G.; formal analysis, H.G. and X.L.; data curation, M.R. and X.L.; writing—review and editing, S.F. and Z.L. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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