

Article

## Analysis of Threshold Voltage Flexibility in Ultrathin-BOX SOI FinFETs †

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**Abstract:** A threshold voltage ( $V_{th}$ ) controllable multigate FinFET on a 10-nm-thick ultrathin BOX (UTB) SOI substrate have been investigated. It is revealed that the  $V_{th}$  of the FinFET on the UTB SOI substrate is effectively modulated thanks to the improved coupling between the Si channel and the back gate. We have also carried out analysis of the  $V_{th}$  controllability in terms of the size dependence such as the gate length ( $L_G$ ) and the fin width ( $T_{Fin}$ ).

**Keywords:** FinFET; SOI; threshold

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**1. Introduction**

Recently, complementary metal oxide semiconductor (CMOS) device technology has faced several difficulties. Short channel effects (SCEs) such as threshold voltage roll-off and sub-threshold slope (s-slope) degradation caused by the reduced drivability of the gate electrode cause significant increase in power consumption and become a limiting factor in MOS devices [1,2]. In addition, variability of the CMOS device increases and reduces the yield of the CMOS circuit [3]. Fortunately, fin-type MOS field effect transistors (FinFETs) provide a potential solution for the nano-scale CMOS technology thanks to their high drive current while maintaining a low sub-threshold (s-) slope [4,5]. However, for FinFETs, adjustment of the threshold voltage ( $V_{th}$ ) is still a tough issue. One way of controlling the  $V_{th}$  of the MG MOSFET is to tune the work function of the gate electrode [6]. However, selection of the metal with the appropriate work function is difficult. A doped silicon channel is effective for  $V_{th}$  tuning; however, it cause severe variability due to the random dopant fluctuation [7,8].

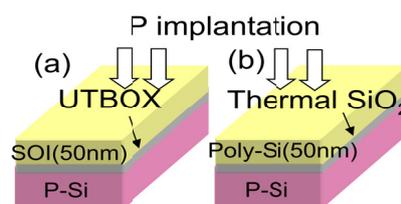
The other way of controlling the  $V_{th}$  of the FinFET is by using the substrate back bias using the SOI substrate [9–10]. In fact,  $V_{th}$  control by the substrate back bias has been investigated for the planar devices [11–14]. However, effectiveness of the back gate bias on the  $V_{th}$  of the FinFET is different due to the narrow channel. Recently, we have demonstrated a flexible  $V_{th}$  tuning for the FinFET by controlling the back bias using a 10-nm-thick ultra-thin (UT) buried oxide (BOX) silicon on insulator (SOI) substrate to demonstrate effectiveness of UTBOX for the  $v_{th}$  control of the FinFET [15,16]. Moreover, we have flexibly controlled the  $V_{th}$  by adding the second gate of the independent-double-gate FinFET [17]. In this study, we have extended the analysis of  $V_{th}$  flexibility in terms of the  $L_G$  and the  $T_{Fin}$  dependence of the  $V_{th}$  controllability using the 10 nm-thick UTBOX SOI substrate.

**2. Experimental**

*2.1. MOS Capacitor*

Prior to the device fabrication, we have evaluated the quality of the UTBOX by comparing the characteristics with thermal  $SiO_2$ . The test structure used in this study is illustrated in Figure 1. The thermal  $SiO_2$  grown at 850 °C is covered with the chemical-vapor-deposited 50-nm-thick poly-Si. Ion implantation was carried out into the top Si layer to fabricate the gate electrode. The thermally grown  $SiO_2$  with the polycrystalline-Si electrode is used as a reference sample.

**Figure 1.** The MOS capacitor test structure. (a) Ultrathin (UT) buried oxide (BOX) silicon on insulator (SOI) substrate; (b) Thermal  $SiO_2$  test structure.



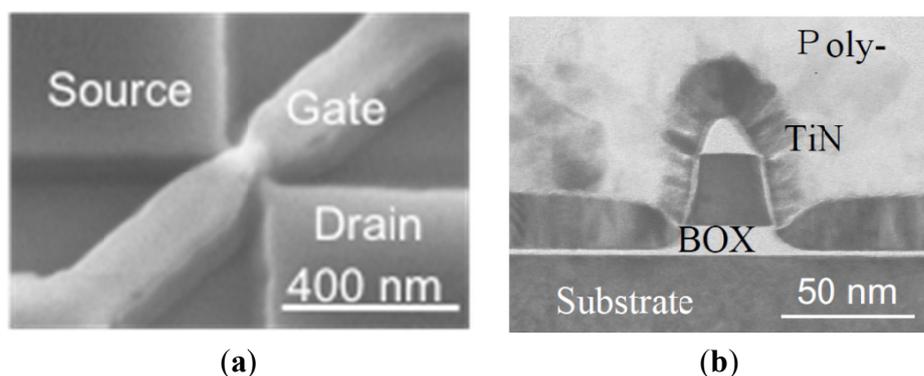
*2.2. Device Fabrication*

In this study, we have used 200-mm UTBOX SOI wafers as an initial material and have fabricated the FinFET devices on a UTBOX SOI substrate. The ellipsometrically measured thickness of the UTBOX was 10 nm. We have also fabricated the FinFET on the 120-nm-thick BOX for comparison. The fabrication process flow is summarized in Figure 2. A 50-nm-thick non-doped silicate glass (NSG) layer and the electron beam (EB) resist masks were formed to make hard masks on the wafer. To fabricate vertical Si-fins, the SOI layer was etched by a conventional reactive ion etching (RIE) using a Cl<sub>2</sub> inductively coupled plasma (ICP) as schematically shown in Figure 2. After the Si-fin etching, a 2.5-nm-thick gate-oxide was formed at 850 °C followed by the TiN and n<sup>+</sup> polycrystalline-Si (poly-Si) gate formation using EB lithography and the RIE. After the gate electrode was formed, a shallow implantation into the extension of the source/drain (S/D) was performed. To distribute impurity atoms uniformly into the vertical channel, 60-degree tilted implantation was carried out at an acceleration energy of 5 keV and a dose of  $2 \times 10^{14} \text{ cm}^{-2}$  in each side [18]. S/D implantation was performed at an acceleration energy of 10 keV and a dose of  $1.5 \times 10^{15} \text{ cm}^{-2}$  after a 50-nm-thick gate-sidewall was formed by using CVD grown SiO<sub>2</sub>. The acceleration energy was set to 10 keV to preserve the seed-crystal layer for the recrystalline annealing. Figure 3 shows the cross sectional transmission electron microscope (TEM) image of the fabricated FinFET and the plane scanning electron microscope (SEM) image of the SRAM cell. The FinFET on the UTBOX SOI is successfully fabricated. The fin height was measured as 30 nm.

**Figure 2.** Schematic process flow for the fabrication of fin-type MOS field effect transistors (FinFETs).

- (100) SOI, undoped
- (110) fin channel patterning
- Gate oxidation (Tox~2.5 nm)
- Gate formation:
  - TiN (with n<sup>+</sup>poly-Si HM)
- Gate patterning
- Extension I/I (As, 5 keV)
- Sidewall (50 nm) formation
- S/D I/I (P 10 keV,  $1.5 \times 10^{15} \text{ cm}^{-2}$ )
- Dopant activation RTA (~830 °C, 2 s)

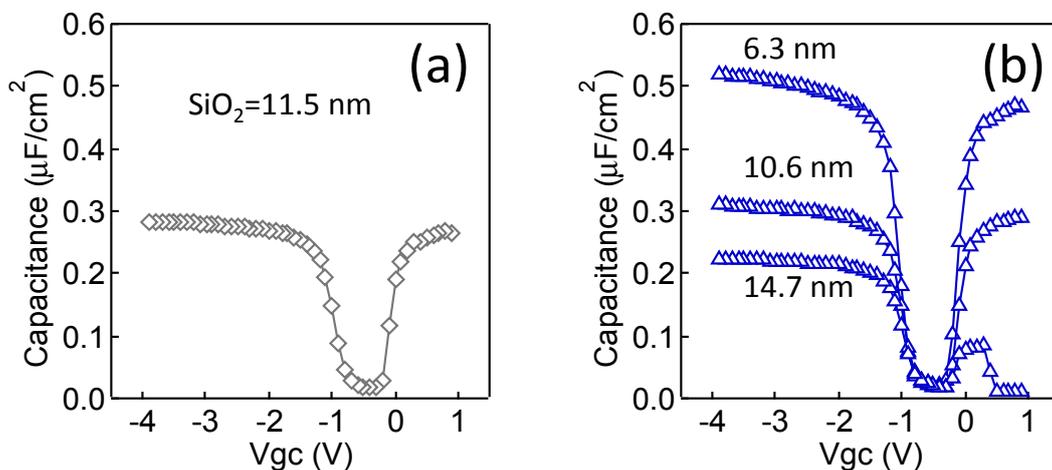
**Figure 3.** (a) SEM image of the fabricated FinFET, (b) Cross-sectional TEM image of the fabricated FinFET.



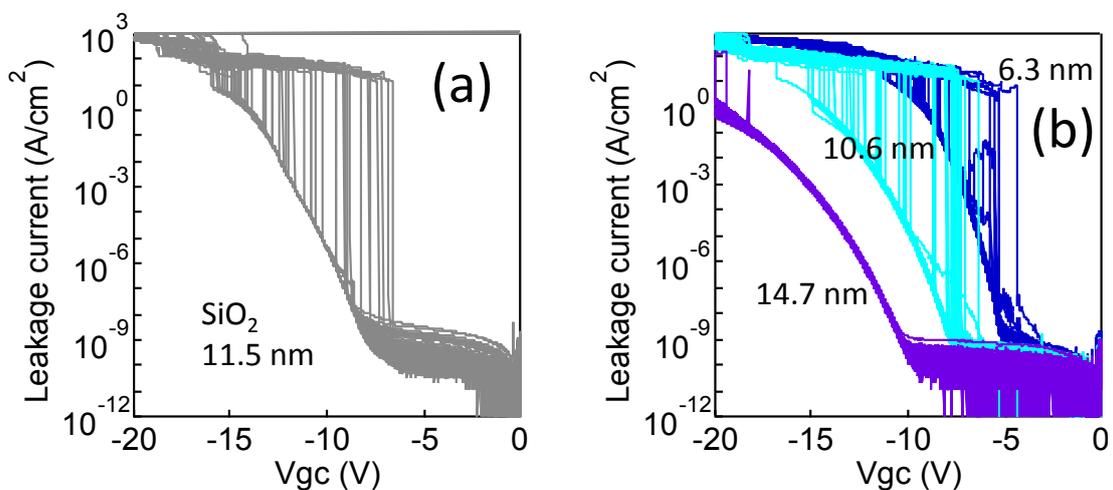
### 3. Results and Discussion

Figure 4 compares capacitance-voltage (C-V) characteristics of the UTBOX layer and the thermal SiO<sub>2</sub>. It is found that the C-V characteristics of the UTBOX layer are similar to that of the thermal SiO<sub>2</sub>. The capacitance equivalent thickness (CET) of the UTBOX is measured as 11.5 nm and the uniformity of the UTBOX thickness is as good as that of the thermal SiO<sub>2</sub>. Figure 5 compares the current-voltage (I-V) characteristics of the MOS capacitor using the UTBOX and the thermal SiO<sub>2</sub>. The I-V characteristics of the MOS capacitor with the same dielectric thickness are also the same. Figure 6 shows the gate voltage of the MOS capacitor where the leakage current exceeds 10<sup>-7</sup> A/cm<sup>2</sup> as a function of the oxide thickness. The gate voltage of the UTBOX completely follows the trend of the thermal SiO<sub>2</sub>. These results strongly indicate that quality of the UTBOX and its interface is as good as that of the thermal SiO<sub>2</sub>.

**Figure 4.** C-V characteristics of the MOS capacitor: (a) UTBOX; (b) thermal SiO<sub>2</sub>.



**Figure 5.** I-V characteristics of the MOS capacitor: (a) UTBOX; (b) Thermal SiO<sub>2</sub>. The glitches in the figure indicate the fluctuation of the breakdown in different MOS capacitors.



**Figure 6.** The gate voltage of the MOS capacitor where the leakage current exceeds  $10^{-7}$  A/cm<sup>2</sup> as a function of the oxide thickness.

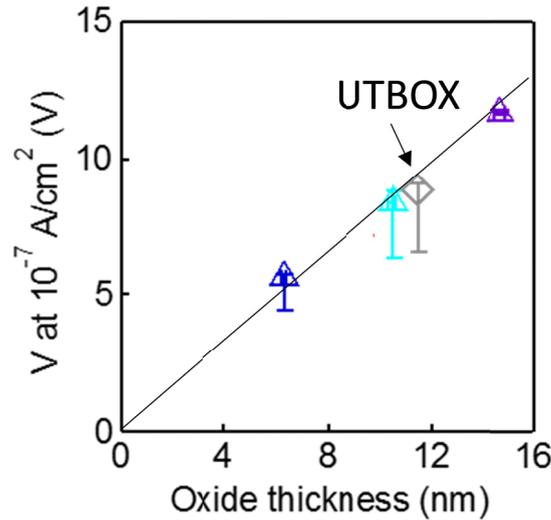
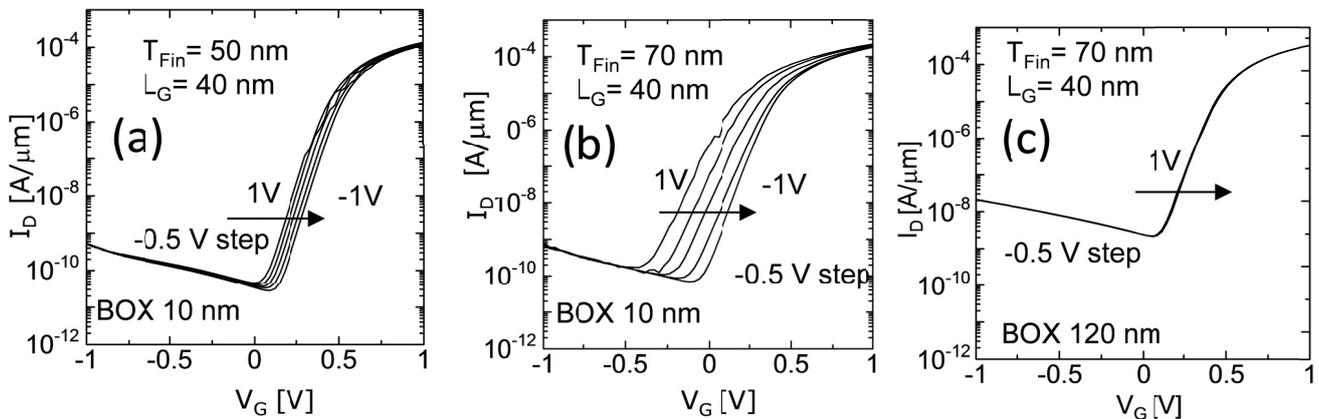


Figure 7 shows the  $I_D$ - $V_G$  characteristics of the FinFET with the UTBOX SOI and the conventional thick BOX SOI. We revealed that the  $I_D$ - $V_G$  characteristics the FinFET on the UTBOX SOI could be flexibly modified by applying the substrate bias voltage. We also found that the FinFET with the thick  $T_{Fin}$  was effective for the  $V_{th}$  modulation. Figure 8 shows the  $V_{th}$  as a function of the  $V_{sub}$ . The  $V_{th}$  is taken by the constant current method. The  $I_D$ - $V_G$  characteristics are fixed and thus the  $V_{th}$  is fixed with the conventional thick BOX substrate. Also, the effectiveness of the thick  $T_{Fin}$  for the  $V_{th}$  modulation is clearly shown. This is caused by the increased coupling between the Si body and the back gate.

**Figure 7.**  $I_D$ - $V_G$  characteristics of the FinFETs with the UTBOX and the conventional thick BOX SOI. The substrate bias voltages are ranging from  $-1$  V to  $1$  V with a  $0.5$  V step: (a)  $T_{Fin}= 50$  nm,  $L_G= 40$ nm, BOX  $10$  nm; (b)  $T_{Fin}= 70$  nm,  $L_G= 40$ nm, BOX  $10$  nm; (c)  $T_{Fin}= 50$  nm,  $L_G= 40$ nm, BOX  $120$  nm.



**Figure 8.** The  $V_{th}$  of the FinFET as a function for the substrate bias.

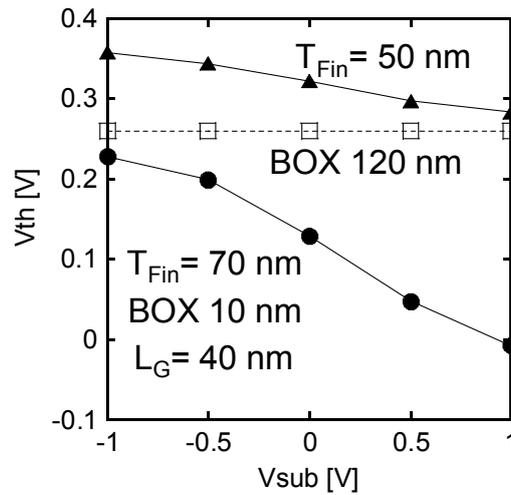
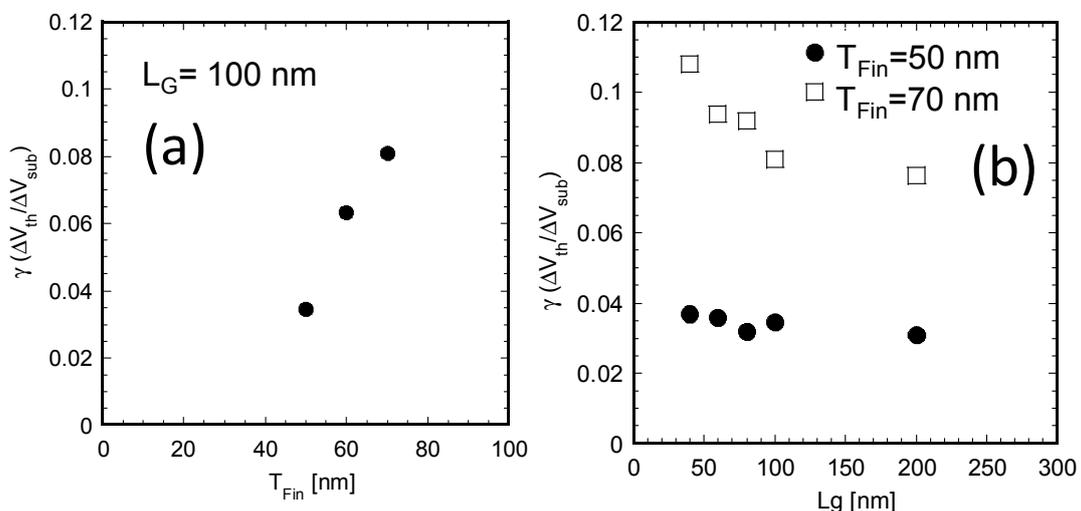


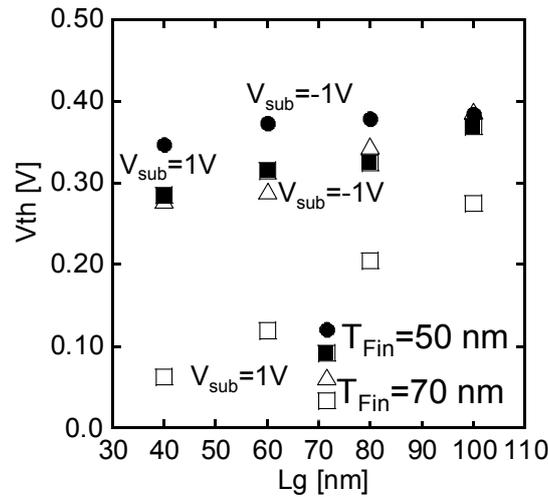
Figure 9 summarizes the size dependence of the body factor  $\gamma$  determined by the  $\Delta V_{th}/\Delta V_{sub}$ . The  $\gamma$  is increased by increasing the  $T_{Fin}$  supporting the effectiveness of the thick  $T_{Fin}$  for the  $V_{th}$  modulation. In contrast to the  $T_{Fin}$  dependence, the opposite trend with the  $L_G$  is shown and the  $\gamma$  is increased by reducing the  $L_G$ . Moreover, the  $\gamma$  exceeded more than 0.1 with the 70-nm-thick fin thanks to the 10-nm-thick UTB SOI. To understand this  $L_G$  dependence, the short channel effect represented by the  $V_{th}$  roll-off is evaluated as shown in Figure 10. We found that the  $V_{th}$  roll-off is more severe for the FinFET with the positive  $V_{sub}$ , small  $L_G$ , and the thick  $T_{Fin}$ . Thus, the  $\gamma$  becomes higher for the FinFET with the small  $L_G$  and the thick  $T_{Fin}$  due to the  $V_{th}$  roll-off. This result is consistent with the previous report on the nanowire FET with the 20-nm-thick BOX SOI [19].

Figure 11 shows the s-slope of the FinFET as a function of the  $L_G$ . The increase of the s-slope by reducing the  $L_G$  due to the short channel effect is clearly shown. It is noteworthy that the s-slope of the FinFET with the negative  $V_{sub}$  is smaller than that of the positive  $V_{sub}$ . Thus, the body bias is also effective for suppressing the short channel effects.

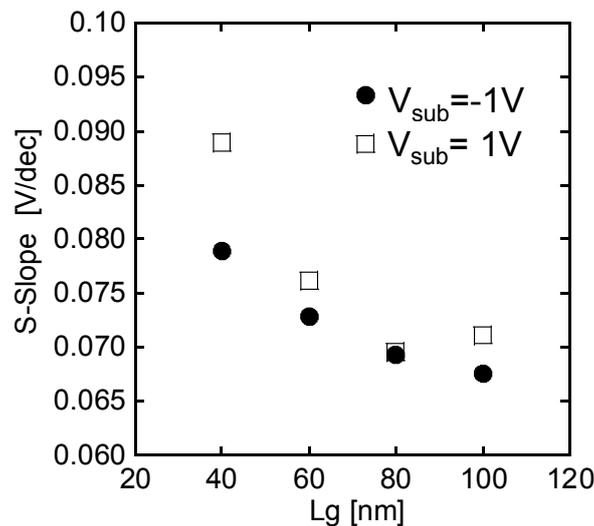
**Figure 9.** The size dependence of the body factor  $\gamma$  determined by the  $\Delta V_{th}/\Delta V_{sub}$ , (a)  $T_{Fin}$  dependence; (b)  $L_G$  dependence.



**Figure 10.**  $V_{th}$  roll-off characteristics for the FinFET with the different  $T_{Fin}$ .



**Figure 11.** The s-slope of the FinFET as a function of the  $L_G$ .



#### 4. Conclusions

The  $V_{th}$  controllable FinFETs using the 10-nm-thick UTB SOI substrate have been successfully fabricated and controllability of the  $V_{th}$  is analyzed in terms of the size dependence. It is shown that the body factor is increased by increasing the  $T_{Fin}$  and reducing the  $L_G$  and it exceeded above 0.1 thanks to the 10-nm-thick UTBOX SOI. The back gate bias is also effective for the reduction of the s-slope. Thus, the UTBOX SOI is promising for the modulation of the  $V_{th}$  and improvement of the short channel effects for the scaled FinFET.

#### Author Contributions

Kazuhiko Endo fabricated the devices and coordinated the overall research. Shinji Migita fabricated the MOS capacitor and investigated quality of the BOX layer. Yuki Ishikawa, Takashi Matsukawa, Shin-ichi O’uchi, Junji Tsukada fabricated the devices. Hitomi Yamauchi observed TEM images.

Wataru Mizubayashi, Yukinori Morita, Hiroyuki Ota, and Meishoku Masahara designed the fabrication process and discussed the results.

### Conflicts of Interest

The authors declare no conflict of interest.

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