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A Fully-Differential CMOS Instrumentation Amplifier for Bioimpedance-Based IoT Medical Devices

Israel Corbacho, Juan M. Carrillo, José L. Ausín, Miguel Á. Domínguez, Raquel Pérez-Aloe and J. Francisco Duque-Carrillo *

Departamento de Ingeniería Eléctrica, Electrónica y Automática, Universidad de Extremadura, Avenida de Elvas s/n, 06006 Badajoz, Spain
* Correspondence: duque@unex.es

Abstract: The implementation of a fully-differential (FD) instrumentation amplifier (IA), based on indirect current feedback (ICF) and aimed to electrical impedance measurements in an Internet of Things (IoT) biomedical scenario, is presented. The IA consists of two FD transconductors, to process the input signal and feed back the output signal, a summing stage, used to add both contributions and generate the correcting current feedback signal, and a common-mode feedback network, which controls the DC level at the output nodes of the circuit. The transconductors are formed by a voltage-to-current conversion resistor and two voltage buffers, which are based on a super source follower cell in order to improve the overall response of the circuit. As a result, a compact single-stage structure, suitable for achieving a high bandwidth and a low power consumption, is obtained. The FD ICF IA has been designed and fabricated in 180 nm CMOS technology to operate with a 1.8-V supply and provide a nominal gain of 4 V/V. Experimental results show a voltage gain of 3.78 ± 0.06 V/V, a BW of 5.83 MHz, a CMRR at DC around 70 dB, a DC current consumption of 266.4 µA and a silicon area occupation of 0.0304 mm^2.

Keywords: CMOS; fully-differential; indirect current feedback; instrumentation amplifier; low-voltage; wide bandwidth

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1. Introduction

Currently, an increase of the life expectancy in the population of developed countries is taking place. Therefore, new habits for healthy lifestyles are being adopted, many of them trying to implement preventive health programs and early detection of diseases, as the most effective way to improve the effectiveness of treatments and therapies and ensure, as far as possible, a high quality of life and a healthy aging. The Internet of Things (IoT) that allows data to be collected and analysed at any time and from anywhere, is called to play a fundamental role to offer a solving strategy in healthcare [1]. In IoT-based healthcare, sensors and devices are developed for a variety of objectives, such as monitoring the medical conditions of people, assisting in the treatment of diseases, and providing access to patient information. In this context, wearable devices are seamlessly connected to improve information delivery and the care-giving process in healthcare services [2]. Given the large-scale challenges caused by chronic diseases, very low cost and effective wearable devices for telemedicine have become of higher importance.

Electrical bioimpedance (EBI), or simply bioimpedance, joins the attributes to become a promising sensor technology in the IoT environment. EBI is a well-established physical concept in which an object's impedance to an applied alternating current over increasing frequencies can be measured, to assess tissue composition [3]. In addition to being economic, lightweight, easy-to-use, and noninvasive, bioimpedance can be used for a wide range of clinical applications, ranging from examine body composition in healthy people to monitoring various types of diseases such as diabetes, hypertension, and others. Therefore,

in recent years, a pronounced trend towards the integration of EBI in wearable systems has been observed.

In practice, for detecting some transient physiological events, bioimpedance spectroscopy (BIS) is used. As with any spectroscopy technique, BIS implies the measurement of the bioimpedance spectrum in a determined frequency range, for which a sequential sweep of analysis varying the frequency is carried out. Typical frequencies in BIS are in the range from several hundreds of Hz to 1 MHz, also known as the β-dispersion range. Therefore, the use of such a broad signal spectrum puts several challenges for the full integration of wearable bioimpedance-based devices into the clinical health care system. In particular, a CMOS integrated BIS system in the IoT horizon requires a great circuit optimization not only in size but also in energy consumption.

The block diagram of a bioimpedance-based IoT system for medical applications is illustrated in Figure 1. The source of power, which can be a battery or an energy harvester, is controlled by a power management unit (PMU), which optimizes and regulates the signals used to supply the rest of the blocks. The bioimpedance under test, Z_{BIO}, is excited by an AC signal, usually a current in order to avoid any damage on the biological sample, and the resulting voltage is acquired and conditioned by the analog front-end (AFE). Then, signals are efficiently processed in the digital domain, by a digital signal processor (DSP), and can be locally stored or transmitted by means a wireless protocol. The user interface allows control of the operation of the overall system.

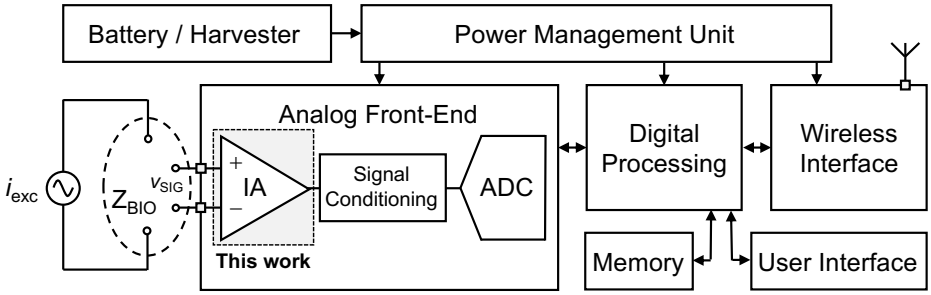


Figure 1. Conceptual block diagram of a bioimpedance-based IoT system for biomedical applications.

The IA is a critical constituent block of the system previously described [4–29]. Indeed, an appropriate signal acquisition is required, which includes a demanding performance in terms of differential-mode (DM) signals amplification, common-mode (CM) signals rejection, and noise, among others, whereas the overall power consumption has to be kept to a minimum extent, which is particularly a challenge in applications that require the processing of signals contained in a wide frequency range and with a relatively large amplitude. The indirect current feedback (ICF) technique results suitable to design a monolithic IA with low-voltage capability [5,22,29]. In addition, a single-stage ICF IA provides compactness and the possibility of achieving operation over a broad frequency range [11,12,22,26,29].

The overall performance of an analog system in general, and of an IA in particular, can be enhanced by adopting a fully differential (FD) implementation [23,25,30]. There are well-known advantages associated to this solution, such as the extension of the signal range, due to the availability of two output terminals, the increase of the linearity, thanks to the ideal cancellation of even-order harmonics, and the decrease of the effects of undesired noises coming from the supply, which can be considered as CM signals. There are also disadvantages related to the use of a FD circuit, such as the increase of the circuitry to obtain a fully symmetrical structure, with the consequent increase in area and power consumption, or the need of a CM feedback (CMFB) network, to control the CM component of the output signal. Therefore, all the pros and cons must be considered and a design tradeoff has to be established.

A FD IA, relying on the ICF technique and suitable for bioimpedance analysis in an IoT biomedical application, is presented in this contribution. An analysis of the main characteristics of the proposed circuit is provided, which is confirmed by means of simulated

and experimental results. In addition, the solution is compared in terms of circuit structure to other differential IA previously reported [29], whereas a performance comparison with similar solutions in the literature is also carried out. The circuit has been designed and fabricated in 180 nm CMOS technology to operate with a single-supply voltage of 1.8 V. The experimental characterization illustrates the robustness of the proposed solution. The rest of the manuscript has been organized as follows. Section 2 deals with the block diagram and the transistor level implementation of the IA, whereas different design considerations are discussed in Section 3. Measurement results are reported in Section 4 and conclusions are drawn in Section 5.

2. Principle of Operation

The block diagram of the proposed FD IA is described in order to clearly understand the role of each constitutive section. In addition, the transistor level implementation of both the core of the IA and the CMFB network are also detailed.

2.1. Block Diagram

Different approaches to implement a differential IA have been previously reported [9,17–20,23–25,29]. Among them, there are solutions based on the ICF technique, as the pseudo-differential (PD) IA proposed in [29], the block diagram of which is illustrated in Figure 2a. The sections G_{mI} and G_{mO} are an input and an output (or feedback) transconductor, used, respectively, to process the input signal and establish the current feedback. When the input signal, $v_{I,DM}$, is applied to the transconductor G_{mI}, a current i_I is generated. Similarly, an output current i_O is produced when the voltage $v_{SENSE} - V_{REF}$ is applied to the input terminals of the voltage-to-current (V-to-I) converter G_{mO}. The voltage v_{SENSE} is used as feedback signal and V_{REF} is a reference voltage used to set the DC component of v_O to the intended level. In the particular case of Figure 2a, a single-stage structure is represented, in which an unitary feedback loop is established. Indeed, the output voltages, v_O^+ and v_O^-, are shorted to the feedback terminals, v_{SENSE}^+ and v_{SENSE}^-, whereas two copies of the block G_{mO} are required to stablish the differential feedback loop. The feedback action around each output transconductor controls individually the DC level at the two output terminals and; hence, no CMFB is needed.

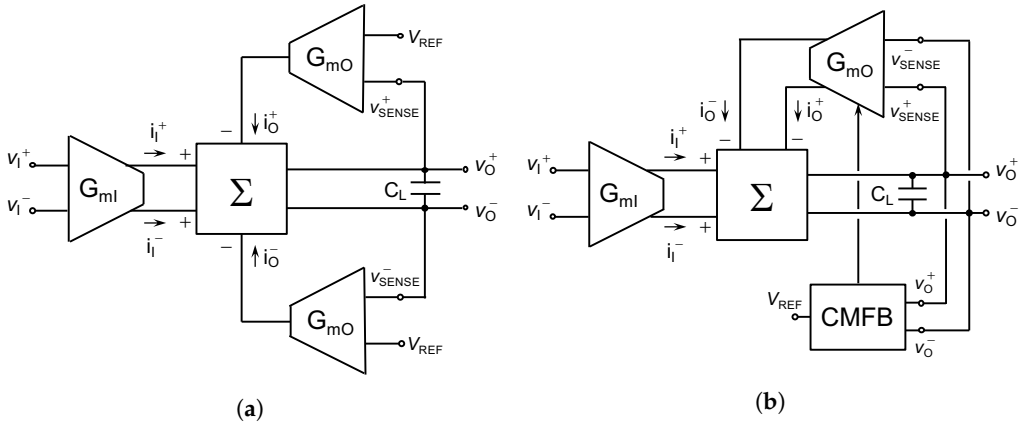


Figure 2. Block diagram of (**a**) a pseudo-differential and (**b**) a fully-differential ICF IA.

The block diagram of the proposed FD IA is depicted in Figure 2b. As observed, the feedback network is implemented differentially and, hence, only one output transconductor is required. Nevertheless, it is well known that the establishment of a differential feedback loop relies on the assistance of a CM control network, in order to dynamically set the CM component of the output voltage to the intended level. With this purpose, the CMFB section illustrated in Figure 2b has been included. As observed, the DC component of the output voltage is induced to be equal to V_{REF} by the CMFB circuit, rather than being applied to the output transconductor, as it is done in the PD structure in Figure 2a. The existence of

well-differenced signal paths for the DM and CM components in the FD approach allows the individual optimization of their response, which is not possible in the PD solution, where the control of the output CM voltage is embedded in the implementation of the output section of the circuit.

A hand analysis of the block diagram in Figure 2b led to the following transfer function for the system:

$$H(s) \equiv \frac{v_o(s)}{v_i(s)} = \frac{G_{mI} \cdot \left(R_{out} \parallel \frac{1}{sC_L}\right)}{1 + G_{mO}\left(R_{out} \parallel \frac{1}{sC_L}\right)} \tag{1}$$

where R_{out} and C_L are the output resistance and the load capacitance, respectively, of the summing stage. Assuming a high gain for the loop around the transconductor G_{mO}, the voltage gain, A_v, and the BW of the IA are inferred from (1) and can be expressed as:

$$A_v \equiv \frac{v_o}{v_{i,dm}} = \frac{G_{mI}}{G_{mO}} \tag{2}$$

$$BW = \frac{G_{mO}}{C_L} \tag{3}$$

The voltage gain of the IA is adjusted by means of the ratio of G_{mI} and G_{mO}. In addition, a proper value of C_L has to be selected in order to ensure an optimal phase margin and, hence, appropriate frequency and time responses.

2.2. Transistor Level Implementation

The transistor level implementation of the proposed FD IA is illustrated in Figure 3, where the different circuit sections are labelled at the bottom. The V-to-I conversion at the input (output) transconductor is carried out by a resistor and two voltage followers. The input (output) voltage is applied to resistor R_I (R_O) through two super-source-follower (SSF) sections, which act as voltage buffers. The SSF block incorporates an implicit feedback loop, implemented by transistors MDI and MFI (MDO and MFO), that reduces the effective output resistance of the block and makes its voltage gain very close to unity, regardless of the value of the linearization resistor. As a result, the value of R_I (R_O) can be greatly reduced without hardly affecting the operation of the SSF sections, which allows a reduction in the noise contribution of the resistor to be made, as well as the silicon area occupied by this passive component. The SSF structures are biased by means of devices MSUI and MSDI (MSUO and MSDO), which are single-transistor current sources providing tail currents $2I_B$ and I_B, respectively. The gate terminals of these transistors are connected to the corresponding bias voltage, V_{BN} or V_{BP}, in the biasing network represented at the left of Figure 3. Capacitors C_{C1} to C_{C4} are used to optimize the phase margin of the feedback loop inherent in each SSF cell. The effective transconductance of the input and output V-to-I cells is equal to:

$$G_{m,eff} \equiv \frac{i}{v_{DM}} = \frac{2}{R} \frac{1}{\left[1 + \left(1 + \frac{2}{R}\frac{1}{g_{m,MD}}\right)\left(\frac{g_{o,MD}+g_{o,MSD}}{g_{mF}}\right)\right]} \approx \frac{2}{R} \tag{4}$$

where $g_{m,Mi}$ and $g_{o,Mi}$ are the transconductance and output conductance, respectively, of transistor Mi, at the input and the output transconductor, R is the linearization, or source degeneration, resistor (R_I or R_O), and $g_m \gg g_o$ has been assumed. The factor of 2 in (4) indicates that the current signal generated in the input and the output transconductor, i_I and i_O, respectively, is conveyed to the output terminals of the IA by the two branches of the circuit section. In addition, the second term in (4), multiplying the main contribution $2/R$, represents the load regulation effect of resistor R on the voltage buffers. In first order of approximation, the effective transconductance of each V-to-I converter is approximately equal to two times the inverse of the linearization resistor.

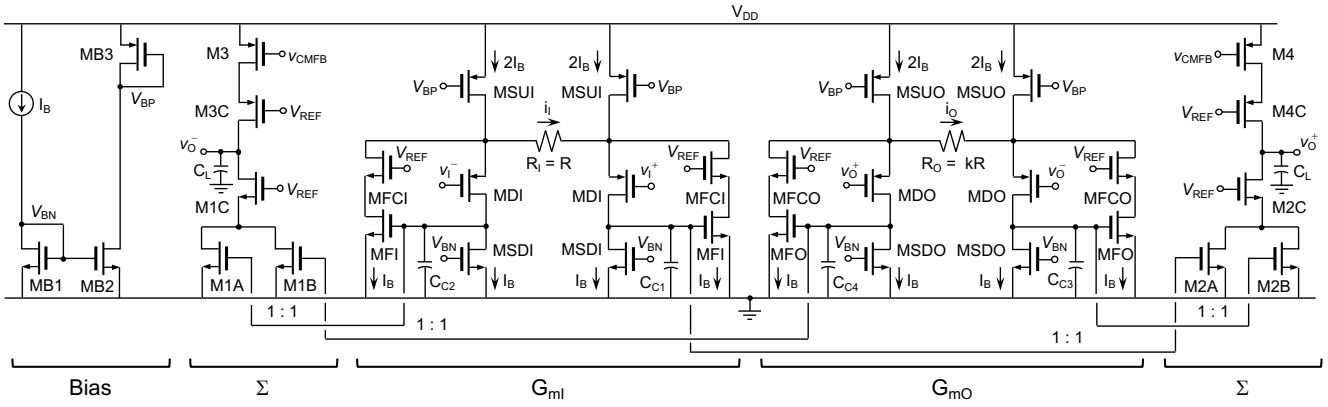


Figure 3. Transistor level implementation of the proposed fully-differential IA.

The current signals generated at G_{mI} and G_{mO} are mirrored to the output nodes of the IA by using current mirrors with gains $1:1$. Cascode transistors are used in the output branches in order to increase the output resistance and, hence, the open-loop voltage gain. In addition, cascode devices MFCI and MFCO are used in G_{mI} and G_{mO}, respectively, to ideally cancel out the systematic offset in the current reflections. Additional design flexibility to adjust the voltage gain and bandwidth of the IA to the intended values can be obtained by sizing the current mirrors with a gain different from unity [29]. The voltage gain and the BW of the proposed IA can be specified by considering the general expressions (2) and (3), along with the equation of the effective transconductance in (4), and can be rewritten as:

$$A_v \approx \frac{R_O}{R_I} \tag{5}$$

$$BW \approx \frac{2}{C_L R_O} \tag{6}$$

The input CM voltage of the FD IA in Figure 3 can be adjusted over a reasonably wide range. Indeed, the operation for input signals around the midsupply is ensured by adequately setting the aspect ratio of the input devices, so that the upper current source transistors, MSUI, can operate in saturation. Thus, the maximum level of the input CM voltage that can be achieved close to V_{DD} is constrained by the operation in saturation of transistors MSUI. Furthermore, the operation for $v_{I,CM}$ around ground can be easily achieved by proper sizing of transistors MFI. Indeed, the voltage at the drain of transistors MDI, which could force their operation in the triode region, can be reduced to an appropriate level by increasing the aspect ratio of transistors MFI, thus ensuring the operation of the input drivers in saturation.

The structure of the CMFB network used to control the DC level of the output voltage is depicted in Figure 4. A current-mode approach, based on generating a CM current signal that is a function of the output CM voltage, has been followed. The output voltages of the FD IA are used as input signals in the CMFB section and are applied to the inputs of two cross-coupled differential pairs. The other two input terminals of the CMFB are connected to the reference voltage V_{REF}. Assuming the voltage difference $v_O^+ - v_O^-$ small and, hence, the differential pairs operating within their linear region, a current signal i_{cm}, proportional to the output CM voltage, is generated. This current, superimposed to a DC level nominally equal to $2I_B$, is mirrored by a NMOS and a PMOS current mirror and injected into the FD IA through the terminal v_{CMFB}. The CM loop is closed through the output branches of the IA, which are connected to the input of the CMFB network. The action of the feedback loop forces the CM component of the output voltage to be equal to V_{REF}, setting the DC level of the output voltage to this value. The dominant pole of the feedback loop established for the CM signal is the same to that of the DM loop and is determined by the load capacitor. The secondary poles in both cases, DM and CM signals, are associated to low impedance nodes,

that is, the corresponding time constants are the product of a low resistance, in general the inverse of a transconductance, and a parasitic capacitance. As a consequence, the frequency compensation of the DM and CM loops in the FD IA can be easily achieved by properly setting the value of the load capacitor. Indeed, the value of C_L must be adjusted to have a phase margin higher than 60º in both the CM and the DM feedback loop.

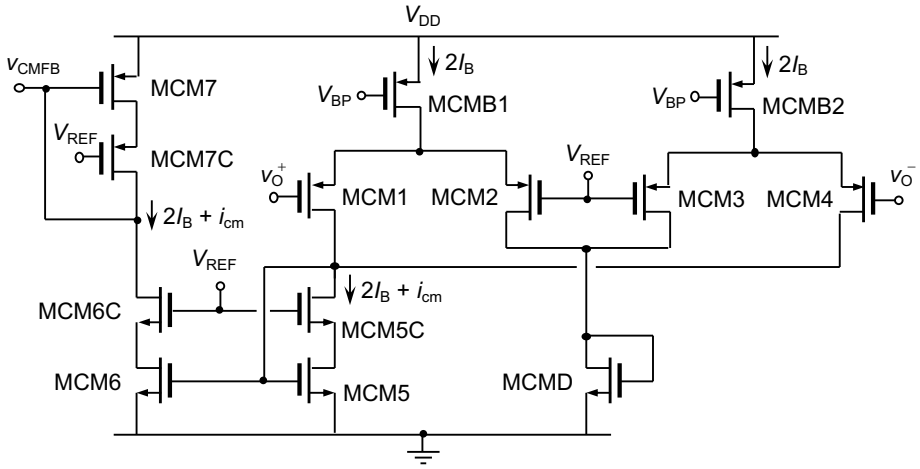


Figure 4. Transistor level implementation of the CMFB network.

3. Design Considerations

The main features of the FD IA proposed are analysed and discussed in view of the fundamental performance, in order to facilitate the design procedure. In a FD implementation, the CM signal must be processed at least with the same accuracy and speed as the DM signal. Therefore, the CMFB network, in particular, and the CM feedback loop, in general, must be designed so that the open-loop gain (LG) and gain-bandwidth product (LGBW) of both components are similar [30]. This requirement can be analytically expressed as

$$LG_{CM} \simeq LG_{DM} \tag{7a}$$

$$LGBW_{CM} \simeq LGBW_{DM} \tag{7b}$$

Therefore, it is recommendable to provide similar paths to the DM and the CM signal in order to accomplish these requisites. In the case of the IA represented in Figures 3 and 4, the output branch of the core circuit (Figure 3) is common to both the DM and the CM section. Nevertheless, the differential input stage of each loop, and hence the corresponding effective transconductance, is different in every case. Indeed, for the DM signal, the input transconductance is given by (4), whereas for the CM component the transconductance is equal to the individual transconductances of transistors MCM1 to MCM4 in Figure 4. As the linearization carried out in G_{mI} implies a reduction of the transconductance value, it is expected that effective input transconductance of the DM loop is lower as compared to the CM loop. This fact ensures that an appropriate treatment of the DM signal will result in an adequate processing of the CM signal.

Regarding the signal processing of the FD IA, only the DM component gives rise to an output current in the input and output V-to-I converters, being the CM signal rejected by the differential structure of these stages. However, a CM signal can also produce an output current, given that the presence of mismatches is unavoidable in a real implementation. In order to evaluate the impact of the join action of a CM signal and the mismatches on the output current produced, the residual transconductance of the input and the output transconductor in the IA, defined as $\Delta G_m \equiv \frac{i}{v_{CM}}$, has been analytically calculated. With this purpose, each small signal parameter g_i has been assumed to have values equal to $g_i + \Delta g_i/2$ and $g_i - \Delta g_i/2$ for a given pair of ideally matched transistors. In addition, the contributions to the residual transconductance, due to considering mismatches in every

pair of transistors, have been evaluated individually. The corresponding expressions were obtained by means of a hand analysis and the main terms were determined by simulations, resulting to be dominant the responses associated to mismatches in the transconductance (Δg_m) and output conductance (Δg_o) of the input driver transistors, MDI and MDO. The corresponding expressions are:

$$\Delta G_m|_{\Delta g_{m,MD}} \approx \frac{2}{R} \cdot \frac{\Delta g_{m,MD} g_{o,MD}}{g_{m,MD}^2} \cdot \frac{1}{\left[1 + \frac{2}{R} \frac{1}{g_{m,MD}} \left(\frac{g_{o,MD}+g_{o,MSD}}{g_{m,MF}}\right)\right]} \tag{8a}$$

$$\Delta G_m|_{\Delta g_{o,MD}} \approx \frac{2}{R} \cdot \frac{\Delta g_{o,MD}}{g_{m,MF}} \cdot \frac{1}{\left[1 + \frac{2}{R} \frac{1}{g_{m,MD}} \left(\frac{g_{o,MD}+g_{o,MSD}}{g_{m,MF}}\right)\right]} \tag{8b}$$

where MD represents the driver transistors in G_{mI} and G_{mO}. The impact of the transconductance and output conductance mismatches of other transistors on ΔG_m is negligible and, hence, is not reported here for the sake of conciseness.

The use of the CM rejection ratio (CMRR) is a very widespread habit in order to compare the magnitude of the CM gain with respect to the DM gain. As the proposed IA has a single-stage structure, the voltage gain for DM and CM signals will be given by the product of the input transconductance and the output impedance. Assuming the same output impedance for both signal components, the CMRR of the IA can be expressed in terms of the ratio of the effective and the residual transconductance, given respectively by (4) and (8b), as:

$$CMRR \equiv \frac{G_{mI}}{\Delta G_{mI}} = \frac{1}{\left(\frac{\Delta g_{m,MDI} g_{o,MDI}}{g_{m,MDI}^2} + \frac{\Delta g_{o,MDI}}{g_{m,MFI}}\right)} \cdot \frac{\left[1 + \frac{2}{R_I} \frac{1}{g_{m,MDI}} \left(\frac{g_{o,MDI}+g_{o,MSDI}}{g_{m,MFI}}\right)\right]}{\left[1 + \left(1 + \frac{2}{R_I} \frac{1}{g_{m,MDI}}\right) \left(\frac{g_{o,MDI}+g_{o,MSDI}}{g_{m,MFI}}\right)\right]} \tag{9}$$

The most-right term in (9) represents the ratio of the load regulation effects of resistor R for the CM and the DM signals, respectively. Thanks to the improved response of the SSF cell, the value of these terms is very close to unity, which allows the expression of the CMRR as a function of the different mismatches in the actual implementation of the circuit. At this point it is worth to mention that, as observed in Figure 2, the structure of the input section of both the PD IA and the FD IA is the same and, hence, both structures present a similar rejection to CM signals form the architecture point of view.

Another key parameter for an IA is the noise, as it indicates the minimum signal level that can be processed. In the case of an IA for bioimpedance spectroscopy, the signal bandwidth required is usually wide and, hence, thermal noise is dominant. The spectral density of the input referred thermal noise has been analytically determined, assuming that the main contributions are due to the input V-to-I converter, and can be expressed as:

$$\frac{v_{iN,th}^2}{\Delta f} = \left[1 + \left(1 + \frac{2}{R_I} \frac{1}{g_{m,MDI}}\right) \left(\frac{g_{o,MDI} + g_{o,MSDI}}{g_{m,MFI}}\right)\right]^2 \cdot 4kTR_I \cdot \left[1 + \frac{4}{3}(g_{m,MDI} + g_{m,MSUI})R_I\right] \tag{10}$$

where k and T are Boltzmann's constant and the absolute temperature, respectively. The first term in (10) represents the conversion factor for referring the noise from the resistor to the input of the circuit, and is the inverse of the load regulation effect of resistor R_I on the SSF cell (see Equation (4)), the second factor is the thermal noise of resistor R_I, and the last term includes the main thermal noise contributions of the devices involved in the circuit implementation of the input V-to-I converter, G_{mI}. It can be inferred from (10) that the noise of the IA can be decreased by reducing the value of the source degeneration resistor R_I, which is possible until a certain limit thanks to the use of SSF sections.

The fact of linearizing the V-to-I converters in the IA by means of a resistor, requires a given level of biasing current to achieve a given input DM voltage range with a determined linearity. In each SSF cell in the input and output transconductors, the bias current $2I_B$ is split into two branches corresponding to the input and feedback transistors. As the tail current of the driver devices is fixed to I_B by the lower current sources, a current equal

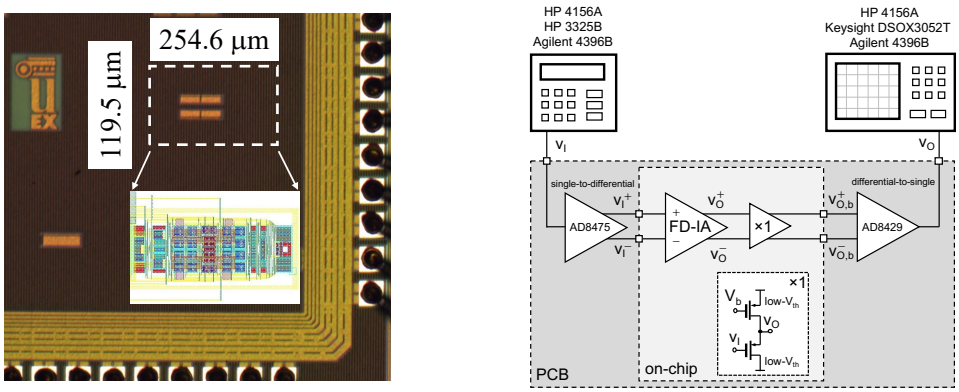
to I_B is steered towards the feedback transistors. Consequently, the maximum input DM signal that can be processed by each V-to-I converter is that leading to a current equal to zero through one of the feedback transistors. This condition can be expressed for G_{mI} as

$$v_{I,DM_{max}} = \pm R_I \cdot I_B \tag{11}$$

where the voltage gain of the SSF cells has been assumed to be equal to unity. Nevertheless, this is an extreme situation that leads to switching off one of the branches of the input transconductor. Instead, a specific criterion, such as considering a given total harmonic distortion (THD) level, is assumed in a practical case to determine the value of $v_{I,DM_{max}}$ in an objective way.

4. Experimental Results

The fully-differential IA illustrated in Figure 3, along with the CMFB section in Figure 4, has been designed and fabricated in 180 nm CMOS technology to operate with a single-supply voltage of 1.8 V. The microphotograph of the chip, including details on the layout, is depicted in Figure 5a, and the aspect ratios of the main transistors in the circuit are reported in Table 1. The measurements have been carried out over 10 samples of the silicon prototype. The testbench implemented for the experimental characterization is represented in Figure 5b, where the on-chip and the PCB levels have been highlighted. An on-chip differential voltage buffer, referred to as $\times 1$, has been included for test purposes in order to isolate the output terminals of the FD IA from heavy loads. The buffer consists of two PMOS source followers including low-V_{th} transistors, so that operation with the general 1.8-V supply is possible. Auxiliary circuits AD8475 and AD8429 in Figure 5b are used to carry out, respectively, a single-to-differential signal conversion at the input of the IA and a differential-to-single signal conversion at the output in order to facilitate measurements. Even though these commercial components have been selected with a bandwidth higher that the circuit under test, their influence on the measurement procedure is unavoidable. The value of the reference voltage V_{REF} used to set the DC level of the output voltage was set to 0.9 V. In addition, this voltage is also used to bias the gate terminal of the cascode transistors. The biasing current of each V-to-I converter, i.e., G_{mI} and G_{mO}, was adjusted as I_B = 10 µA. The source degeneration resistors R_I and R_O were implemented with non-salicided high-resistance polysilicon having values equal to R_I = 5 kΩ and R_O = 20 kΩ, thus leading to a nominal voltage gain of 4 V/V (12.04 dB).



(**a**) (**b**)

Figure 5. (**a**) Chip microphotograph and (**b**) measurement setup.

Table 1. Transistor aspect ratios (μm/μm) for the FD IA (Figure 3).

Device	W/L (μm/μm)	Device	W/L (μm/μm)
MDI	200/1	MDO	200/1
MFI	80/0.5	MFO	80/0.5
MFCI	20/0.5	MFCO	20/0.5
MSDI	16/1	MSDO	16/1
MSUI	48/1	MSUO	48/1
M1A, M2A	80/0.5	M1B, M2B	80/0.5
M1C	20/0.5	M2C	20/0.5
M3, M4	30/0.5	M3C, M4C	60/0.5

The load capacitors, C_L, were built on-chip as metal-insulator-metal devices to make stable the feedback loop established around the transconductor G_{mO}. The design criterion selected was to ensure a phase margin of 60º considering the nominal value of the load capacitors, equal to 1.33 pF each, and the parasitic capacitance also connected to the output terminals due to the test buffer. In addition, it is worth to point out that the effective value of the parasitic capacitance introduced by the test buffer slightly relies on the value of the total external capacitance, associated to the PCB and the test probe used for measurements. This external capacitance has been estimated to be around 30 pF in most of the test configurations followed. Under these conditions, the open-loop frequency response of the DM and CM signal paths has been simulated and is represented in Figure 6. For the DM signal LG_{DM} = 58.0 dB and $LGBW_{DM}$ = 5.9 MHz with a phase margin of 52.8º and a gain margin of 17.6 dB, whereas the CM signal response provides LG_{CM} = 64.2 dB and $LGBW_{DM}$ = 18.1 MHz with a phase margin of 75.5º and a gain margin of 14.3 dB. These results show the stability of both the DM and the CM feedback loop and confirm the requirements imposed in (7a) and (7b) to the CM signal path. The bandwidth of the CM signal is noticeably higher than that of the DM component. This is due to the fact that the linearization carried out in the input differential structure of the IA leads to a lower effective transconductance as compared to the CMFB section, which results in a narrower frequency range.

The DC measurements on the 10 available samples allowed to obtain an average DC supply current for the IA equal to 266.4 μA, with a standard deviation of 2.6 μA. The DC voltage level shift introduced by the on-chip buffer did not allow characterizing the actual output voltage of the IA, expected to be very close to V_{REF}. Hence, only the standard deviation of the buffered output voltage, equal to 3.63 mV, is reported in order to determine the variability of the output voltage among the different samples. The experimental $v_I - v_O$ DC transfer characteristic of the IA is represented in Figure 7. The CM level of the output voltage, defined as $(v_O^+ + v_O^-)/2$, has been used to shift all plots from their original DC level down to zero, so that results can be more easily interpreted. A linear voltage range at DC larger than ±50 mV can be inferred for the differential output response. As observed in Figure 7, the non-linearity appreciable in v_O^+ and v_O^- is cancelled out when the overall output signal is obtained as the difference of the individual responses, i.e., $v_O = v_O^+ - v_O^-$.

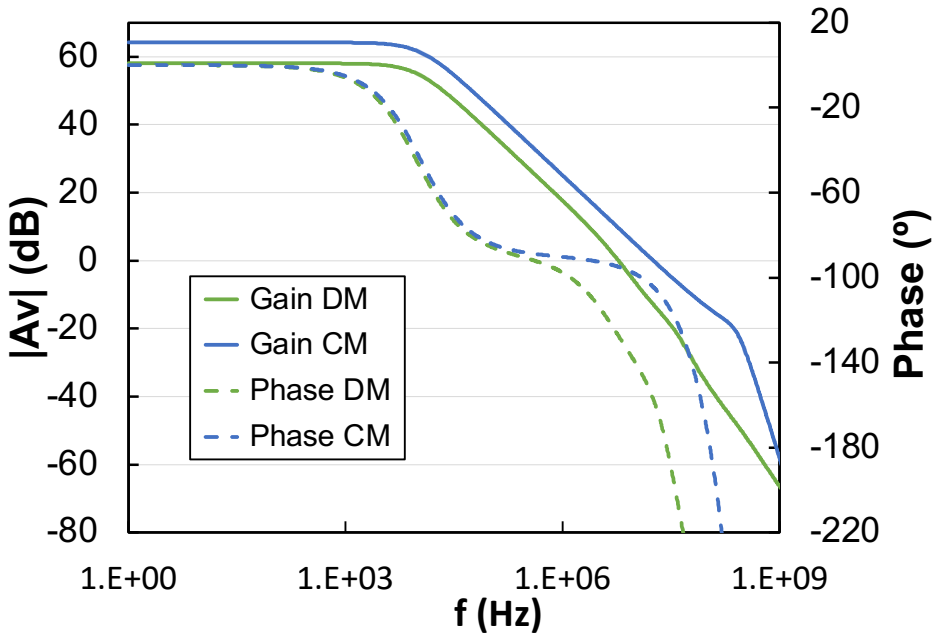


Figure 6. Simulated open-loop frequency response of the DM and CM signal paths in the proposed IA.

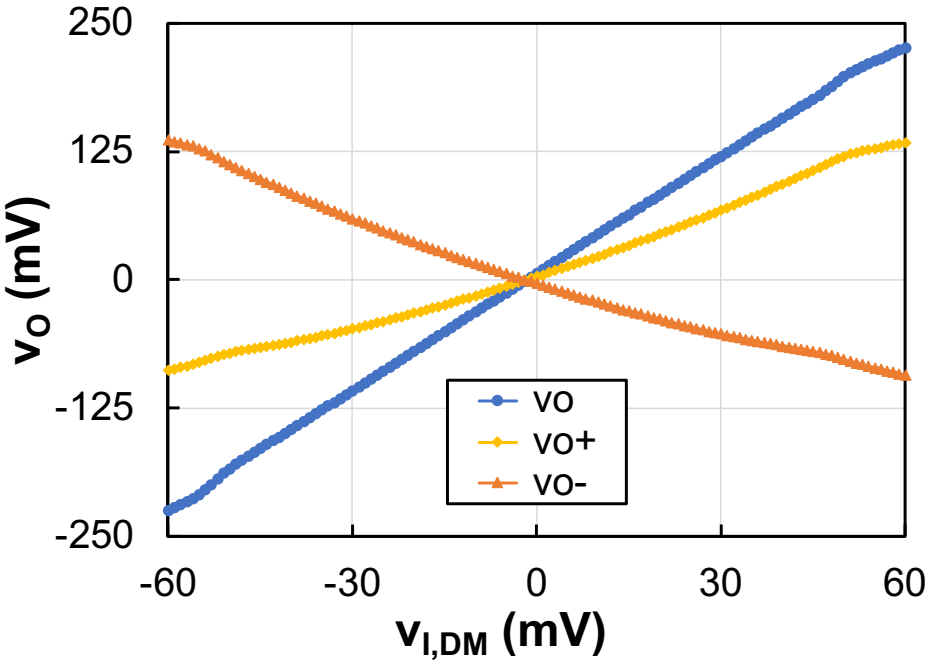


Figure 7. Input−output DC transfer characteristic.

The simulated and experimental frequency response of the IA is illustrated in Figure 8, where the magnitude of the DM voltage gain is depicted. From the experimental response the voltage gain in the passband, A_v, and the BW of the IA can be extracted, obtaining values equal to 3.78 V/V (11.4 dB) and 5.83 MHz, respectively. The gain value is in close agreement with the design value of 4 V/V or 12.4 dB (relative error of 5.0%) and with the simulated value of 3.69 V/V or 11.34 dB (relative error of 2.4%), whereas the measured BW deviates from the corresponding simulated value, equal to 7.76 MHz (relative error of 24.8%). The difference between the simulated and the experimental responses in Figure 8 has two possible reasons. On the one hand, it has been found that the on-chip voltage buffer is more sensible to external load capacitors than expected from simulations. On the other

hand, the BW of the IA is determined by the on-chip load capacitors illustrated in Figure 3, the value of which can suffer important absolute variations during the fabrication process. The nominal simulated value of the BW has been complemented with the result extracted from a 1000-run Montecarlo analysis, considering mismatch and process variations, which has been found to be equal to 10.27 ± 4.70 MHz. Considering the standard deviation as a suitable error margin, the lower bound of the statistically simulated BW encloses the values of both the nominally simulated and the measured BW. The time response of the proposed IA, depicted in Figure 9, has been used to confirm its stability. In particular, a 100-mV$_{pp}$ input signal (yellow plot) is applied and an appropriate establishment of the output voltage (green plot) can be observed.

The response to CM signals has also been obtained. The CMRR has been simulated and measured as a function of the frequency of the input signal and is shown in Figure 10. In the simulated plot (in green color), the average value, extracted from a 1000-run Montecarlo analysis including mismatch and process variations, is represented, whereas the error bars indicate the standard deviation, σ. As observed, the experimental CMRR lays below the error margin when the standard deviation is considered, but it has been proved that is enclosed by a 3-σ error region. The measured CMRR at low frequencies and at the frequency of the BW is equal to 73.3 dB and 42.0 dB, respectively. Furthermore, the impact of process, voltage, and temperature (PVT) variations on the CMRR at DC has been determined by nesting a 100-run Montecarlo analysis and a corner analysis. In particular, typical-typical (*tt*), slow-slow (*ss*), fast-fast (*ff*), fast-n-slow-p (*fs*), and slow-n-fast-p (*sf*) corners were considered for the active devices, whereas the temperature was set to values (0,27,80) ºC and the supply voltage was adjusted to (1.62,1.8,1.98) V, i.e., a variation equal to ±10% was assumed. The corresponding results are summarized in Figure 11, where in the axis corresponding to the temperature the considered range has been replicated for each corner of the active devices. As observed, the CMRR varies between 74.8 dB and 90.5 dB.

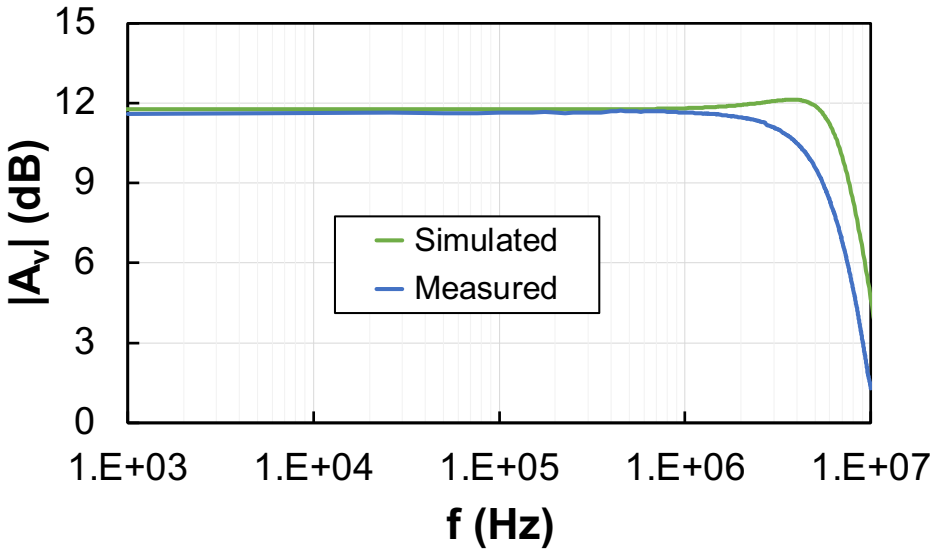


Figure 8. Simulated and measured frequency response of the proposed IA.

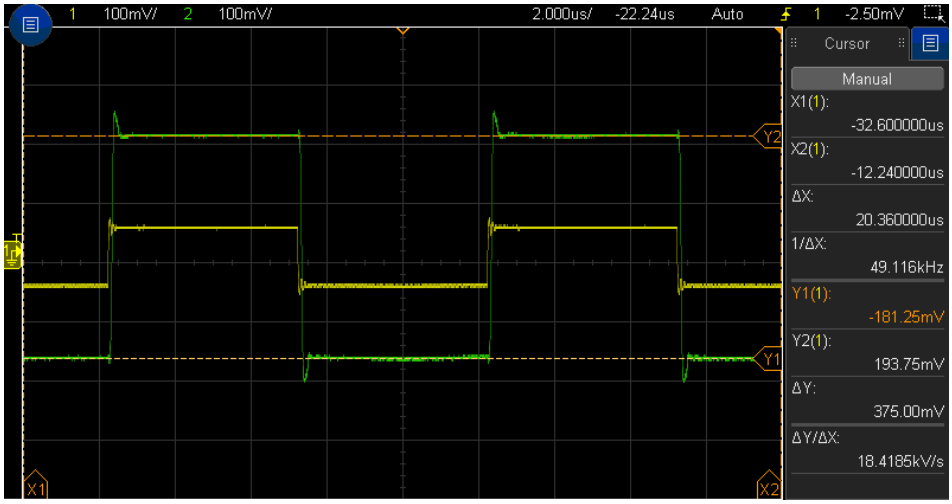


Figure 9. Transient response of the IA output voltage (green) to a 100-mV$_{pp}$ input square wave (yellow).

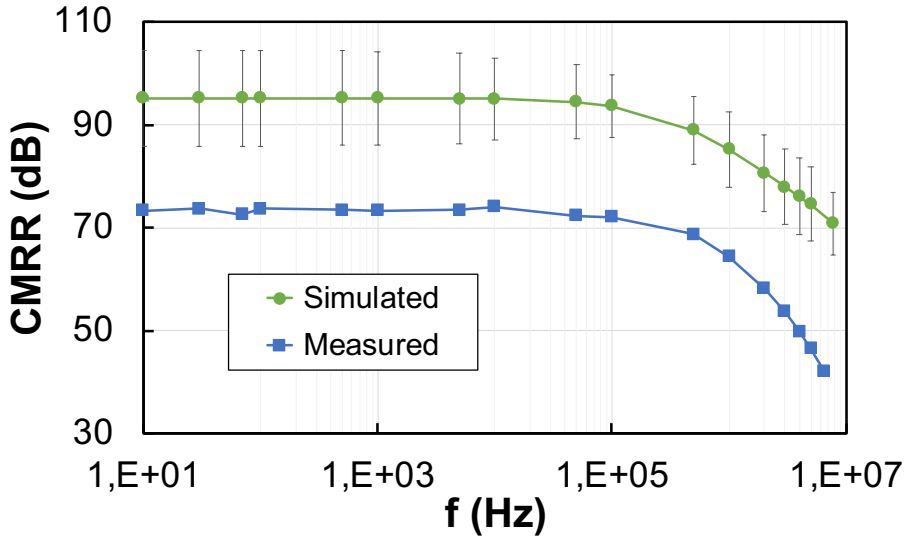


Figure 10. Simulated and measured CMRR vs. frequency.

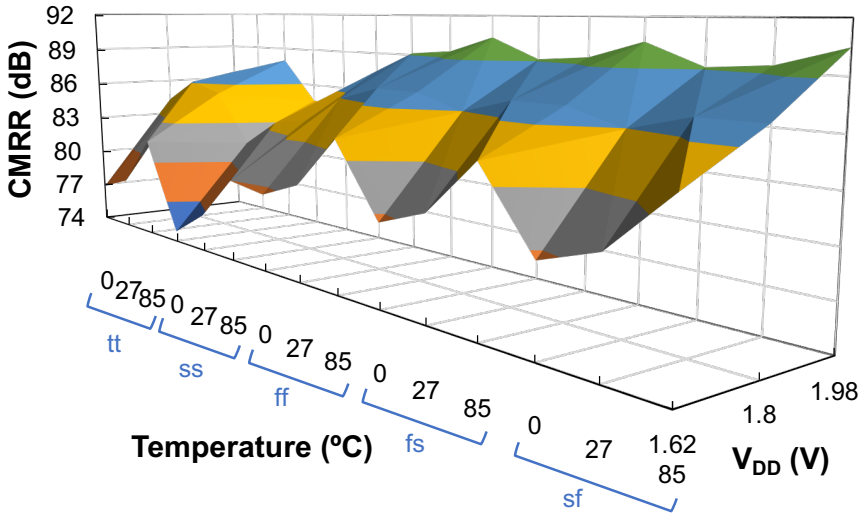


Figure 11. CMRR extracted from a Montecarlo analysis for the different corners.

The noise response of the FD IA has also been characterized. In particular, the spectral density of noise has been simulated and measured and is depicted in Figure 12. In addition, the noise has been integrated over a frequency band between 100 Hz and the frequency of the BW, obtaining a value equal to 86.4 μV_{rms}. The calculated experimental noise is slightly higher than the actual value, due to the finite approximation followed to integrate the noise. In any case, the simulated noise, equal to 74.7 μV_{rms} (relative error of 15.7%), is much lower. The reason of the noise increase in measurements is ascribed to the experimental setup and to the contributions of the different auxiliary circuits used for the test, as illustrated in Figure 5b and already indicated at the beginning of this section. The THD has been used to asses the linearity of the dynamic response of the FD IA. In Figure 13 the simulated and experimental THD of the output voltage is represented as a function of the input DM signal amplitude for frequencies of 1 kHz and 10 kHz. The simulated THD is reduced as compared to the experimental response for small values of the input signal due to the lower noise floor level in simulations. Nevertheless, for high input signals the measured response results even more linear. Using the widespread criterion of considering the 1%-THD as a limit to determine the maximum input signal that can be processed with reasonable linearity, experimental values of 59.6 mV and 57.6 mV were obtained for input frequencies of 1 kHz and 10 kHz, respectively.

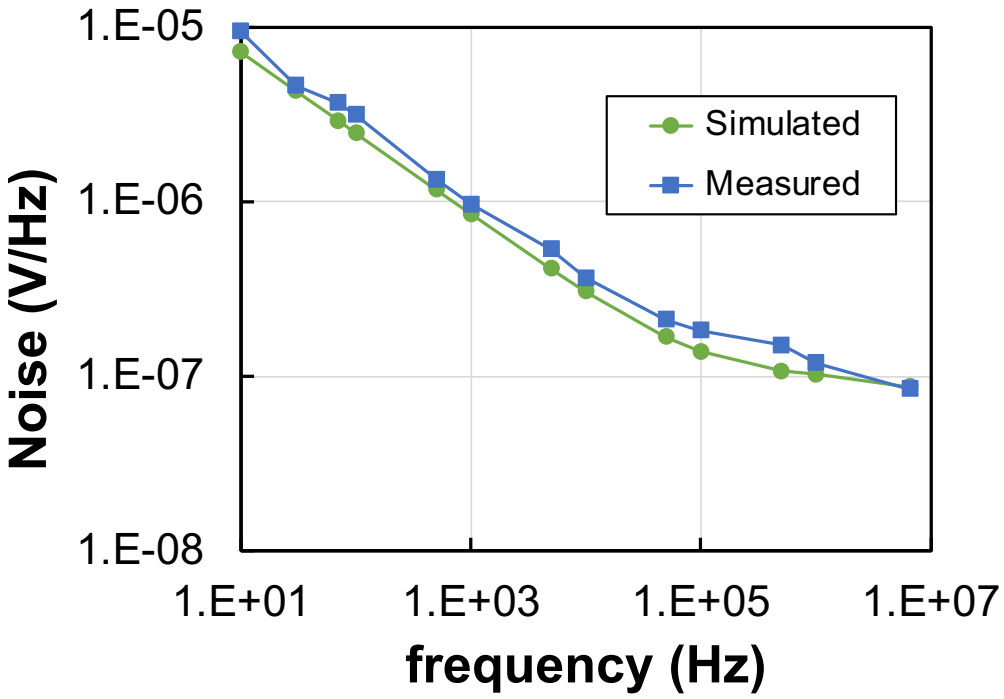


Figure 12. Spectral density of noise vs. frequency: simulated (green) and measured (blue) responses.

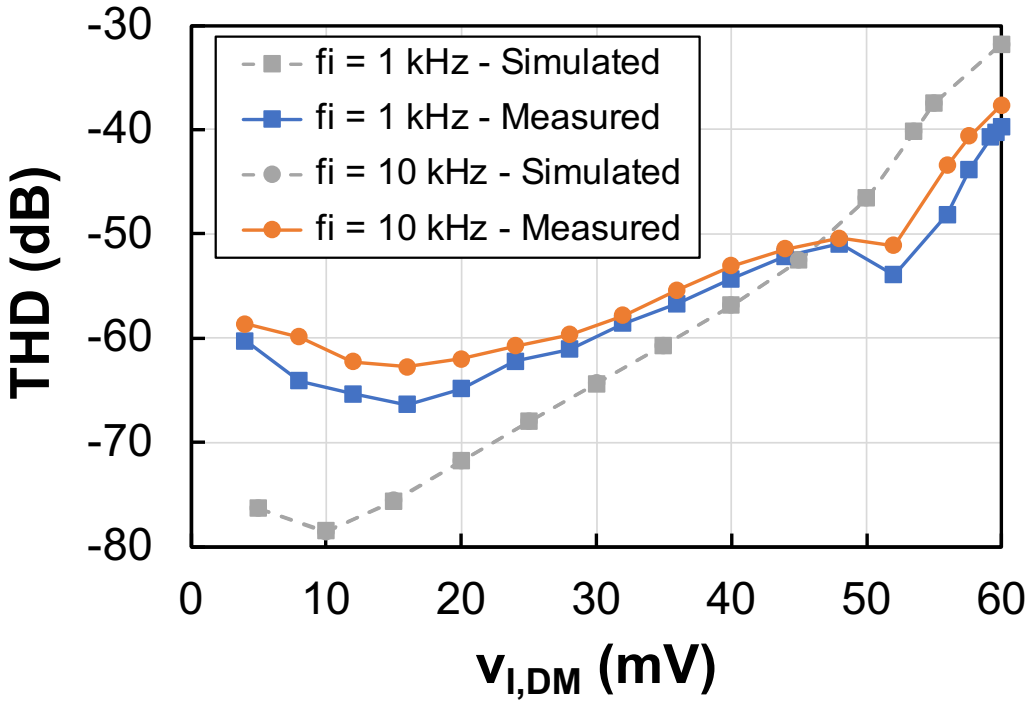


Figure 13. Simulated and experimental THD vs. $v_{I,DM}$ for f_I equal to 1 kHz and 10 kHz.

The performance of the designed and fabricated FD IA is summarized in Table 2, where simulated and measured results are reported. The data expressed as the mean value plus/minus the standard deviation were obtained from a 1000-run Montecarlo analysis with mismatch and process variations in the case of simulations and from the measurements on 10 samples in the case of experimental results. In general, there is a good agreement between the simulated and the measured metrics, being the corresponding differences due to the variations of the process parameters during fabrication. One exception is the case of the noise, which, as discussed previously, greatly increases in measurements with respect to simulations.

The comparison of the previous metrics for different IAs is done usually in terms of a widespread figure-of-merit (FoM) known as noise efficiency factor (NEF) [4]. This parameter indicates how large is the noise of a system as compared to the white noise of a single MOS transistor with the same drain current and bandwidth, and is defined as:

$$NEF = V_{iN,rms}\sqrt{\frac{2I_{DD}}{\pi V_T 4kTBW}} \tag{12}$$

where I_{DD} and V_T are the supply current of the IA and the thermal voltage, respectively. Nevertheless, this parameter does not take into account the amplitude of the signals to be processed. Indeed, when large input signals must be handled, a high biasing current is required, thus resulting in a penalty in therms of NEF. In this case, the dynamic range (DR), defined as

$$DR = 20 \cdot \log\left(\frac{v_{I,DM_{max}}}{V_{iN,rms}}\right) \tag{13}$$

can be used as a complementary FoM for performance comparison.

Table 2. Simulated vs. experimental performance of the FD IA (Technology: 180 nm CMOS, V_{DD} = 1.8 V, $A_{v,nom}$ = 4 V/V).

Parameter	Simulated	Measured
Voltage gain (V/V)	3.69 ± 0.07	3.78 ± 0.06
Voltage gain error (%)	−7.7	−5.5
BW (MHz)	10.27±4.70	5.83
$\sigma(v_O)$ (mV)	5.14	3.63
$v_I\|_{THD=-40\ dB}$ @ 1 kHz (mV)	53.5	59.6
$v_I\|_{THD=-40\ dB}$ @ 10 kHz (mV)	53.5	57.6
$v_I\|_{THD=-40\ dB}$ @ 100 kHz (mV)	53.2	59.0
$v_I\|_{THD=-40\ dB}$ @ 1 MHz (mV)	44.8	38.0
SR^+/SR^- (V/μs)	10.4/10.4	8.3/8.3
CMRR @ DC (dB)	95.1 ± 9.2	73.3
CMRR @ BW (dB)	70.8 ± 6.2	42.0
$V_{iN,rms}$ [100 Hz-BW] (μV_{rms})	74.7	86.4
I_{DD} (μA)	199.1	266.4

The FD IA presented is compared in Table 3 to other works previously reported and with similar characteristics, i.e., based on current feedback and presenting a wide bandwidth. The work by Worapishet et al. [11] presents very good values of NEF and DR, especially considering that measured results are given, but the BW is more limited than in the other solutions. The IAs in [12,22] have a good response in general, even tough they are solutions supported by simulated results. In [26] a very high bandwidth is achieved but no data regarding the size of the processed signals and the noise are reported. The IA proposed in [29] has also a differential structure and achieves a higher BW than the IA proposed here, but the signal processed are smaller and the noise is higher, thus resulting in a higher NEF and a lower DR. The proposed IA has a BW suitable for electrical bioimpedance analysis and is able to process the largest input differential signals for similar supply currents. In addition, it is a compact solution in terms of silicon area as compared to most of the other solutions, especially considering that it has a FD structure. Finally, it is worth to point out that the increase of the experimental noise, previously indicated, leads to a noticeable reduction of the measured DR and to an increase of the experimental value of the NEF. Indeed, the simulated characterization of the IA reported values for the NEF and the DR equal to 14.6 and 57.1, respectively.

Table 3. Performance comparison of the proposed IA with other works previously reported.

Parameter	[11] TCAS-I'11	[12] IMCSSD'12	[22] IJEC'20	[26] TCAS-II'21	[29] Electronics'22	This Work
Technology	0.35-µm CMOS	0.35-µm CMOS	0.35-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18 µm CMOS
Technique (*)	LCF	LCF	ICF	G_m-TI	ICF	ICF
Results	Meas.	Sim.	Sim.	Sim.	Meas.	Meas.
V_{DD} (V)	3	2	3	1.8	1.8	1.8
I_{DD} (μA)	285	240	250.6	162	219.3	266.4
Gain (dB)	34	8	34	0/40	11.4	11.4
BW (MHz)	2.0	4.0	7.6	6.7×10^{-6}/87.0	8.0	5.83
CMRR (dB)	>90 @ DC	80 @ 1 MHz	99.5 @ DC	164.4 @ 100 kHz	80.6 @ DC	73.3 @ DC
THD (dB) @ v_I (mV_{pp})	−56.2 @ 10	N.A.	−57.4 @ 10	N.A.	−61.6 @ 20	−64.9 @ 20
$v_{I,max}$ (mV)	30	N.A.	8	N.A.	53	59.6
$V_{iN,rms}$ (μV_{rms})	16	36	32.4	N.A.	92.0	86.4
Area (mm^2)	0.068	0.037	—	0.0569	0.0291	0.0304
NEF	5.9	10.8	7.2	N.A.	26.3	21.3
DR	65.5	N.A.	47.9	N.A.	52.2	56.8

(*) LCF: local current feedback; ICF: indirect current feedback; G_m-TI: transconductance-transimpedance.

5. Conclusions

An IA suitable for bioimpedance-based IoT applications and based on the ICF technique has been presented. The SSF structure has been incorporated in the design of the IA in order to reduce input referred noise and silicon area. In addition, a FD implementation has been selected to enhance the overall performance of the circuit. The proposed ICF FD IA been designed and fabricated in 180 nm CMOS technology to operate with a supply voltage of 1.8 V and provide a voltage gain of 4 V/V. Measurements on 10 different samples of the silicon prototype showed wide bandwidth, high CMRR and linear signal processing, thus confirming the suitability of the proposed solution for the intended application.

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