Article

Minimum Active Component Count Design of a PI$^{\lambda}$D$^{\mu}$ Controller and Its Application in a Cardiac Pacemaker System [†]

Julia Nako [1], Costas Psychalinos [1,*] and Ahmed S. Elwakil [2,3,4]

1 Department of Physics, Electronics Laboratory, University of Patras, GR-26504 Rio Patras, Greece
2 Department of Electrical and Computer Engineering, University of Sharjah, Sharjah P.O. Box 27272, United Arab Emirates
3 Nanoelectronics Integrated Systems Center (NISC), Nile University, Giza 12677, Egypt
4 Department of Electrical and Software Engineering, University of Calgary, Calgary, AB T2N 1N4, Canada
* Correspondence: cpsychal@upatras.gr
† This paper is an extended version of our paper published in the 2022 Panhellenic Conference on Electronics & Telecommunications (PACET), Nako J.; Psychalinos C. Heart Rate Controller Design for Cardiac Pacemaker, 2022 Panhellenic Conference on Electronics & Telecommunications (PACET), Tripolis, Greece, 2–3 December 2022; pp. 1–4, doi:10.1109/PACET56979.2022.9976347.

Abstract: A generalized structure for implementing fractional-order controllers is introduced in this paper. This is achieved thanks to the consideration of the controller transfer function as a ratio of integer and non-integer impedances. The non-integer order impedance is implemented using RC networks, such as the Foster and Cauer networks. The main offered benefit, with regards to the corresponding convectional implementations, is the reduced active and, also, passive component count. To demonstrate the versatility of the proposed concept, a controller suitable for implementing a cardiac pacemaker control system is designed. The evaluation of the performance of the system is performed through circuit simulation results, using a second-generation voltage conveyor as the active element.

Keywords: fractional-order controllers; fractional-order integrators; fractional-order capacitors; curve fitting approximation; pacemakers; second generation voltage conveyors

1. Introduction

The functional block diagram of a fractional-order proportional-integral-derivative (PI$^{\lambda}$D$^{\mu}$) controller is demonstrated in Figure 1. Assuming that K_p, K_i and K_d are constants associated with the proportional, integral, and derivative stages, respectively, and $0 < \lambda, \mu < 1$, being the order of the integration and differentiation stages, respectively, then the transfer function of a PI$^{\lambda}$D$^{\mu}$ controller is given by (1)

$$C(s) = K_p + \frac{K_i}{s^{\lambda}} + K_d s^{\mu}. \tag{1}$$

The extra degrees of freedom, originating from the non-integer order of the integration and differentiation stages of fractional-order controllers, offer the capability of easily and accurately adjusting the shape of the open-loop frequency response of control systems in order to meet the specifications related to the phase margin and settling time. This is in contrast to their integer-order counterparts, where only the associated time constants of the integration and differentiation stages can be adjusted [1–8]. A detailed discussion about the performance of the fractional-order controllers with regards to their integer-order counterparts has been provided in [9–11].
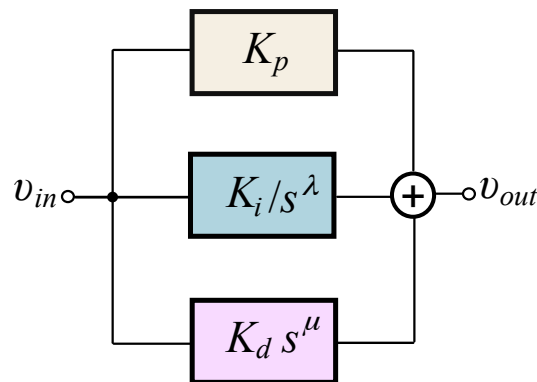
J. Low Power Electron. Appl. **2023**, *13*, 13

2 of 16

Figure 1. Typical functional block diagram of a fractional-order PI$^\lambda$D$^\mu$ controller.

The realization of the functional block diagram in Figure 1 can be performed by the following ways:

(a) utilizing RC networks (e.g., Cauer or Foster type) for approximating the behavior of fractional-order capacitors of the corresponding integration and/or differentiation stages, which are derived form their integer-order ones through the substitution of conventional capacitors by fractional-order capacitors [12]. This has been followed in [1,13–15]. The problem is that each-one of the required fractional-order capacitors must be substituted by a RC network, resulting in complicated structures in terms of passive component count. Although this is an easy procedure, in the sense that just only one design step is required for deriving the structure of the fractional-order controller, there is not capability of electronic adjustment of the characteristics of the controller.

(b) utilizing approximation tools, such as Oustaloup [16], continued fraction expansion etc., of the fractional-order Laplacian operator in order to approximate the behavior of the intermediate fractional-order transfer functions of the controller (i.e., integrator and differentiator). The resulting integer-order rational transfer functions are implemented using conventional filter design techniques, such as the employment of multi-feedback or cascaded structures. This procedure has been followed in [17–20]. Considering an nth–order approximation of the Laplacian operator s^r, with $0 < r < 1$ being the order of the operator, the resulting transfer function has the form of (2)

$$s^r \simeq \frac{P_n s^n + P_{n-1} s^{n-1} + \ldots + P_1 s + P_0}{s^n + Q_{n-1} s^{n-1} + \ldots + Q_1 s + Q_0} , \tag{2}$$

with P_i and Q_j ($i = 0 \ldots n$, $j = 0 \ldots n - 1$) being positive and real coefficients. Taking into account that a PI$^\lambda$D$^\mu$ controller is constructed from stages of different orders, the resulting transfer function that describes the behavior of the controller will have an order equal to $2n$, where n is the order of the approximation. Therefore, this solution suffers from the increased active and passive component count, worsening the performance of the system in terms of circuit complexity and power dissipation. On the other hand, it might be useful in the case where electronic adjustment of the characteristics of the controller would be required.

The motivation of this work is the development of PI$^\lambda$D$^\mu$ controllers structures, which have almost halved circuitry of that required in the cases where the conventional synthesis methods are followed. The main contributions made in this work can be summarized as follows: (a) the consideration of the controller's transfer function as a ratio of integer and non-integer impedances, instead as a sum of the outputs of scaling, integration, and differentiation stages, and (b) the approximation of the frequency behavior of the fractional-order impedance using a curve-fitting based approximation tool available in MATLAB. The approximation impedance function can be implemented by Cauer or Foster RC networks.

J. Low Power Electron. Appl. **2023**, 13, 13

3 of 16

An attractive feature is that only one RC network is required for implementing the whole structure of the controller.

With regards to our previously published paper in [21] the enhancements are the following: (a) a detailed comparison of the proposed structure with the conventional implementations is performed, (b) possible RC networks for approximating fractional-order impedances are considered, (c) possible implementations of the introduced concept are presented, and (d) the implementation of the controller has been performed using an alternative active element and, therefore, new simulation results are presented. The employed active element is the second generation voltage conveyor (VCII), which contributes to further reduce the power dissipation of the circuits, because of its relatively simple structure. As an application design example, a heart rate control system suitable for pacemakers is designed, and its performance is evaluated using the Cadence IC Design suite and MOS transistor models provided by the Austria Mikro Systeme (AMS) 0.35 μm CMOS process.

This work is organized as follows: the conventional implementations as well as the proposed one, using various types of active elements, are presented in Section 2, where the offered benefits are also discussed. The application example is provided in Section 3, while its behavior is evaluated in Section 4 through simulation results.

2. Proposed Implementation of Generalized Controller

2.1. Conventional Topologies

A typical implementation of the functional block diagram in Figure 1, using operational amplifiers (op-amps) as active elements, is demonstrated in Figure 2a [1]. As the impedance of a fractional-order capacitor is given by the general expression in (3)

$$Z_\alpha(s) = \frac{1}{C_\alpha s^\alpha} \, , \tag{3}$$

with $0 < \alpha < 1$ being the order of the element and C_α being the pseudo-capacitance (in Farad/s$^{1-\alpha}$) [22], the realized transfer function is

$$C(s) = \frac{R_{p_2}}{R_{p_1}} + \frac{1}{R_\lambda C_\lambda s^\lambda} + R_\mu C_\mu s^\mu \, . \tag{4}$$

Equalizing the coefficients of (1)–(4) the design equations, summarized in (5), are readily obtained

$$K_p = \frac{R_{p_2}}{R_{p_1}}, \quad K_i = \frac{1}{R_\lambda C_\lambda}, \quad K_d = R_\mu C_\mu \, . \tag{5}$$

Another alternative is the employment of second-generation current conveyors (CCIIs) as active elements, and the resulting structure is shown in Figure 2b. Considering the basic properties of the terminals of CCII (i.e., $v_X = v_Y$, $i_Y = 0$, $i_X = \pm i_Z$), the realized transfer function as well as the design equations are the same as those in (4) and (5). A drawback of this structure is the requirement of employing extra voltage buffers, in order to avoid the effect of loading from subsequent stages. This can be resolved using Current Feedback Operational Amplifiers (CFOAs), which are actually CCIIs with an extra buffer internally embedded in their structure. The behavior of CFOAs is described by the formulas: $v_X = v_Y, i_Y = 0, i_X = i_Z, v_Z = v_O$ and, therefore, the topology in Figure 2c implements the transfer function in (4).

The last active element which will be considered is the second-generation voltage conveyor (VCII), which is described by the following set of equations: $v_Y = 0, i_X = \pm i_Z, v_Z = v_X$. In other words, it can be considered as a special case of a CFOA with its Y terminal grounded, offering the aforementioned benefits of the CFOA. In addition, thanks to its internal structure constructed from one voltage and one current buffer, in contrast to the CFOA where 2 voltage buffers and one current buffer are required, its circuitry is simpler to that of the CFOA, offering also reduced power consumption [23–28]. The topology

J. Low Power Electron. Appl. **2023**, *13*, 13

4 of 16

depicted in Figure 2d, realizes the same transfer function as the aforementioned ones and, consequently, the design equations in (5) are still valid.
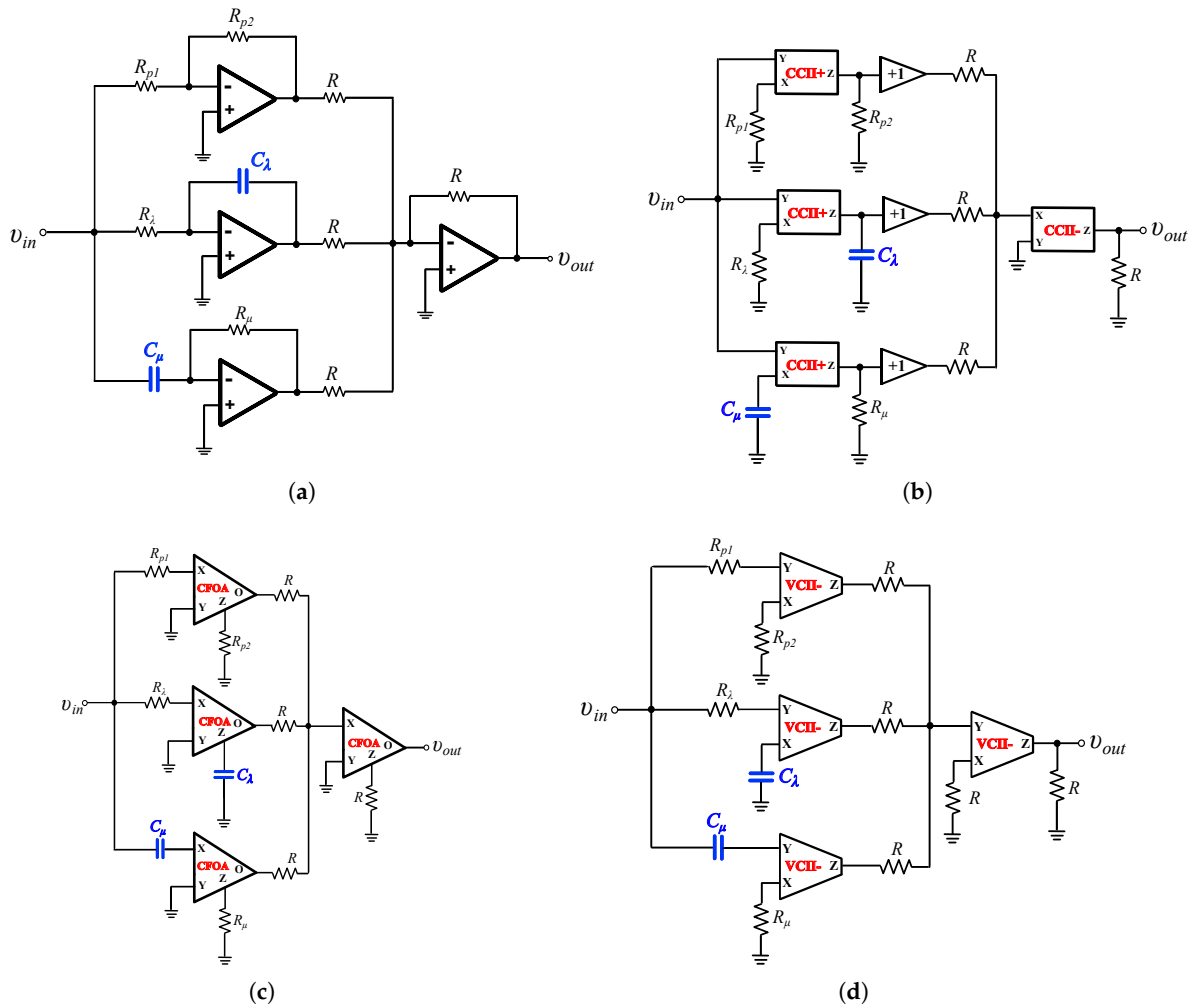

Figure 2. Typical implementations of a $PI^\lambda D^\mu$ controller using (**a**) op-amps, (**b**) CCIIs, (**c**) CFOAs, and (**d**) VCIIs as active elements.

Due to the absence of fractional-order capacitors in the market, their behavior will be emulated through the utilization of appropriately configured Foster or Cauer RC networks. Following this procedure and choosing among a variety of approximation tools, such as the Oustaloup, continued fraction expansion etc., the expression of the impedance of a fractional-order capacitor (C_α) is approximated by an nth–order rational integer-order impedance function of the form in (6)

$$Z_{approx}(s) \simeq \frac{B_n s^n + B_{n-1} s^{n-1} + \ldots + B_1 s + B_0}{s^n + A_{n-1} s^{n-1} + \ldots + A_1 s + A_0}, \tag{6}$$

with A_i $(i = 0 \ldots n-1)$ and B_j $(j = 0 \ldots n)$ being positive and real coefficients.

The impedance function in (6) can be implemented by the Cauer or Foster networks depicted in Figure 3. In the case of the Cauer type-I and type-II networks, the associated design equations are summarized in (7) and (8) respectively.

$$R_0 = q_0 \qquad R_i = q_i \qquad C_j = q_j, \ \ i = 2, 4 \ldots 2n \ \ j = 1, 3 \ldots 2n - 1, \tag{7}$$

J. Low Power Electron. Appl. **2023**, 13, 13

5 of 16

$$R_0 = \frac{1}{q_0} \qquad R_i = \frac{1}{q_i} \qquad C_j = \frac{1}{q_j}, \quad i = 2, 4 \ldots 2n \quad j = 1, 3 \ldots 2n - 1, \tag{8}$$

where $q_{i(j)}$ are the coefficients of the continued fraction expansion of the $Z_{approx}(s)$ in (6) [22].

Accordingly, the design equations of the Foster type-I and type-II networks are given by (9) and (10)

$$R_0 = B_n \qquad R_i = \frac{r_i}{|p_i|} \qquad C_i = \frac{1}{r_i}, \quad (i = 1, 2 \ldots n), \tag{9}$$

$$R_0 = \frac{1}{B_n} \qquad R_i = \frac{1}{r_i} \qquad C_i = \frac{r_i}{|p_i|}, \quad (i = 1, 2 \ldots n), \tag{10}$$

with r_i and p_i being the residues and poles of $Z_{approx}(s)$.
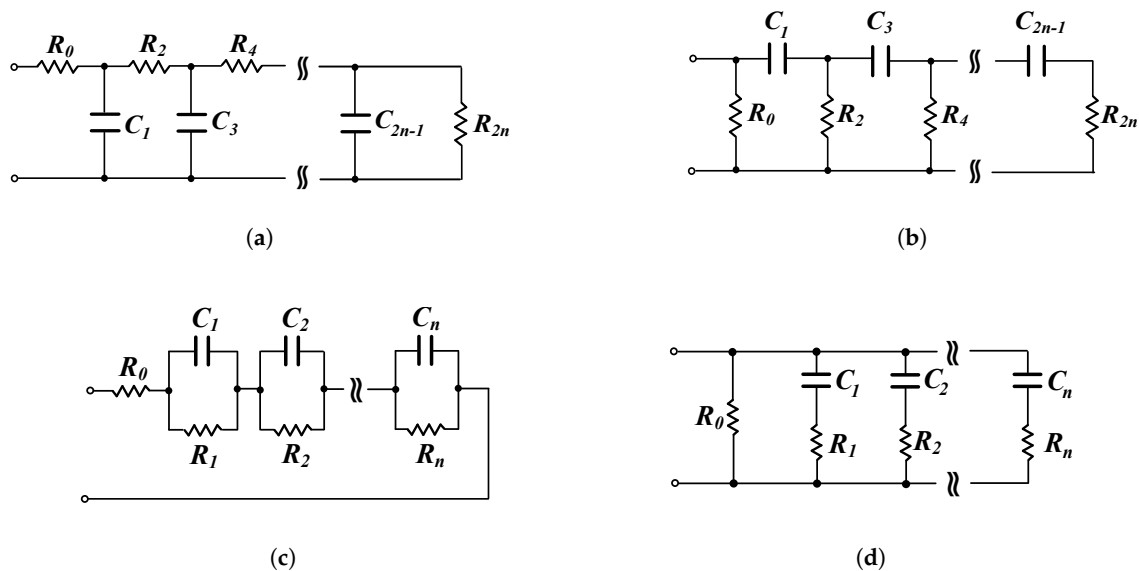

(a)

(b)

(c)

(d)

Figure 3. RC networks for approximating the behavior of the fractional-order capacitors, which are required for implementing the controllers in Figure 2. (**a**) Cauer type-I, (**b**) Cauer type-II, (**c**) Foster type-I, and (**d**) Foster type-II.

Considering an nth–order approximation, the number of required active and passive elements for implementing a $\text{PI}^\lambda \text{D}^\mu$ controller following the conventional methods are summarized in Table 1. It is obvious that the complexity of the structure rapidly increases with the order of the approximation.

Table 1. Passive and active component count for implementing the controllers in Figure 2, employing an nth–order approximation for emulating the behavior of the fractional-order capacitors.

Topology	Number of Active Elements	Number of Resistors	Number of Capacitors
Figure 2a	4	$2n + 10$	$2n$
Figure 2b	4 (plus 3 buffers)	$2n + 10$	$2n$
Figure 2c	4	$2n + 10$	$2n$
Figure 2d	4	$2n + 11$	$2n$

J. Low Power Electron. Appl. **2023**, *13*, 13

6 of 16

2.2. Proposed Generalized Structure

In order to overcome the aforementioned problem, the transfer function in (1) is written as

$$C(s) = \frac{R_{ex} \cdot \left(K_p + \frac{K_i}{s^\lambda} + K_d s^\mu \right)}{R_{ex}}, \tag{11}$$

with R_{ex} being an arbitrary value resistance.

The associated design equations are provided in (12)

$$Z_1 = R_{ex} \qquad Z_2(s) = R_{ex} \cdot C(s), \tag{12}$$

with $C(s)$ given by (1).

Another option is writing the transfer function in (1) as

$$C(s) = \frac{R_{ex}}{\frac{R_{ex}}{K_p + \frac{K_i}{s^\lambda} + K_d s^\mu}}, \tag{13}$$

with the associated design equations summarized in (14)

$$Z_1(s) = R_{ex}/C(s) \qquad Z_2 = R_{ex}. \tag{14}$$

Generalizing, the transfer function of the controller can be expressed as a ratio of two impedances Z_1 and Z_2

$$C(s) = \frac{Z_2}{Z_1}. \tag{15}$$

The choice of the impedance which will have fractional-order form depends on the behavior of the frequency response of the controller. Taking into account that the frequency behavior of the RC networks in Figure 3 is capacitive (i.e., the magnitude of the impedance decreases with the frequency) because they intend to approximate the behavior of fractional-order capacitors, then $Z_2(s) = R_{ex} \cdot C(s)$ in the case that the controller has such behavior. In the opposite case, $Z_1(s) = R_{ex}/C(s)$ in order to ensure that the fractional-order impedance is realizable by the RC networks in Figure 3.

The implementation of (15), using op-amps, CCIIs, CFOAs, and VCIIs as active elements is demonstrated in Figure 4a–d.
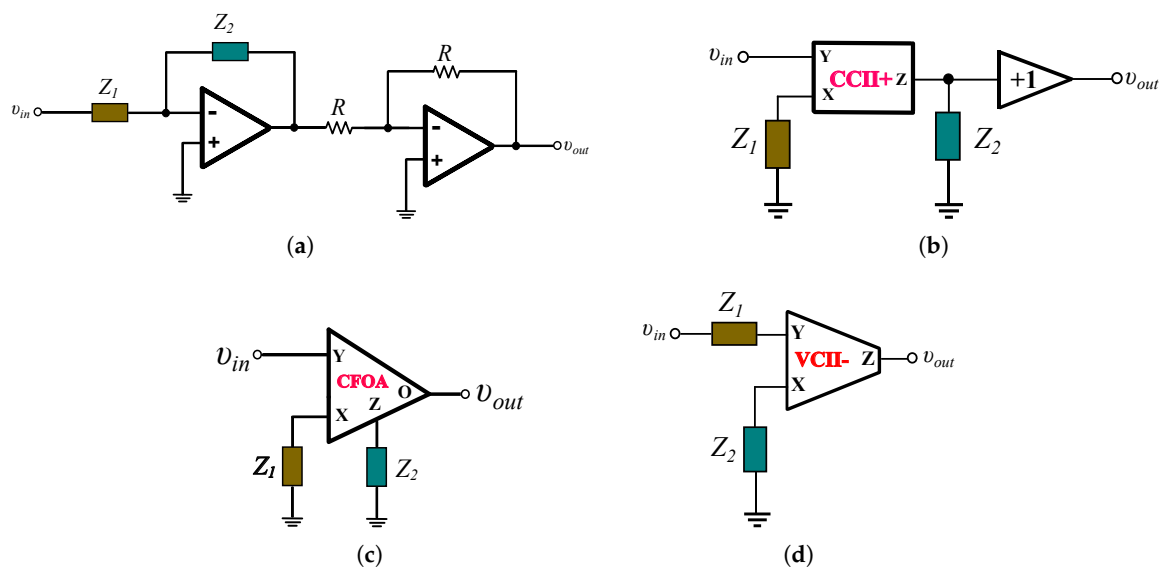

(a)

(b)

(c)

(d)

Figure 4. Proposed implementations of a PI$^\lambda$D$^\mu$ controller using for (**a**) op-amps, (**b**) CCIIs, (**c**) CFOAs and (**d**) VCIIs as active elements.

J. Low Power Electron. Appl. **2023**, *13*, 13

7 of 16

The implementation of the fractional-order impedance function can be performed by the following techniques:

(a) Approximating the intermediate terms that form the impedance using suitable tools such as the Oustaloup and the continued fraction expansion methods. Considering a nth–order approximation, the resulting order of the impedance $Z_1(s)$ or $Z_2(s)$ will be equal to $2n$ and therefore the number of passive components of the RC networks will be equal to $4n + 2$.

(b) Approximating the magnitude and phase frequency characteristics of the impedance. The approximation is performed using the Sanathanan-Koerner (S-K) least square iterative method based on the following steps [21,29].

- Obtain the frequency response data of the impedance, within the desired frequency range, using the MATLAB *freqresp* and *frd* functions.
- Assuming an approximation order, obtain the state-space model of the data using the command *fitfrd*, and then convert this model to a transfer function using the MATLAB command *ss2tf*.

The resulting integer-order rational impedance function will be given by (6) and, consequently it always has an order equal to the order of the employed approximation (i.e., equal to n). Therefore, the number of passive components of the RC networks will be equal to $2n + 1$. In other words, the number of resistors and capacitors required for constructing the Cauer of Foster networks is halved, compared to those required by employing the approximation of the intermediate terms of the impedance. In order to compare the implementations depicted in Figure 4a–d, in terms of complexity, Table 2 is established.

Table 2. Passive and active component count for implementing the controllers in Figure 4a–d, employing an nth–order approximation for emulating the behavior of a fractional-order impedance.

Topology	Number of Active Elements	Number of Resistors	Number of Capacitors
Figure 4a	2	$n + 4$	n
Figure 4b	1 (plus 1 buffer)	$n + 2$	n
Figure 4c	1	$n + 2$	n
Figure 4d	1	$n + 2$	n

Inspecting Tables 1 and 2, it is readily concluded that the proposed concept offers significant reduction in terms of active and passive component count, making it attractive for implementing control systems with reduced circuit complexity and, also, power dissipation. According to the results of Table 2, it seems that CFOAs and VCIIs implementations are the most beneficial ones. Taking into account that the internal structure of a CFOA is constructed by two voltage buffers and a current follower, while the VCII is formed by only one voltage buffer and a current follower, the VCII will be utilized in the next Section, where a design example will be provided, due to its simpler structure.

3. Design Example: Controlling the Heart Rate in a Pacemaker

A pacemaker is a battery-operated implantable device used to overcome arrhythmia situation, and uses slow electrical pulses for sustaining the heart rhythm at a normal rate. It is constructed from the sensing unit which senses the patient's heart rate, and the output unit, which sends out electrical signals to heart muscles. In the case of bradycardia (the heart rate becomes slow) the output unit starts sending excitation signals to the heart muscles for maintaining the heart rate at the normal rhythm.

Let us consider for example the closed-loop system of the cardiac pacemaker, where $C(s)$ is the transfer function of the controller, $P(s)$ is the product of the transfer functions which describe the dynamics of the pacemaker and the heart [30–32]. The transfer function of the controller in [32] has been derived using the Particle Swarm Optimization (PSO)

J. Low Power Electron. Appl. **2023**, *13*, 13

8 of 16

algorithm. The objective of the PSO algorithm is to minimize systems' several error functions, including integral absolute error (IAE), integral time absolute error (ITAE), integral square error (ISE), and integral time square error (ITSE), subject to time or frequency domain constraints, such as the maximum overshoot, rise time and settling time, or system's gain and phase margins. The resulting transfer function is given by the expression in (16)

$$C(s) = 0.72594 + \frac{0.1}{s^{0.01}} + 0.1s^{0.9786},$$ (16)

while the dynamics of the heart and pacemaker are described by (17)

$$P(s) = \frac{1352}{s(s + 20.8)(s + 8)}.$$ (17)

The transfer function $C(s)$ has such behavior that the choice $Z_2 = R_{ex}$ and $Z_1(s) = R_{ex}/C(s)$ is the suitable one, according to the discussion provided in Section 2.2.

Assuming that $R_{ex} = 10\,k\Omega$ and utilizing a 3$^{\text{rd}}$–order Oustaloup approximation in the range $[10^{-1}, 10^2]$ rad/s, then the resulting expression of $Z_1(s)$ is the following

$$Z_1(s) = \frac{15.76\,s^3 + 1.114 \cdot 10^5 s^2 + 4.958 \cdot 10^6\,s + 2.199 \cdot 10^7}{s^3 + 55.96\,s^2 + 626.8\,s + 1822}.$$ (18)

The magnitude and phase responses obtained through the MATLAB software are provided in the plots of Figure 5, where the corresponding ideal ones are also plotted by dashes. In addition, the accuracy of the utilized approximation is evaluated at transfer function level and the results are provided in Table 3, where it is evident that a satisfactory level of accuracy is achieved.
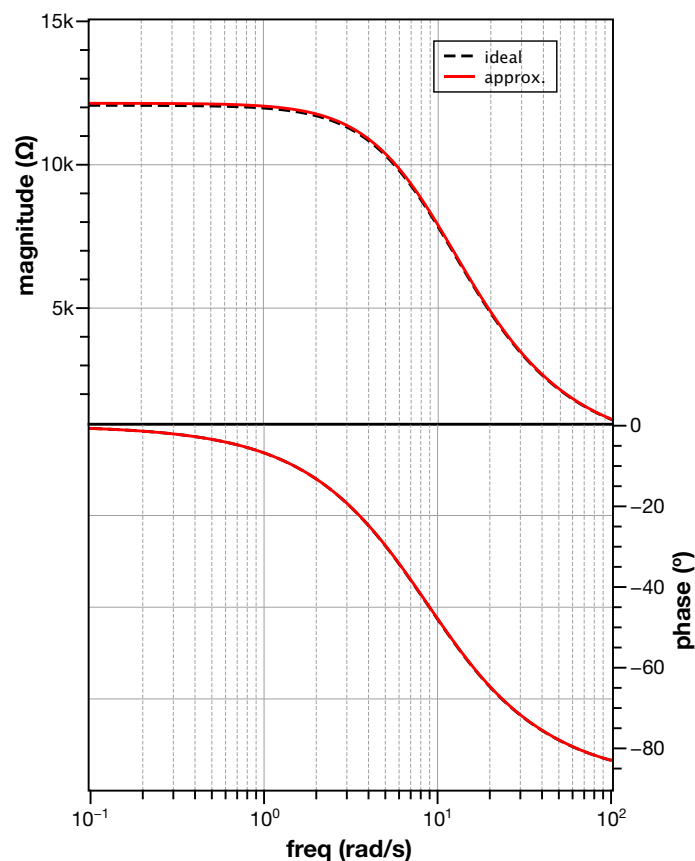

Figure 5. Magnitude and phase frequency responses of the impedance $Z_1(s)$, approximated by (18).

J. Low Power Electron. Appl. **2023**, *13*, 13

9 of 16

Table 3. Comparison of the theoretical and approximated open and closed-loop performances of the control system [21].

Parameter	Theoretical	Approximation
Phase margin (°)	70.39	70.34
Gain crossover frequency (rad/s)	6.34	6.34
Rise-time (ms)	308.1	236.4
Settling-time (ms)	472.7	355.4

4. Simulation Results

The performance of the controller will be evaluated using the Cadence IC design suite and the design kit provided by the AMS 0.35 μm CMOS process. The circuitry of the employed VCII- is depicted in Figure 6 [26]. The dc power supply voltages are $V_{DD} = -V_{SS} = 1.5$ V, and the dc bias current (I_0) is equal to 20 μA. The dc power dissipation of the controller is 613 μW. The aspect ratios of the MOS transistors are summarized in Table 4.
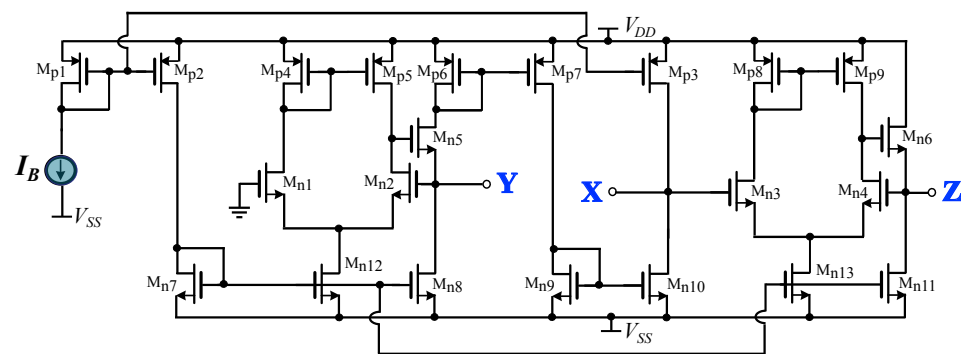
Figure 6. Internal structure of the VCII- employed in simulations [26].

Table 4. MOS transistors aspect ratios of the VCII- topology in Figure 6.

Transistor	Aspect Ratio (μm /μm)
M_{p1}–M_{p9}	200/2
M_{n1}–M_{n4}	20/2
M_{n5}–M_{n6}	20/0.4
M_{n7}–M_{n11}	2/2
M_{n12}–M_{n13}	4/2

The values of the passive elements of the RC networks in Figure 3 calculated using (7)–(10), rounded to the E96 series defined in IEC 60063 standard, are summarized in Tables 5 and 6.

Table 5. Passive elements of Cauer networks in Figure 3a,b, for approximating the impedance $Z_1(s) = R_{ex}/C(s)$.

Element	Cauer Type-I	Cauer Type-II
R_0	15.8 Ω	12.1 kΩ
R_2	1 kΩ	931 Ω
R_4	1.96 kΩ	118 Ω
R_6	215 Ω	18.7 Ω
C_1	9.09 μF	9.76 μF
C_3	15.8 μF	178 μF
C_5	953 μF	196 μF

J. Low Power Electron. Appl. **2023**, *13*, 13

10 of 16

Table 6. Passive elements of Foster networks in Figure 3c,d, for approximating the impedance $Z_1(s) = R_{ex}/C(s)$.

Element	Foster Type-I	Foster Type-II
R_0	15.8 Ω	12.1 kΩ
R_1	187 Ω	15.8 Ω
R_2	10.7 kΩ	60.4 kΩ
R_3	1.24 kΩ	511 kΩ
C_1	127 μF	9.09 μF
C_2	10.2 μF	0.412 μF
C_3	174 μF	0.392 μF

Choosing, for demonstration purposes, the Foster type-I network in order to implement the impedance $Z_1(s)$, the obtained magnitude and phase responses are demonstrated in Figure 7, where the theoretically predicted ones are also plotted as dashes. The sensitivity performance of the RC network is evaluated using the Monte-Carlo analysis tool offered by the Analog design Environment of the IC design suite. The obtained statistical plots of the magnitude and phase of the impedance at the gain crossover frequency (i.e., 6.34 rad/s), for $N = 500$ runs and 10% random tolerances of the passive elements values, are demonstrated in Figure 8. As the values of the standard deviation of the magnitude and phase are 6.8 Ω and 0.04°, and the associated mean values are 9.72 kΩ and −35.2°, it is verified the robustness of the employed network.
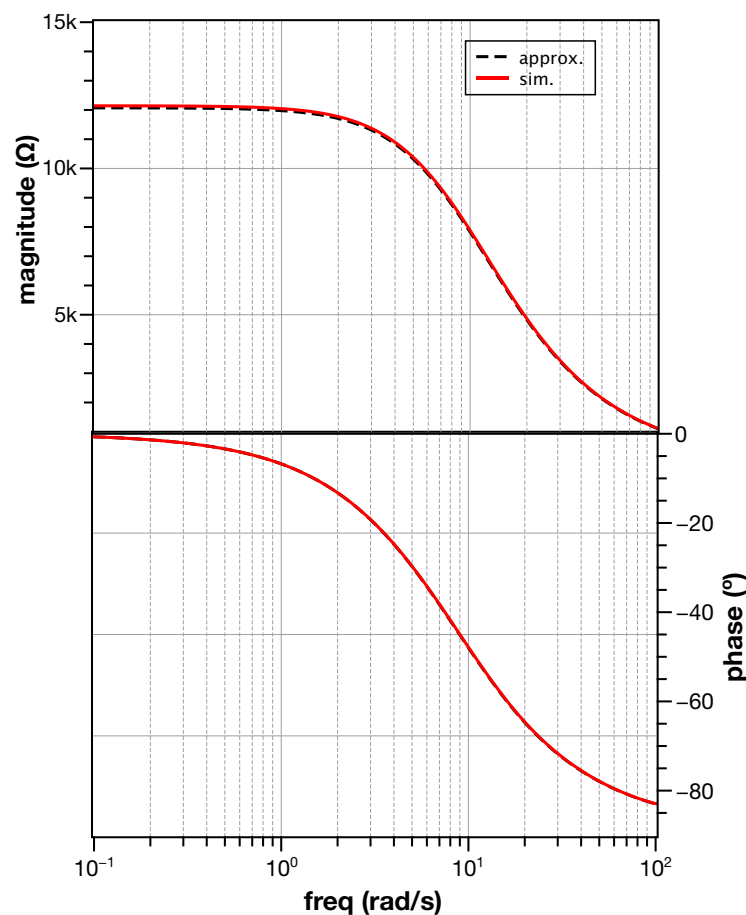
Figure 7. Simulated gain and phase responses of the Foster type-I network, realized using the values in Table 6, for approximating the impedance $Z_1(s)$.
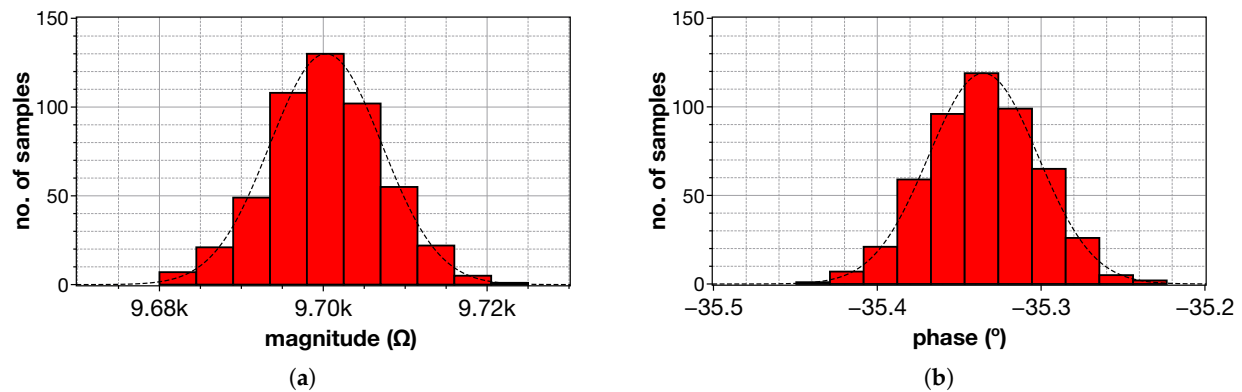
J. Low Power Electron. Appl. **2023**, *13*, 13

11 of 16

Figure 8. Monte Carlo analysis results about the (**a**) magnitude, and (**b**) phase of the impedance $Z_1(s)$, approximated by a Foster type-I network.

The magnitude and phase frequency responses of the controller are provided in Figure 9, with the corresponding theoretically predicted ones given as dashes, confirming the accurate operation of the introduced scheme of the controller. The open-loop responses of the controller-plant system are demonstrated in Figure 10.

The closed-loop behavior of the system is evaluated by stimulating it by a step voltage and the derived output waveform is provided in Figure 11. The derived performance simulation results for both open-loop and closed-loop configuration are given in Table 7, where it is readily obtained that the system behaves in a satisfactory level of accuracy.
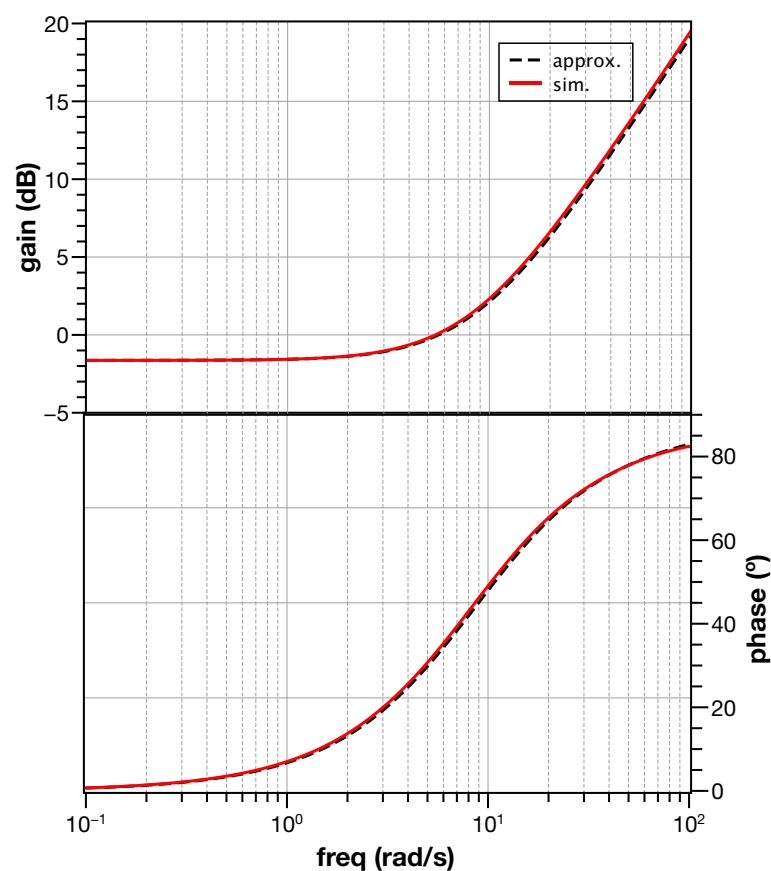

Figure 9. Simulated gain and phase responses of the proposed controller.
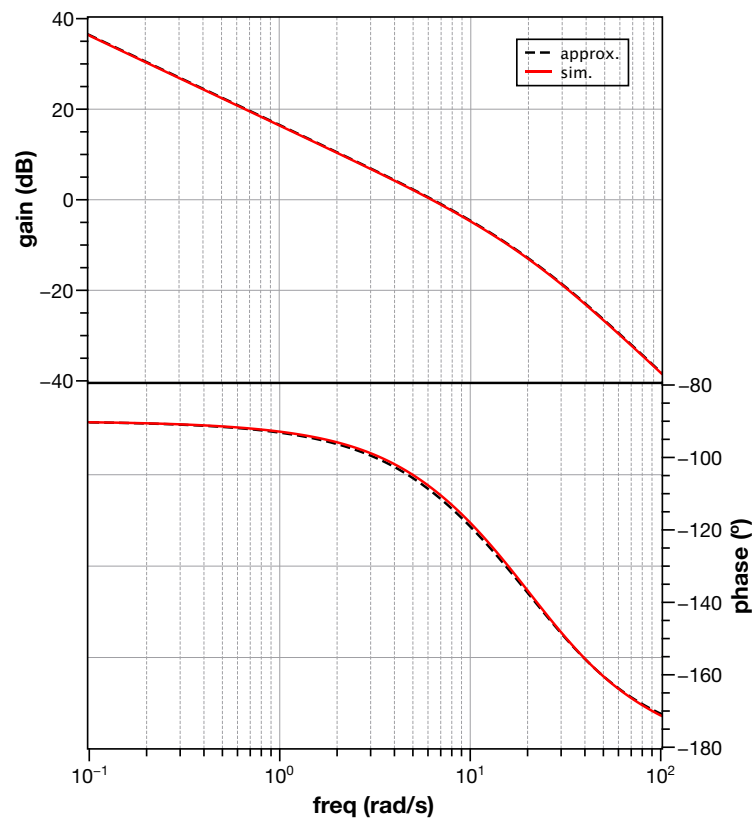
J. Low Power Electron. Appl. **2023**, *13*, 13

12 of 16

Figure 10. Open-loop gain and phase responses of the system controller-plant.
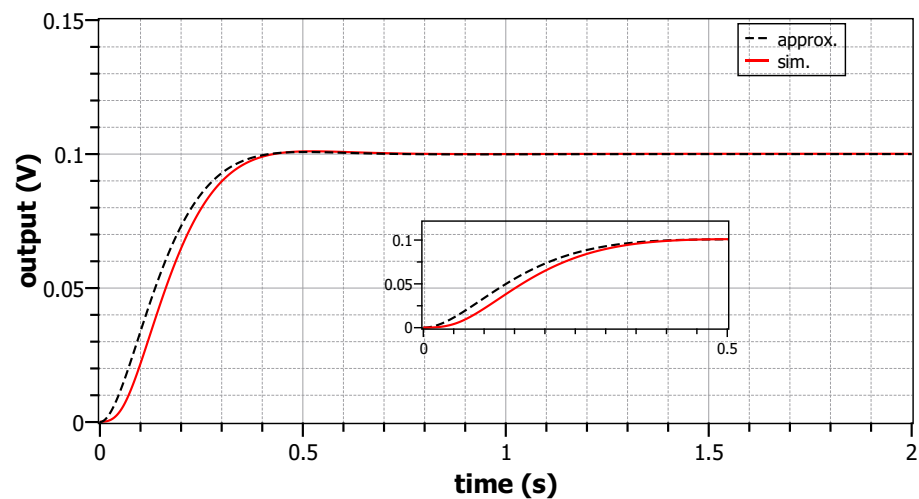

Figure 11. Step response of the system controller-plant.

Table 7. Comparison of the approximated and simulated open and closed-loop performances of the control system.

Parameter	Approximation	Simulation
Phase margin (°)	70.34	71.14
Gain crossover frequency (rad/s)	6.34	6.42
Rise-time (ms)	236.4	230.6
Settling-time (ms)	355.4	341.5

The sensitivity of the system is evaluated using the Monte-Carlo analysis tool and considering the effect of mismatching of MOS transistors, as well as of the process parameters

J. Low Power Electron. Appl. **2023**, *13*, 13

13 of 16

variations. The obtained statistical plots of the phase margin and gain crossover frequency are demonstrated in Figure 12a,b, where the associated values of the standard deviation are 0.2°, and 0.07 rad/s. Taking into account that the corresponding mean values are 71.14° and 6.42 rad/s, it is concluded that the proposed implementation offers reasonable sensitivity characteristics.

In addition, a corner analysis is performed considering ±10% variation of the dc power supply voltages, corners of the temperature equal to 0 °C and 40 °C, and worst case transistor models determines as slow NMOS and slow PMOS. The derived step responses are demonstrated in Figure 13, where the worst case values of the rise-time and settling-time are 226 ms and 320.3 ms, with the nominal values being 230.6 ms and 341.5 ms, respectively. The above results confirm the robustness of the designed system.
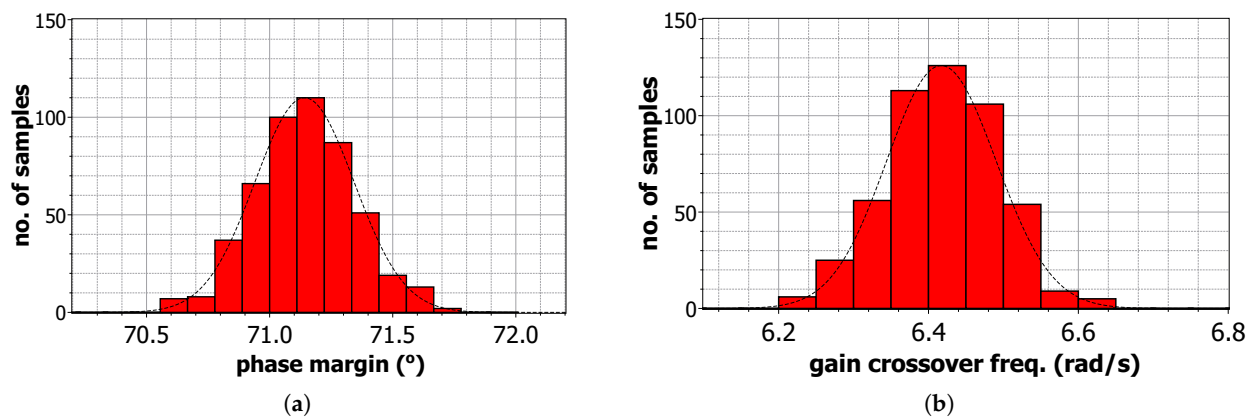

(a)

(b)

Figure 12. Monte-Carlo analysis results of the (**a**) phase margin, and (**b**) gain crossover frequency of the control system ($N = 500$ runs).
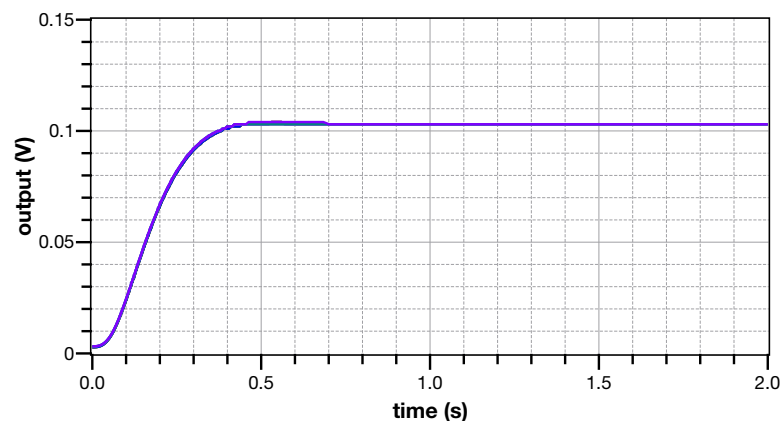

Figure 13. Output waveforms for a step input equal to 100 mV, obtained through corner analysis.

5. Conclusions

The novel concept, where the transfer function of a $PI^\lambda D^\mu$ controller is expressed as an impedance ratio has been presented in this paper. The main offered benefit is that the resulting structures are very simple, in the sense that the number of active and passive components is minimized, with regards to the conventional procedure where each one of the fractional-order Laplacian operator terms is approximated. This is achieved because, in the presented procedure, the whole impedance transfer function is approximated instead of the intermediate terms of the transfer function. Thanks to this approach, the resulting rational-order transfer function has half of the order of that derived by the conventional approach.

As a demonstration example, a heart rate control system for pacemakers has been realized and the derived simulation results confirm the correct operation of the controller and, also, its attractive sensitivity performance. A 3rd–order approximation has been

J. Low Power Electron. Appl. **2023**, *13*, 13

14 of 16

chosen for implementing the resulting approximation function; generally, the order of the approximation depends on the frequency range of interest and a trade-off between the level of accuracy and the circuit complexity is performed for choosing the optimal value of the order.

It must be also mentioned at this point that the presented procedure is general and, therefore, future research steps could include the following: (a) application of the procedure in other types of fractional-order controllers, such as PI^λ, PD^μ, (b) application of the procedure in the case of power-law controllers, and (c) exploitation of possible Field Programmable Gate Array (FPGA) or Field Programmable Analog Array based (FPAA) implementations [33–37] of the controller, where digital programmability will be offered. Last point is the following: the presented procedure is oriented to the MATLAB software and the exploitation of the suitability of open-source software, such as the SciLab software [7] or the development of a Python language based routine, might be useful for further enhancing its versatility and availability.

Author Contributions: Conceptualization, C.P., J.N. and A.S.E.; methodology, J.N. and C.P.; software, J.N.; validation, J.N.; formal analysis, J.N.; investigation, J.N. and C.P.; writing—original draft preparation, C.P.; writing—review and editing, C.P. and A.S.E.; project administration, C.P. and A.S.E. All authors have read and agreed to the published version of the manuscript.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AMS	Austria Mikro Systeme
CCII	Second-Generation Current Conveyor
CFOA	Current Feedback Operational Amplifier
CMOS	Complimentary Metal-Oxide Semiconductor
FPAA	Field Programmable Analog Array
FPGA	Field Programmable Gate Array
IAE	Integral Absolute Error
ITAE	Integral Time Absolute Error
ISE	Integral Square Error
ITSE	Integral Time Square Error
MOS	Metal-Oxide Semiconductor
OP-AMP	Operational Amplifier
$PI^\lambda D^\mu$	Fractional-Order Proportional Integral Derivative
RC	Resistor Capacitor
S-K	Sanathanan-Koerner
VCII	Second-Generation Voltage Conveyor

References

1. Podlubny, I.; Petráš, I.; Vinagre, B.M.; O'leary, P.; Dorčák, L. Analogue realizations of fractional-order controllers. *Nonlinear Dyn.* **2002**, *29*, 281–296. [CrossRef]
2. Monje, C.A.; Chen, Y.; Vinagre, B.M.; Xue, D.; Feliu-Batlle, V. *Fractional-Order Systems and Controls: Fundamentals and Applications*; Springer Science & Business Media: Berlin, Germany, 2010.
3. Xue, D. Fractional-order control systems. In *Fractional-Order Control Systems*; de Gruyter: Berlin, Germany, 2017.
4. Azar, A.T.; Radwan, A.G.; Vaidyanathan, S. *Fractional Order Systems: Optimization, Control, Circuit Realizations and Applications*; Academic Press: Cambridge, MA, USA, 2018.

J. Low Power Electron. Appl. **2023**, *13*, 13

15 of 16

5. Dastjerdi, A.A.; Vinagre, B.M.; Chen, Y.; HosseinNia, S.H. Linear fractional order controllers; A survey in the frequency domain. *Annu. Rev. Control* **2019**, *47*, 51–70. [CrossRef]
6. Petráš, I. *Applications in Control*; Walter de Gruyter GmbH & Co KG: Berlin, Germany, 2019.
7. Bingi, K.; Ibrahim, R.; Karsiti, M.N.; Hassan, S.M.; Harindran, V.R. *Fractional-Order Systems and PID Controllers*; Springer: Berlin, Germany, 2020.
8. Muresan, C.I.; Birs, I.; Ionescu, C.; Dulf, E.H.; De Keyser, R. A Review of Recent Developments in Autotuning Methods for Fractional-Order Controllers. *Fractal Fract.* **2022**, *6*, 37. [CrossRef]
9. Chevalier, A.; Francis, C.; Copot, C.; Ionescu, C.M.; De Keyser, R. Fractional-order PID design: Towards transition from state-of-art to state-of-use. *ISA Trans.* **2019**, *84*, 178–186. [CrossRef]
10. Tepljakov, A.; Alagoz, B.B.; Yeroglu, C.; Gonzalez, E.; HosseinNia, S.H.; Petlenkov, E. FOPID controllers and their industrial applications: A survey of recent results. *IFAC-PapersOnLine* **2018**, *51*, 25–30. [CrossRef]
11. Tepljakov, A.; Alagoz, B.B.; Yeroglu, C.; Gonzalez, E.A.; Hosseinnia, S.H.; Petlenkov, E.; Ates, A.; Cech, M. Towards industrialization of FOPID controllers: A survey on milestones of fractional-order control and pathways for future developments. *IEEE Access* **2021**, *9*, 21016–21042. [CrossRef]
12. Buscarino, A.; Caponetto, R.; Graziani, S.; Murgano, E. Realization of fractional-order circuits by a constant phase element. *Eur. J. Control* **2020**, *54*, 64–72. [CrossRef]
13. Domansky, O.; Sotner, R.; Langhammer, L.; Jerabek, J.; Psychalinos, C.; Tsirimokou, G. Practical design of RC approximants of constant phase elements and their implementation in fractional-order PID regulators using CMOS voltage differencing current conveyors. *Circuits Syst. Signal Process.* **2019**, *38*, 1520–1546. [CrossRef]
14. Kapoulea, S.; Psychalinos, C.; Baranowski, J.; Bauer, W. CCII based realization of fractional-order PD controller for a position servo. In Proceedings of the 2019 42nd International Conference on Telecommunications and Signal Processing (TSP), Budapest, Hungary, 1–3 July 2019; pp. 102–105. [CrossRef]
15. George, M.A.; Kamat, D.V.; Kurian, C.P. Electronically tunable ACO based fuzzy FOPID controller for effective speed control of electric vehicle. *IEEE Access* **2021**, *9*, 73392–73412. [CrossRef]
16. Oustaloup, A.; Levron, F.; Mathieu, B.; Nanot, F.M. Frequency-band complex noninteger differentiator: Characterization and synthesis. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **2000**, *47*, 25–39. [CrossRef]
17. Dimeas, I.; Petras, I.; Psychalinos, C. New analog implementation technique for fractional-order controller: A DC motor control. *AEU-Int. J. Electron. Commun.* **2017**, *78*, 192–200. [CrossRef]
18. Sotner, R.; Jerabek, J.; Kartci, A.; Domansky, O.; Herencsar, N.; Kledrowetz, V.; Alagoz, B.B.; Yeroglu, C. Electronically reconfigurable two-path fractional-order PI/D controller employing constant phase blocks based on bilinear segments using CMOS modified current differencing unit. *Microelectron. J.* **2019**, *86*, 114–129. [CrossRef]
19. Bauer, W.; Baranowski, J. Fractional PI$^\lambda$D Controller Design for a Magnetic Levitation System. *Electronics* **2020**, *9*, 2135. [CrossRef]
20. George, M.A.; Kamat, D.V.; Indiran, T. OTA-C Realization of An Optimized FOPID Controller for BLDC Motor Speed Control. *IETE J. Res.* **2021**, 1–19. [CrossRef]
21. Nako, J.; Psychalinos, C. Heart Rate Controller Design for Cardiac Pacemaker. In Proceedings of the 2022 Panhellenic Conference on Electronics & Telecommunications (PACET), Tripolis, Greece, 2–3 December 2022; pp. 1–4.
22. Tsirimokou, G. A systematic procedure for deriving RC networks of fractional-order elements emulators using Matlab. *AEU-Int. J. Electron. Commun.* **2017**, *78*, 7–14. [CrossRef]
23. Safari, L.; Barile, G.; Ferri, G.; Stornelli, V. High performance voltage output filter realizations using second generation voltage conveyor. *Int. J. RF Microw.-Comput.-Aided Eng.* **2018**, *28*, e21534. [CrossRef]
24. Safari, L.; Barile, G.; Stornelli, V.; Ferri, G. An overview on the second generation voltage conveyor: Features, design and applications. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *66*, 547–551. [CrossRef]
25. Safari, L.; Barile, G.; Ferri, G.; Stornelli, V. Traditional Op-Amp and new VCII: A comparison on analog circuits applications. *AEU-Int. J. Electron. Commun.* **2019**, *110*, 152845. [CrossRef]
26. Safari, L.; Yuce, E.; Minaei, S.; Ferri, G.; Stornelli, V. A second-generation voltage conveyor (VCII)–based simulated grounded inductor. *Int. J. Circuit Theory Appl.* **2020**, *48*, 1180–1193. [CrossRef]
27. Yesil, A.; Minaei, S. New simple transistor realizations of second-generation voltage conveyor. *Int. J. Circuit Theory Appl.* **2020**, *48*, 2023–2038. [CrossRef]
28. Yuce, E.; Safari, L.; Minaei, S.; Ferri, G.; Barile, G.; Stornelli, V. A New Simulated Inductor with Reduced Series Resistor Using a Single VCII±. *Electronics* **2021**, *10*, 1693. [CrossRef]
29. Bingi, K.; Ibrahim, R.; Karsiti, M.N.; Hassam, S.M.; Harindran, V.R. Frequency response based curve fitting approximation of fractional-order PID controllers. *Int. J. Appl. Math. Comput. Sci.* **2019**, *29*, 311–326. [CrossRef]
30. Arunachalam, S.P.; Kapa, S.; Mulpuru, S.K.; Friedman, P.A.; Tolkacheva, E.G. Intelligent fractional-order PID (FOPID) heart rate controller for cardiac pacemaker. In Proceedings of the 2016 IEEE Healthcare Innovation Point-of-Care Technologies Conference (HI-POCT), Cancun, Mexico, 9–11 November 2016; pp. 105–108.
31. Bajpai, S.; Alam, M.; Ali, M. Intelligent Heart Rate Controller using Fractional Order PID Controller Tuned by Genetic Algorithm for Pacemaker. *Int. J. Eng. Res. Technol.* **2017**, *6*, 715–720.

J. Low Power Electron. Appl. **2023**, *13*, 13

16 of 16

32. Momani, S.; Batiha, I.M.; El-Khazali, R. Design of $PI^{\lambda}D^{\delta}$-Heart Rate Controllers for Cardiac Pacemaker. In Proceedings of the 2019 IEEE International Symposium on Signal Processing and Information Technology (ISSPIT), Ajman, United Arab Emirates, 10–12 December 2019; pp. 1–5.
33. Tolba, M.F.; AboAlNaga, B.M.; Said, L.A.; Madian, A.H.; Radwan, A.G. Fractional order integrator/differentiator: FPGA implementation and FOPID controller application. *AEU-Int. J. Electron. Commun.* **2019**, *98*, 220–229. [CrossRef]
34. Singh, K. Load frequency regulation by de-loaded tidal turbine power plant units using fractional fuzzy based PID droop controller. *Appl. Soft Comput.* **2020**, *92*, 106338.
35. Silva-Juárez, A.; Tlelo-Cuautle, E.; De La Fraga, L.G.; Li, R. FPAA-based implementation of fractional-order chaotic oscillators using first-order active filter blocks. *J. Adv. Res.* **2020**, *25*, 77–85. [CrossRef]
36. Tlelo-Cuautle, E.; Pano-Azucena, A.D.; Guillén-Fernández, O.; Silva-Juárez, A. *Analog/Digital Implementation of Fractional Order Chaotic Circuits and Applications*; Springer: Berlin/Heidelberg, Germany, 2020.
37. Gude, J.J.; García Bringas, P. A Novel Control Hardware Architecture for Implementation of Fractional-Order Identification and Control Algorithms Applied to a Temperature Prototype. *Mathematics* **2022**, *11*, 143. [CrossRef]