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Editorial

Graphene Frameworks for Nanodevices

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Graphene, a two-dimensional (2D) crystal consisting of one layer of carbon atoms, received intense interest in the last few decades due to its rich physics for diverse applications [1]. It is known as a semimetal material with high intrinsic electrical conductivity and can be used as electrodes due to the gapless band structure [2]. Interestingly, owing to the lower carrier concentrations near the Dirac point, the tunable work function with respect to graphene can be implemented via electrostatic doping or chemical doping, which eventually paved the way for deep root research for next-generation devices [3,4]. Together with ultrahigh carrier mobility (~200.000 $cm^2V^{-1}s^{-1}$) at room temperature, a low sheet resistance (~100 Ωsp^{-1}), high transparency (97.7%), flexibility and stretchability with a strain of ~13%, and ultra-broad spectra absorption (up to infrared range), graphene was shown to be an essential basic building unit for a wide range of electronics and optoelectronics applications [1,5,6]. Inspired by the discovery of graphene, many other 2D materials covering a wide range of electrically conductive materials, from semiconductors to insulators such as transition metal dichalcogenides (TMDCs) and boron nitride, have been investigated [7,8]. These 2D materials demonstrated highly distinct lattice structures, large surface areas, bonding-free properties, clean interfaces, etc., which allow the fabrication of many building blocks that are physically assembled via weak van der Waals (vdW) forces [9]. The advances in the key metrics in 2D-based devices compared to bulk 3D conventional devices include reducing power consumption, scaling down the gate's length and channel's length, and obtaining controllable Schottky barriers in semiconductor devices, which are expected to replace Si CMOS technology or are compatible with it [10].

The need for data processing and application-specific functions at the system level is highly dependent on computing capabilities, which forces continual improvements with respect to the performance of the underlying transistors. In advanced transistor nodes, the requirements are as follows: high speeds, high density integration, high current density, small gate length, low power consumption, and channel thicknesses that require thinning down in order to maintain the effective gate electric field modulation [11]. Compared to the conventional Si transistor, graphene-based transistors hold great promise because they have an atomic sheet layer that is less than 1 nm thick and do not suffer from channel shrinking problems. High-speed graphene transistors demonstrated high intrinsic cut-off frequencies of 100–300 GHz, large on-currents (3.32 mA/μm), and high transconductance (1.27 mS/μm) [12]. In order to increase the number of transistors in a chip, vertical field-effect transistors (VFET) with a high deliverable current density over 5000 A/cm^2 have been used in various approaches. In this concept, graphene has strong impacts as an electrode, which allow vertical current flows, while the bottom gate can effectively modulate the semiconductor channel via graphene due to a lower carrier concentration at the Dirac point, which can switch the device between on and off states [10]. Many studies have attempted to scale down the gate length of the transistor; however, obtaining a physical gate length at the sub-1nm level has been challenging due to the limitation of lithography techniques. Recently, a one-atom-thick layer of graphene demonstrated a side edge gate length of 0.34 nm, and this received substantial interest with respect to the development of future transistors [13]. Another important aspect of traditional transistors still comprises high-power consumption, which is normally restricted by the thermionic limitation of

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a subthreshold swing (SS) of ~60 mV/dec. A recent innovation in combination with graphene and carbon nanotubes used Dirac-source field-effect transistors (DS-FETs) with a substantially lower supply voltage of 0.5 V and a steeper SS of 35 mV/dec in the off state [14].

On the other hand, with the increasing amount of data that have to processed in today's electronic devices that facilitate classification tasks in applications such as image recognition, autonomous driving, or machine learning, more attention with respect to the development of memory devices is required. Floating-gate memory (FGM) has received more interest than phase-change memory (PCM) and resistive random-access memory (RRAM). This is because the FGM can allow simultaneous memory reading and writing without additional device such as transistors and diodes to build up a synaptic array. In addition, the FGM device works based on carrier injections and tunneling rather than oxygen vacancy movements in RRAM, resulting in higher operating speeds. Graphene has been demonstrated as an ideal component of FGM as a floating gate, where the charge carrier from the semiconductor channel can easily be trapped in the floating gate by utilizing a tunneling barrier and a clean interface. Within this device's architecture, an ultrafast writing/erasing speed of 20 ns, on/off current ratio of ~10^6, and non-volatile characteristics have been observed. Nevertheless, the conventional FGM with three terminals (source, drain, and gate) increases the circuit's complexity and limits the integration density in chips [15]. Therefore, a two-terminal tunnelling random access memory (TRAM) has been developed by using graphene, boron nitride, and MoS_2 as the floating gates and by tunneling the oxide layer and semiconductor channel. In this architecture, the charge carrier from the semiconductor channel can tunnel through the oxide layer and is trapped/stored in the graphene floating gate. The advantage of the graphene floating gate compared to conventional metal floating gates is that the tunable graphene work function is attributed to change in bending bands at the graphene/oxide barrier rather than the fixed barrier height at the metal/oxide junctions. TRAM provided an ultra-low off-current (10^{-14} A), ultra-high on/off current ratio (>10^9), high retention time (>10^4 s), high endurance (>10^5 cycles), and multi-level resistance states. Compared to the conventional FGM, TRAM used only two terminals (source and drain) without a gate terminal for operations, and this has potential for applications in learning networks that require a synapse-like function [16].

Although graphene has been proven to be one of the most influential materials in future nanodevices, the highest-quality graphene, however, is produced so far by the exfoliation method from bulk graphite via a weak vdW force, which is normally limited by the size and uncontrollable layer thickness and restricts the construction of more complex circuits in industries. Therefore, high-quality graphene in large-scale areas is highly demanded for future applications. Recently, centimeter-scale single-layer graphene has been realized by chemical vapor deposition (CVD) techniques applied on Cu substrates. Nevertheless, this technique resulted in a polycrystalline graphene film, which basically included many domains with different lattice orientations, leading to the formation of grain boundaries [17]. The presentation of such grain boundaries possibly increases the defect state, implying a reduction in the physical and/or chemical properties of graphene. Thus, the most challenging approach comprises growing single crystalline graphene structures at the wafer scale without grain boundaries via CVD techniques. In parallel, alternative methods for developing unavoidable graphene grain boundaries are under consideration with respect to the new research era. Several approaches have been developed to observe graphene grain boundaries at the nano- and/or macro-scale, such as dark-field transmission electron microscopy (TEM), high-resolution TEM, scanning tunneling microscopy (STM) or optical microscopy, and scanning electron microscopy (SEM). The observed the grain boundaries introduced an interesting subject for fundamental research. One creative way for developing short-channel-length transistors based on graphene grain boundaries is to apply selective etching processes at the grain boundaries using hydrogen plasma, where the perfect lattice within the graphene frames cannot be etched. Within this, short channel lengths can be fabricated below 4 nm, while graphene frames can comprise an electrode

(source and drain). This method provides a facile route toward the lithography-free fabrication of short-channel-length electronic devices [18]. In addition, the production of the CVD multilayer graphene film is another challenge for practical devices. It is noted that the fundamental properties of graphene are strongly dependent on the number of graphene layers. For example, single-layer graphene absorbs ~2.3% of light in the visible range, and a proportional increase is observed with an increase in graphene layers. Single-layer graphene has gapless band structures; in contrast, multilayer graphene exhibits a tunable bandgap. Thus, controlling the number of graphene layer is very important in order to further build up new functional device applications. Recent research demonstrated that well-controlled multilayer graphene (from single layer to four layers) can be implemented with a defined crystallographic stacking sequence using a SiC alloy on the surface of a Cu substrate [19]. This introduces many advantages for future large-scale applications such as FGM, where the multilayer graphene (more than four layers) floating gate has demonstrated a higher charge storage capacity, stable electron affinity (~4.6 eV), and higher density of states than single-layer graphene [15].

Amongst the different kinds of approaches that are used in nanodevice fabrication, graphene film transfer processes are essential parameters for determining the performance of nanodevices. In principle, graphene has been successfully grown in various metal substrates, such as Au, Pt, Ni, and Cu. Depending on the different purposes of the device's architecture, graphene films need to be transferred onto the target's substrate via chemical processes with the assistance of various organic polymers. However, this process results in extensive contamination, wrinkles, or cracks, which significantly degrade the graphene's quality and device performance. Recently, many efforts have been developed to obtain high-quality graphene by using different functional polymers, which can be easily cleaned. Another solution is to directly grow the graphene film onto a desired substrate, but controlling the temperature is extremely hard when adapting to industrial technologies such as back-end-of-line (BEOL), which normally requires temperatures below 450 °C. Furthermore, there are difficulties in reproducing other important device aspects, such as contact resistance and clean interfaces. Considering the ultra-flat surface and clean and large-scale film, graphene has been developed using layer-assisted transfers. With this strategy, the minimum interfacial trapping states and uncompromised performance are essentially retained. Recent plug-and-probe approaches have been developed via a transfer and lamination process to pick up the prefabricated device's stack from the sacrificial substrate [20]. Either the metal contact and/or the insulator layer can be transferred onto any desired target (e.g., semiconductor channel or other functional electrode, etc.), which provide the sharp interface of semiconductor/metal or semiconductor/oxide heterojunctions. As a result, a low-energy formation that does not produce damage on the semiconductor's surface can be obtained, which further eliminates the Fermi-level pinning effect and produces minimum complications from fabrications induced by any external defects or trapping states. Thus, many of the device's aspects are enhanced, such as having a small subthreshold swing, low operating voltages, and high mobility. Although this approach is able produce fabrications at the large wafer scale, its integration into more complicated circuits and access to CMOS markets is still a challenge.

Overall, despite such great developments and achievements in many types of graphene-based device applications, there are many remaining challenges, including weak absorption characteristics and the small built-in potential that limits the photonic properties of the graphene photodetectors, which suffer from a small external quantum efficiency (EQE) range of ~0.1%–1% and a low responsivity of a few mA W^{-1} [21]. Other technical issues include wafer-scale synthesis, grain boundary, layer controller, stacking orientation, transfer techniques, and scalable fabrication, etc. Therefore, the route toward using graphene in future nanodevices requires sustained research and development in order to meet the requirements of contemporary semiconductor technologies. This would also generate many new possibilities for the integration of graphene with other dimensions materials to

provides a promising opto-electronics structure by taking into account the unique properties of each dimension [22,23].

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