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# Effect of Ge Concentration on the On-Current Boosting of Logic P-Type MOSFET with Sigma-Shaped Source/Drain

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**Abstract:** Silicon german ium (SiGe) has attracted significant attention for applications in the source/drain (S/D) regions of p-type metal-oxide-semiconductor field-effect transistors (p-MOSFETs). However, in SiGe, as the Ge concentration increases, high-density defects are generated, which limit its applications. Therefore, several techniques have been developed to minimize defects; however, these techniques require relatively thick epitaxial layers and are not suitable for gate-all-around FETs. This study examined the effect of Ge concentration on the embedded SiGe source/drain region of a logic p-MOSFET. The strain was calculated through nano-beam diffraction and predictions through a simulation were compared to understand the effects of stress relaxation on the change in strain applied to the Si channel. When the device performance was evaluated, the drain saturation current was approximately 710  $\mu$ A/ $\mu$ m at an off current of 100 nA/ $\mu$ m with a drain voltage of 1 V, indicating that the current was enhanced by 58% when the Ge concentration was optimized.

**Keywords:** silicon germanium; p-type metal-oxide-semiconductor field-effect transistors; source/drain (S/D) regions; epitaxial growth; thermal annealing

## 1. Introduction

In recent years, silicon germanium (SiGe) has been widely used in the source/drain (S/D) regions of p-type metal-oxide-semiconductor field-effect transistors (p-MOSFETs) to induce a uniaxial strain in the channel region. When a 65-nm-transistor-node is used for three-dimensional structures, such as a fin field-effect transistors (FETs) or gate-all-around FETs, the lateral dimensions, including the junction depth, of these regions becomes more significant. Thus, embedded SiGe technology, namely e-SiGe, was adopted to increase the S/D volume. The SiGe epitaxy process has been used in S/D to induce a compressive strain in its channel, thereby increasing hole mobility [1–4]. Since Si and Ge have the same crystallographic structure, both materials can be easily alloyed [5]; the lattice constant of SiGe increases as the Ge concentration increases. Thus, to increase the transistor current, several studies have aimed to induce compressive strain in the channel by increasing the Ge concentration [6,7]. SiGe is useful for strain engineering and it also effectively reduces the contact resistance in the S/D regions by reducing the Schottky barrier heights [8–10]. As the transistor size decreases, achieving a low contact resistivity becomes crucial. A contact resistivity of <1  $\times$  10<sup>-9</sup>  $\Omega \cdot cm^2$  is required in a <7 nm node [11].

E-SiGe is an effective method that can increase the uniaxial compressive strain applied to the channel, and a selectively epitaxial growth (SEG) of SiGe in the recessed S/D region is essential for this. SiGe is particularly suitable for the SEG process because it can be selectively deposited on the exposed S/D regions and etched at high selectivity for Si and SiO<sub>2</sub> [12–14]. When performing SEG of SiGe using a chemical vapor deposition (CVD), it is also necessary to consider how many chips of the patterned wafer are adjacent to each other [15]. The strain applied to the channel is affected by the shape of the sigma cavity and concentrations of Ge and B [16–19]. The strain is compensated when the concentration



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**Copyright:** © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). of B increases to realize a low contact resistance of S/D. Therefore, increasing the Ge concentration remains crucial in a gate-all-around FET.

However, as the Ge concentration increases, high-density defects are generated in the grown layers because the difference in the lattice parameter between the Si substrate and the SiGe layer increases [12,13]. Therefore, several techniques have been developed to minimize defects, such as epitaxial lateral overgrowth [12] and thermal cyclic annealing [13]. However, these techniques require relatively thick epitaxial layers and are not suitable for gate-all-around FETs.

Herein, we studied the current boosting and defect generation in a nano-sized sigmashaped SiGe pattern, which was designed to implement the S/D shape in a gate-all-around FET. The strain behavior in the Si channel and the formation of misfit dislocations in SiGe were investigated for various values of concentrations of Ge ( $C_{Ge}$ ). The strain inside the channel was analyzed using nano-beam diffraction (NBD) and simulation. Furthermore, the change in stress owing to an e-SiGe and its effect on the electrical performance of a 28-nm-p-MOSFET were also evaluated. In this study, intrinsic SiGe was grown in one sigma cavity structure, but B-doped SiGe will be grown in various sigma cavities in the future to study changes in device characteristics.

#### 2. Materials and Methods

The  $C_{Ge}$  effect in current boosting by SiGe was examined using a p-MOSFET device with a planar gate structure. A multilayer SiGe, comprising layer 1 (L1)/layer 2 (L2)/layer 3 (L3), was formed using the process flow shown in Figure 1a after a sigma cavity was created to implement the S/D shape in a gate-all-around FET. The  $C_{Ge}$  distribution in SiGe was confirmed using a transmission electron microscopy-energy dispersive X-ray (TEM-EDX, X-MAX 80 TLE detector, Oxford , Abingdon, England) and atomic probe tomography (APT, LEAP5000XR, CAMECA, Gennevilliers, France). The misfit dislocations in the sigma-shaped cavity of the e-SiGe S/D region were analyzed using high-resolution TEM (HR-TEM, JEM2100F, JEOL, Tokyo, Japan). The strain induced in the channel was calculated using a fast Fourier transform image obtained through the nano-beam diffraction (NBD) method and simulated using ANSYS software (version 19, ANSYS, Workbench, PA, USA). The electrical properties of the p-MOSFETs were characterized using a semiconductor parameter analyzer (Agilent, B1500A, CA, USA).



**Figure 1.** (a) The process flow and schematic structure at each step. (b) Anisotropic Si etch through dry etching using HBr, Cl<sub>2</sub>, He. (c) The sigma-shaped cavity was formed through wet etching. (d) Multilayer SiGe epitaxial growth. (e) Cross-sectional TEM image after SiGe growth.

#### 3. Results and Discussion

Figure 1 shows the formation of sigma cavity in the transistor for inducing a strain in the Si channel. After the Si was anisotropically patterned through dry etching, as shown in Figure 1b, a sigma-shaped cavity, as shown in Figure 1c, was formed at an angle of 54° through the anisotropic etching of the Si (111) plane with tetramethyl ammonium

hydroxide (TMAH) [20,21], which directly affects the electrical performance, especially the on-current [22]. To understand the intrinsic  $C_{\text{Ge}}$  effect of SiGe, a sigma cavity was created through minimization in the range of 3-sigma (0.67%), which could minimize the variation in the sigma cavity shape. L1, L2, and L3 were grown on a sigma-shaped cavity and they played different roles, as shown in Figure 1d. L1 was a buffer layer with a relatively low  $C_{\text{Ge}}$  of 25 at.%, which improved the poor coverage of the sigma-shaped cavity; this originated from the low growth rate of the Si (100) plane, caused by the narrow width of the bottom layer. In addition, L1 suppressed the strain relaxation due to the lattice mismatch between the Si substrate and L2 and the punch between the source and the drain. L2 possessed a relatively high  $C_{\text{Ge}}$  of 50 at.%–60 at.% and was epitaxially grown as a main stressor. This layer induced a strong compressive strain in the channel because of the lattice mismatch originating from its high  $C_{\text{Ge}}$ , which, in turn, boosted the channel current. Finally, the L3 layer was made of pure Si fabricated using the epitaxy method, which capped the L2 layer. The L3 layer acted as a sacrificial layer to supply the necessary Si for forming the silicide-reduced contact resistance in the S/D region. To supply hole carriers in the S/D region, boron was incorporated in situ at doping concentrations of less than  $1 \times 10^{19}$  and  $2 \times 10^{20}$  atoms/cm<sup>3</sup> in L1 and L2, respectively. After the native oxide was removed through in situ dry cleaning, the L1, L2, and L3 layers were epitaxially grown by remote plasma chemical vapor deposition without a vacuum break, as shown in Figure 1d. The SiGe or Si epitaxial layers of L1, L2, and L3 were grown using  $SiCl_2H_2$ (dichlorosilane, DCS) and  $GeH_4$  as precursors, and the selectivity was determined by co-flowing HCl gas [23–25]. L1, L2, and L3 were grown at 660, 620, and 750 °C, respectively. The fabricated MOSFETs showed uniformly patterned sigma-shaped cavities in the S/D region with critical dimensions of approximately 10, 30, and 30 nm for the top, center, and depth of the cavity, respectively, as shown in Figure 1e. Both L1 and L2 were uniformly grown at different growth rates induced by the crystal plane of the Si substrate [26].

Figure 2 shows the vertical and longitudinal distributions of  $C_{Ge}$  in SiGe, as measured using TEM-EDX. The *x*-axis in Figure 2a,b correspond to the red and blue dots, respectively, in the inset of Figure 2a. Ge was not detected at vertical positions 1 and 2, indicating that they corresponded to the Si substrate. At vertical position 3,  $C_{Ge}$  was approximately 22.6 at.%–28.5 at.%, which increased to approximately 30.2 at.%–36.6 at.% at vertical position 5. It fluctuated between 51 at.% and 61 at.% at vertical positions 6–9, and then dropped steeply to 0 at.% at vertical positions 11 and 12. This indicates that L1, L2, and L3 were formed cleanly without any intermixing between L1 and L3. In the longitudinal direction,  $C_{Ge}$  was distributed across the five regions. Regions I and V had  $C_{Ge}$  of 0 at.%, which indicates that these corresponded to the Si substrate. In regions II and IV, C<sub>Ge</sub> was distributed between 20 at.% and 26 at.%, and in region III, C<sub>Ge</sub> was 46.9 at.%, 54.6 at.%, and 58.7 at.%. To precisely determine C<sub>Ge</sub>, APT was used to analyze the sigma-shaped cavity, which included L2 with  $C_{Ge}$  = 55 at.%. This region is marked by white dots, as shown in the inset of Figure 2a. Although the data are not shown,  $C_{\text{Ge}}$  was 57.22 at.%, which is similar to the results obtained by TEM-EDX. The change in strain due to variations in  $C_{\text{Ge}}$ in L2 was evaluated according to the misfit dislocations and NBD analysis.



**Figure 2.**  $C_{\text{Ge}}$  distribution for (**a**) vertical and (**b**) longitudinal direction of  $C_{\text{Ge}}$  = 50, 55, and 60 at.% in SiGe of L2.

Figure 3 shows the simulated strain map of L2 in the p-MOSFETs for various  $C_{\text{Ge}}$ . The strain is expressed as a normalized value because the material properties set for the simulation did not precisely coincide with the actual films. The compressive and tensile stresses are represented by negative and positive values, respectively. A negative strain was generated below the tip of the sigma-shaped cavity and applied to the Si channel. In addition, the regimen of generated negative strain widened with increasing  $C_{\text{Ge}}$  in L2. Finally, the strain in the channel shifted to a negative value with an increase in the  $C_{\text{Ge}}$ . This implies that the negative strain increased the compressive stress in the Si channel. Thus, increasing the  $C_{\text{Ge}}$  should boost the current by inducing compressive stress in the Si channel.



**Figure 3.** Simulated strain maps for (**a**)  $C_{\text{Ge}} = 50 \text{ at.\%}$ , (**b**) 55 at.% and (**c**) 60 at.% in SiGe of L2.

To verify the change in actual strain of the Si channel, the strain was measured at five points through NBD analysis, as marked by red circles in the inset of Figure 4a. The Si channel with the e-SiGe S/D region, including L2 at  $C_{Ge} = 50$  at.%, displayed a strain of approximately -0.44% at the center (point 3). This value remained almost constant regardless of the measurement position. When the  $C_{\text{Ge}}$  was increased to 55 at.%, the strain shifted to approximately -1.02%. This indicates that the compressive stress induced by the extended S/D was effectively applied to the Si channel, and the stress increased with an increased  $C_{\text{Ge}}$  in L2. The strain in the Si channel at L2 for  $C_{\text{Ge}}$  = 55 at.% showed a parabolic distribution with the highest value at position 3. This value can be attributed to the symmetric placement of the S/D [27]. However, when the  $C_{\text{Ge}}$  in L2 was increased to 60 at.%, the strain became less negative, i.e., the applied stress decreased. Thus, the number of misfit dislocations was counted to verify the change in stress relaxation with increasing  $C_{\text{Ge}}$  in L2, as shown in Figure 4b. The number of misfit dislocations generated for 100 sigma-shaped cavities was evaluated and statistically organized. L2 with  $C_{\text{Ge}} = 50 \text{ at.}\%$ , 55 at.%, and 60 at.% showed 2.10, 6.15, and 21.05 misfit dislocations with standard deviations of 1.25, 1.90, and 5.27, respectively. This indicates that an increase in  $C_{\text{Ge}}$  is accompanied by local stress relaxation. In addition, the misfit dislocations were not generated linearly with increasing  $C_{Ge}$ . The steep increase in the number of misfit dislocations between  $C_{\text{Ge}} = 55 \text{ at.}\%$  and 60 at.% indicates a critical  $C_{\text{Ge}}$  of approximately 55 at.%–60 at.% for relaxing the stress induced between SiGe and Si. The abovementioned results reveal that the strain induced in the Si channel can be maximized by optimizing the  $C_{\text{Ge}}$  with respect to stress generation and relaxation.



**Figure 4.** (a) Strain distributions measured for various  $C_{\text{Ge}}$  in SiGe of L2 by NBD analysis and (b) the number of misfit dislocation included in L2 (counted for 100 sigma cavities and statistically calculated).

To determine the effect of the changes in stress on the electrical performance of the p-MOSFET, electrical properties, such as the off current ( $I_{off}$ ) and drain saturation current ( $I_{dsat}$ ), were evaluated. The p-MOSFET with L2 ( $C_{Ge} = 25 \text{ at.}\%$ ) was used as a reference for comparison with the p-MOSFETs having the e-SiGe S/D regions. Figure 5 shows that  $I_{dsat} = 450 \ \mu\text{A}/\mu\text{m}$  was obtained at  $I_{off} = 100 \ \mu\text{A}/\mu\text{m}$  with a drain voltage ( $V_{DD}$ ) of 1 V for the reference p-MOSFET. For L2 layers with  $C_{Ge} = 50 \ \text{at.}\%$  and 55 at.%,  $I_{dsat}$  values of approximately 710  $\mu\text{A}/\mu\text{m}$  were obtained; this indicates an improvement of approximately 58%. However,  $I_{dsat}$  decreased to 620  $\mu\text{A}/\mu\text{m}$  when the  $C_{Ge}$  in L2 was increased to 60 at.%.

This tendency coincides with the change in strain with increasing  $C_{\text{Ge}}$  in L2, as shown in Figure 4a. This shows strong evidence that the local compressive strain should be maximized by increasing the  $C_{\text{Ge}}$  in L2 to suppress stress relaxation and boost the current in the channel.



**Figure 5.**  $I_{off}$  versus  $I_{dsat}$  for 28-nm-logic p-MOSFET with various  $C_{Ge}$  of L2 in SiGe of embedded S/D.

#### 4. Conclusions

In this work, SiGe was grown by the epitaxy method with various  $C_{Ge}s$  in L2 through remote plasma CVD. The effect of varying  $C_{Ge}$  for L2 in the sigma-shaped cavity for the S/D region of a 28-nm-p-MOSFET was quantitatively investigated using TEM-EDX and APT. The different layers of e-SiGe were clearly defined, and the L2 layer possessed a  $C_{Ge}$ of 50 at.%–60 at.%. The simulated strain map showed that the strain near the tip of the sigma-shaped cavity was locally focused and increased with the  $C_{Ge}$  in L2. In contrast, the measured strain in the sigma-shaped cavity revealed that the strain decreased when  $C_{Ge} = 60$  at.% in L2 owing to local stress relaxation caused by the formation of misfit dislocations. The change in  $I_{off}$  caused by a change in  $I_{dsat}$  strongly coincided with the change in local strain with increasing  $C_{Ge}$  in L2. This clearly verifies that the channel current can be boosted by maximizing the  $C_{Ge}$  in SiGe to suppress local stress relaxation, thus resulting in the formation of misfit dislocations.

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