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Transport Characteristics of Silicon Multi-Quantum-Dot Transistor Analyzed by Means of Experimental Parametrization Based on Single-Hole Tunneling Model

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Abstract: The transport characteristics of a gate-all-around Si multiple-quantum-dot (QD) transistor were studied by means of experimental parametrization using theoretical models. The device was fabricated by using the *e*-beam lithographically patterned Si nanowire channel, in which the ultrasmall QDs were self-created along the Si nanowire due to its volumetric undulation. Owing to the large quantum-level spacings of the self-formed ultrasmall QDs, the device clearly exhibited both Coulomb blockade oscillation (CBO) and negative differential conductance (NDC) characteristics at room temperature. Furthermore, it was also observed that both CBO and NDC could evolve along the extended blockade region within wide gate and drain bias voltage ranges. By analyzing the experimental device parameters using the simple theoretical single-hole-tunneling models, the fabricated QD transistor was confirmed as comprising the double-dot system. Consequently, based on the analytical energy-band diagram, we found that the formation of ultrasmall QDs with imbalanced energetic natures (i.e., imbalanced quantum energy states and their imbalanced capacitive-coupling strengths between the two dots) could lead to effective CBO/NDC evolution in wide bias voltage ranges.

Keywords: quantum dot; Coulomb blockade; single-electron tunneling; transport mechanism

Citation: Lee, Y.; Jun, H.; Park, S.; Kim, D.Y.; Lee, S. Transport Characteristics of Silicon Multi-Quantum-Dot Transistor Analyzed by Means of Experimental Parametrization Based on Single-Hole Tunneling Model. *Nanomaterials* **2023**, *13*, 1809. https://doi.org/10.3390/nano13111809

Academic Editor: Antonio Di Bartolomeo

Received: 24 April 2023
Revised: 29 May 2023
Accepted: 2 June 2023
Published: 5 June 2023

1. Introduction

Recently, to manipulate the vast amount of electronic information data (e.g., big data processes, artificial intelligence, the Internet of Things, etc.), many research groups have devoted their work to demonstrating how novel semiconductor quantum-dot (QD) devices can realize future quantum computations [1–5]. Among various semiconductor QD devices, the silicon (Si) QD-based single-electron (or single-hole) tunnel-junction transistor is one of the most promising device schemes because of its unique transfer and output characteristics. Namely, owing to the strong sub-band modulation in Si QDs, one could effectively demonstrate the unique features of both Coulomb blockade oscillation (CBO) and negative differential conductance (NDC) in a single device system even at room temperature [6–11]. Additionally, from both scientific and technical perspectives, the Si process platform is still powerful for driving significant advancements in future nanodevice fabrication technology. By utilizing CBO and NDC characteristics, several types of extraordinary data-processing circuits have been conceived and demonstrated on various Si QD device architectures (e.g., multi-functional logic circuits [12], multi-valued logic circuits [8,13], stochastic data-processing circuits [14,15], quantum cellular automata [16], etc.). To establish a tangible application platform of such astonishing functionalities, the precise control of single-electron (or single-hole) tunneling must be satisfied, particularly at an elevated temperature above 300 K. In other words, electrical one-electron (or one-hole) addition energy (i.e., charging/discharging energy for single-electron (or one-hole)

tunneling into/from the Si QD) should be precisely controlled by changing the external bias voltages of the fabricated QD tunnel-junction transistor. Typically, the dot potential of the three-terminal QD transistor is controlled by the gate voltage (V_G) and the drain voltage (V_D) of the QD transistor so that the CBO and NDC behaviors can take place via one-by-one single-electron (or one-hole) tunneling through the quantum energy states. In lithographically patterned CMOS-compatible Si QD transistors, however, co-tunneling effects and thermally activated carrier conduction often occur because of the parasitic metal-oxide-semiconductor field-effect transistor (MOSFET) [17–19]. To solve this issue, in our previous studies we investigated effective ways to reduce thermal quenching and thermal broadening of CBO and NDC by forming an ellipsoidal Si QD structure [8,20] and/or constructing a Si multi-QD system [12,21]. The former utilizes the large quantum-level spacings of the ellipsoidal Si single-QD system, and the latter uses the reduced electron temperature in the multiple-tunnel-junction system. To take full advantage of these Si QD transistors, as a primary task, one needs to understand their transport mechanisms. In the case of single-QD systems, the single-electron (or single-hole) transport mechanisms are well understood due to many substantial studies being conducted on both theoretical models and experimental analyses [22–28]. However, in the case of the multi-QD devices, experimental understandings of their transport behaviors were somewhat restricted because of stochastic tunneling events. Therefore, it is essential to find an easy approach that can enable experimental understandings of the single-electron (or single-hole) transport mechanisms in the multi-QD transistors.

Based upon all of the above background information, we fabricated a Si multi-QD transistor and characterized its transport mechanisms by means of experimental parametrization, which was fully based on the theoretical single-hole-tunneling model. The device was devised in the form of the gate-all-around (GAA) Si nanowire-channel MOSFET, in which self-assembled multiple Si QDs were created along the Si nanowire channel. Herein, the single-hole transport characteristics of the fabricated Si multi-QD transistor are thoroughly examined and discussed through comprehensive studies on both experimental characterization and theoretical analysis.

2. Experimental Section

Figure 1a schematically illustrates the device configuration of the fabricated Si multi-QD transistor, which was constructed in the form of the CMOS-compatible GAA Si nanowire-channel MOSFET. To devise such an architecture, firstly, the [100] Si nanowire channel (l: 200 nm, w: 40 nm) was patterned by e-beam lithography onto the silicon-on-insulator substrate (t_{Si}: 10 nm). Subsequently, the volumetric size of the patterned Si nanowire was further reduced by isotropic wet etching using the SC-1 solution (NH_4OH:H_2O_2:H_2O = 1:1:6). Through this step, the width of the Si nanowire was shrunk to be approximately 10 nm (Figure 1b). Next, with the aim of constructing the GAA structure, a part of the buried oxide (i.e., SiO_2 underneath the Si nanowire) was removed through oxide etching by using diluted hydrogen fluoride (HF:H_2O = 1:10). After this step, only a small part of the Si nanowire channel was suspended from the buried oxide because the large source (S) and drain (D) areas could still support the beam shape of the Si nanowire channel. To create the gate oxide of the GAA MOSFET structure, the surface of the suspended Si nanowire channel was then oxidized through dry oxidation at 900 °C. Due to oxidation of the Si nanowire surface, the cross-sectional diameter of the Si nanowire (d_{NW}) was eventually further decreased down to approximately 5 nm [6,29]. Thereafter, the formation of the GAA stack was completed by depositing the additional layers of SiO_2 (approximately 30 nm) and polycrystalline n^+-Si (approximately 250 nm). Finally, the S and D reservoirs ($p \approx 10^{20}$ cm^{-3}) were formed by BF_2^+ ion implantation and thermal activation at 950 °C.

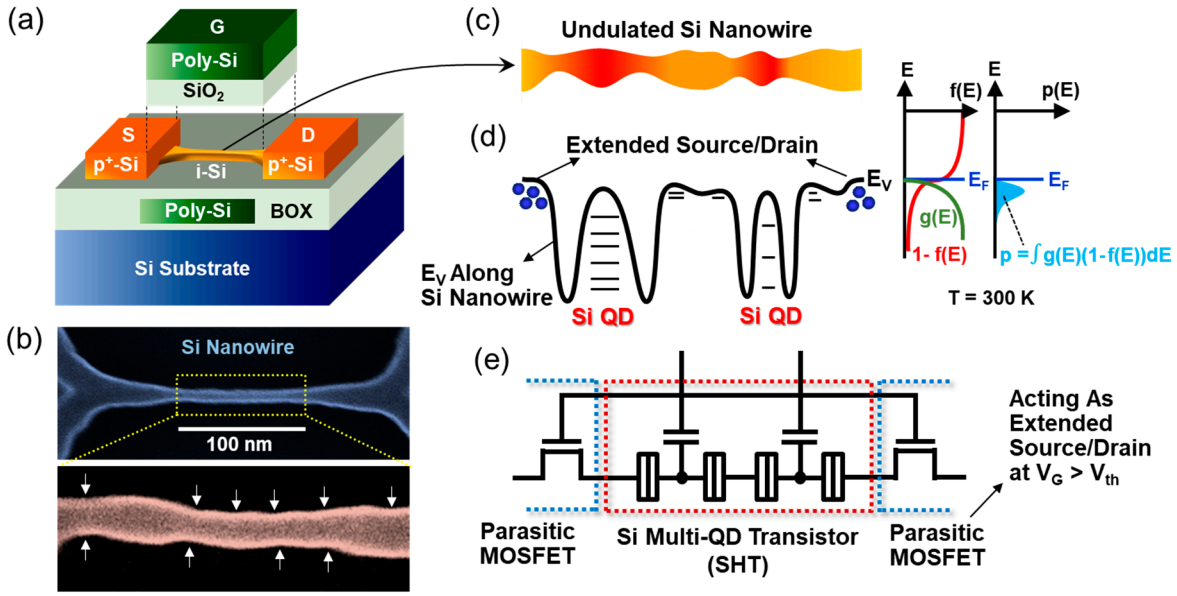

Figure 1. (**a**) Schematic configuration of the fabricated Si multi-QD transistor. (**b**) SEM image of the volumetrically undulated Si nanowire channel. (**c**) Schematic illustration of the undulated Si nanowire channel. (**d**) Expected energy-band diagram at the valence band region of the undulated Si nanowire channel and its corresponding Fermi–Dirac distribution function, density of state function, and carrier distribution function. E_V and E_F denote the valence band and the Fermi level, respectively. (**e**) Equivalent circuit composed of the active device of the Si multi-QD transistor with two parasitic MOSFETs at S/D regions.

3. Results and Discussion

Prior to discussing the electrical characteristics of the fabricated device, we will explain our device fabrication method that was employed to perform the room-temperature operation of the fabricated Si QD transistor. We obtained the self-created Si QDs through oxidation of the volumetrically undulated ultra-narrow Si nanowire. Notably, no intentional design of the QD sites and sizes was employed in our experiment. According to previous studies [30–35], there are two main approaches to devise two types of high-performance Si QD transistors: one is Si QD transistors based on epitaxially grown Si QDs [30–32], and the other is lithographically fabricated Si QD transistors [30–32]. Although the former could allow for the operation of the fabricated devices at elevated temperatures, the method is inappropriate for practical applications because of difficulties in both size and site controls. On the other hand, the latter is useful for controlling both the size and the site of the QDs. Hence, many researchers have devoted their studies to fabricating high-performance Si QD transistors by using lithography techniques. For example, forming the double/multiple barrier tunnel junctions by pattern-dependent oxidation (PADOX) [36–38] and creating the electrical dots/barriers by side-gate formation [39–41] are typical examples that can enable the fabrication of high-performance CMOS-compatible Si QD transistors. When considering the device operation temperature, however, these techniques do not satisfy the conditions for room-temperature operation because conventional lithography techniques only allow for the formation of large QD sizes and small tunnel barrier heights. We therefore adopted the QD self-formation method by using a volumetrically undulated ultra-narrow Si nanowire. Although the proposed method cannot ensure the precise size/site/number control of the Si QDs, we believe the method will be good for use in future CMOS-compatible Si QD device technology. This is because the method used here is already compatible with CMOS fabrication processes and can be further developed when advanced nanolithography techniques are well established in the near future. In other words, if the intentional patterning of the regularly undulated sub-5 nm Si nanowire is available when using the advanced lithography techniques (e.g., extreme ultraviolet

lithography [42,43], heavy-ion lithography [44], scanning probe lithography [45], block copolymer self-assembly [46], etc.), one can easily control the number, sizes, and sites of the Si QDs by employing the PADOX process method as well.

Next, we interpreted the QD nature inside the volumetrically undulated ultra-narrow Si nanowire channel. As schematically illustrated in Figure 1c, during the isotropic wet-etching process, the magnitude of d_{NW} fluctuated along the undulated Si nanowire direction. Here, it can be noticed that such a volumetric d_{NW} fluctuation is much more significant after thermal oxidation of the Si nanowire surface. Thus, the d_{NW} sizes at the squeezed regions are much smaller than 5 nm because the d_{NW} at the central Si nanowire area was confirmed to be approximately 5 nm [6,29]. According to the quantum-mechanical energy-band calculation [47–49], the sub-band modulation in the [100] Si nanowire significantly increases with decreasing d_{NW}. For instance, when d_{NW} is <2 nm in the [100] Si nanowire, the ground state is located at more than 400 meV below the valence band (E_V) of the bulk Si [8,48]. In the present type of the volumetrically undulated Si nanowire channel, therefore, the Si multi-QD system can be self-assembled along the nanowire. In other words, the large potential barriers are formed at the squeezed Si nanowire areas (i.e., $d_{NW} << 5$ nm), and the quantum dots are created at the rest areas (i.e., $d_{NW} \approx 5$ nm), as represented in Figure 1d. This allows the fabricated GAA Si nanowire-channel MOSFET to act as the Si multi-QD transistor. At this point, one can disregard the presence of large dots since their quantum-level spacings are too small to significantly contribute to the tunneling transport characteristics. In short, at 300 K, both the large thermal fluctuation at the bigger dots and the broad hole carrier distribution at the S/D reservoirs smear the presence of the large dots. Additionally, it should be remembered that the GAA gate stacks cover the nanowire edges at the S/D and multi-QD regions. Thus, these two nanowire edges (i.e., extended S/D regions) play a role as the parasitic MOSFET (Figure 1e), which may eventually give rise to the increase in the valley current of the present CMOS-compatible GAA MOSFET-based Si multi-QD transistor. For example, when the gate bias voltage (V_G) is greater than the threshold voltage (V_{th}) of the parasitic MOSFET, the drift current component of the parasitic MOSFET largely contributes to the increase in total drain current (I_D) of the actual device (Figure 2a). This would, in turn, smear out the CBO features at the higher V_G region.

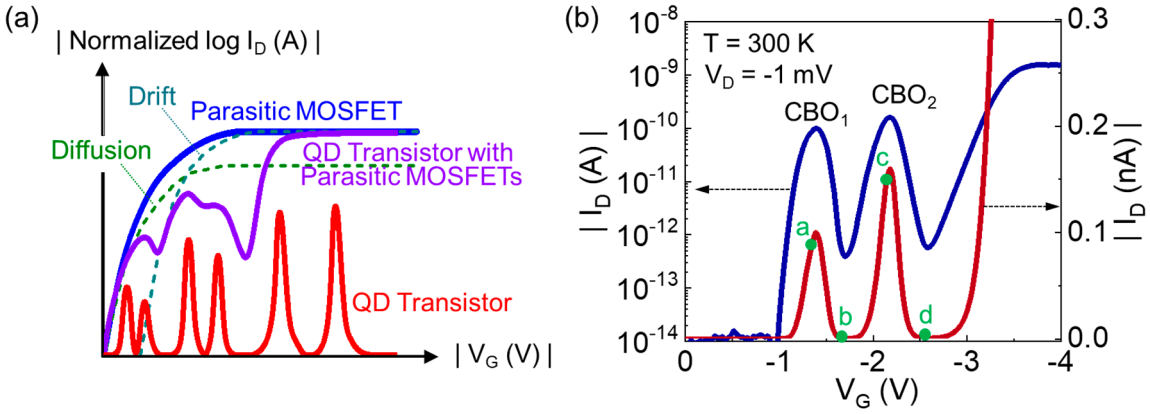

Figure 2. (**a**) Normalized I_D for the Si multi-QD transistor, parasitic MOSFET, and fabricated device including both the Si multi-QD transistor and the parasitic MOSFET. (**b**) Transfer characteristic curves of the fabricated device (i.e., I_D–V_G at $V_D = -1$ mV).

Despite such a parasitic MOSFET effect, the fabricated Si multi-QD transistor clearly exhibits two large CBO peaks at 300 K in its I_D–V_G characteristic curves (Figure 2b). The magnitudes of the peak-to-valley current ratio (PVCR) are 261 and 288 for the first CBO_1 and the second CBO_2, respectively. In addition, the values of the full width at half-maximum (FWHM) are approximately 192 and 188 mV for CBO_1 and CBO_2, respectively. In principle, for the room-temperature observation of such clear CBO characteristics, the one-electron

(or hole)-addition energy (E_a) should be sufficiently larger than the thermal energy at room temperature (i.e., $E_{th} \approx 26$ meV at 300 K) [20,50]. E_a is given by

$$E_a = E_C + \Delta\varepsilon \quad (1)$$

$$E_C = q^2/C_{QD} \quad (2)$$

$$C_{QD} = 2\pi\varepsilon\varepsilon_0 d_{QD} \quad (3)$$

where E_C, $\Delta\varepsilon$, q, C_{QD}, ε, ε_0, and d_{QD} are the charging energy, quantum-level spacing, unit charge, QD capacitance, dielectric constant of SiO_2, and vacuum permittivity, respectively. Thus, one can conclude that the present device includes ultrasmall QDs (i.e., $d_{QD} < 5$ nm) inside the Si nanowire channel. Furthermore, since both PVCR and FWHM are closely related to the thermal fluctuation of the QDs [51,52], the observed large PVCR and small FWHM values obviously indicate that the present device contains ultrasmall QDs that may possess large $\Delta\varepsilon$ values (>>26 meV).

The existence of the ultrasmall QDs can be further elucidated from the charge stability diagram of the fabricated Si multi-QD transistor. As denoted by CB_1 and CB_2 in Figure 3a, the device exhibits the two Coulomb blockade regions, which correspond to CBO_1 and CBO_2 in Figure 2b, respectively. Here, it should be noticed that both the CB_1 and CB_2 regions are extended toward the A and B directions. In the case of CB_1, particularly, the extended CB regions do not disappear even at a high V_D up to $\pm$0.8 V. According to our previous studies [51,53], such a long and clear CB extension is attributed to both the large quantum-level spacings and the large tunneling barrier heights. Additionally, as indicated by CB_3, the present device shows the overlapped CB region, which is also extended toward the A′ and B′ directions. This depicts how present device comprises the multi-QD system with irregular dot-and-barrier shapes. As previously mentioned, in the present device, the multi-QD system was self-formed along the undulated Si nanowire at the volumetrically shrunken areas (i.e., squeezed regions = tunnel barriers and their adjacent areas = dots). Thus, both the quantum-level spacings and the tunnel barrier heights are inhomogeneous. This might result in imbalanced energetic CB conditions for each QD; hence, the stochastic tunneling events would occur throughout the entire multi-QD system [54]. Therefore, some parts of the adjacent CB regions could be overlapped at certain bias voltages.

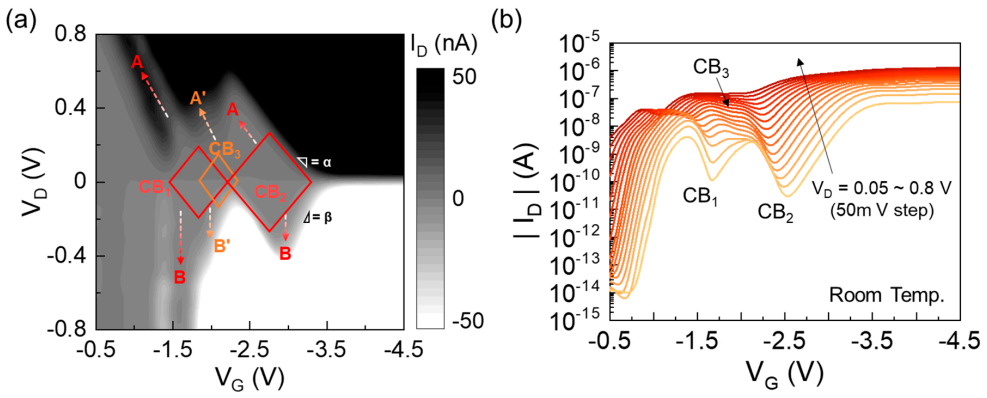

Figure 3. (**a**) Contour plot of I_D as functions of V_G and V_D. (**b**) CBO evolution at the positive V_D region (=0.05–0.8 V).

The split of the CBO peaks can also verify the formation of the multi-QD system. For example, when applying a high V_D that can break a certain stochastic tunneling condition, the multi-QD system begins to renormalize its energetic condition for stochastic tunneling. Namely, some of the quantum states start and/or stop contributing their energetic pathways to the renormalized stochastic tunneling transport condition. Then, the CBO peaks eventually split at the high V_D [12]. In the present device, as can be seen from Figure 3b, the

CBO peaks are split at the high V_D region so that the additional CB_3 region starts appearing in between the CB_1 and CB_2 regions. This corresponds to the extension of the CB_3 region toward the A′ direction, as observed in the charge stability diagram (Figure 3a). Based upon these results, one can surmise that the present device is composed of multiple Si QDs. According to both theoretical and experimental studies [21,55], the formation of the multi-QD system is helpful for reducing the co-tunneling effect so that the valley current (I_{valley}) of the CBO can be decreased at the higher V_D region. Correspondingly, the present device exhibits the clear valley states even at a high V_D above 0.5 V (Figure 3b).

According to the co-tunneling model [21,56], I_{valley} is given by

$$I_{valley} \equiv G_b^{N+1}\left\{(eV_D)^2 + \left(2\pi k_B T_{eff}\right)^2\right\}^N V_D \quad (4)$$

where G_b^{N+1} is the conductance multiplication for every tunnel barrier, N is the number of QDs, k_B is the Boltzmann constant, and T_{eff} is the effective electron temperature. Therefore, one can easily deduce the number of QDs by using the above equation. For example, when N = 1 (i.e., single-QD system), 2 (i.e., double-QD system), and 3 (i.e., triple-QD system), I_{valley} can be described as follows:

$$I_{valley(N=1)} = \alpha G_S G_D\left\{e^2 V_D^3 + \left(2\pi k_B T_{eff}\right)^2 V_D\right\} \quad (5)$$

$$I_{valley(N=2)} = \beta G_S G_i G_D\left\{e^4 V_D^5 + 2e^2\left(2\pi k_B T_{eff}\right)^2 V_D^3 + \left(2\pi k_B T_{eff}\right)^4 V_D\right\} \quad (6)$$

$$I_{valley(N=3)} = \gamma G_S G_{i1} G_{i2} G_D\left\{e^6 V_D^7 + 3e^4\left(2\pi k_B T_{eff}\right)^2 V_D^5 + 3e^2\left(2\pi k_B T_{eff}\right)^4 V_D^3 + \left(2\pi k_B T_{eff}\right)^6 V_D\right\} \quad (7)$$

where α, β, and γ are the proportional factors, and G_S, G_i, and G_D are the source, intermediate, and drain conductance values, respectively. By fitting the experimental I_{valley} values to Equations (5)–(7), one can find out the number of QDs in the multi-QD transistor. Figure 4a,b shows the I_{valley} values as a function of V_D for CBO_1 and CBO_2, respectively. The closed circles are the experimental I_{valley} data at each CB state, and the dot-dashed, solid, and dashed lines are the best-fitted curves obtained by using Equations (5)–(7), respectively. As can be confirmed from Figure 4a,b, the experimental I_{valley} values of CBO_1 and CBO_2 were well fitted only when N = 2. One can therefore conjecture that the present multi-QD transistor was constructed with the double-dot system.

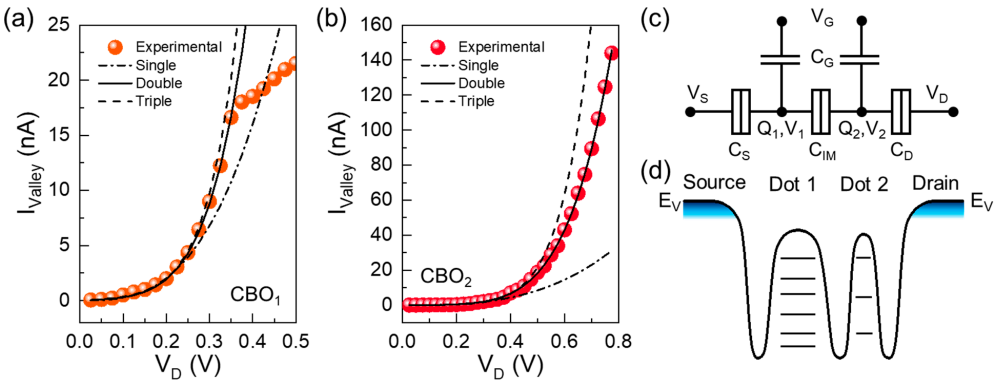

Figure 4. I_{valley} as a function of V_D for (**a**) CBO_1 and (**b**) CBO_2. (**c**) Equivalent circuit of the Si multi-QD transistor. (**d**) Energy-band diagram at the valence band region along the S-channel-D direction expected from fitting the experimental data to the theoretical models.

At this point, it should be noted that the sizes and the shapes of both the dots and the barriers are inhomogeneous in the present multi-QD transistor. This strongly affects the energy-band profile of the multi-QD system. To qualitatively infer the energy-band diagram of the present device, we analyzed the capacitance ratios because these values provide electrostatic information on the dots and barriers. Firstly, we assume that, based upon the above results, the present device includes two QDs (i.e., $N = 2$). As represented in the equivalent circuit (Figure 4c), each QD is separated by tunnel barriers (i.e., C_S: source-side tunnel barrier; C_{IM}: QD-to-QD intermediate tunnel barrier; and C_D: drain-side tunnel barrier) and is capacitively coupled to the GAA stack (i.e., C_G: gate oxide). In this double-QD system, the total charge in each dot (Q_1 or Q_2) equals the sum of charges stored in all the capacitors connected to the dot, and it can be described by [19,57]

$$Q_1 = C_S(V_1 - V_S) + C_G(V_1 - V_G) + C_{IM}(V_1 - V_2) \tag{8}$$

$$Q_2 = C_D(V_2 - V_D) + C_G(V_2 - V_G) + C_{IM}(V_2 - V_1) \tag{9}$$

where V_1 and V_2 are the electrostatic potentials for QD_1 and QD_2, respectively. Accordingly, V_1 and V_2 can also be determined by the following relationship:

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \frac{1}{C_1C_2 - C_{IM}^2} \begin{pmatrix} C_2 & C_{IM} \\ C_{IM} & C_1 \end{pmatrix} \times \begin{pmatrix} Q_1 + C_SV_S + C_GV_G \\ Q_2 + C_DV_D + C_GV_G \end{pmatrix} \tag{10}$$

where C_1 and C_2 are the total electrostatic capacitances of QD_1 and QD_2 at the charged states under the given bias voltages (i.e., $C_1 = C_G + C_S + C_{IM}$ and $C_2 = C_G + C_D + C_{IM}$), respectively. Here, it should be noted that the CB state begins to appear when the electrostatic potentials of the two electrical dots are the same. When assuming $V_1 = V_2$, Equation (10) can be solved as follows:

$$(C_2 - C_1)C_GV_G = (C_1 - C_{IM})C_DV_D - (C_2 - C_{IM})C_SV_S \tag{11}$$

From Equation (11), therefore, the electrostatic charge states at given bias conditions can be described by the following relationships:

$$\frac{V_S}{V_G} = -\frac{(C_2 - C_1)C_G}{(C_2 - C_{IM})C_S} = -\alpha \text{ (for D grounded state; i.e., when } V_D = 0) \tag{12}$$

$$\frac{V_D}{V_G} = \frac{(C_2 - C_1)C_G}{(C_1 - C_{IM})C_D} = \beta \text{ (for S grounded state; i.e., when } V_S = 0) \tag{13}$$

Based on the above model, we determined the magnitudes of $|\alpha|$ (=0.73) and $|\beta|$ (=1.6) from the charge stability diagram (Figure 2a). When considering that the total capacitances of the electrical dots are $C_1 = C_G + C_S + C_{IM}$ and $C_2 = C_G + C_D + C_{IM}$, the obtained result of $|\alpha/\beta| < 0$ represents the fact that C_S is greater than C_D (i.e., $|\alpha/\beta| \propto C_D/C_S < 0$). Again, since $C_S > C_D$, it can be concluded that $C_1 > C_2$ because both C_G and C_{IM} are common in the double-QD system. By means of the above analysis, consequently, one can expect that the source-side QD is larger than the drain-side QD in our Si double-QD transistor. Considering that the smaller QD possesses the lager $\Delta\varepsilon$, the expected potential profile of the present device can be drawn with a bigger source-side QD (i.e., smaller $\Delta\varepsilon$) and a smaller drain-side QD (i.e., larger $\Delta\varepsilon$) (see the valence band profile in Figure 4d).

By using the above analytical energy-band diagram (Figure 4d), we can interpret the possible carrier transport mechanisms of the fabricated Si multi-QD transistor. First, we will explain the double CBO characteristics of the present device. Prior to discussing the carrier transport mechanism, it is important to note that the dot potential is mostly governed by V_G rather than V_D because of the strong capacitive coupling from the GAA structure [29,58]. Thus, we firstly assume that the double-QD transistor is set at specific bias conditions of a moderate $|-V_{G1}|$ and low V_{D1}, at which the initial stage of single-hole tunneling can take place (Figure 5a). At this stage, the hole carrier can be transferred from

D to S via the quantum states of QD_2 and QD_1. When increasing the magnitude of $-V_{G2}$ (e.g., $|-V_{G2}| > |-V_{G1}|$) while maintaining V_D at low V_{D1}, the dot potential decreases. Then, the Si double-QD transistor would be set on the blockade state due to the large $\Delta\varepsilon$ in QD_2 (Figure 5b). As one keeps increasing the magnitude of $-V_G$ (e.g., $|-V_{G3}| > |-V_{G2}|$) at low V_{D1}, the device needs to be set in the on-state to allow single-hole tunneling from D to S via QD_2 and QD_1 (Figure 5c). When further increasing V_G from $|-V_{G3}|$ to $|-V_{G4}|$, the blockade state would appear again because of the large $\Delta\varepsilon$ in QD_2 (Figure 5d). This may allow us to observe the double CBO features from the fabricated device, as depicted in Figure 2b. In short, Figure 5a–d corresponds to the operation points a–d depicted in Figure 2b, respectively.

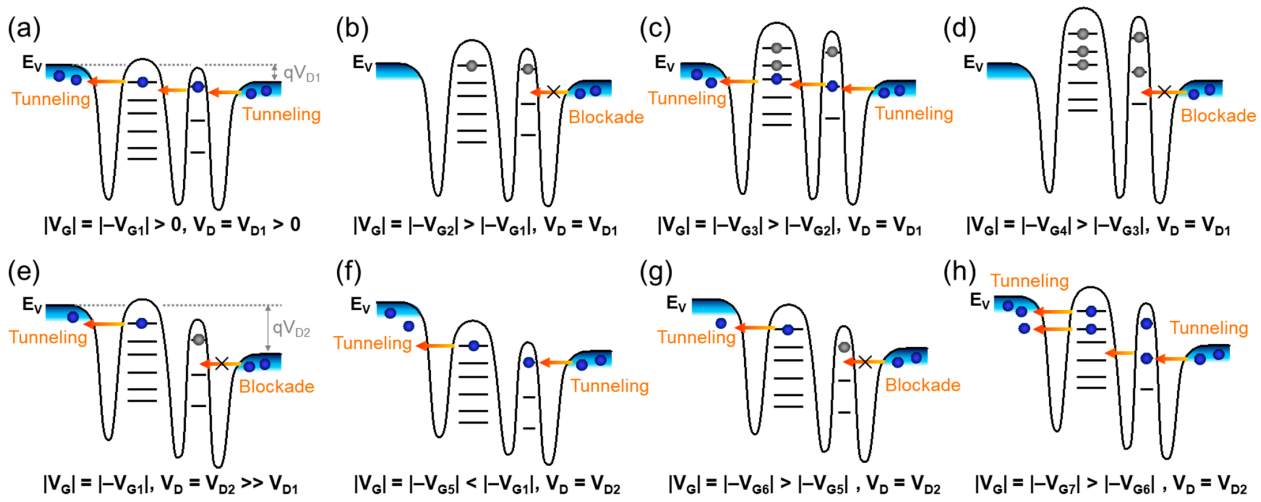

Figure 5. Carrier transport mechanisms of CBO for the double-QD transistor represented in the energy-band diagrams at various bias conditions: (**a**) $|V_G| = |-V_{G1}| > 0$ and $V_D = V_{D1} > 0$, (**b**) $|V_G| = |-V_{G2}| > |-V_{G1}|$ and $V_D = V_{D1}$, (**c**) $|V_G| = |-V_{G3}| > |-V_{G2}|$ and $V_D = V_{D1}$, (**d**) $|V_G| = |-V_{G4}| > |-V_{G3}|$ and $V_D = V_{D1}$, (**e**) $|V_G| = |-V_{G1}|$ and $V_D = V_{D2} >> V_{D1}$, (**f**) $|V_G| = |-V_{G5}| < |-V_{G1}|$ and $V_D = V_{D2}$, (**g**) $|V_G| = |-V_{G6}| > |-V_{G5}|$ and $V_D = V_{D2}$, and (**h**) $|V_G| = |-V_{G7}| > |-V_{G6}|$ and $V_D = V_{D2}$.

Next, we explain the V_D-dependent CBO evolution, which can be observed in Figure 3a,b. For this, firstly, we assume that the device was set on the initial single-hole-tunneling stage at $|-V_{G1}|$ and V_{D1} (i.e., Figure 5a). If one increases V_D from V_{D1} to V_{D2}, the dot potential also increases (Figure 5e) because the capacitive coupling between QD and D would be no longer negligible at a high V_D [17]. At this stage, the single-hole-tunneling event would suddenly stop because the imbalanced capacitive-coupling strengths between G-QD and QD-D would break the tunneling condition (i.e., blockade state). To perform the single-hole-tunneling transport under the same V_{D2} condition, the dot potential should be increased until the D-side Fermi level can meet the first excited quantum state of QD_2. Therefore, one needs to decrease the magnitude of $-V_G$ from $|-V_{G1}|$ to $|-V_{G5}|$ (where $0 < |-V_{G5}| < |-V_{G1}|$) when V_D is increased from V_{D1} to V_{D2} (Figure 5f). Namely, when V_D is positively increased, the V_G bias point should also be positively shifted to satisfy the tunneling-on condition via the first excited state. This eventually leads to the CBO shift toward the A and A′ directions, as already observed in Figure 3a,b. From this bias point (i.e., $|-V_{G5}|$ and V_{D2}), one can demonstrate the multiple CBO peaks by increasing the magnitude of $|-V_G|$ over $|-V_{G5}|$. For example, at the same V_{D2}, the second and/or the third CBO peaks can be demonstrated by repeating the tunneling-off (i.e., $|-V_{G6}| > |-V_{G5}|$, Figure 5g) and tunneling-on (i.e., $|-V_{G6}| > |-V_{G5}|$, Figure 5h) conditions. Here, it should be also noted that the overall quantum energy states are energetically split between QD_1 and QD_2 because of the high V_{D2}. Namely, the overall dot potential of QD_1 is lower than that of QD_2 due to the high V_D. This eventually gives rise to the increase in co-tunneling

events because of the energetic imbalance between QD_1 and QD_2. As a result, the device exhibits the extra CBO peak through the renormalization of stochastic tunneling conditions at a higher V_D (e.g., CB_3 in Figure 3a,b).

The existence of an ultrasmall QD (i.e., large $\Delta\varepsilon$) may allow us to observe the clear NDC features in the output characteristics of the QD transistor. To trace the NDC behaviors, we examined the differential drain conductance (dI_D/dV_D) characteristics of the present device. Figure 6a shows the contour plot of dI_D/dV_D as functions of V_G and V_D. The device clearly reveals the NDC region. For example, with the increasing V_D at a certain V_G (e.g., V_{G8} and V_{G9}), the color of dI_D/dV_D is changed into "white-gray-white-black", which is indicative of the sudden drop in drain conductance at a certain V_D point (i.e., NDC). Interestingly, the NDC region is also extended toward the A direction (Figure 6a). Correspondingly, the NDC peaks shift toward the low V_D region as $|-V_G|$ increases (Figure 6b). These features are analogous to those of CBO, as observed through the CBO evolution along the extended CB region (Figure 3a,b).

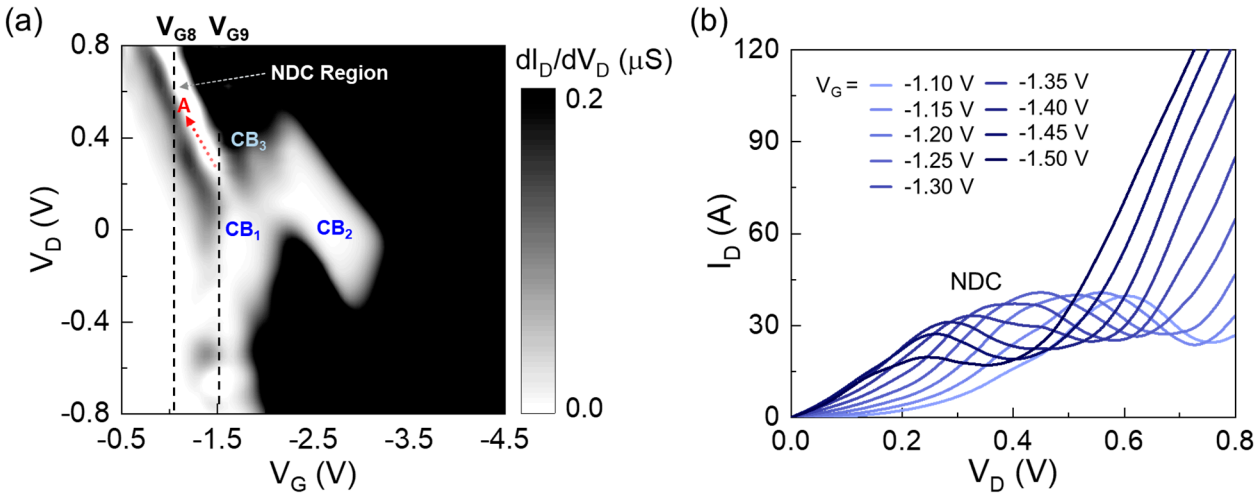

Figure 6. (**a**) Contour plots of dI_D/dV_D as functions of V_G and V_D. (**b**) I_D–V_D characteristic curves at V_G of −1.1–−1.5 V.

The NDC evolution can also be explained by using the aforementioned analytical energy-band diagram. Firstly, we interpret the NDC mechanism of the present device at a low V_G (e.g., $V_G = |-V_{G8}| > 0$). At this V_G bias condition, no hole carriers could transfer from D into QD_2 because the Fermi level of D is far from the first excited state of QD_2 (Figure 7a). In other words, due to the large $\Delta\varepsilon$ of QD_2, it is hard to perform the resonance state when both V_D and V_G are low. The similar situation is maintained unless the magnitude of V_D is increased to match the on-resonance condition (Figure 7b,c). When increasing V_D after the on-resonance at the first excited state, the tunneling event is prohibited again because of the large $\Delta\varepsilon$ between the first and the second excited quantum states (Figure 7d). Thus, one can surmise that the NDC could occur at the relatively high V_D region when V_G is low. Next, we explain the NDC evolution toward the lower V_D region, which was observed when the higher V_G was applied (Figure 6b). Here, let us assume that the device was set at the on-resonance state at an increased V_G (i.e., $|-V_{G9}| > |-V_{G8}|$), even if the magnitude of V_D is the same as the initial V_{D3} above (Figure 7e). From this bias point, if one increases the magnitude of V_D (i.e., $V_D = V_{D4'} > V_{D3}$), the resonance state is immediately changed from 'on' to 'off' (Figure 7f). When increasing V_D more from $V_{D4'}$ to $V_{D5'}$, the second on-resonance state occurs at the second excited state (Figure 7g). At a high V_D (e.g., $V_{D6'} > V_{D5'}$), the on-resonance state would be retained because, at the high V_D, the dot potential would also be capacitively coupled to the drain potential (Figure 7g). As a result, the NDC can occur at the relatively lower V_D region when a higher V_G is applied to

the device. To briefly summarize, the NDC evolution would take place toward the low V_D region as V_G increases.

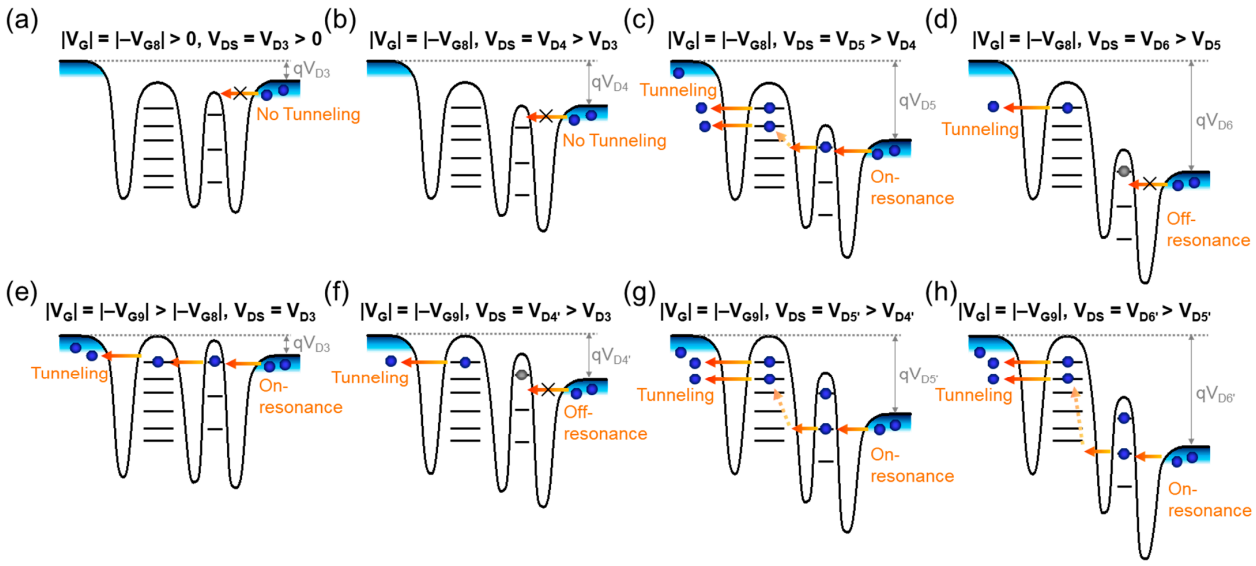

Figure 7. Carrier transport mechanisms of NDC for the double-QD transistor represented in the energy-band diagrams at various bias conditions: (**a**) $|V_G| = |-V_{G8}| > 0$ and $V_{DS} = V_{D3} > 0$, (**b**) $|V_G| = -|V_{G8}|$ and $V_{DS} = V_{D4} > V_{D3}$, (**c**) $|V_G| = |-V_{G8}|$ and $V_{DS} = V_{D5} > V_{D4}$, (**d**) $|V_G| = |-V_{G8}|$ and $V_{DS} = V_{D6} > V_{D5}$, (**e**) $|V_G| = |-V_{G9}| > |-V_{G8}|$ and $V_{DS} = V_{D3}$, (**f**) $|V_G| = |-V_{G9}|$ and $V_{DS} = V_{D4'} > V_{D3}$, (**g**) $|V_G| = |-V_{G9}|$ and $V_{DS} = V_{D5'} > V_{D4'}$, and (**h**) $|V_G| = |-V_{G9}|$ and $V_{DS} = V_{D6'} > V_{D5'}$.

4. Summary and Conclusions

We fabricated a high-performance room-temperature-operating Si multi-QD transistor in the form of the CMOS-compatible GAA Si nanowire-channel MOSFET. Due to the formation of ultrasmall QDs (i.e., large $\Delta\varepsilon$) inside the volumetrically undulated Si nanowire channel, the device clearly exhibited multiple CBO features at 300 K. Owing to the formation of GAA (i.e., strong capacitive coupling to the gate), the device displayed CBO evolution at wide V_D and V_G ranges toward the extended CB region. Because of the large $\Delta\varepsilon$ in the self-formed Si QDs, furthermore, the device not only clearly revealed the NDC oscillation peak but also showed its evolution within wide V_D and V_G ranges. Through experimental parametrization by using the theoretical models, it was found that the fabricated device involves two predominantly ultrasmall QDs. Based upon the analytical energy-band diagram, the carrier transport mechanisms were comprehensively interpreted. Consequently, the present study provides a simple analysis method (i.e., analysis of experimental device parameters in terms of simple theoretical models), which can allow an easy understanding of the experimental single-charge transport behaviors in the multi-QD transistors, holding great promise for future nanoelectronic information technology.

Author Contributions: Conceptualization, Y.L.; methodology, Y.L.; formal analysis, Y.L.; investigation, H.J., S.P. and Y.L.; data curation, H.J., S.P. and Y.L.; validation, D.Y.K. and S.L.; writing—original draft preparation, Y.L.; writing—review and editing, S.L.; supervision, D.Y.K. and S.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the National Research Foundation of Korea through Basic Science Research Programs (2016R1A6A1A03012877, 2021R1I1A1A01049638, and 2023R1A2C1005421) funded by the Korean government.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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