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Study of Silicon Nitride Inner Spacer Formation in Process of Gate-all-around Nano-Transistors

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Abstract: Stacked SiGe/Si structures are widely used as the units for gate-all-around nanowire transistors (GAA NWTs) which are a promising candidate beyond fin field effective transistors (FinFETs) technologies in near future. These structures deal with a several challenges brought by the shrinking of device dimensions. The preparation of inner spacers is one of the most critical processes for GAA nano-scale transistors. This study focuses on two key processes: inner spacer film conformal deposition and accurate etching. The results show that low pressure chemical vapor deposition (LPCVD) silicon nitride has a good film filling effect; a precise and controllable silicon nitride inner spacer structure is prepared by using an inductively coupled plasma (ICP) tool and a new gas mixtures of CH₂F₂/CH₄/O₂/Ar. Silicon nitride inner spacer etch has a high etch selectivity ratio, exceeding 100:1 to Si and more than 30:1 to SiO₂. High anisotropy with an excellent vertical/lateral etch ratio exceeding 80:1 is successfully demonstrated. It also provides a solution to the key process challenges of nano-transistors beyond 5 nm node.

Keywords: inner spacer; gate-all-around (GAA); nanowire; nanosheet; field effect transistor; nanostructure manufacture; high anisotropy; high etch selectivity

1. Introduction

In order to overcome challenges such as short channel effect brought by scaling down metal-oxide-semiconductor field-effect transistors (MOSFETs), many new devices e.g., fin field effective

transistors (FinFETs), tunneling field-effect transistors (TFETs), ultra-thin-body transistors (ULBTs) and gate-all-around nanowire transistors (GAA-NWTs) have been developed [1–3]. However, among this group, nanowire transistors are considered to be the most competitive devices in the future [4,5]. In general, there are two main solutions for manufacturing the (horizontal or vertical) nanowires: one is a bottom-up bulk silicon-based process [6,7]; the other is a top-down fabrication approach using SiGe/Si stacks and selectively etch SiGe as channel material. The latter is more likely to become the mainstream solution for the technology generation below 5nm technology node, because the device's process is very similar to conventional FinFET process flow [8,9].

Inner spacer was designed to reduce the parasitic capacitance between the gate and source/drain in stacked SiGe/Si structure GAA-NWTs [10,11]. The main process flow of GAA devices including the inner spacer process module is shown in Figure 1. The steps with challenges are SiGe cavity etching step and inner spacer formation with precise profile control and no damaging for the nanowires [12,13]. There have been several research reports on SiGe cavity etching [14–16], but a systematic investigation on the formation of inner spacers has still not been investigated.

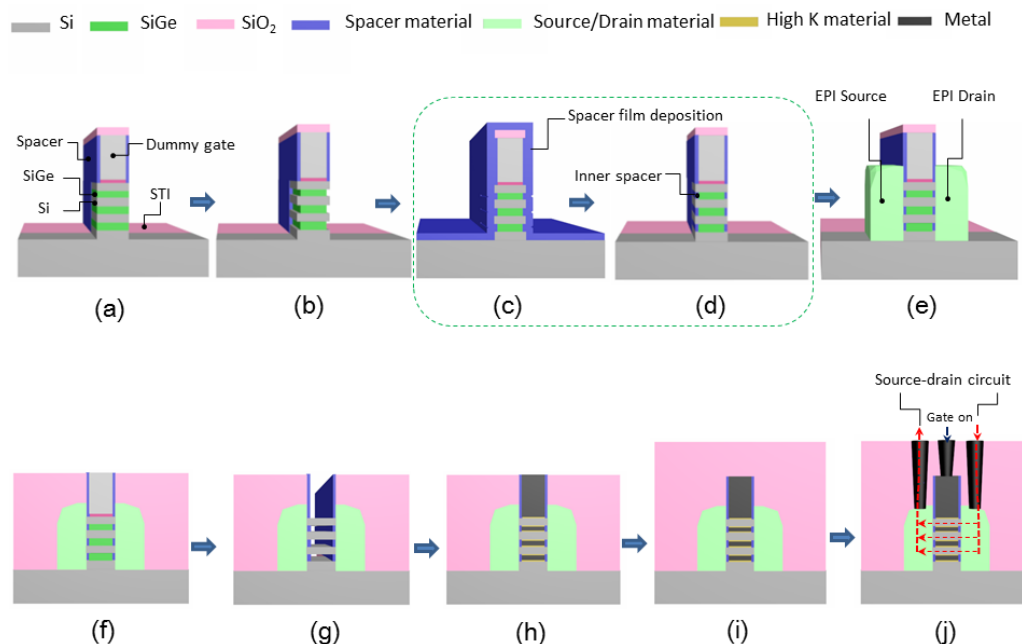


Figure 1. Process flow of nanowires with inner spacer: (a) source/drain Fin recess for opening active area; (b) SiGe cavity etching for defining the growth position and size of the inner spacer; (c) inner spacer film deposition; (d) controlled etching of spacer film and formation of inner spacer; (e) source and drain epitaxial growth; (f) dielectric deposition and planarization; (g) dummy gate removal and silicon nanowires formation; (h) filling and planarization of high-K metal gates; (i) interlayer dielectric deposition; (j) metal contact plug and current direction when device is on.

In comparison with the conventional spacer process, the inner one has more process challenges. As shown in Figure 2a, the requirement of conventional spacer etching is that the spacer material on the top and bottom sides of the gate need to be etched completely, leaving the spacer material on the sidewall. Therefore, this process does not require a high etching selectivity and anisotropy. However, the higher anisotropy and etching selectivity are required to meet the requirements without any causing device failures in process of inner spacers formation [12,17], as shown in Figure 2b,b'.

SiNx with atomic ratio for Si to N of 3:4 is commonly used as spacer material [18,19]. For the etching of SiN, $\text{CF}_4/\text{O}_2/\text{N}_2$, CF_4/CH_4 , SF_6/CH_4 and NF_3/CH_4 were used for conventional plasma etching in the early period, but the selectivity etching of SiN to SiO_2 and Si are not high when the polymer is produced properly [20]. Using neutral beam reaction system, the SiN etch selectivities of 18.6 to SiO_2 and 6.2 to Si can be achieved [21]. Later, BEE Kastenmeier et al. found that the use of microwave

remote plasma can significantly improve the etch selectivity of SiN to Si and SiO₂, and the ratio can reach to 70:1 [22]. However, because of the characteristics of partial isotropic etching, remote plasma is more suitable for SiN sacrificial layer removal than SiN spacer etching.

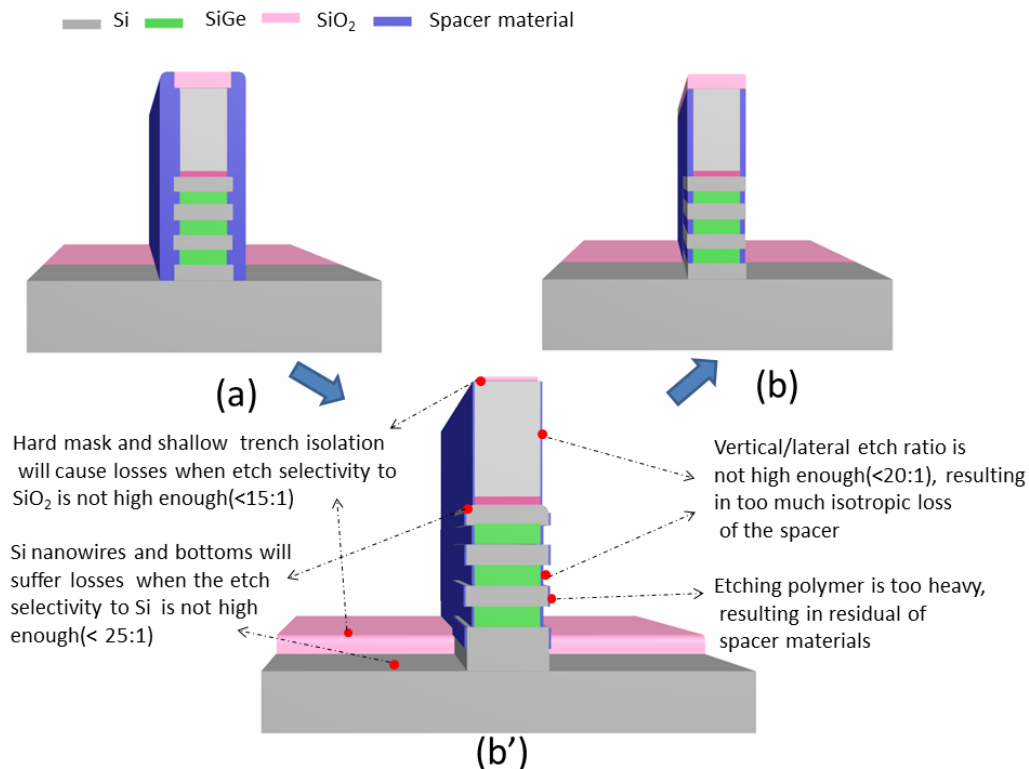


Figure 2. Spacer morphology and inner spacer process challenges: (a) conventional spacer; (b) inner spacer; (b') the process challenges need to be overcome from conventional spacer to inner spacer.

In recent years, quasi-atomic layer etching (QALE) of SiN has emerged [23], mainly using a two-step alternating method. At first, the surface is modified by using hydrogen ion implantation or plasma treatment, and then etching this surface with F-based process gas. Then, these two processes are alternately performed to achieve the purpose of quantitative etching. This method takes into account both the etching selection ratio and the anisotropic, but the quasi-atomic layer etching equipment is complex and the productivity is low, and no related public report shows that it has been used in the GAA nanowire inner spacer module [24–27].

In this work, a novel gas mixture of CH₂F₂/CH₄/O₂/Ar was used for etching the SiN inner spacer in GAA transistors in a conventional inductively coupled plasma (ICP) tool. This method avoids using specially designed hardware equipment and offers higher process efficiency than solutions such as ALE. Moreover, the conformal deposition and selective anisotropic etching process of inner spacer were also systematically studied. Firstly, the influence of the film deposition process on the filling effect of the inner spacer is discussed by comparing the plasma enhanced chemical vapor deposition (PECVD) and low-pressure chemical vapor deposition (LPCVD) methods. Later, the effects of main etching process parameters (CH₄ flow, O₂ flow and pressure) on the etch selectivity, anisotropy and etching morphology are investigated. Finally, high-resolution scanning electron microscope (HRSEM) (Hitachi Inc., Tokyo, Japan), high-resolution transmission electron microscope (HRTEM) (Thermo Fisher scientific Inc., Waltham, MA, USA) and energy dispersive spectrometer (EDS) (Thermo Fisher scientific Inc., Waltham, MA, USA) were used to analyze the microscopic details of the filling and etching of the inner spacer.

2. Materials and Methods

All the materials in this work were performed on 8-inch (100) silicon wafers. The experimental process and method are shown in Figure 3:

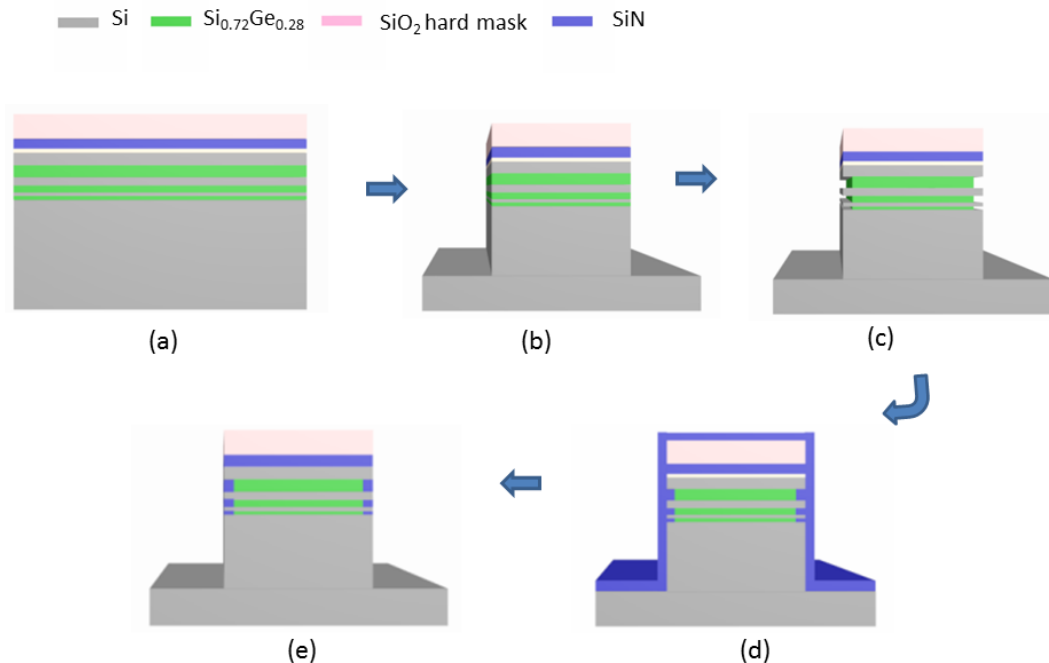


Figure 3. Schematic view of process flow to form the inner spacer: (a) $\text{Si}_{0.72}\text{Ge}_{0.28}$ /Si multilayer structure (MLs) and hard mask growth, (b) lithographic patterning and plasma anisotropic etching, (c) $\text{Si}_{0.72}\text{Ge}_{0.28}$ isotropic selective etching; (d) SiN thin film deposition and filling and (e) SiN inner spacer anisotropic selective etching.

Step 1: Three cycles of SiGe/Si multilayers were grown by using reduced pressure chemical vapor deposition (RPCVD) technique [28,29], and then an oxide-nitride-oxide (ONO) hard mask were grown on the top silicon by applying plasma enhanced chemical vapor deposition (PECVD). In order to examine the film filling and etching performance of inner spacer in detail, $\text{Si}_{0.72}\text{Ge}_{0.28}$ stacks with different thicknesses are designed.

Step 2: 3 μm equally spaced line arrays were patterned, and the whole structure including the hard mask and $\text{Si}_{0.72}\text{Ge}_{0.28}$ /Si stack are vertically etched to the substrate silicon by using the plasma etching. Finally, oxygen plasma is used to remove the photoresist [15].

Step 3: In the ICP etching tool, the $\text{Si}_{0.72}\text{Ge}_{0.28}$ layers were selectively etched by $\text{CF}_4/\text{O}_2/\text{He}$ gas without any bias power, to obtain the lateral depth of 50–70 nm [15].

Step 4: For the cavity formed in the step 3, PECVD (AMAT Producer 200 mm (Applied Materials Inc., Santa Clara, CA, USA)) and low-pressure chemical vapor deposition (LPCVD) (AMAT Centura 200 (Applied Materials Inc., Santa Clara, CA, USA)) equipments were used to grow 40 nm SiN in the filling experiments. The growth temperature of PECVD was at 400 $^{\circ}\text{C}$, while for LPCVD was at 750 $^{\circ}\text{C}$. The growth temperatures at these steps were kept below 800 $^{\circ}\text{C}$, in order to avoid the interdiffusion at the interfaces between Si/SiGe [30].

Step 5: Finally, the prepared samples were etched in an ICP tool (TCP 9400DFM (Lam Research Inc., Fremont, CA, USA)), where a gas mixture of $\text{CH}_2\text{F}_2/\text{O}_2/\text{CH}_4/\text{Ar}$ and a chuck temperature of 80 $^{\circ}\text{C}$ were used. The research focuses on the effects of etching process parameters on selection ratio, anisotropy (vertical/lateral etch ratio) and etch morphology.

3. Results and Discussion

3.1. Effect of Thin Film Process on Gap Filling

Inner spacers require thin films to grow uniformly to the sidewalls in the cavity; therefore, a good gap filling ability is required for the film growth. Atomic layer deposition (ALD) high-K materials (such as HfO_2 , ZrO_2) have very good filling properties, but these materials increase parasitic capacitance and are detrimental to device performance, therefore these materials are not suitable choices. However, the fabrication of the GAA Si-Ge based nanowire devices using FinFET process flow usually requires special nanowire/sheet selective etching and surface processing including interfacial layer removal, diameter reduction and rounding in the advanced replacement metal gate (RMG) module [31,32]. These processes may bring great fabrication challenges for conventional low K material spacer. Therefore, the highly resistant and density SiN (K value is ~ 7) is still the best choice for spacer materials [12]. Meanwhile, for structures with lateral openings, then high-density plasma chemical vapor deposition (HDPCVD), which has good filling performance in the vertical hole structure becomes theoretically ineffective [33] and the damage caused by high-density plasma is inevitable. In this study, the filling effects of two conventional SiN thin film deposition techniques, PECVD and LPCVD were compared. The results are shown in Figure 4: The filling effect of LPCVD silicon nitride is significantly better than that of PECVD. The HRSEM micrographs reveals that, there are obvious holes in the PECVD grown layers, and the ratio of the voids in the original cavity: SiGe layers $10\text{ nm} > 20\text{ nm} > 30\text{ nm}$. Meanwhile, silicon nitride which was grown by LPCVD did not show any holes in SiGe cavity with depths of 10 nm, 20 nm or 30 nm, showing LPCVD as a better conformal growth. More importantly, LPCVD SiN has better corrosion resistance than PECVD to facilitate subsequent process integration. This good property of using LPCVD is due to lower chamber pressure and higher temperature, which results in slower growth rate, better conformal coverage and higher density [34]. More detailed results on LPCVD silicon nitride will be discussed in the subsequent TEM and EDS characterizations in Section 3.5.

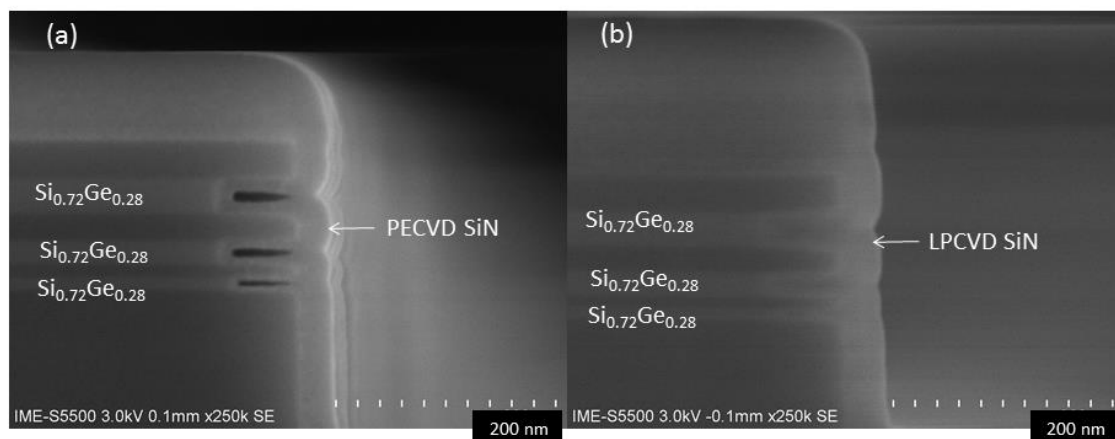


Figure 4. SEM images of the SiN inner spacer filling by using: (a) plasma enhanced chemical vapor deposition (PECVD) and (b) low-pressure chemical vapor deposition (LPCVD).

3.2. Effect of CH_4 Flow on Inner Spacer Etching

More investigations were carried out to find the impact of CH_4 gas flow on the etching profile while all other parameters were kept constant. The CH_4 flow rate was varied by applying the following conditions: 80 mTorr/source RF 250 W/bias RF 35 W/x sccm CH_4 /25 sccm CH_2F_2 /20 sccm O_2 /50 sccm Ar. The results are shown in Figure 5a. When there is no CH_4 gas in the reaction chamber, it is found that the silicon nitride on sidewall is etched completely, while the top hard mask is totally consumed and the Si/SiGe stack is seriously damaged (Figure 5b), due to the etch selectivity as well as anisotropy are poor in absence of CH_4 . Meanwhile, as CH_4 is inserted in the chamber, then the anisotropy during the

etching is significantly improved. This is linked to the C-based polymer produced by CH_4 passivates the sidewalls and increases the vertical/lateral etch ratio. This refers to the fact that CH_4 reaction system has the highest C/F ratio compared to other CH_xF_y mixed gases. The vertical/lateral etch ratio increases with the decrease in the thickness of the SiGe layer, because the aspect ratio dependent etch rate (ARDE) effect leads to a lower lateral etch rate for small-sized trenches under the same conditions [35].

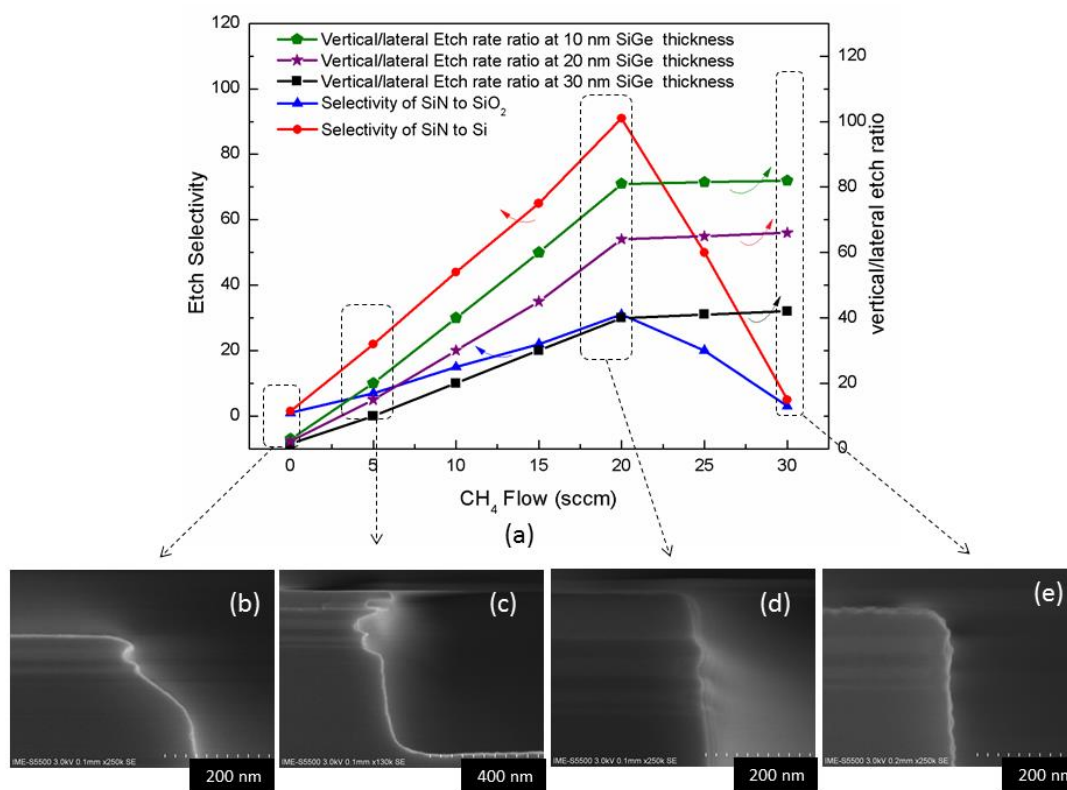


Figure 5. Impact of CH_4 flow on etching: (a) the dependence of etch selectivity and vertical/lateral etch ratio on CH_4 flow; (b) etching profile without CH_4 ; (c) etching profile of 5 sccm CH_4 flow; (d) etching profile of 20 sccm CH_4 flow; (e) etching profile of 30 sccm CH_4 flow;

At the same time, the increasing flow rate of CH_4 improves the etch selectivity of silicon nitride to Si and SiO_2 . The mechanism is explained as the C and H elements in CH_4 combine with the N in silicon nitride to form volatile HCN, which promotes the silicon nitride etching reaction. In addition, the selectivity ratio of silicon nitride to Si is higher than that of SiO_2 because of C in CH_4 which combines F in CH_2F_2 and O in SiO_2 to form volatile COF_2 does not affect the Si in similar way. Then, this trend reaches a peak when the flow of CH_4 was 20 sccm, and the profile is relatively well controlled (Figure 5d). Finally, by continuing to increase CH_4 , the contribution to the anisotropy becomes small and the contribution of sidewall passivation reaches to a saturation level. The increase of CH_4 flow greatly reduces the proportion of the F-based source gas CH_2F_2 , then the silicon nitride etching rate decreases since the Si in silicon nitride needs to be combined with more F atoms to generate volatile SiF_4 . As the etch selectivity decreases, the hard mask material on the top of the structure is significantly consumed and the roughness of the sidewalls becomes worse (Figure 5e).

3.3. Effect of O_2 Flow on Inner Spacer Etching

In these experiments, O_2 flow was changed while the other process parameters were unchanged as following: 80 mTorr/source RF 250 W/bias RF 35 W/20 sccm CH_4 /25 sccm CH_2F_2 /x sccm O_2 /50 sccm Ar. The results are shown in Figure 6a. When there is no oxygen, a polymer deposition occurs on the surface of the structure (Figure 6b). When the O_2 flow is increased to 10 sccm, the deposition is reduced,

but the deposition is still visible on the side walls (Figure 6c). The polymer produced in the reaction is too heavy and the sidewalls are difficult to be completely etched. The mechanism can be explained that in the absence of O, CH₂F₂ and CH₄ can easily form CH_xF_y polymers. Then, introducing O₂ will generate volatile CO which reduces the amount of polymer formation but allowing other elements such as F to be released for etching silicon nitride [35]. When the amount of O₂ reaches to 20 sccm, an equilibrium point is obtained. The etch selectivity and anisotropy are improved and as a result the etch profile becomes better (Figure 6d). As the amount of O₂ continues to increase, the etching appears isotropic (Figure 6e is a typical SiN isotropic etching). The reason for this outcome is that O₂ excessively consumes C in the reaction gas to form CO volatiles, which leads to a serious shortage of the CH_xF_y amount which is necessary for the protection of the side walls.

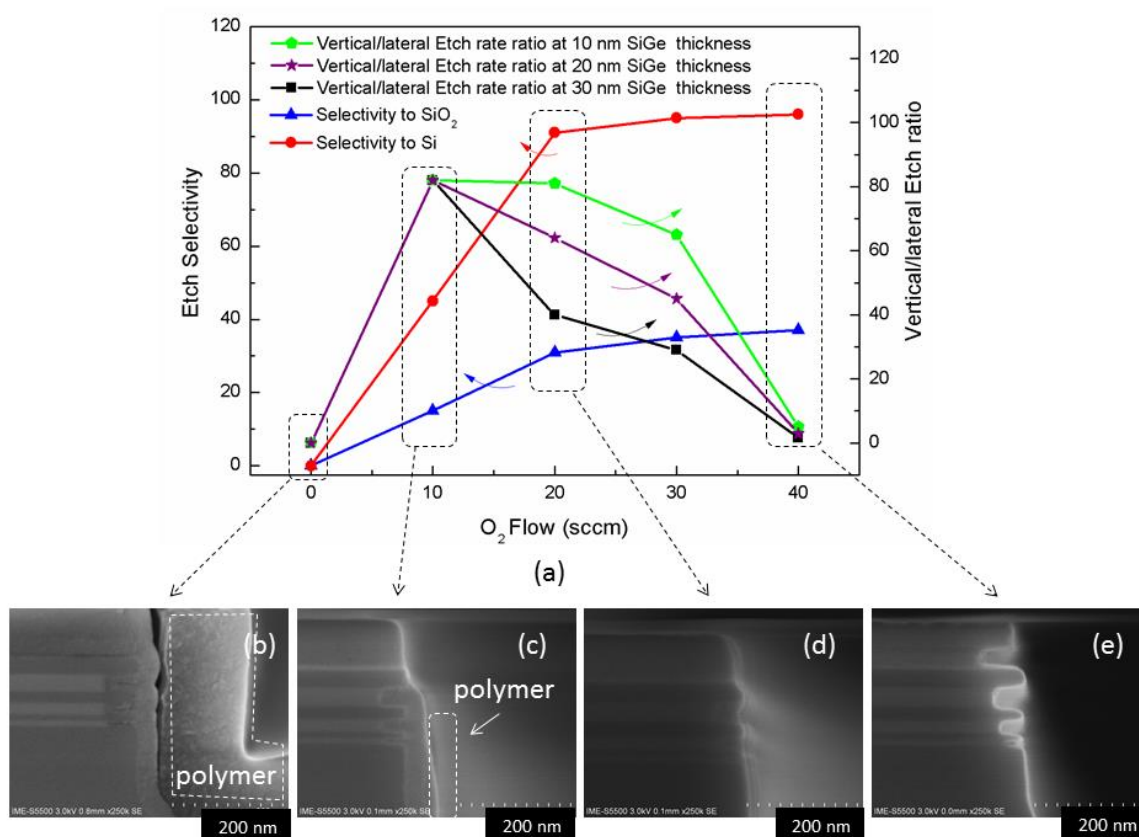


Figure 6. Effect of O₂ flow on etching: (a) the dependence of etch selectivity and vertical/lateral etch ratio on O₂ flow; (b) etching profile without O₂; (c) etching profile of 10 sccm O₂ flow; (d) etching profile of 20 sccm O₂ flow; (e) etching profile of 30 sccm O₂ flow.

3.4. Effect of Pressure on Inner Spacer Etching

It is well known that the process pressure is an important parameter for plasma etching, because it greatly affects the average free path and energy of ions. In this study the influence of pressure on the etch profile has been investigated according to parameters: x mTorr/source RF 250 W/bias RF 35 W/20 sccm CH₄/25 sccm CH₂F₂/20 sccm O₂/50 sccm Ar. It can be seen from Figure 7a that the etching selection ratio has been increasing along with the increasing pressure, especially over 50 mT. This mechanism can be explained by increasing the pressure and reducing the bombardment energy of the ions [35]. The anisotropy is slightly reduced, but the change is relatively small, which also helps to completely etch the silicon nitride on the outside of the sidewall. From Figure 7b–e, it can be seen that the amount of silicon nitride remaining on the sidewall gradually decreases until Figure 7e which shows no obvious residue (more detailed characterization will be performed at 3.5), and the remaining hard mask is getting thicker and thicker, indicating that the selectivity becomes getting higher. It should be

noted that, due to the limitation of the vacuum gauge of the etcher tool (TCP 9400 DFM), the full-scale pressure can only be tested to 80 mT, therefore, whether higher pressure has better results remains to be studied in the future.

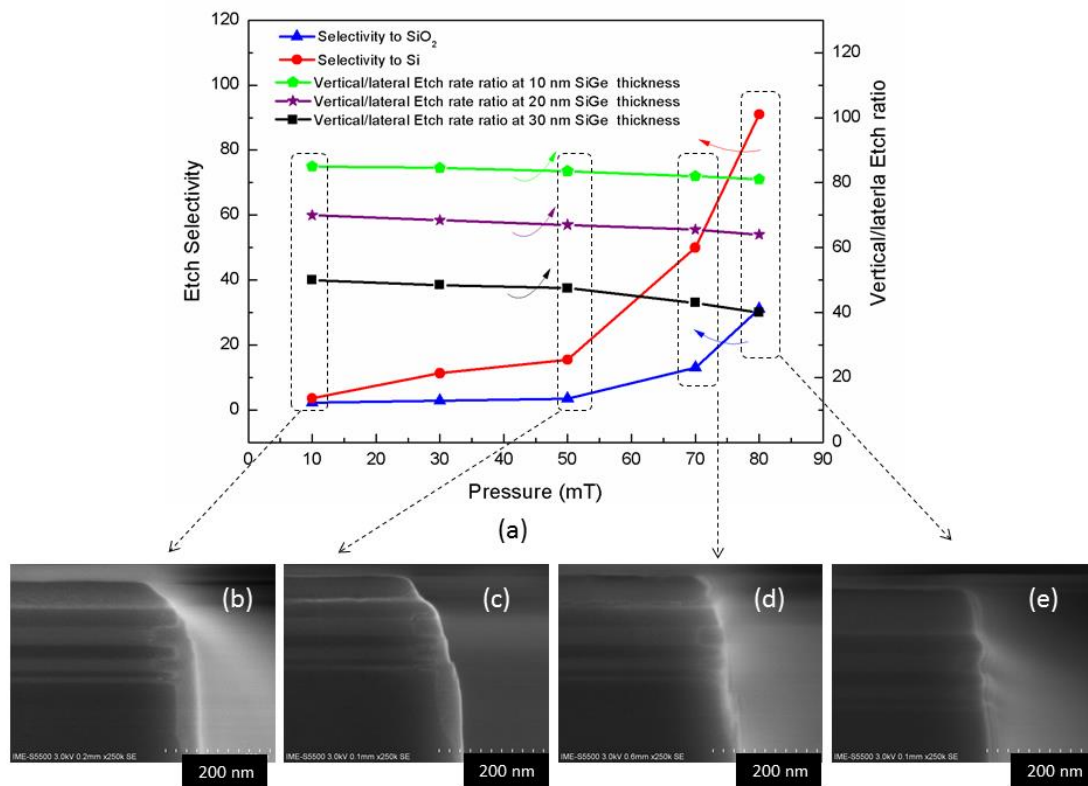


Figure 7. Effect of pressure on etching: (a) the dependence of etch selectivity and vertical/lateral etch ratio on pressure; (b) etching profile of 10 mT; (c) etching profile of 50 mT; (d) etching profile of 70 mT; (e) etching profile of 80 mT.

In order to provide a larger insight of our results, a comparison was made with previously published references as shown in Table 1. The etching selectivity ratio in this study have some advantages over conventional etching results. Comparing with remote plasma and QALE, the selectivity to SiO₂ is lower, but it has obvious advantages in etching anisotropy, which is crucial to control the accuracy of the final thickness of inner spacer.

Table 1. Selectivity of SiN etch to Si and SiO₂, vertical/lateral etch ratio and etch accuracy for SiGe/Si inner spacer structure.

Parameter	Data in This Work ¹	Ref. [21] ²	Ref. [22] ³	Ref. [24] ⁴
Selectivity to Si	101.5	6.2	100	— ⁵
Selectivity to SiO ₂	31.6	18.6	70	100
Vertical/lateral etch ratio	82.5	— ⁵	1	8
Etch accuracy (%)	2	— ⁵	— ⁵	— ⁵

¹ Pressure 80 mTorr/source RF 250 W/bias RF 35 W/20 sccm CH₄/25 sccm CH₂F₂/20 sccm O₂/50 sccm Ar. ² Data of typical conventional plasma methods. ³ Data of special method—typical remote downstream plasma. ⁴ Data of special method—typical quasi-atomic layer etching. ⁵ Related data are unknown

3.5. Material Quality and Interface Analysis

In order to more accurately characterize the results of the relatively optimal processes in this study, TEM and EDS characterizations were performed on the relatively optimal conditions of LPCVD filling and etching inner spacers. The outcome is shown in Figure 8. The figure shows that the silicon nitride film

fills the Si/SiGe stack cavity in the sidewall very well, and only a small gap is found in the high-resolution TEM picture. These small gaps do not affect device integration and performance, but on the contrary, these gaps will improve device performance as it will further reduce parasitic capacitance [36].

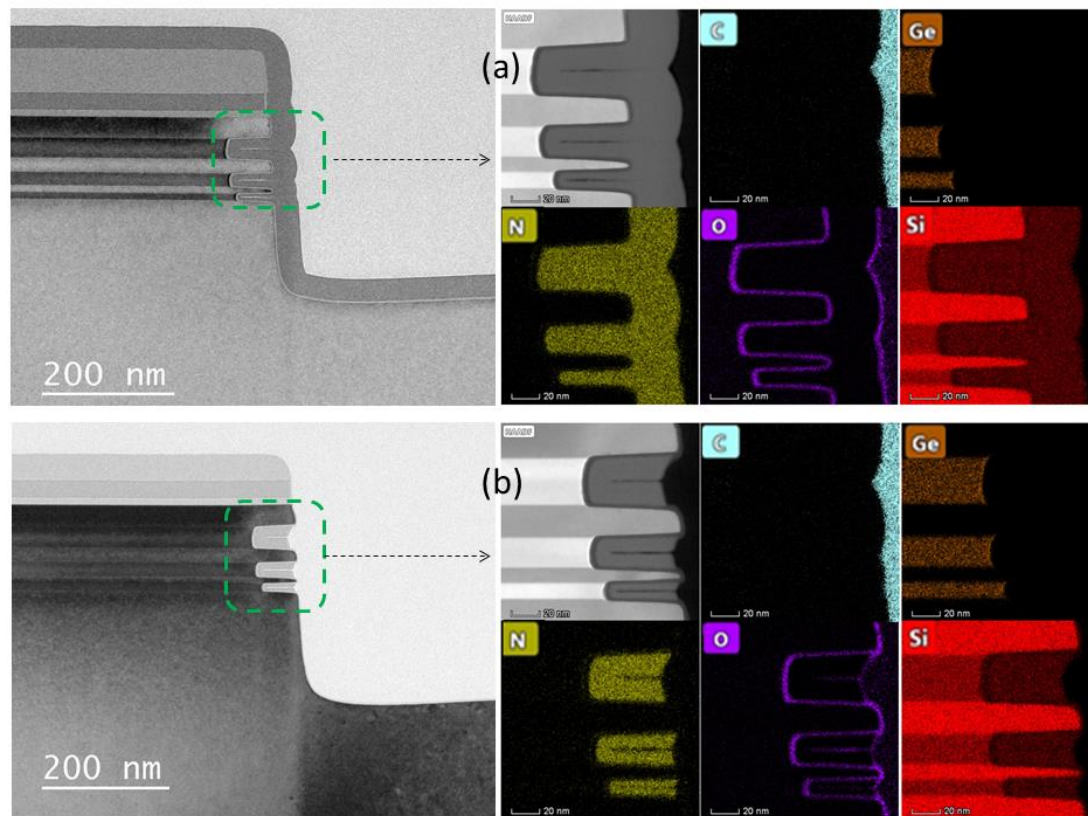


Figure 8. TEM and EDS micrographs: (a) LPCVD Silicon nitride inner spacer deposition; (b) inner spacer after etching under optimal conditions.

The EDS mapping results show the distribution of silicon nitride film. The Si, Ge and O elements are basically consistent with the expected design results, there is no Ge diffusion during the LPCVD process. The C element is mainly from the TEM sample preparation, because it uses a carrier containing C and can only be referenced. It can be seen from Figure 8b that after the inner spacer is etched, except for the silicon nitride in the Si/SiGe stack cavity, the silicon nitride in the other positions have been etched completely. In particular, the end of the Si nanosheet is free of N elements (there is no silicon nitride residues), and only a thin layer of SiO₂ is formed. Subsequently, this silicon oxide can be further removed during the growth of the epitaxial source and drain.

4. Conclusions

Inner spacer for GAA nano-structure, LPCVD silicon nitride has significantly better cavity filling effect than PECVD. The conventional ICP etching tool and the optimized CH₂F₂/O₂/CH₄/Ar gas mixtures can control the silicon nitride inner spacer etching effect very well. The ratio of silicon nitride etch selectivity to Si is more than 100:1, and that for the selectivity to SiO₂ is more than 30:1. The vertical/lateral etch ratio is related to the thickness of SiGe, that is, the thinner the thickness of SiGe is, the higher the ratio is. For the nano-structure with a SiGe thickness of 10 nm, the vertical/lateral etching ratio reaches 80:1. The high-resolution TEM and EDS mapping results show that the SiN on the end face of the nanosheet is totally etched while the SiN in the cavity remains relatively intact. This method proposed in this study has the advantages of simple hardware equipment, high etching selectivity and excellent vertical/ lateral etching ratio.

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