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Towards Reconfigurable Electronics: Silicidation of Top-Down Fabricated Silicon Nanowires

Muhammad Bilal Khan [1,2,3,*], Dipjyoti Deb [1,2,3], Jochen Kerbusch [1,2], Florian Fuchs [1,3,4,5], Markus Löffler [3,6], Sayanti Banerjee [2,3,6], Uwe Mühle [7], Walter M. Weber [2,3,8], Sibylle Gemming [1,2,3,4,9], Jörg Schuster [2,3,4,5,9], Artur Erbe [1,2,3] and Yordan M. Georgiev [1,3,10,*]

1 Institute of Ion Beam Physics and Materials Research, Helmholtz-Zentrum Dresden-Rossendorf (HZDR), 01328 Dresden, Germany
2 International Helmholtz Research School for Nanoelectronic Network, HZDR, 01328 Dresden, Germany
3 Center for Advancing Electronics Dresden, Dresden University of Technology, 01062 Dresden, Germany
4 Institute of Physics, Chemnitz University of Technology, 09126 Chemitz, Germany
5 Fraunhofer Institute for Electronic Nano Systems, 09126 Chemnitz, Germany
6 Dresden Center for Nano-Analysis, Dresden University of Technology, 01062 Dresden, Germany
7 Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Dresden, 01277 Dresden, Germany
8 Namlab gGmbH, Nöthnitzer Strasse 64, 01187 Dresden, Germany
9 Dresden Center for Computational Materials Science, Dresden University of Technology, 01062 Dresden, Germany
10 On leave of absence from the Institute of Electronics at Bulgarian Academy of Sciences, 72, Tsarigradsko Chausse Blvd., 1784 Sofia, Bulgaria
* Correspondence: m.khan@hzdr.de (M.B.K.); y.georgiev@hzdr.de (Y.M.G.)

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Featured Application: This work has implications for the fabrication of nickel silicide–silicon Schottky junction-based devices such as reconfigurable field-effect transistors.

Abstract: We present results of our investigations on nickel silicidation of top-down fabricated silicon nanowires (SiNWs). Control over the silicidation process is important for the application of SiNWs in reconfigurable field-effect transistors. Silicidation is performed using a rapid thermal annealing process on the SiNWs fabricated by electron beam lithography and inductively-coupled plasma etching. The effects of variations in crystallographic orientations of SiNWs and different NW designs on the silicidation process are studied. Scanning electron microscopy and transmission electron microscopy are performed to study Ni diffusion, silicide phases, and silicide–silicon interfaces. Control over the silicide phase is achieved together with atomically sharp silicide–silicon interfaces. We find that {111} interfaces are predominantly formed, which are energetically most favorable according to density functional theory calculations. However, control over the silicide length remains a challenge.

Keywords: Schottky junction; field-effect transistors; nickel silicide; annealing

1. Introduction

In the last few decades, the conventional downscaling of complementary metal-oxide-semiconductor (CMOS) transistors dominantly relied on the reduction of size to improve the performance as well as to reduce the costs and the power consumption of devices. With the end of physical scaling of field-effect transistors (FETs), further device performance enhancement is expected to be based on new concepts. These concepts include new materials (e.g., high mobility channel materials [1–3] such as 2D materials), metal gates with high-k gate dielectrics [4], new device

architectures (e.g., 3D integration) [5], new computation principles (e.g., spintronics) [6], and new functionality (e.g., reconfigurability) [7]. Reconfigurability, in particular, can be achieved by selectively injecting a chosen type of charge carrier in the channel and controlling the concentration of these charge carriers at Schottky junctions [8]. This concept is typically implemented by fabricating Schottky junction-based FETs, also known as reconfigurable FETs (RFETs) [9]. In RFETs, undoped silicon nanowires (SiNWs) are nickel (Ni) silicided from both ends using annealing, and the Ni diffusion process creates a silicide–silicon–silicide structure with two Schottky junctions. The observed silicide phases vary in terms of the sheet resistance, Schottky barrier height, built-in strain etc. [10,11]. Hence, the phase of the silicide influences the performance of devices as the injection and the extraction of charge carriers in the silicide–silicon junction depend on the properties of the phase [12,13]. Since the performance of RFETs strongly depends on the quality of the Schottky junctions, proper control over the silicidation process (silicide phase, sharpness of the silicide–Si interfaces, silicide length along the nanowire) in these devices is very important but remains a challenge [14].

This work aims at understanding the Ni-silicide diffusion mechanism and attaining specifically the $NiSi_2$ phase in top-down fabricated SiNWs by studying the silicide–Si interfaces. The formation of $NiSi_2$–Si contacts is attractive because $NiSi_2$ exhibits similar electron and hole barriers [10]. It also has a low lattice mismatch of 0.4% with respect to Si at room temperature, which allows the formation of single-crystalline structures [10,15]. $NiSi_2$ forms an abrupt heterojunction to Si, thus enabling its use in unipolar devices such as RFETs [16]. To understand the sequence of phase formation within the desired temperature range, various studies have been reported for bottom-up grown nanowires [17–31]. However, fewer studies are available for top-down fabricated nanowires [32,33]. In addition to the formation of the suitable silicide phase, control over the sharpness of silicide–Si interfaces, and the silicide length is important for applications such as RFETs and Schottky barrier FETs [34].

Silicides are mostly formed by a temperature-induced interfacial reaction of a transition metal with Si. This process is called the reactive phase formation, which indicates diffusion between two adjacent phases leading to the formation of a single or multiple products along the chemical gradient between those phases [35,36]. Silicidation is governed by diffusion [37,38] and nucleation [35,39] and can be controlled by steps involved in the reaction phase formation.

Ni-silicide formation on bulk Si substrates has been extensively studied in the past [39–43]. Moreover, Ni-silicided nanowires can be produced by direct synthesis or by solid-state reaction of Ni with SiNWs. Wu et al. [44] reported single-crystalline NiSi nanowires produced by radial silicidation of vapor–liquid–solid grown SiNWs, which were coated with thermally-evaporated Ni and annealed at 550 °C in forming a gas atmosphere to produce single-crystalline NiSi NWs. The first report of the longitudinal growth of metal silicides in nanowires and the formation of flat and abrupt interfaces to silicon was given by Weber et al. [16] by the example of $NiSi_2$–Si nanowire hetero-structures. Schmitt et al. [45] published a detailed review of several processes to produce transition metal silicide nanowires. The desired silicide phase formation is facilitated by proper control of annealing parameters [46] in an axial hetero-structure. These hetero-structures have been used for FET applications and exploration of innovative device concepts [8,16,45,47,48].

The silicide diffusion and phase formation in SiNWs has been described in various publications. Appenzeller et al. [29] demonstrated that the longitudinal growth of silicide in SiNWs is a function of the radius or the cross-sectional area of the nanowire and the produced silicide phase. The nature of the Si–silicide interface also influences the growth and the phase of silicide. The most common Ni-silicide phases in SiNWs are Ni_2Si, NiSi, and $NiSi_2$. The phase of silicide can be controlled by a proper choice of Ni quantity and quality [27,39], conditions of the reaction [30], strain in the nanowire [28,49], and crystal orientation of nanowires [26]. In <112> nanowires, the hexagonal θ-Ni_2Si is formed at 300 °C, whereas this phase is not observed till 800 °C in bulk structures [47]. In <111> nanowires, first the epitaxial $NiSi_2$ is formed and it withstands temperatures upto 700 °C. The low-resistive NiSi is formed at 700 °C [26]. The thermal history of the SiNW influences the silicidation rate. Yamashita et al. [50] presented a comparative illustration of silicidation rate for SiNWs fabricated by two different processes:

The "doping first" process, where the annealing for dopant activation is carried out before the NW patterning; and the "patterning first" process, where NWs are patterned first and then subjected to further heat treatment for oxidation and dopant activation. They concluded that the silicidation rate in "patterning first" approach nanowires is higher than that for the "doping first" approach, as the oxidation induced strain in the "patterning first" approach is altered and distributed by dopant activation annealing in the later process step.

Here we present the results of our investigations on the Ni silicidation of top-down fabricated SiNWs. In the next section, details of the SiNW fabrication and the analysis techniques are given. The initial investigations were carried out on Si thin film structures to identify the process window for SiNW silicidation. In the third section, the results obtained from scanning electron microscopy (SEM) and transmission electron microscopy (TEM) are presented and compared to simulations. Results of electrical characterization of back-gated RFETs are also presented.

2. Materials and Methods

The devices were fabricated on (100) surface-oriented silicon-on-insulator (SOI) substrates. One set of substrates had a 20 nm top Si layer and a 102 nm buried SiO_2 (BOX) layer, while the second set of substrates had a 50 nm top Si layer with a 110 nm BOX layer. SiNWs were fabricated using electron beam lithography (EBL) and inductively-coupled plasma (ICP) etching. EBL was performed with a Raith e-Line Plus system at an acceleration voltage of 10 kV, 1200 μC/cm^2 dose, 30 μm aperture size, and with 2 nm area beam step size using the negative tone EBL resist, hydrogen silsesquioxane (HSQ) from Dow Corning (X-1541). HSQ is known to have sub 5 nm resolution and high etch resistance [51]. The original 6% HSQ solution was diluted to 2% concentration in methyl isobutyl ketone (MIBK) and spin coated at 2000 rpm for 30 s to yield a 40 nm thick HSQ layer. Then the samples were baked at 90 °C for 2 min and exposed using the EBL tool. After EBL, the samples were developed with a high-contrast tetramethylammonium hydroxide (TMAH) based development process [52] and dried with a N_2 gun. The HSQ patterns were transferred into the top SOI layer using a SENTECH's ICP-Reactive Ion Etcher SI 500. The parameters of the etching process were: ten standard cubic centimeters per minute (sccm) SF_6, 20 sccm C_4F_8, 5 sccm O_2, 0.9 Pa chamber pressure, 400 W ICP power, and 12 W RF power. After the SiNW fabrication, a second EBL-based patterning was performed for Ni contact formation using a positive tone resist, ZEP520A (ZEON Corporation, Tokyo, Japan). The exposure parameters were: A total of 10 kV acceleration voltage, 10 μm aperture size and area dose of 40 μC/cm^2. The development was performed in n-amyl acetate solution (ZED-N50, ZEON Corp.). This was followed by baking at 200 °C for 5 min to smoothen the side walls of the patterned structures. Prior to Ni sputtering, the Si native oxide was etched away from NWs using 1% buffered hydrofluoric acid (BHF) solution and then the samples were transferred into the sputtering chamber. The sputtering was performed at 10 keV with a Gatan 681 High-Resolution Ion Beam Sputter Coater. The sample holder was rotated at a speed of 40 rpm for uniform deposition of Ni at a rate of 1.3 ± 0.2 Å/s. The thickness of Ni was varied between 35 and 50 nm according to the requirements of the experiments. After the sputtering step, lift-off was carried out in N-methyl-2-pyrrolidone (NMP) at 50 °C for 10 min. The samples were then rapid thermally annealed (RTA) at 450 °C in forming gas atmosphere (a mixture of 10% H_2 and 90% N_2) for silicidation of the NWs. The annealing time was varied in order to control the axial diffusion length of Ni into the SiNW. The role of the Ni pads was two-fold: Firstly, they acted as a Ni reservoirs for silicidation of NWs, and secondly, they served the purpose of a contact electrode.

To investigate silicidation of nanowires covered with an oxide shell, the samples were thermally oxidized. The oxidation process started with removal of the native oxide from the samples by dipping them in 1% BHF for 15 s. This was followed by an immediate transfer of samples in a pre-heated (875 °C) rapid thermal oxidation chamber. The samples were kept in the chamber for 10 min in the presence of an oxygen flow of 10 standard liters per minute (slm). Subsequently, the samples were annealed at 875 °C in a nitrogen environment for 5 min. This was followed by annealing in forming gas atmosphere. The oxidation process generates heavy stress in the nanowire due to the volume

expansion. This impacts the oxygen diffusion in Si and the surface reaction rate at the Si–SiO_2 interface drops. Therefore, the oxidation process is self-limited [53,54] (i.e., the stress generated by the oxidation process prevents further oxidation of the nanowires). After the oxidation of nanowires, a second EBL step for Ni contacts formation and subsequent annealing for silicidation was performed according to the aforementioned conditions.

To analyze the silicidation process, SEM and TEM investigations were performed. The systems used for SEM and TEM were Raith e-Line Plus and Zeiss Libra 200 TEM, respectively. TEM samples were prepared using focused ion beam (FIB) in a FEI Helios Nanolab 660 machine applying low-damage recipes to preserve the native crystal structure [55].

3. Results and Discussion

3.1. Silicidation in Si Thin Film Structures

To study silicidation in thin films structures, Si pads were patterned in Si substrates in <110> and <100> orientations using EBL and dry etching processes. Ni sputtering and subsequent annealing for silicidation was carried out according to conditions mentioned in Section 2. The purpose of this first study was to determine an initial process window for the nanowire silicidation. Figure 1 shows top-view SEM images of a sample after silicidation. Annealing was performed at 450 °C in forming gas atmosphere for 10 min. It is evident from the bright regions of the Si pads in Figure 1 that the Ni diffusion was not fast enough to reach the nanowires and it was confined within the Si pads. Moreover, the silicide–Si interface has different shapes in Si pads with <110> and <100> orientations. The silicide makes a 90° angle with Si in <110> orientation, whereas in the <100> orientation, the silicide has a step-like interface with Si.

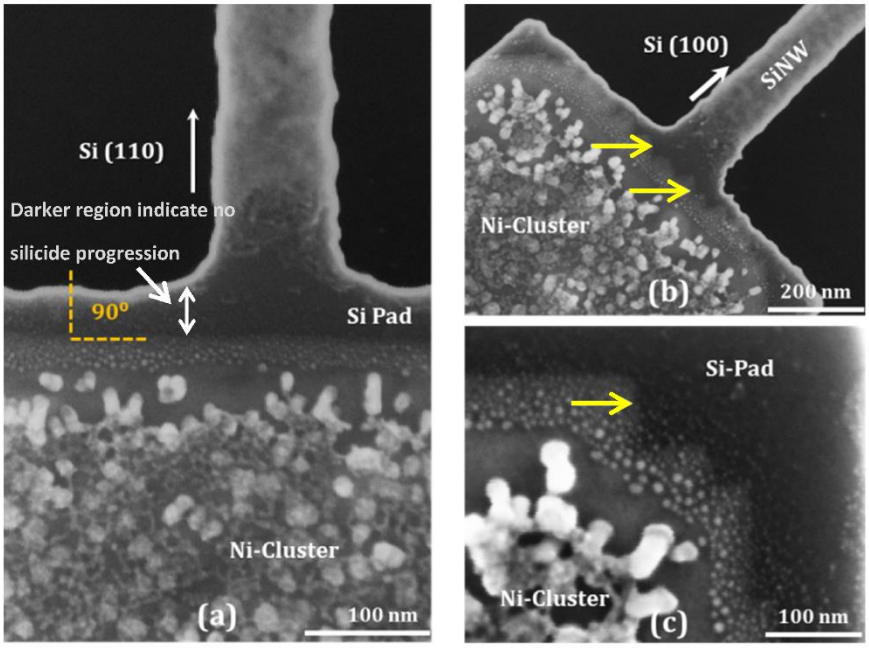

Figure 1. Top-view scanning electron microscopy (SEM) images of silicon nanowires (SiNWs) with Si pads in (**a**) <110> and (**b**,**c**) <100> orientations. The silicided regions of the Si pads are brighter. Silicide–Si interface appears to be flat in <110> pads while in the case of <100> it has a step-like shape, as indicated by yellow arrows.

TEM analysis was performed on lamellas, prepared by FIB, from the selected samples. The cross-section was inspected by high-resolution transmission electron microscopy (HREM) and electron energy loss spectrum (EELS). Figure 2 shows the overview of the cross-section with the different layers included in it. The top most sample layer is covered by a carbon protection layer, which is part of the

FIB milling process to mitigate the damage incurred by FIB. Below the carbon layer, there are two Ni silicide layers and the Si substrate. The top Ni-containing layer depicts a Ni-rich silicide phase (region I). The following layer has a Si-rich silicide phase (region II). The interface between region I and II is smooth, whereas the interface between regions II and the Si substrate (region III) is rough and jagged. It is evident from Figure 2b–d that the silicide in region II has followed preferential crystal directions. The HRTEM image in Figure 3e shows an abrupt change in the silicide phase from NiS_2 to Ni-rich phase.

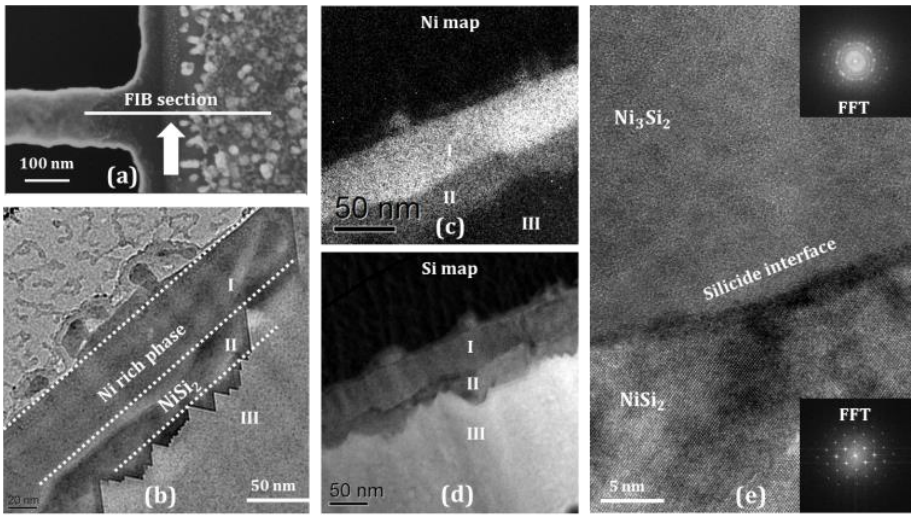

Figure 2. Cross-sectional transmission electron microscopy (TEM) analyses of a lamella taken from the sample shown in Figure 1. (**a**) SEM top-view image of a SiNW with a Si pad. Focused ion beam (FIB) section was made along the white line to get the cross-sectional image of silicidation in the Si pad. (**b**) TEM image of the cross-section showing three different regions. Region I: Ni-rich Ni-silicide phase; Region II: Si-rich Ni-silicide phase; and Region III: pure Si from the Si pads. (**c**) Energy-filtered TEM (EFTEM) image of Ni to confirm its concentration in the three different regions. Higher brightness corresponds to higher concentration of Ni. (**d**) EFTEM image of Si of the same regions. Higher brightness corresponds to higher concentration of Si. (**e**) High resolution transmission electron microscopy (HRTEM) image of the interface between Region I and Region II, showing an abrupt change in the silicide phase.

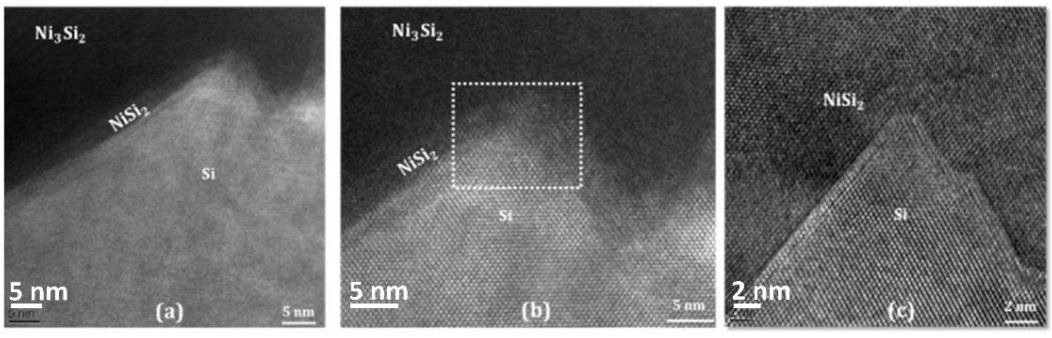

Figure 3. TEM analysis of silicide junctions. (**a**) Overview of inter-phases between Ni-rich phase and Si-rich phase. (**b**,**c**) Magnified images show atomically sharp $NiSi_2$–Si junction.

To further investigate the silicidation process, zero-loss TEM was performed [56]. The images are presented in Figure 3. The Ni map shows higher concentration of Ni in region I compared to region II. Fast Fourier transform (FFT) confirms that the silicide phase in region II has a cubic lattice structure in accordance to $NiSi_2$. The silicide in region I is Ni-rich and it has a non-cubic structure. The $NiSi_2$–Si interface is atomically sharp (Figure 3c).

3.2. Silicidation in Nanowires

After determining an initial silicidation process window from the experiments for silicidation in thin film structures presented in the previous section, experiments for nanowire silicidation were performed. For these experiments, nanowires were fabricated in <100> and <110> crystallographic orientations using the top-down approach. Ni was sputtered according to the conditions described in the Materials and Methods section and, subsequently, rapid thermal annealing was performed at 450 °C in forming gas atmosphere for 80 s. The resulting structures are shown in Figure 4.

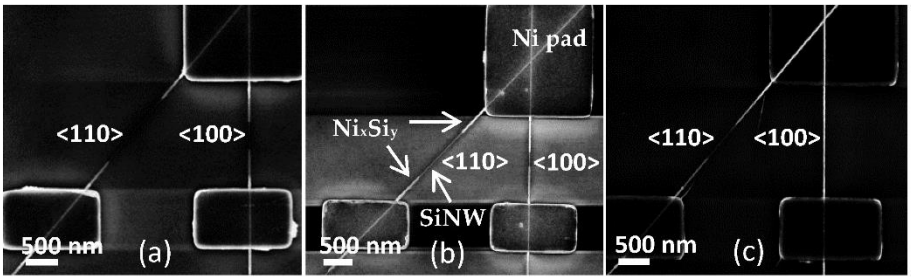

Figure 4. SiNWs in <110> and <100> crystallographic orientations: the brighter segments of NWs indicate silicide formation. Silicidation is faster in <100> NWs. Annealing is performed at 450 °C for 80 s.

As illustrated in Figure 4, the silicide diffusion length is larger in <100> NWs compared to <110> NWs. Appenzeller et al. [29] have shown that silicidation diffusion length is inversely proportional to square of the diameter of the NW. The widths of <100> and <110> NWs in Figure 4a are 28 and 24 nm, respectively, while the silicide diffusion lengths are 745 and 628 nm, respectively. This shows a strong dependence of silicide length on the nanowire orientation. To investigate in detail the dependence of Ni diffusion and silicide formation on crystallographic orientations of NWs, a circular array of NWs with five-degree separation was fabricated. It was followed by the aforementioned steps for silicidation. The results are shown in Figure 5.

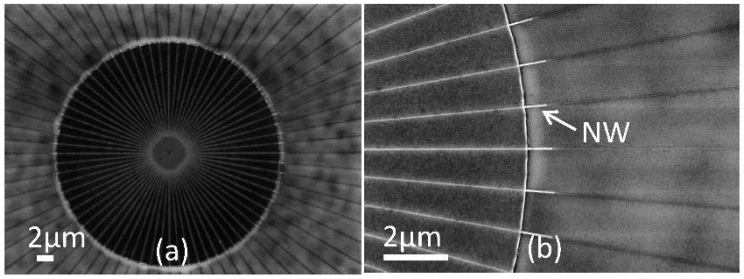

Figure 5. SEM images showing (**a**) nanowires fabricated in circular array with a five-degree separation to study the dependence of silicide diffusion length on the nanowire orientation; and (**b**) a higher magnification image showing clearly different diffusion lengths in different NWs. Annealing is performed at 450 °C for 80 s.

Although the silicide diffusion length varies in different crystallographic orientations of the NWs, it was not possible to extract a clear relation since the results vary in different arrays. To further investigate the orientation dependence of the silicide formation, silicidation of nanowire arrays fabricated in <100> and <110> crystallographic orientations was carried out and the results are presented in Figure 6a–d. The width of the NWs is 20 nm. The average silicide diffusion length in <100>- and <110>-oriented SiNWs is 812 and 744 nm, respectively (see Figure 6e). The images distinctly show that the diffusion of Ni and the silicide progression into the NWs of the same array is not homogeneous and on average has scattering of up to 300 nm in <100> and 400 nm in <110> NWs. Silicidation rates are known to vary

based on different factors, including the quality of interface between the Ni reservoir and the NW [21]. However, our investigation shows this variation also within an array of NWs, which is processed under the same conditions. We attribute this variation in silicide length to different surfaces of NWs, as these NWs are top-down fabricated and their surfaces can be different due to the subtractive nature of the etching process. Because of this uncontrolled silicide formation and scattered positioning of the Schottky junctions, large top gates have to be placed to ensure that they properly cover the junctions at the two sides of the NWs [14,34]. This limits the possibilities for downscaling the size of devices and compromises their large-scale fabricability.

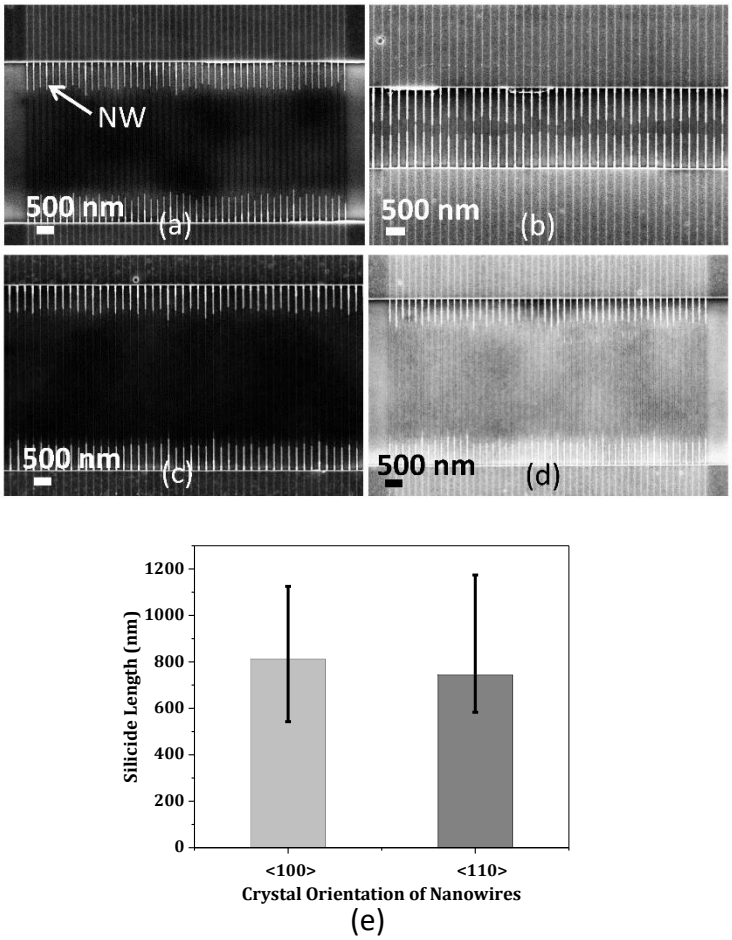

Figure 6. SEM images showing silicidation flow in arrays of NWs fabricated in (**a**,**b**) <100> and (**c**,**d**) <110> crystallographic orientations. Large scattering of silicidation length is evident in NWs within each array. (**e**) Graph showing average silicide diffusion length (rectangular bars) and its scattering (linear "error bars") in <100> and <110> SiNWs: silicide diffusion length is higher for <100> NWs, while large scattering is observed in both types of NWs. Annealing is performed at 450 °C for 80 s.

To have better control over the silicidation length, further investigations were carried out with sets consisting of two and three NWs. The results are shown in Figure 7. It was expected that the outer two NWs might consume excess Ni, giving a better control over the silicide progression in the central NW. However, it was still not possible to obtain a proper control over the silicide progression with this technique. The silicide diffusion length varied in different groups of NWs. Interestingly, the outer nanowires appear to exhibit a distinct silicide phase compared to the inner ones, as indicated by their higher brightness. While the inner NWs appear to have a $NiSi_2$ phase with a comparable lattice constant to that of Si, the outer ones have Ni-rich phases with a larger lattice constant. This might be

an effect of Ni source "competition" between neighboring nanowires. Apparently, the outer nanowires receive their Ni supply from a longer extent, thereby limiting that supply to the inner nanowires.

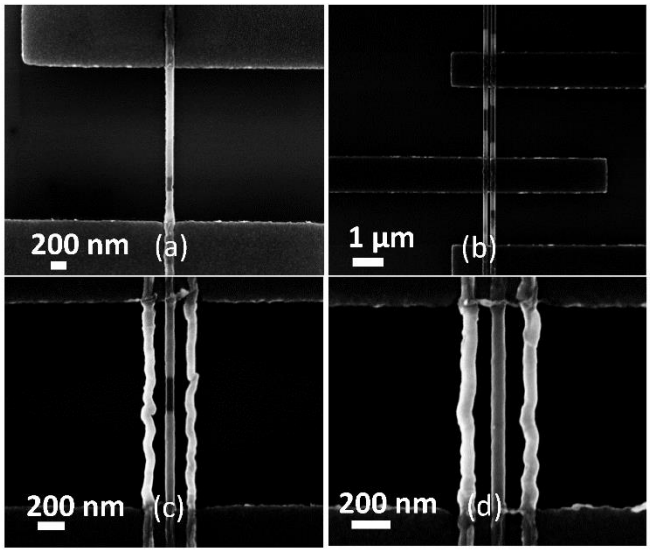

Figure 7. SEM images of (**a**) single, (**b**) double, and (**c**,**d**) triple nanowires, showing uncontrolled silicidation. The outer nanowires in images (**c**,**d**) have Ni-rich silicide phase while the inner ones appear to have $NiSi_2$. Annealing is performed at 450 °C for 10 min.

Dellas et al. [27] and Lin et al. [28] claimed that an oxide shell around the NWs hinders diffusion of silicide into the NWs. Therefore, expecting a better control, further investigations were made with oxidized NWs. However, it also resulted in non-uniform diffusion of silicide into the NW, as shown in Figure 8.

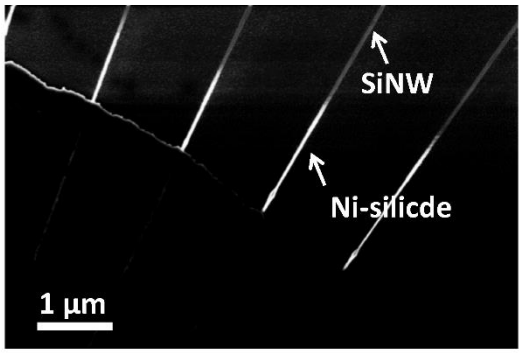

Figure 8. SEM micrograph of silicidation of oxidized nanowires. Annealing is performed at 450 °C for 80 s.

3.3. Properties of Silicide–Si Interface

To investigate the phase of the silicide and the quality of the silicide–Si interface, an exemplary NW was sectioned parallel to its length. Subsequently, HRTEM was performed. The resulting images are shown in Figure 9. Starting with Ni-rich phases near the Ni-reservoir, the Si fraction increases towards the silicide–Si interface.

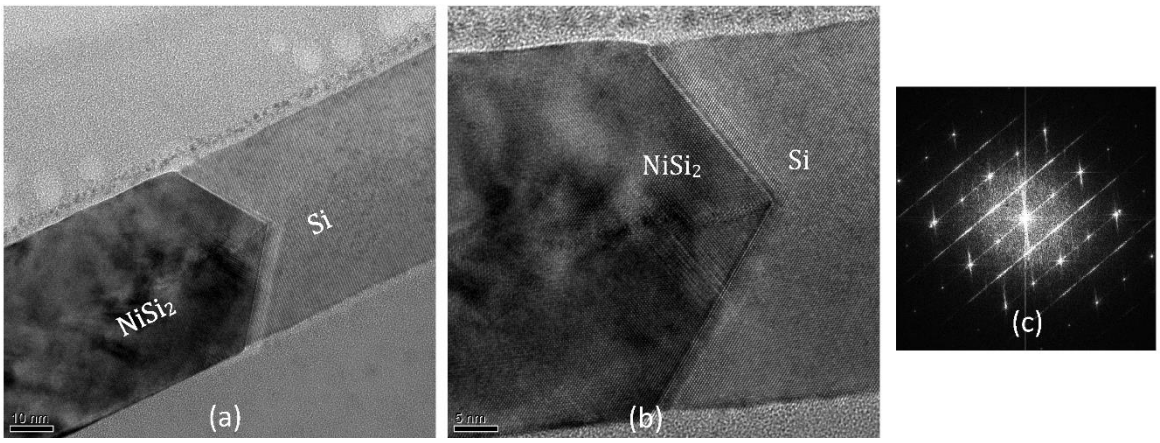

Figure 9. HRTEM images of silicide–Si Schottky junction: (**a**) NW sectioned along the NW length, (**b**) high magnification image of the interface showing an atomically-sharp Schottky junction, and (**c**) Fast fourier transform (FFT) studies confirm formation of $NiSi_2$ phase near the silicide–Si interface. Annealing is performed at 450 °C for 80 s.

HRTEM images show the formation of an atomically sharp Schottky junction, which is required for size downscaling and enhanced performance of the devices. FFT studies confirmed the formation of the desired $NiSi_2$ near the silicide–Si interface. The interface orientation is {111} in accordance with [16].

In order to better understand our experimental observations, we calculated interface energies using density functional theory (DFT) as implemented in Atomistix ToolKit 15.1 [57]. The Perdew–Burke–Ernzerhof exchange-correlation function from [58] was used and the reciprocal space was sampled with a spacing of around 0.25 nm^{-1}.

A periodic structure consisting of alternating silicon and $NiSi_2$ was studied. The length of the resulting supercell perpendicular to the interface was at least 12 nm. Periodic boundary conditions were employed in the parallel directions. The atomic arrangements of the studied interfaces are described in [59]. In order to mimic our experimental setup of a nanowire lying on a substrate, the lattice constants in the silicon and $NiSi_2$ regions were both fixed to the silicon lattice constant of the undisturbed silicon crystal. The atomic coordinates of all atoms within a 10 nm neighborhood around the interface were relaxed.

We defined the interface energy density as:

$$\epsilon_{\text{interface}} = \left(E_{\text{supercell}} - N_{\text{NiSi}_2} E_{\text{NiSi}_2} - N_{\text{Si}} E_{\text{Si}}\right)/2A. \quad (1)$$

$E_{\text{supercell}}$ is the total energy of the calculated supercell, $E_{\text{NiSi}_2/\text{Si}}$ are the total energies of bulk unit cells, and $N_{\text{NiSi}_2/\text{Si}}$ follows from the number of unit cells in the supercell. A is the cross-section of the system and the factor 2 arises because two interfaces are included in a single supercell.

The calculation resulted in interface energy densities of around 2.2 eV/nm^2 for the {111} interface (an A-type interface was assumed, see [59] for details) and around 4.2 eV/nm^2 for the {110} interface. This effect is partially compensated by the higher area of a {111} interface in a <110> nanowire, because an angle of 35° between the normal vector of the interface and nanowire orientation occurs. For geometrical considerations, the interface area is increased by a factor of around 1.2 compared to a {110} interface. Hence, the total energy contribution of the interface is smaller for a tilted {111} interface, which makes such an interface energetically more favorable. The experimental observations of the {111} interface are; therefore, explained by the calculated interface energy densities.

3.4. Electrical Characterization of Fabricated Devices

To test the outcome of the silicidation process, electrical characterization of devices based on single unoxidized NWs patterned in both <100> and <110> orientations was carried out by back-gating. The back-gate voltage (V_{bg}) was swept between −40 to 40 V in a butterfly loop (0 to 40 V, 40 to −40 V, and −40 to 0 V). The drain to source voltage (V_{ds}) was varied from 0.25 to 1 V. The devices exhibit large hysteresis as the nanowires are not passivated. We extracted a single sweep from the transfer characteristics, as illustrated in Figure 10. The minimum of the curves was shifted to left by 17 V to center the curves around 0 V. An ambipolar behavior of devices was found. The currents in <110>-oriented devices are higher compared to the currents in <100> devices. At V_{ds} = 1 V, the values of *n*- and *p*- currents in <110> devices are 40.7 and 450.0 nA, while in <100> the values are 16.8 and 207.0 nA, respectively. The shift of original curves away from 0 V is attributed to a built-in potential on the NW surface in ambient conditions in the absence of passivation with, for example, an oxidation layer [34]. Unipolar behavior in these devices can be attained by using multiple gate electrodes [9], while *p*/*n* current symmetry, which is required for energy efficient functioning of circuits based on RFETs, can be tuned by oxidation induced stress [9,14].

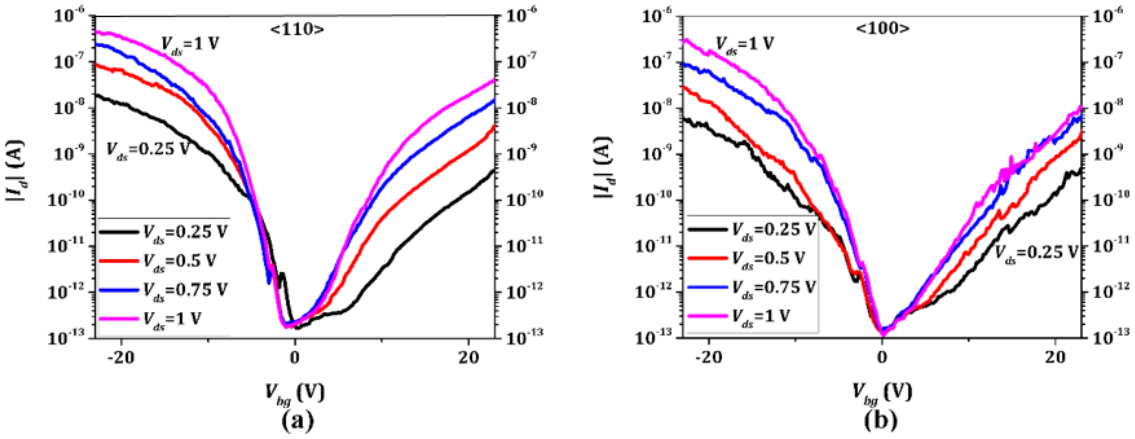

Figure 10. Electrical characterization with back-gate sweeping of single NWs-based devices with (**a**) <110> and (**b**) <100> orientations. The devices show ambipolar behavior. To facilitate a *p*- and *n*-current comparison, curves were shifted left by 17 V to center. Currents in <110>-oriented devices are higher than those in <100>. Channel width and length for both types of nanowires are 20 nm and 3 μm, respectively.

4. Conclusions

In this work, we studied Ni silicidation of silicon thin films and top-down fabricated SiNWs by using the RTA technique. We paid special attention to the formation of the required silicide phase ($NiSi_2$), the quality of the Schottky junctions, and the reproducibility of the silicide length along the nanowires, which are very important for device performance and scalability. To investigate the influence of the NW orientations on the silicidation process, SiNWs with different crystallographic orientations were silicided. Although large scattering in the silicidation lengths of nanowires was observed even for the nanowires of the same orientation, the silicidation in <100> nanowires is found to be faster than that in <110> nanowires. Furthermore, TEM and FFT analyses revealed the formation of sharp Schottky junctions with {111} interfaces and the $NiSi_2$ phase of silicide required for the fabrication of RFETs. Density functional theory calculations showed that {111} interfaces are energetically favorable. Control over the diffusion length of silicide into the NW was not achieved. This makes placing of top gates on the Schottky junctions and downscaling of devices a challenge. Alternative annealing techniques with shorter annealing times, like, for example, flash lamp annealing, may be employed to have better control over the silicidation process. Transfer characteristics of the back-gated devices with single unoxidized NWs patterned in <100> and <110> orientations illustrate

ambipolar behavior, with currents in <110>-oriented devices being higher compared to the currents in <100> devices.

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