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An Enhancing Fault Current Limitation Hybrid Droop/V-f Control for Grid-Tied Four-Wire Inverters in AC Microgrids

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Abstract: Microgrid integration and fault protection in complex network scenarios is a coming challenge to be faced with new strategies and solutions. In this context of increasing complexity, this paper describes two specific overload control strategies for four-wire inverters integrated in low voltage four-wire alternating current (AC) microgrids. The control of grid-tied microgrid inverters has been widely studied in the past and mainly focused on the use of droop control, which hugely constrains the time response during grid-disconnected operation. Taking into account the previous knowledge and experience about this subject, the main contribution of these two proposals regards providing fault current limitation in both operation modes, over-load capability skills in grid-connected operation and sinusoidal short-circuit proof in grid-disconnected operation. In the complex operation scenarios mentioned above, a hybrid combination of AC droop control based on dynamic phasors with varying virtual resistance, and voltage/frequency master voltage control for grid-(dis)connected operation modes are adopted as the mechanism to enhance time response. The two proposals described in the present document are validated by means of simulations using Matlab/Simulink and real experimental results obtained from CENER (The National Renewable Energy Centre) experimental ATENEA four-wire AC microgrid, obtaining time responses in the order of two-three grid cycles for all cases.

Keywords: microgrids; control strategies; three-phase four-wire systems; fault current limitation

1. Introduction

In the coming years, it is expected that classical electrical grids will drive forward to a smarter, more flexible, reliable, efficient and bidirectional format leading to a more complex framework. All of these benefits should be supported by an appropriate infrastructure. In this context, microgrids [1,2], and mainly alternating current (AC) microgrids, play a key role in a new electrical paradigm pushed by the increasing penetration of Distributed Energy Resources (DER). This paradigm will deal with the variability and unpredictability associated with DERs and local demand fluctuations. This versatility generates a way to delay the renovation of an aged infrastructure that cannot withstand

an existing rising demand [3]. A new outline, constituted by several interconnected AC/DC (direct current) microgrids or nano-grids [4], conventional energy sources, and loads will create future viable smartgrids [5].

Microgrids can provide potential economic and environmental benefits, but their implementation implies great technical difficulties in control, energy/power management and protection. Some authors focus on the low level loops for the inverters' operation; AC droop [6–9], voltage and current control loops [10–12]. Other ones concentrate on the high management level based on cooperative distributed strategies [13,14] or optimal-smart operation [15–18]. Considering the previously mentioned antecedents in the literature, the authors of this paper consider it very relevant to pay attention to fault protection [19,20] and secure operation in seamless transference between operation modes [12,21–23].

On one hand, in traditional AC four-wire distribution systems, protective device coordination during faults is achieved by selecting appropriate circuit-breaker current–time characteristics under clear regulations. This choice does not imply intercomponent communication [21,24] and assumes high short-circuit power levels [24]. However, the situation is the opposite in the case of microgrids based on power electronics, the over-load capability being, hereinafter Fault Current Limitation (FCL), constrained. In a microgrid context, it should be adaptive and fast in terms of voltage and current limitations [25], and should be able to behave sinusoidally to not affect the response of conventional protective breakers.

On the other hand, inverters in a microgrid can play two main roles: one as a controlled voltage source and the other as a controlled current source [26], and can adopt two control hierarchies, master–slave or peer-to-peer [27]. In addition, in the peer-to-peer hierarchy, the conventional AC droop voltage control strategy, based on the steady-state or quasi-static power transference model between AC sources [6,28], is a widely applied alternative to face both operation modes (grid-(dis)connected) and parallellize various inverters, but generates poor dynamics, mainly in grid-disconnected operation. This last situation get worse with the typical use of low-pass filters to emulate synchronous generator mechanical inertias [28]. The combination of droop-based control with the use of virtual impedances is a widespread mechanism to support the soft-start challenge under a peer-to-peer hierarchy [29,30]. Furthermore, conventional AC droop control presents low adaptability when the operation point differs significantly from the planned rated point. In this situation, the recent use of dynamic phasors can be used to improve the adaptability of conventional AC droop control strategies [31].

The motivation of this paper regards considering strategies that provide FCL capabilities in both operation modes. It can be found in [24,32,33] examples based on separating the fault from the grid rapidly but without an AC fault management strategy. However, previous examples as well as others, focus on faults at the DC-link of the inverter [34], observing the effect on the AC side. On the other side, others references concentrate directly on DC microgrids [35–37]. The last two scenarios mentioned above are far away from this paper target. Another studied solution is to face FCL under the assumption that the inverter is droop-based in both operation modes. In [38,39], examples for three-phase three-wire microgrids are exposed. Different types of short circuits are studied in [38], but the fault current limitations offer dynamics of about 200 ms to achieve steady-state, while in [39] only a tretrapolar short-circuit is evaluated obtaining time responses of about 100 ms. In [40], some results are just simulated for AC droop-based four-wire systems. Finally, other alternatives exist applied to series filters or obtaining FCL by changing the output inductances as detailed in [41,42].

The main contribution of the present paper is the demonstration by simulation and real results of the advantages and flexibility of a fast time response hybrid combination of voltage control techniques that ensures proper FCL capabilities introducing two strategies for this purpose: one for each operation mode. This allows for applying specific control strategies and solutions in a context of increasing complexity scenarios avoiding the use of generic solutions that are not always the most appropriate ones.

Firstly, the AC droop control based on dynamic phasors is adopted for the grid-connected mode, but a master voltage-frequency (V/f) control strategy is embraced for the grid-disconnected mode, offering better dynamic responses during the grid-disconnected operation thanks to disabling the AC droop loop. The use of a variable virtual resistance supports not only soft-starts but also the transference between the operation modes. Varying virtual resistance enhances the voltage restoration during the transference.

Secondly, two control strategies will assist the FCL capability of the inverter connected to an AC microgrid. An over-load supervisor is proposed to characterize and limit the over-load magnitude, providing thermal recovery when extra current has to be dispatched during grid-connected mode. In addition, a short-circuit proof strategy supports the operation of the inverter under different short-circuit situations and fault clearances for grid-disconnected operation, obtaining time responses below 60 ms. To achieve the same response from the protective devices' viewpoint, the short-circuit proof algorithm allows for maintaining current and voltage sinusoidal and totally controlled, as required in a microgrid operation framework.

All strategies are thought to be compatible with a four-wire microgrid because, as detailed in [43–45], this is the proper solution for addressing independently three-phase current control and facing imbalances. These strategies become an efficient way to face common situations in low voltage microgrids interfaced with distribution networks.

Thus, the paper is organized as follows. Section 2 defines the system. Section 3 describes the proposed strategies for the FCL and the adaptive virtual resistance mechanism adopted for a seamless smooth transference. Section 4 presents the simulated results using Matlab/Simulink (R2017b, The MathWorks, Inc., Natick, MA, USA, 1984) and exposes the experimental ones validated in the experimental ATENEA four-wire microgrid at The National Renewable Energy Centre (CENER). Finally, Section 5 provides the conclusions.

2. System Definition

The following sub-sections define the experimental ATENEA microgrid and the converter considered in this paper.

2.1. The Experimental ATENEA Microgrid

The Renewable Energy Grid Integration Department in CENER (National Renewable Energy Centre of Spain) has developed and deployed a microgrid (ATENEA) placed in the Rocaforte industrial area (town of Sangüesa, Navarra, Spain) according to the interest in an industrial test scenario and environment. The generation equipment of the facility can be seen in Figure 1.

It consists of an AC architecture with total installed power of about 120 kW that can supply part of the Wind Turbine Test Laboratory (LEA), electric loads and Rocaforte industrial lighting area. It also can be used as a test-bench for different generation and storage technologies and control strategies. The generation equipment available in the facility can be seen in Figure 1.

The ATENEA microgrid structure is based on an AC low voltage three-phase, four-wire bus (400 V, 50 Hz) connected to all of the equipment. This experimental microgrid has two configurations: grid-connected and grid-disconnected. Its main objective is to manage generation and demand in order to obtain high ratios of energy self-efficiency. In grid-connected mode, the microgrid is connected to the network and the V/f performance is fixed by its own network. In the grid-disconnected scenario, one of the converters linked with an energy storage system (flow battery, Valve-Regulated Lead-Acid (VRLA) battery, Li-ion battery) or a diesel generator is configured to form the grid, mastering the V/f. In this way, the ATENEA microgrid adopts a master–slave control in the grid-isolated configuration and the slaves work under a PQ control, P and Q being active and reactive power, respectively.

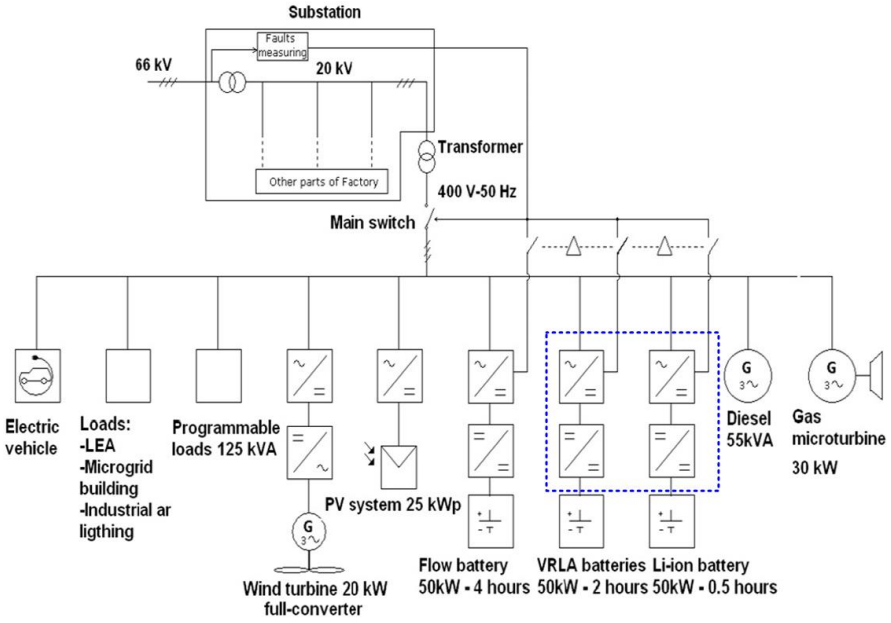


Figure 1. Diagram of the ATENEA microgrid at The National Renewable Energy Centre (CENER). A blue dashed box indicates the two possible direct current–alternating current (DC–AC) converters that can implement the proposed strategies.

2.2. The Converter

According to Section 2.1, a two-stage converter is considered to interface with the VRLA or the Li-ion 50 kW batteries of Figure 1 (blue dashed box) with the four-wire microgrid. It has been decided to use a common two-level three-leg power stack to maintain homogeneity for both power stages (see Figure 2).

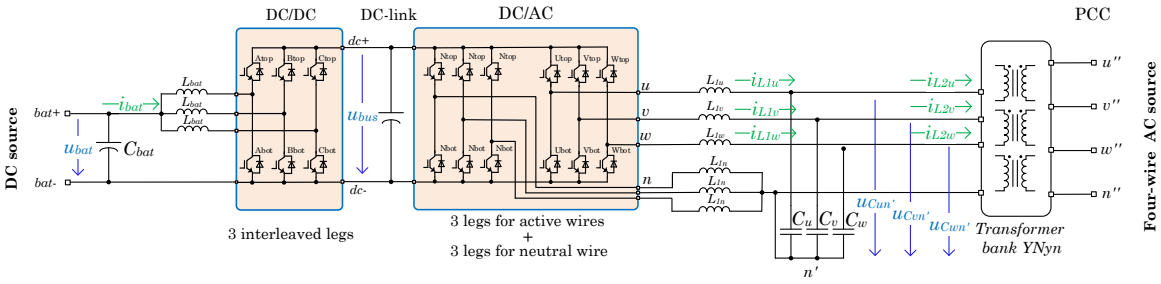


Figure 2. Scheme of the full direct current–direct current (DC–DC) and DC–AC proposed converter.

In consonance with the available storage technologies, a DC voltage u_{bat} range from 150 to 500 VDC is considered. With this configuration, a DC–DC converter interfaces with this wide DC voltage range by means of a three-phase interleaved topology. By the use of an interleaved topology, the output inductive filter size is split and reduced, so it makes for easier operation and maintenance tasks. At the same time, high power converters could be designed with lower current modules, reducing the voltage and current ripple in the DC-link and decreasing the power capacity of the inductors [46]. Thus, as cited in [47], the reliability of an interleaved DC–DC converters increases compared with conventional one leg devices.

In order to manage AC unbalanced loads, an inverter topology able to control any current sequence is required. The inverter stage is constituted by two three-leg bridges: one dedicated for the active phases and the other one for the neutral wire. This configuration allows for controlling each line current independently using optimized modulation techniques such as Space Vector Pulse Width Modulation (SVPWM) [48]. An LCL-type coupling filter completes the inverter where an isolation

free-flux YNyn transformer bank is assumed as part of the LCL-type filter providing galvanic isolation and offering different possible neutral schemes [49].

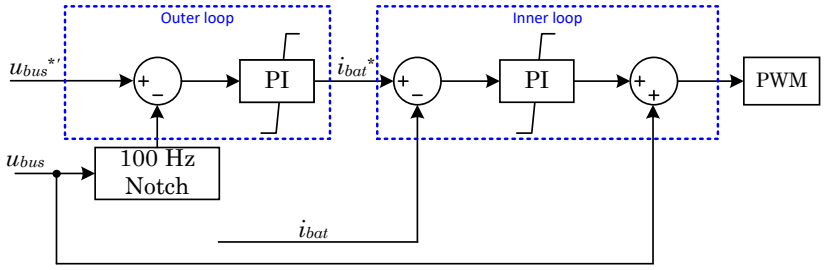
3. Control Strategies

The following sub-sections define the main control strategies of the proposed converter in Section 2 that will be applied in the experimental ATENEA microgrid.

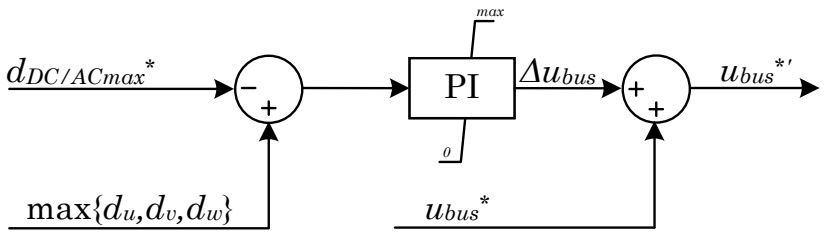
3.1. DC–DC Interleaved Converter Control

DC–DC power stage is not the aim of this paper, but, in the context of this paper, it has been considered relevant to briefly mention its high level control details. In the operation context described in this document, the DC–AC inverter operation requires a proper DC-link voltage level to hold an adequate behaviour under unbalances or nonlinear needs. In addition, it has been considered that the DC energy storage system presents a large voltage range. Due to this voltage wide voltage range, an uncontrolled constant DC-link voltage level can affect inverter's operation. The purpose of the DC–DC converter is to step-up the voltage of the storage system and provide an autonomous way to regulate the DC-link voltage level against different AC requirements.

The DC–DC converter is controlled by means of two nested control loops, as shown in Figure 3a. The inner control loop manages the battery inductor, L_{bat}, and limits the maximum desired battery current, i_{bat}. As detailed in Section 2.2, an interleaved topology is chosen, so a $2\pi/3$ rad/s shifted phase PWM strategy is used with the same duty cycle for all the converter's legs. The outer control loop controls the DC-link voltage, u_{bus}. Because of the unbalanced nature of AC connected loads, low frequency voltage ripples (at $\simeq$100 Hz) in the DC-link can be severe. This voltage control loop needs a high bandwidth to overcome this ripple and keep constant u_{bus}. Thus, an adaptive 100 Hz notch filter [50] is used in the feedback control chain for this purpose to quickly compensate for any variation around the fundamental rated grid frequency (50 Hz).



(**a**) DC–DC interleaved converter nested control loops



(**b**) Adaptive DC-link voltage reference generator (higher level preventive controller)

Figure 3. Interleaved DC–DC converter control schemes. Proportional Integral (PI).

To avoid over-modulation situations in the DC–AC stage, a preventive controller is suggested at the higher level of the DC–DC control scheme in order to provide an increment of u_{bus}, Δu_{bus}, to the rated DC-link voltage. Thus, the reference $u_{bus}{}^{*\prime} = u_{bus}^{*} + \Delta u_{bus}$ is generated where u_{bus}^{*} is the desired standard DC-link voltage, as can be deduced from Figure 3b. The maximum available duty cycle of the inverter, $d_{DC--AC_{max}}{}^{*}$, is compared with the maximum of the duties of the inverter's active

phases (d_u, d_v and d_w). If there is not enough DC bus for the inverter, the DC reference is stepped up to its maximum threshold, taking into account the limitations of the DC-link. In another case, Δu_{bus} is equal to zero in the steady-state as a consequence of the lower saturation limit of the PI controller, as shown in Figure 3b. Thanks to this method, the DC-link voltage is increased as required only under imminent over-modulation situation.

3.2. DC–AC Four-Leg Converter Control

The DC–AC power stage is responsible for operating the AC side in the two operation modes defined in Section 2.1: grid-connected and grid-disconnected. In this paper, and following the operation philosophy of ATENEA's operation, a strategy based on maintaining the voltage source behaviour in both modes has been adopted. However, and as a difference from the solutions proposed in the literature review of Section 1, the grid-connected operation adopts an AC droop control, but, in grid-disconnected operation, the voltage behaviour is maintained disabling the external droop loop. In this last case, the voltage/frequency control is assumed by the inverter being the voltage master of the microgrid. In this scenario, the obtained dynamics are less limited in time-response due to the absence of droop constraints.

As defined in Section 2, the inverter is based on a three-phase four-leg topology to be fully compatible with ATENEA four-wire microgrid. This allows the inverter to be controlled by means of three independent single phase systems in order to provide direct, indirect and homopolar sequence control capability. Each phase has its own master AC droop control (only for grid-connected mode) and two inner cascaded stationary frame controllers [51] for the voltage ($u_{C_{xn'}}$) and current ($i_{L_{1x}}$) loops, x phase being u, v or w. The inner loops are tuned considering [49,52] and the tuning values are presented in Section 4.

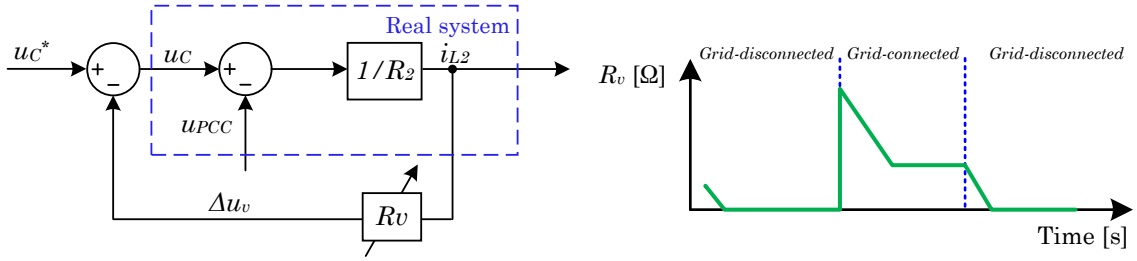
3.2.1. Control Assumptions

Classical AC droop control operation principles are obtained from the steady-state equations that describe the power flow between two AC voltage sources connected by an inductive line, as widely detailed in [6,28]. A predominant resistive behaviour is adopted by using the virtual impedance concept [29,30] to provide a reliable relationship between the sets active-reactive power and voltage-frequency, being as independent as possible from the grid impedance. The virtual resistance concept is described in Figure 4. In Figure 4a, u_C designs the controlled AC voltage, u_{PCC} is the voltage of Point of Common Coupling (PCC), R_2 the physical equivalent series resistance of L_2, and R_v is the value of the virtual resistance (see Figure 2).

The adaptive virtual resistance concept is currently used for hot-swapping (soft-start) [6] and to smooth the effect of grid fluctuations. In this case, it is also applied to enhance the transference between operation modes, as is later shown in Section 4.2. It should be noted that the virtual resistance should be disabled progressively to not affect the operation of a pure V/f strategy in the grid-disconnected mode. Figure 4b illustrates the proposed behaviour of the R_v module during and between the operation modes. Furthermore, as it has been aforementioned, this fact makes it possible to improve the time response performance in grid-disconnected mode thanks to the master voltage role change between the mains and the converter.

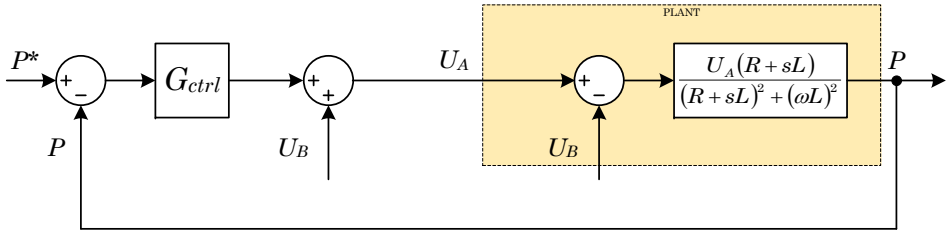
It is possible to deduce the dynamic AC control droop schemes depicted in Figure 5 under a resistive behaviour assumption and considering dynamic phasors [31]. This control schemes are the basis control schemes adopted for the grid-connected operation in the paper. In Figure 5, G_{ctrl} represents the transfer function of the AC droop control law between the node A that is the AC controlled capacitor and a node B corresponding to the PCC. For the G_{ctrl}, it is assumed that a τ_f time constant for emulating mechanical inertias of synchronous generators [28]. P^*/Q^*-P/Q are the active/reactive powers set-points and measured values, and U_A and U_B represent the voltage at the mentioned nodes A and B. The ω_{UB} is the angular frequency at the PCC, θ_{UA} and θ_{U2} are again the phases at nodes A and B, respectively. Finally, R and L are the total resistive and inductive part

between A and B. Note that R is the addition of the real equivalent series resistance of the wiring, the output transformer involved and the forced virtual part R_v.

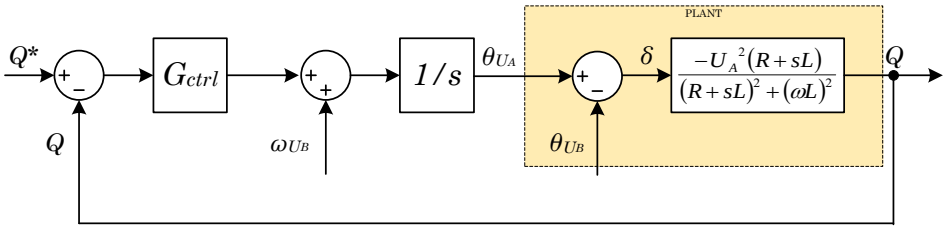


(**a**) R_v control scheme (**b**) R_v evolution according to operation mode

Figure 4. The virtual resistance R_v operation.



(**a**) Active power close loop system



(**b**) Reactive power close loop system

Figure 5. Resistive case power close loop scheme under dynamic phasors.

3.2.2. Power Over-Load Supervisor for the Grid-Connected Mode

As it is well known, the inertial and over-load capability of power electronics is limited. Moreover, it is common to consider pulsed drain currents of two to three times the continuous drain current for about 1 ms. On the contrary, in traditional AC systems, the rotary machines and transformers can be over-loaded up to 20–30 times in a timescale of minutes [24]. In this case, it has been considered to over-size the converter allowing a certain over-load capability. This fact provides a more flexible interaction between the inverter and the AC microgrid. The oversizing is achieved using high current switching devices. This choice allows for a more compact converter placing the burden of oversizing only on the cost of switching devices, a not really sensitive part today. Thus, the cooling system is designed to suit the nominal power. However, the thermal time lag of the used cooling method is usually enough and within the range of seconds to minutes. Furthermore, the use of thermal masses such as aluminium plates, or the consideration of phase change materials are options to increase the thermal inertia [53,54], being a good trade-off between cost and volume, if required.

In order to manage the over-load capability, the maximum AC current is handled by a power over-load supervisor algorithm based on thermal criteria. This current limitation is achieved by means of the apparent power s (in per unit). An over-load observer, ol_o, limits the power per phase. The over-load observer fulfills this task through the formula

$$ol_o = \int_0^t \left(i^{*2} - 1 \right) dt \tag{1}$$

based on the i^2t computation. In this sense, the term ol_o is an indicator of the over-load energy exchanged, i^* is the desired current and t is the time interval of the over-current. The over-load algorithm is managed according to the state diagram shown in Figure 6. Time t begins when $|s^*| > 1$, s^* being the maximum apparent power per phase reference. When $|s^*| > 1$, the observer enters to the *Wake-up* step, starting to compute ol_o (Equation (1)) and ol_t (accumulative time under the over-load situation). If the ol_o value reaches zero, the observer returns to a *Sleep* step, where ol_o and ol_t are reset. If the ol_o is bigger than zero, depending on the present s value, the accumulated time ol_t is incremented or maintained. Keeping the ol_t time constant, it is ensured that the inverter is not over-loaded intermittently producing possible thermal degradations. In the case that the ol_t term becomes higher than a pre-set threshold $T_{max\,ol}$, the system evolves to the *Prolonged over-load error* step and s is limited to 0.8. In this way, ol_o is forced to decrease until zero. Then, the system evolves to the *Sleep* step again.

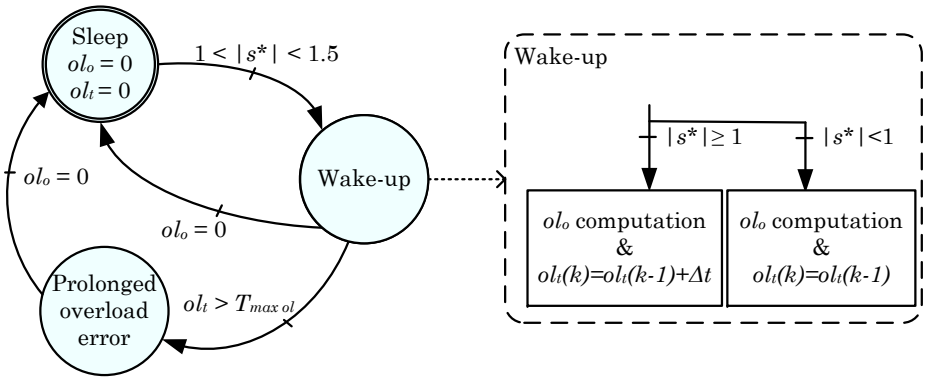


Figure 6. Scheme of the power over-load supervisor algorithm.

3.3. Short-Circuit Proof Algorithm for Grid-Disconnected Mode

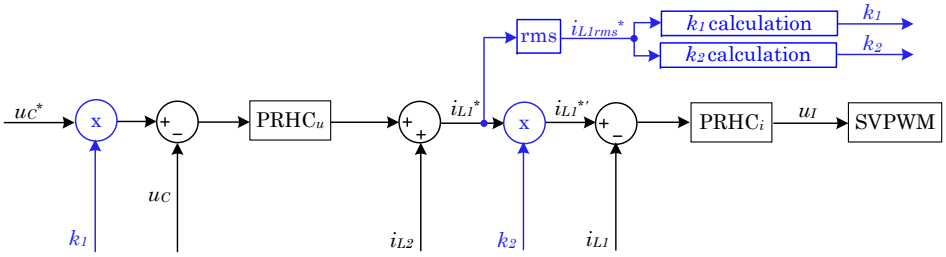
As detailed in Section 2, the inverter operates as the voltage master when the ATENEA microgrid is grid-disconnected operated. The inverter must provide sinusoidal currents even under an over-load or short-circuit occurrence reducing the voltage accordingly. In this way, the aim of the microgrid inverter and this paper is to generate a totally controlled short-circuit power regulating sinusoidal currents. Right after, this information can be used to (re)configure certain protection devices' distributed thresholds along the AC microgrid [25]. In this sense, the time response of the breaker that feeds the fault should be affected minimally.

Figure 7 shows the proposed block diagram of the short-circuit proof mechanism. The conventional voltage and current stationary frame controllers can be seen in black, i.e., Proportional Resonant with Harmonic Compensator (PRHC) controllers, where the subscript u and i refer to voltage and current, respectively. u_C^* is the objective AC capacitor voltage, U_C the current AC capacitor voltage, and u_I the inverters' output voltage. i_{L1} and i_{L2} are the inverters' output inductance and grid coupling inductance. The superscript * designs the reference, and the subscript *rms* is the root mean square (rms) computed value.

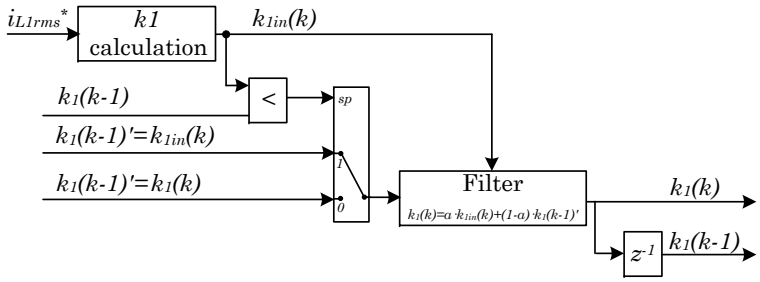
The blue parts are added with respect to a conventional voltage-current nested loop for the short-circuit proof enhancement. The algorithm is based on the per phase rms value of the current reference on the AC side, i_{L1}^*, and two factors k_1 and k_2. The first factor k_1 allows for dynamically regulating the voltage set-point to attenuate it under short-circuit or high over-load situations, as follows:

$$k_1 = \begin{cases} 1, & \text{if} \quad i_{\text{rms}} \leq I, \\ (K+1) - \frac{i_{\text{rms}} K}{I}, & \text{if} \quad I < i_{\text{rms}} < (K+1)\, I, \\ 0, & \text{if} \quad i_{\text{rms}} \geq (K+1)\, I, \end{cases} \tag{2}$$

where I is the maximum desired rated output current (at the L_1 inductance). The parameter K in k_1 calculation allows for adapting the system response speed to face the over-load or short-circuit occurrence.



(**a**) Algorithm implementation



(**b**) k_1 filter calculation for fault clearance in discrete time

Figure 7. Control schemes of the sinusoidal wave short-circuit proof algorithm.

The second factor k_2 limits the current to the rated value when the fault situation appears as

$$k_2 = \begin{cases} 1, & \text{if} \quad i_{\text{rms}} < I, \\ \frac{I}{i^*_{L1rms}}, & \text{if} \quad i_{\text{rms}} \geq I. \end{cases} \tag{3}$$

If only the previous algorithm is applied, the behaviour under the fault clearance is undesired. This is due to the fast response of the k_1 factor. To avoid this kind of undesired dynamics, when the current $k_{1in}(k)$ value is higher than the previous computed one $k_1(k-1)$, i.e., this criterion is used as a fault recovery indicator, the applied $k_1(k)$ gain for the inner current control reference is filtered according to Figure 7b.

4. Results

This section describes a 90 kVA converter with a 50% over-load capability. A set of simulations developed in Matlab/Simulink and experimental results obtained at ATENEA microgrid are showed for the validation of the aforementioned control contributions. Hereinafter, the ITI curve [55] defined by the Information Technology Industry Council is considered as a pattern of acceptable time-duration/magnitude voltage transients.

4.1. The Converter Set-Up

The converter presented in Section 2 is based on three Semikron IGD-2-424 power stacks (Semikron, Nuremberg, Germany). The control is implemented into two TMS320F2809 DSP-based control boards, one dedicated to control the general operation state machine and the DC–DC interleaved converter and the other committed to controlling the inverter. Control strategies are executed at 8 kHz. The hardware and software relevant parameters for the DC–AC and the DC–DC converters are summarised in Tables 1 and 2. Figure 8 shows a picture of the full converter. Furthermore,

all short-circuit faults and recoveries are generated using a switch-line breaker (ABB OT200) and considering wires with less than 0.1 mΩ.

Table 1. Interleaved DC–DC (direct current–direct current) converter parameters. PI (Proportional Integral).

	Parameter	Value	Units
Adaptive DC-link PI controller	k_p	0.043	
	k_i	1.43	
Adaptive 100 Hz filter [50]	Adaptive coefficient μ	0.05	
	Attenuate B coefficient of cut-off frequency	4	
PI Voltage controller	k_p	3.5	
	k_i	70	
PI Current controller	k_p	0.16	
	k_i	33.75	
DC–DC converter	Switching & control frequency	8	kHz
	L_{bat} (each interleaved inductance)	400	µH
	C_{bat}	420	µF
	$C_{\mathrm{DC-link}}$	7.2	mF

Table 2. Four-wire DC–AC (direct current–alternating current) converter parameters. PRHC (Proportional Resonant with Harmonic Compensator).

	Parameter	Value	Units
Droop controller	m for active power loop	0.000003	s
	n for reactive power loop	0.000004	
	k_i for reactive power loop	0.0009	
	t_f Low-pass filter (LPF) constant	0.1	
PRHC Voltage controller	k_p	0.27	
	k_{i_0}	0.26	
	k_{i_3}	0.001	
	k_{i_5}	0.001	
PRHC Current controller	k_p	0.7468	
	k_{i_0}	3.93	
	k_{i_3}	0.1	
	k_{i_5}	0.04	
Fault current limiters	K	0.9	
	I	130	A
	α (over-load filter parameter)	0.01	
Virtual impedances	R_v (initial-state grid-connected)	1.0	Ω
	R_v (steady-state grid-connected)	0.2	Ω
	R_v (steady-state grid-disconnected)	0	Ω
	R_v change ratio	−0.16	Ω/s
DC–AC converter	Switching & control frequency	8	kHz
	L_1 (active phases & neutral wire)	250	µH
	C (star connected)	350	µF
	L_2 (leakage transformer inductance)	70	µH

4.2. Simulated Results

This section focuses on demonstrating by the use of simulations the virtual resistance contribution to a fast and seamless transference between operation modes, the power over-load supervisor operation, and the fault current limitation strategy for an ideal (<1 mΩ impedance) short-circuit occurrence and clearance.

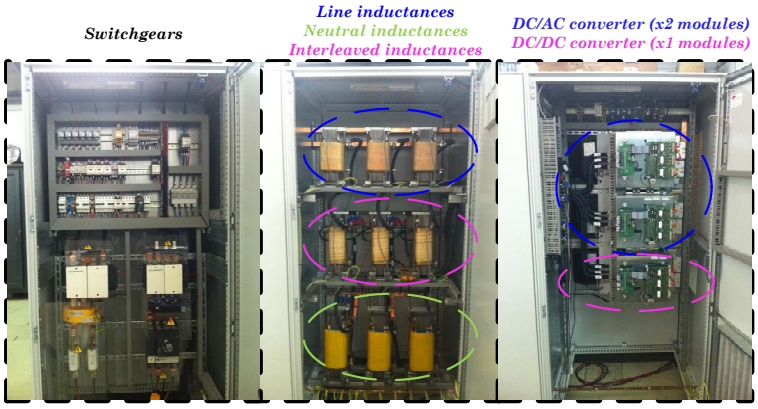
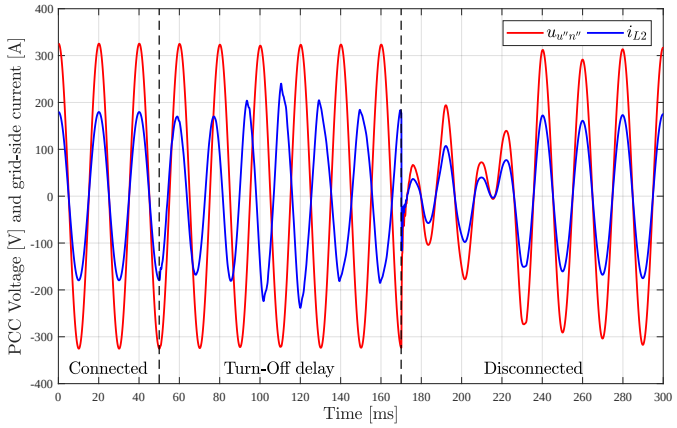


Figure 8. Converter installed in the ATENEA experimental microgrid.

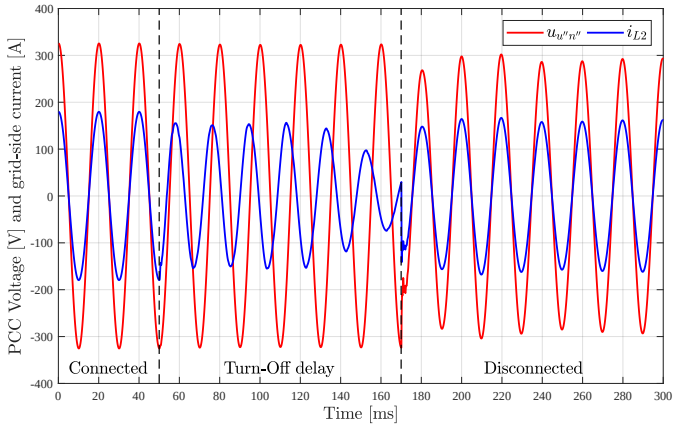
4.2.1. Virtual Resistance Effect on the Transference

For this analysis, a transference is forced to 50 ms time. A main switch to segregate the mains from the microgrid with a turn-on/off delay of 40/120 ms has been assumed.

In Figure 9, the effect of the R_v value on the voltage $u_{u''n''}$ and the delivered current i_{L2} can be observed when a grid-connected to grid-disconnected transference takes place. In the initial situation, P_u* is set at 30 kW before t = 50 ms and a local load of 1.81 Ω is connected at any time. The use of an initial R_v allows for smoothing the transference in terms of voltage and currents.



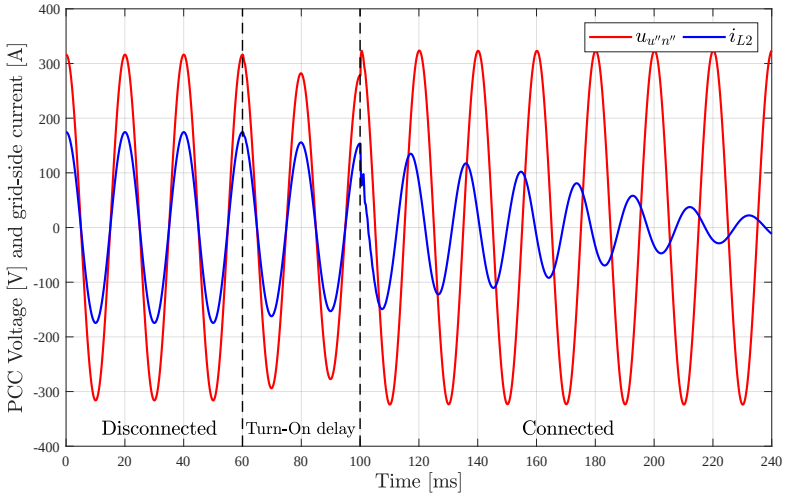
(a) R_v is set to 0 Ω immediatly after the grid-disconnection



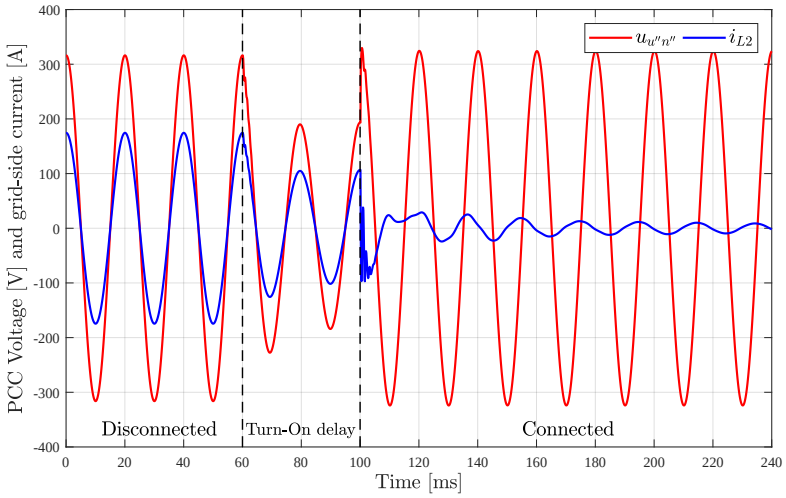
(b) R_v is set to 0 Ω progressively at a -0.16 Ω/s ratio after the grid-disconnection

Figure 9. R_v (0.2 Ω initially) effect during grid-connected to grid-disconnected transference at t = 50 ms.

In Figure 10, the effect of the R_v value on the voltage $u_{u''n''}$ and the delivered current i_{L2} can be observed when a reconnection transference takes place. In this case, in the initial situation, a load of 1.81 Ω is connected and maintained after the reconnection. No PQ references are considered in this case. As in the disconnection case, the use of an initial R_v smooths the transference in terms of voltage and currents. The use of high R_v values helps to extinguish the i_{L2} current faster but creates a voltage dip. However, this virtual resistance allows for making the system less sensitive due to interfacing with a virtual current limiter during the reconnection process. Then, a trade-off R_v value has to be used when the reconnection occurs. According to the mentioned reasons, an R_v equal to 1 Ω is suggested as a proper compromise value, also used in the experimental validation in Section 4.3.1.



(**a**) R_v is set to 0.2 Ω after the grid-connection



(**b**) R_v is set to 1 Ω after the grid-connection

Figure 10. R_v (0 Ω initially) effect during grid-disconnected to grid-connected transference at t = 50 ms.

4.2.2. Power Over-Load Supervisor

Figure 11 shows the behaviour of the power over-load supervisor strategy presented in Figure 6. In Figure 11, s^* refers to the power set-point received from any external manager, while s^*_{int}, represents the inner reference managed by the mentioned over-load supervisor strategy. Note that the current tracking is supposed to operate properly, as it is illustrated in Section 4.

In Figure 11, three different study cases framed in yellow can be observed. The first one refers to a short-time over-load demand. The second one accumulates two over-load queries. Finally, the third one evaluates a prolonged over-load target. The maximum over-load time, $T_{max\,ol}$, is set to 1 s.

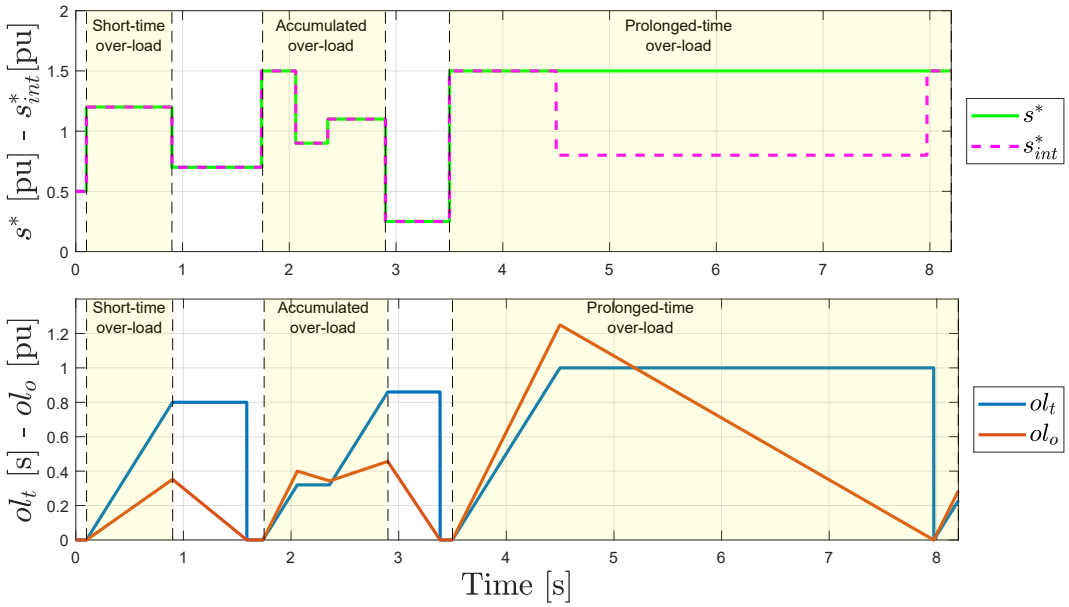


Figure 11. Example of the power over-load supervisor algorithm behaviour.

Regarding the short-time scenario, when s^* is higher than 1, the o_{l_t} and o_{l_o} values increase. When s is lower than 1, the o_{l_t} time is held while o_{l_o} decreases progressively according to Equation (1). In this sense, the generated thermal stress on the cooling system is limited. This situation is exemplified in the accumulated over-load region. Although the set-point s is reduced transiently, the o_{l_t} time continues increasing due to not achieving o_{l_o} equal to zero. Lastly, for a prolonged-time, an over-load region can be observed as to how the over-load strategy limits the inner set-point s^*_{int} to 0.8 [pu]. This situation is produced when o_{l_t} reaches a pre-configured $T_{max\,ol}$ and remains unaltered until the o_{l_o} reaches zero. Note that the maximum over-load time, $T_{max\,ol}$, can be configured for each phase according to any specific design of the cooling system. Thus, the 1 s previously selected is just an example.

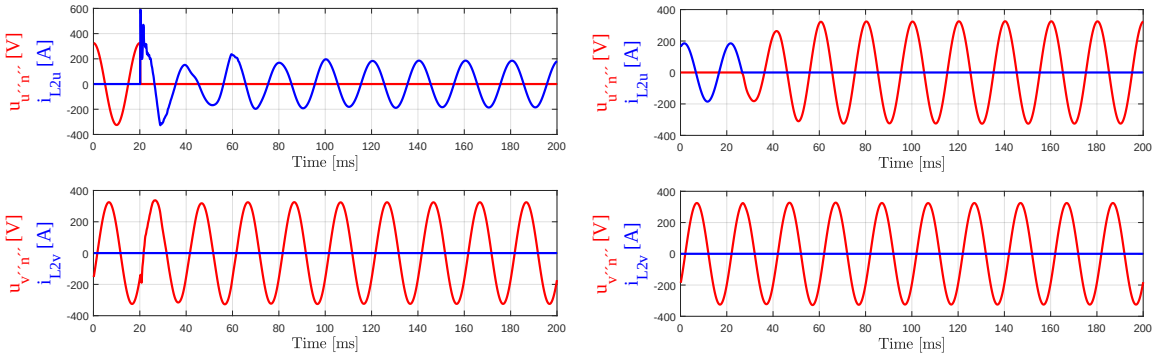
4.2.3. Short-Circuit Proof Algorithm

Scenario 1—Phase to neutral short-circuit. Figure 12a,b show the behaviour of the voltage and current of phases u'' and v'' when a unipolar $u''n''$ short-circuit is generated and recovered, respectively. It can be seen that the voltage goes to zero when the fault appears maintaining the current limited with a sinusoidal waveform. When the fault is recovered, the voltage increases progressively without producing any problematic over-voltage. In both cases, the time response is less than 60 ms.

Scenario 2—Phase to phase short-circuit. Figure 13a,b show the behaviour of the voltage and current of phases u'' and v'' when a bipolar $u''v''$ short-circuit is generated and recovered. It can be deduced $i_{L2u} = -i_{L2v}$ and $u_{u''n''} = u_{v''n''}$, as can be also observed in Figure 13b. This case is particularly interesting because, although the current is properly managed in the steady-state, it can be seen that the voltage does not go to zero after the fault.

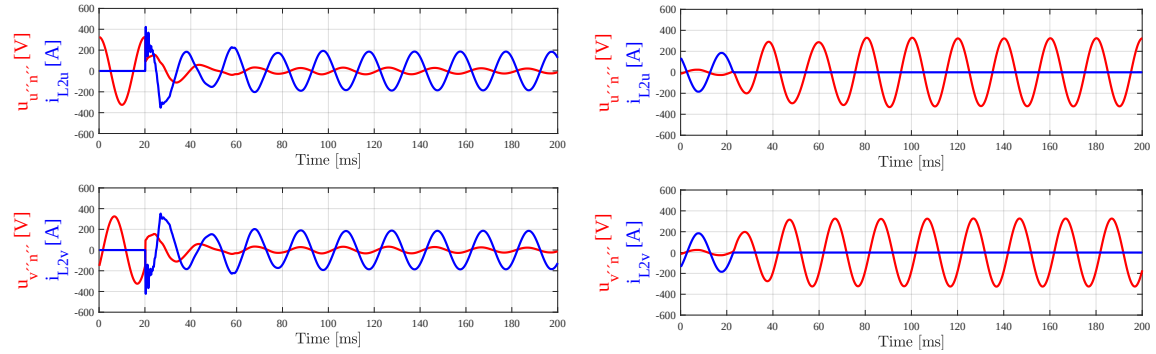
When the fault occurs, it is possible that, in one of the two involved phases, its voltage control action, PRHC$_u$ output, plus the short-circuit current, i_{L2}, adds up to more than in the other case (see Figure 7b). The phase with more errors rapidly produces a k_1 gain that moves from one to zero. As the other phase operates with higher k_1 values, it starts to control the current without necessarily a k_1 gain equal to zero. This means without the correspondent phase-to-neutral voltage equal to zero.

When the fault is recovered, the voltage increases progressively without producing any problematic over-voltage. As in the unipolar case, the transients are resolved in less than 2–3 grid cycles.



(**a**) u'' to n'' fault occurrence (**b**) u'' to n'' fault clearance

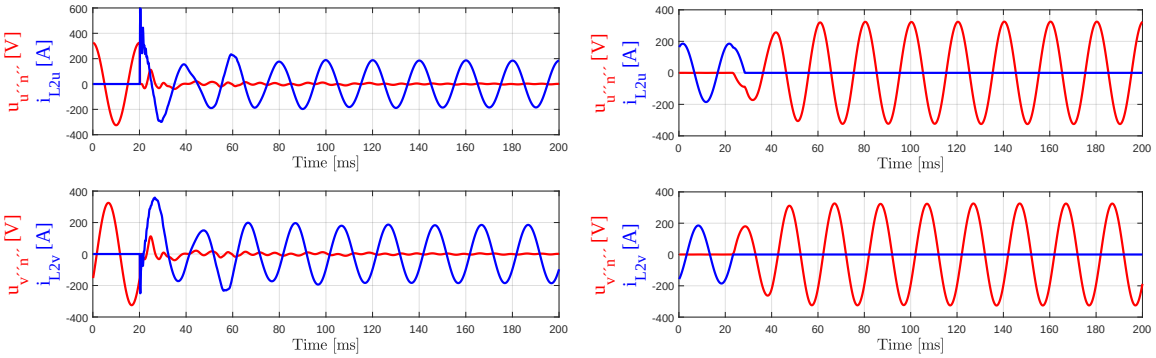
Figure 12. Scenario 1 (simulated phase to neutral short-circuit fault).



(**a**) u'' to v'' fault occurrence (**b**) u'' to v'' fault clearance

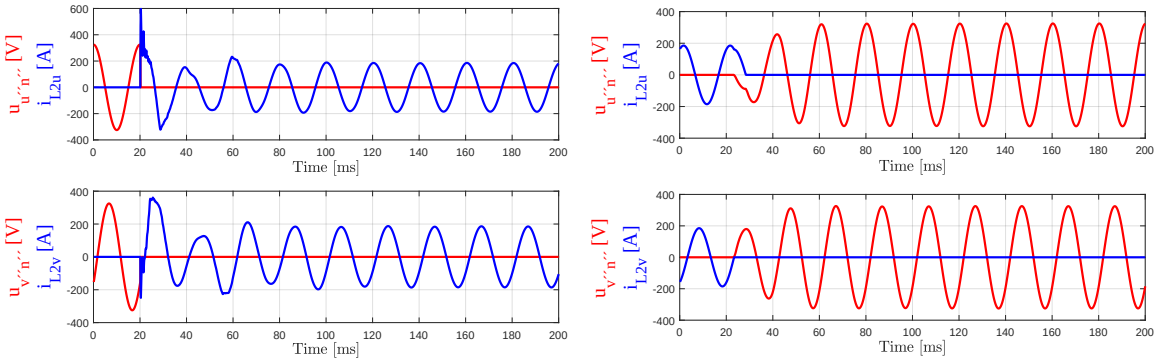
Figure 13. Scenario 2 (phase to phase short-circuit fault).

Scenarios 3–4—Three-phase short-circuit and Three-phase to neutral short-circuit. Figures 14 and 15 show the behaviour of the voltage and current of phases u'' and v'' when a tripolar between phases or a tetrapolar short-circuit is enforced and recovered, respectively. As in the previously studied cases, the behaviour of the current and voltage follows similar time responses.



(**a**) $u''v''w''$ fault occurrence (**b**) $u''v''w''$ fault clearance

Figure 14. Scenario 3 (three-phase short-circuit).



(**a**) $u''v''w''$ to n'' fault occurrence (**b**) $u''v''w''$ to n'' fault clearance

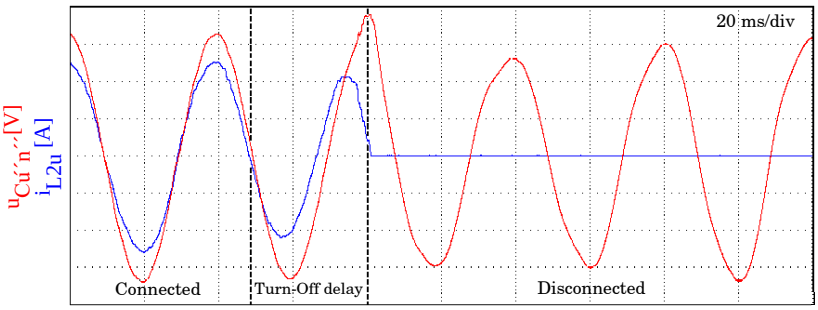
Figure 15. Scenario 4 (three-phase to neutral short-circuit).

4.3. Experimental Results

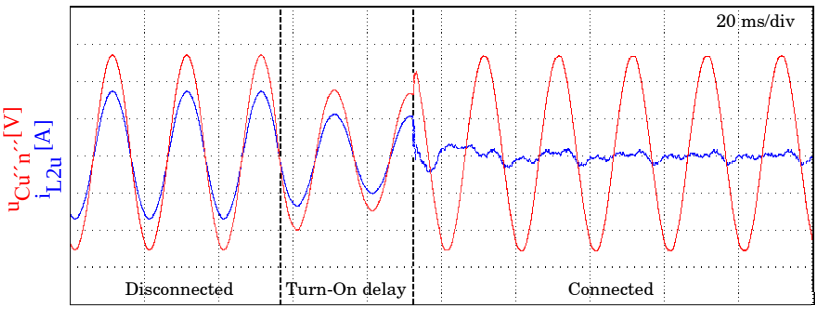
This section is divided into three subsections to validate the suggested proposals along the paper and check the simulation results presented in the previous section.

4.3.1. Virtual Resistance Effect on the Transference

In Section 4.2.1, the theoretical effectiveness of the virtual resistance algorithm to smooth the transference between grid-(dis)connected modes was demonstrated by simulations. For the experimental validation, only the R_v value of 1 Ω has been used when the reconnection occurs, as detailed in Section 4.2.1. Figure 16 shows the experimental results for two scenarios, grid-connected to grid-disconnected and vice versa. A load of 1.81 Ω has been considered.



(**a**) Island transference $u_{C_{u''n''}}$ (100 V/div) and i_{L2u} (100 A/div) when P_u is 45 kVA



(**b**) Reconnection transference $u_{C_{u''n''}}$ (120 V/div) and i_{L2u} (100 A/div) with 1.81 Ω load

Figure 16. Scenario 1 (**a**) and 2 (**b**). Microgrid transitions between operation modes.

Scenario 1—Transition from grid-connected to grid-disconnected at maximum power without local loads. Phase u is delibering 45 kW while the other two phases are with null PQ requests. Then, a non-intentional disconnection to start operating in grid-disconnected is done. Figure 16a

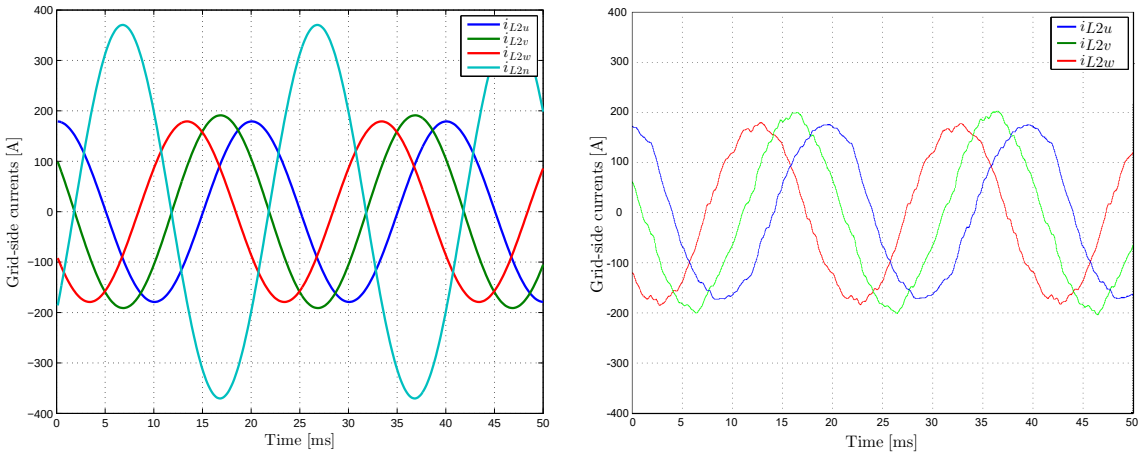
shows the proper behaviour of the voltage, creating a short-duration dip that meets the ITI curve. After the transition, the delivered current goes to zero and the voltage of the microgrid is maintained.

Scenario 2—Transition from grid-disconnected to grid-connected with load. A reconnection procedure is intentionally done with a high current local load. Figure 16b allows for observing that, after the reconnection, the $u_{C_{u''n''}}$ voltage suffers a dip during two cycles, but the current i_{L2} is extinguished just after the reconnection is finished. The experimental results are close to the simulation shown in Figure 10b, validating the exposed method.

In both cases, the PCC voltage suffers an alteration, the transition from grid-disconnected to the grid-connected mode being more critical. However, in both cases, the voltage alterations are resolved by control in less than 40 ms, meeting the ITI curve requirements. This trade-off permits a safe system connection even in weak grids while complying the regulation requirements.

4.3.2. Four Quadrant Control Capability

The objective of this section is showing the capability of the inverter to control unbalanced phase currents as mentioned in Section 1 and required for the proper use of the over-load supervisor strategy suggested in Section 4.2.2. In this scenario, the inverter is operating in grid-connected mode with rated (non over-loaded) unbalanced PQ set-points. The set-points per phase are $P_u = P_w = 30$ kW, $P_v = -30$ kW and Q_{uvw} all nulls. Figure 17 shows that the inverter is able to synthesize non-balanced currents from non-balanced PQ references.



(**a**) Simulated results (**b**) Experimental results

Figure 17. Inverter in grid-connected mode. Unbalanced set-point: $P_u = P_w = 30$ kW, $P_v = -30$ kW and $Q_{uvw} = 0$ kvar.

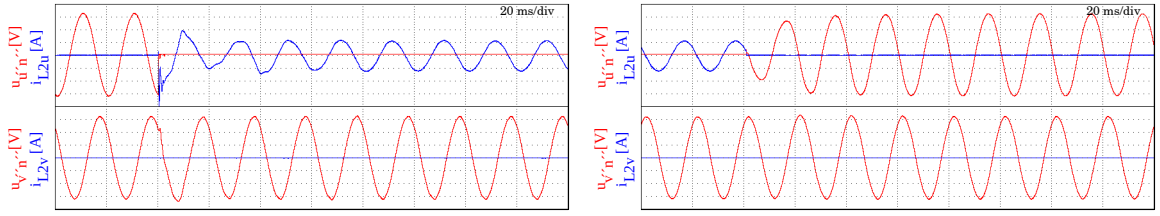
Figure 17a shows a simulation of the expected active phase and neutral wire output currents, respectively. Figure 17b presents the captured oscilloscope active currents. It is demonstrated that there is no problem to track unbalanced PQ set-points. Thus, it is possible to ensure that if an over-load supervisor manages the inner converter references, called s^*_{int} in Figure 11, the inverter can provide autonomous over-load capability per phase.

4.3.3. Short-Circuit Proof Algorithm

In this section, the four scenarios simulated in Section 4.2.3 are reproduced in the experimental platform to validate the real capabilities of the proposed fault current limitation strategy. In the following lines, it is demonstrated that the time response for the fault current limitation action and voltage recovery offers superior time responses than in the current literature [38–40].

Scenario 1—Phase to neutral short-circuit. Figure 18 shows the behaviour of the voltage and current of phases u'' and v'' when unipolar $u''n''$ is produced. Analogously with Figure 12a, it can

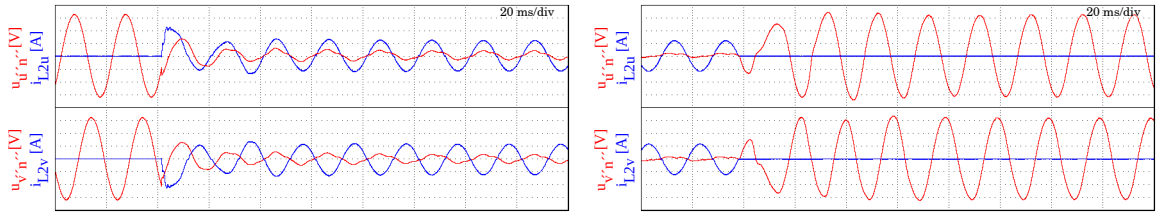
be seen in Figure 18a that, when the fault appears, the control maintains the current limited with a sinusoidal waveform presenting a minor oscilation that is resolved in less than 30 ms. Figure 12b shows the system behaviour when the fault is cleared, recovering the nominal voltage value progresively in less than two grid cicles, in the same way as the simulation reproduced in Figure 12b.



(**a**) u'' to n'' fault occurrence (**b**) u'' to n'' fault clearance

Figure 18. Scenario 1 (phase to neutral short-circuit fault). $u_{x''n''}$ (100 V/div) and i_{L2x} (150 A/div).

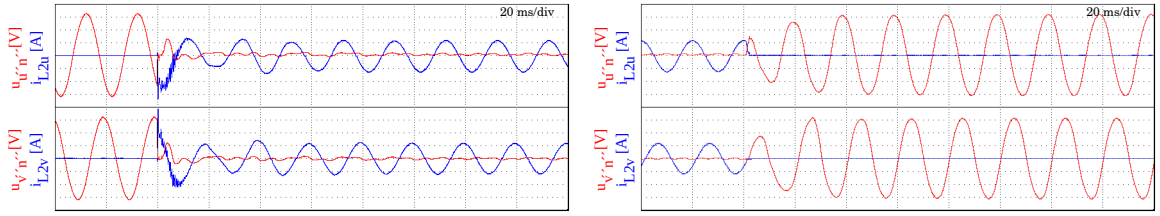
Scenario 2—Phase to phase short-circuit. Figure 19 shows the behaviour of the voltage and current of phases u'' and v'' when a bipolar $u''v''$ short-circuit is generated and recovered, analogous to simulations shown in Figure 13. In Figure 19a, it can be seen that the initial transient of current u'' and v'' is less than two times the maximum current, achieving steady-state values in less than 30 ms. When the fault is recovered, the voltage increases progressively achieving the steady-state in less than 40 ms as shown in Figure 19b.



(**a**) u'' to v'' fault occurrence (**b**) u'' to v'' fault clearance

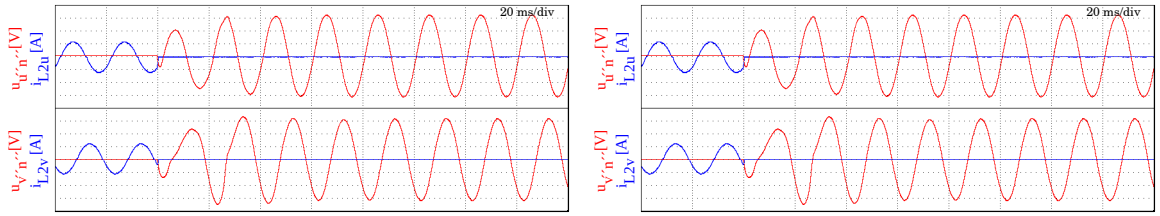
Figure 19. Scenario 2 (phase to phase short-circuit fault). $u_{x''n''}$ (100 V/div) and i_{L2x} (150 A/div).

Scenarios 3–4—Three-phase short-circuit and Three-phase to neutral short-circuit. Figures 20 and 21 show the behaviour of the voltage and current of phases u'' and v'' when a tripolar and tretrapolar fault is produced. As in the simulated cases shown in Figures 14 and 15, the control algorithm limits the fault current in the expected time, being less than 40 ms. The fault recovery is also achieved rapidly, in less than two grid cycles.



(**a**) $u''v''w''$ fault occurrence (**b**) $u''v''w''$ fault clearance

Figure 20. Scenario 3 (three-phase short-circuit). $u_{x''n''}$ (100 V/div) and i_{L2x} (150 A/div).



(**a**) $u''v''w''$ to n'' fault occurrence (**b**) $u''v''w''$ to n'' fault clearance

Figure 21. Scenario 4 (three-phase to neutral short-circuit). $u_{x''n''}$ (100 V/div) and i_{L2x} (150 A/div).

5. Conclusions

This paper has presented two control strategies to achieve a fast and proper fault current limitation for four wire microgrid inverters. Both strategies are supported by a dynamic virtual resistance mechanism that allows for a fast transference between grid-(dis)connected operation modes.

Concerning the AC side inverter operation, a seamless transference between grid-(dis)connected modes has been ensured obtaining short transients, below three grid cycles. For this purpose, a combination of an AC droop control based on dynamic phasors when grid-connected and master voltage/frequency control when grid-disconnected has been proposed. It has been demonstrated not only that this is a valid option to maintain the voltage behaviour between operation modes, but also it is able to make the grid-disconnected operation independent from the AC droop control loop constraints. Thus, the transients in grid-disconnected mode are only limited by the settling time of the voltage control loop. Furthermore, a varying virtual resistance is suggested for achieving the mentioned seamless transference, disabling the resistance value progressively when entering in grid-disconnected operation. It has been illustrated that the proper selection of the steady-state virtual resistance and the used variation ratio helps to avoid voltage sags in the transient phase between the operation modes, allows for being less sensitive to the reconnection process and, finally, provides a predominant resistive behaviour for the grid-connected operation.

An over-load manager supervisor strategy based on thermal criteria has been introduced. This over-load strategy provides an increase in managing flexibility to a microgrid inverter in a grid-connected mode. The over-size challenge is then delegated to higher current switching devices, a not really cost sensitive component today in power converters. Thus, if the cooling system has enough thermal time lag, it is possible to obtain over-load skills in which the available over-load currents are managed by the proposed strategy. In case of prolonged over-load, the situation is detected and the inverter simply delivers a percentage of the nominal current to relieve the accumulated thermal stress.

Finally, a short-circuit proof strategy is introduced as a fault current limiter and voltage regulator. This short-circuit proof strategy is validated though unipolar, bipolar, tripolar and tetrapolar pure short-circuits. As the control in grid-disconnected mode is only based on voltage and current control loops, the suggested strategy only considers voltage and current, but not power. The strategy is mainly based on computing the rms value of the delivered current. Then, the current and voltage can be quickly adapted to handle the fault occurrence and clearance. This is done maintaining sinusoidal waveforms in both cases by a simple calculation of two proportional factors and the use of a filter. In this sense, the time response of protective devices will be affected minimally. The time response has been a priority in this paper, obtaining fault current limitation and voltage regulation in the order of two–three grid cycles even considering low impedance short-circuits, a superior capability compared to similar literature.

The feasibility of the proposed converter has been demonstrated not only at control level by simulation using Matlab/Simulink but also experimentally at a CENER-ATENEA four-wire microgrid.

Author Contributions: Conceptualization, D.H.-P., M.P.-G. and C.C.-A.; Software, D.H.-P., M.P.-G. and C.C.-A.; Validation, M.S., D.R. and M.A.; Formal Analysis, D.H.-P.; Investigation, D.H.-P., M.P.-G. and C.C.-A.; Methodology, D.M.-M.; Resources, M.S., D.R. and M.A.; Writing—Original Draft Preparation, D.H.-P.; Writing—Review D.H.-P., C.C.-A.

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