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Thermomechanical Stresses in Silicon Chips for Optoelectronic Devices

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Abstract: The growing interest in improving optoelectronic devices requires continuous research of the materials and processes involved in manufacturing. From a chemical point of view, the study of this sector is crucial to optimize existing manufacturing processes or create new ones. This work focusses on the experimental evaluation of residual stresses on samples that are intended to simulate part of the structure of an optoelectronic device. It represents an important starting point for the development of optoelectronic devices with characteristics suitable for future industrial production. Silicon chips, with a thickness of 120 µm, were soldered onto copper and alumina substrates, using different assembly parameters in terms of temperature and pressure. Using Raman spectroscopy, the stress evaluation was estimated in a wide temperature range, from −50 to 180 °C. Silicon chips soldered with AuSn alloy on copper substrates demonstrated at 22 °C a compressive stress, developed in the center of the assembly with a maximum value of −600 MPa, which reached −1 GPa at low temperatures. They present a stress distribution with a symmetric profile with respect to the central area of the chip. The silicon chip assembled on a ceramic substrate without pressure turned out to be extremely interesting. Even in the absence of pressure, the sample did not show a large shift in the Raman position, indicating a low stress.

Keywords: optoelectronic devices; silicon (Si); soldering; thermomechanical stress; Raman shift

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1. Introduction

Semiconductor silicon chips are used for various applications, including consumer electronics, industrial purposes, telecommunication, and in the automotive field. Being the second most abundant element on Earth, silicon is a relatively inexpensive material and is highly reliable due to its versatility and physical–chemical properties [1]. Its thermal expansion coefficient is low compared to most metals, making most of the effects negligible due to thermal shock and fatigue. Silicon is fairly inert under standard environmental conditions, it does not react with most acidic compounds, but reacts with diluted alkalis and halogens, and its electrical conductivity can be tuned by adding small amounts of impurities [2]. For these reasons, semiconductor silicon remains the core component of many microelectronic devices, it is an essential component of integrated circuits (ICs), the building block of power devices such as computers and smartphones, and it is essential for photovoltaics to manufacture solar cells. In particular, single-crystal silicon is the most widely used semiconductor material in the micro-electromechanical (MEMS) manufacturing and electronic and optoelectronic circuits industry. In addition, the continuous demand for compact and miniaturized devices has increased the need for more functionalities from a single device. This means that today an IC chip is requested to house a larger number of components to support more features. A silicon-integrated circuit chip is realized by embedding and overlaying different elements of a wide variety of materials, each characterized by different elastic and thermal properties. Therefore, it follows that many structural elements, by

virtue of their formation processes, exhibit intrinsic stresses. Stress problems are prevalent in silicon technology and become critical, as they can impact the performance of the ICs. For these reasons, understanding the nature and origin of stresses is a fundamental issue. It is strategic to investigate the stresses developed during the assembly process, as a function of the working parameters, using an experimental technique and predictive theoretical models. Raman spectroscopy is an efficient tool to measure residual stress by correlating the effects with the optical change in the materials [1–7]. Moreover, it is a nondestructive and noncontact method, characterized by a high spatial resolution, and has already been widely used to investigate silicon, such as in cubic crystals [8,9], microelectronic devices [10–13], and nanostrips [14].

Selecting the right substrate materials for the production of microelectronics is one key point in the process. The substrate must be highly reliable, in configurations precisely chosen to meet the needs of a specific application. Several substrate materials are used, which are carefully chosen on the basis of the performances needed to reach, but also following other criteria like safety, environmental impact, economic costs, and process complexity. Organic-based composite materials in polymeric form have attracted considerable attention because they offer the opportunity to produce substrates with multiple customizable functionalities, they cover large areas, and are flexible, lightweight, and are relatively low in cost [15–18]. There is an immense scope for the future of flexible organic electronics. However, the current performance and lifetimes of electronic devices based on organic substrates are still lower than those of traditional ceramic or other inorganic materials [19], such as aluminium nitride or copper. Ceramic substrates are well known for high-temperature electronic integration. Copper substrates are widely used in microelectronics because of the advantageous properties of copper, such as low electrical resistivity, high electromigration resistance, high thermal conductivity, excellent chemical and thermodynamic characteristics, antimicrobial properties, and low cost. A problem with Cu is the tendency to form oxides on the surface; this problem can be overcome using formic acid or formate salts to prevent the formation of oxides, as reported for LED assembled on copper substrates [20].

The focus of this work is the evaluation of residual stresses on silicon samples that are intended to simulate part of the structure of an optoelectronic device. This study represents an important starting point for the development of optoelectronic devices with characteristics suitable for future industrial production. The aim is to experimentally investigate the stresses induced on the devices during the assembly procedure as a function of different process parameters, such as the physical and chemical characteristics of the involved substrates, temperature, and pressure. The samples examined consist of a silicon chip, with a thickness of 120 μm, soldered under different conditions on copper or alumina (Al_2O_3) substrates, with a thickness of 1 mm. A stress evaluation was performed, using a micro-Raman spectroscopic technique. Measurements were carried out at room temperature and at different temperatures, ranging from −50 to 180 °C, a temperature range for the use of electronic devices. The results obtained suggest advantages and disadvantages in terms of stress in the use of ceramic substrate over copper substrate and the effect of applied pressure during the assembly process of the samples.

2. Materials and Methods

2.1. Materials and Sample Preparation

The assembly structure of the developed samples consists of a substrate, above which an interconnection material is located, and a Si chip, which is placed above it, as represented in Figure 1.

In this work, two types of substrate were adopted: a copper substrate, with dimensions ($5 \times 5 \times 1$) mm^3, and an Al_2O_3 ceramic substrate, with dimensions ($2.4 \times 2.4 \times 1$) mm^3, covered with gold metallization, reported in Figure 2a,b.

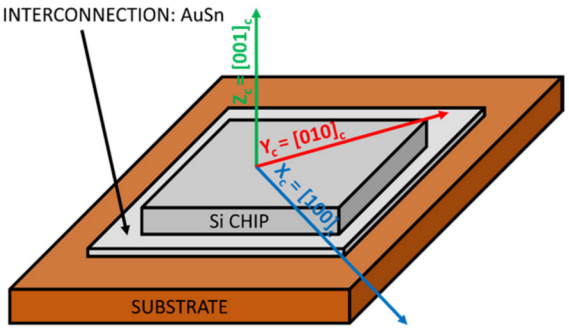


Figure 1. Schematic illustration of an assembled device showing three main components: Si chip on top, substrate on bottom, and interconnection material in between. The cartesian axis system reflects the geometric symmetry of the Si crystal.

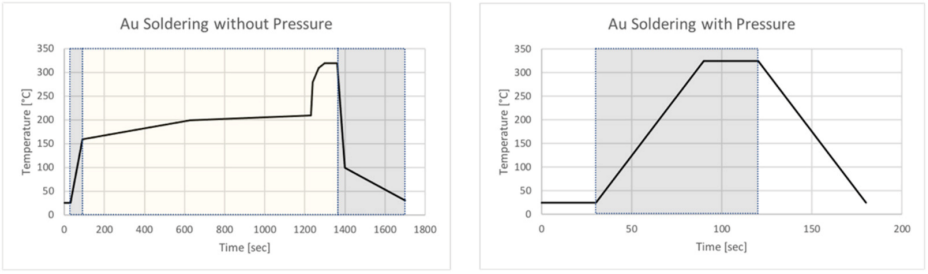
(**a**) (**b**)

Figure 2. Images of (**a**) copper and (**b**) Al_2O_3 ceramic substrates.

The copper substrates were mechanically treated first by rubbing the surfaces on abrasive discs with different grains, taking care not to avoid scratches; then they were placed in an ultrasonic bath of 4% hydrochloric acid, and finally in an ultrasonic bath with isopropanol. Ceramic substrates were used without any prior treatment.

Silicon chips were adopted with dimensions 1500 × 1500 × 120 μm^3, (001) oriented, and with gold metallization at the bottom. An interconnection material, for the soldering process, was used to build the devices: it consists of a thin layer of Au80Sn20 eutectic alloy with a thickness of 25 µm [21,22]. The soldering procedure was carried out following two different working processes, depending on the application or not of an external pressure. All Si-chips were soldered to the substrate using a vacuum-assisted closed reflow oven (Unitemp, RSS-160). For efficient soldering, surface oxides and undesired residuals were removed using formic acid vapor, which has strong reducing effects. The assemblies were prepared at 320 °C, using a bonding time of 80 s (for the samples without additional pressure) and 30 s (for the samples with additional pressure). Several assemblies were prepared to confirm the reproducibility of the experimental results. Figure 3 shows the temperature profiles in the reflow oven. Before proceeding with the Raman measurements, the final assemblies were optically inspected by a 3D digital microscope (Keyence VHX-900F).

For the samples prepared under pressure, the soldering process was carried out at 5 N, both in air and in N_2 atmosphere, according to the scheme reported in Figure 3b. Pressure was applied through a Fineplacer bonder (FineTech® AP2.4 145/FP 145 Pico ma), placing the chip and applying an established pressure perpendicular to the substrate surface by heating and controlling the environment of the system together. The value of 5 N was selected because it represents the maximum applicable pressure to avoid damaging the silicon chip during the assembly process.



(**a**) (**b**)

Figure 3. Temperature profile used for the soldering process with AuSn alloy as the interconnection material, without (**a**) and with (**b**) pressure. The grey regions indicate an N_2 atmosphere, while the light-yellow region indicates the additional presence of formic acid gas in the oven.

The list of all the assembled and investigated samples is specified in Table 1. Four types of Si chip samples were prepared via a soldering process: samples mounted on Cu substrates, without any pressure (A_AuSn) or using a pressure of 5 N (A_AuSn_p), or on ceramic substrates, without any pressure (B_AuSn) or using a pressure of 5 N (B_AuSn_p). Together with the mounted samples, the starting silicon chip (Si_unmounted) was also analyzed, which has not been assembled to a device.

Table 1. Investigated samples: unmounted Si chips or mounted with a soldering process using an interconnection of AuSn.

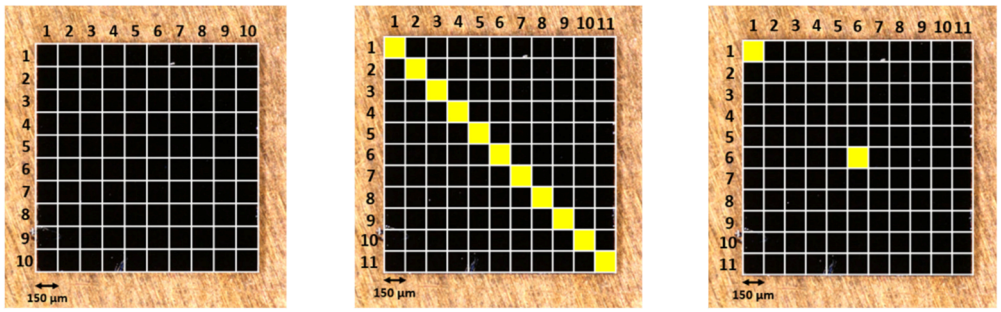
Sample Name	N° Samples	Substrate Material	Soldering Pressure [N]
Si_unmounted	1	/	/
A_AuSn_p	3	Copper	5
A_AuSn	3	Copper	0
B_AuSn_p	3	Ceramics	5
B_AuSn	3	Ceramics	0

2.2. Methods

The optical characterization of the samples was performed by recording Raman spectra at different positions on the surface of the chip, in the temperature range from −50 to 180 °C.

The Raman setup consists of a micro-Raman instrument working in a backscattering configuration. An argon–ion laser operating at a wavelength of 514.5 nm (Spectra Physics® Stabilite 2017-output power 1 W) is used as an excitation source. The focalization of the laser was realized through an optical microscope (Olympus® BX 40), equipped with interchangeable lenses 4×, 10×, 20×, 50×, 100×, and with a sample holder table movable in three directions (x, y, z) to regulate the sample position. A camera was coupled to the microscope to observe and correctly choose the area of the sample that was scanned by the laser beam. The typical spot diameter in the focus, working with a 20× objective, was 3 µm. The backscattered radiation was analyzed using a 2400 grid spectrograph and converted into an electronic signal by a nitrogen-cooled charge coupled device (CCD). A temperature controller (Linkam® THMS600) was used to conduct micro-Raman measurements at specific temperatures, where a modified atmosphere with 100% nitrogen was created to avoid problems due to water in the chamber.

The Raman signal of the samples was measured by mapping the surface of the chip in 10 × 10 positions (reported in Figure 4a) or by detecting the signal along the diagonal in 11 positions (Figure 4b) or in two defined positions, corresponding to the corner [1, 1] and the central [6, 6] positions of the chip (Figure 4c). In all cases, the instrument was set to ensure that the Raman signal was recorded in the central position of each squared area of the desired location.



(**a**) (**b**) (**c**)

Figure 4. Schematic subdivision of the surface of silicon chips (**a**). The Raman signal is acquired at the center position of each square. The diagonal points [1, 1] to [11, 11] are colored yellow in panel (**b**), while the positions [1, 1] and [6, 6] are colored yellow in panel (**c**).

Each point was recorded using the 20× lens and setting the software with an acquisition time of 5 s. The final spectrum was obtained by averaging five repeated measurements. The slit of the spectrograph was set at 40 µm and kept constant during the analysis of all samples. The input power of the laser was set at 40 mW.

The Raman spectra were acquired at different temperatures, ranging from −50 to 180 °C, using the temperature controller: starting from −50 °C and raising the temperature to 180 °C, waiting 5 min at a constant temperature before signal acquisition, and vice versa, starting from 180 °C and cooling to −50 °C.

To ensure a correct calibration of the spectrograph, we used the Raman signal from a standard commercial silicon wafer. Moreover, all the spectra of samples were normalized with respect to a plasma line signal, to ensure that the position of the band of interest is not affected by instrumental errors. All of the collected Raman spectra were interpolated with a Lorentzian function to determine their parameters, such as area, intensity, amplitude, and peak position.

2.3. Determination of Stress from Raman Spectra in Si

The frequencies of the Raman modes are affected by thermomechanical strains or stresses. Raman measurements are used to quantify the local residual stress of Si, using the secular equation of Equation (1):

$$\begin{bmatrix} p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) - \lambda & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22} + q(\varepsilon_{33} + \varepsilon_{11}) - \lambda & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) - \lambda \end{bmatrix} = 0 \quad (1)$$

where p, q and r represent the deformation potentials, which are material constants, and ε_{ij} are the strain phonon tensor components along each direction [23,24], related to the strain tensor (σ) through the Hooke's law $\varepsilon_{ij} = S_{ij}\sigma$. S_{ij} are the elastic compliance tensor elements of silicon, reported in Table 2.

Table 2. Elastic compliance constants and phonon deformation potential values for silicon [3,9,11,25].

S_{11} $[\mathbf{Pa^{-1}}]$	S_{12} $[\mathbf{Pa^{-1}}]$	$p[s^{-2}]$	$q[s^{-2}]$
$7.68{\cdot}10^{-12}$	$-2.14{\cdot}10^{-12}$	$-1.85{\cdot}{\omega_0}^2$	$-2.31{\cdot}{\omega_0}^2$

From the eigenvalues λ_j (j = 1,2,3), it is possible to calculate the difference in Raman frequencies for each mode in the presence (ω_j) and in the absence (ω_{j0}) of stress: $\lambda_j = \omega_j^2 - \omega_{j0}^2$ or

$$\Delta\omega_j = \omega_j - \omega_0 \approx \frac{\lambda_j}{2\omega_{j0}} \quad (2)$$

Given the values of S_{11}, S_{12}, p, and q, it is possible to solve the secular matrix of Equation (1). The biaxial stress along the [100] and [010] directions (xy plane, see Figure 1), for back scattering from a (001) surface, will be

$$\Delta\omega_3 = \frac{\lambda_3}{2\omega_0} = \frac{1}{2\omega_0}[pS_{12} + q(S_{11} + S_{12})](\sigma_{xx} + \sigma_{yy}) \quad (3)$$

Consequently, the biaxial stress values can be calculated using Equation (4).

$$(\sigma_{xx} + \sigma_{yy}) = -2.26 \times 10^5 \frac{\Delta\omega_j}{\omega_0} \quad (4)$$

In general, a Raman frequency value higher than the stress-free frequency indicates compressive stress in the sample, while a Raman frequency value lower than the stress-free frequency indicates tensile stress [24].

The evaluation of the stress induced in the chips by the assembly process can be performed considering the unmounted chip as a reference (providing the value of ω_0) and measuring the position of the Raman shift of the assembled samples.

3. Results

3.1. Raman Spectra of Si

Silicon is a diamond-type material. The Raman spectrum of the unmounted Si sample, reported in Figure 5, consists of an intense Raman signal with full width at a half maximum of ca. 8 cm^{-1}, centered at ~520 cm^{-1}, and corresponding to the zone-center (q = 0) optical phonon O(Γ), and a broad peak at 950 cm^{-1}, the second order Raman signal. These signals are comparable to those reported in the literature [26]. The first peak is associated with two transverse and one longitudinal branches, which are labelled as a single LTO branch. In the figure, plasma lines are also observable at 116 and 265.5 cm^{-1}.

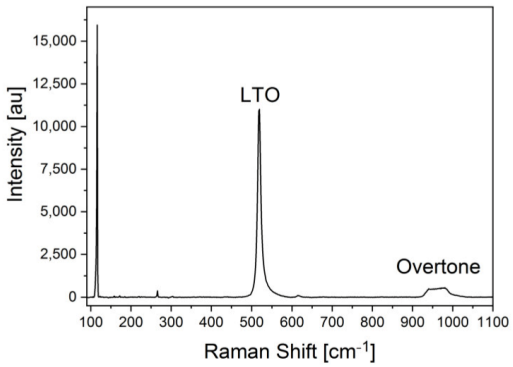


Figure 5. Raman spectrum of the silicon unmounted chip, measured using 514.5 nm radiation from an Ar laser.

3.2. Mapping Raman Spectra of Si Samples at Room Temperature

The Si phonon shift is measured as a function of the position on the sample to obtain the stress patterns of the samples, at room temperature. The Raman peak, corresponding to the LO phonon mode, collected at room temperature at the diagonal points of the chip (outlined in the central panel of Figure 4) is reported in Figure 6. From these data, it is evident that samples mounted on copper substrates with and without pressure have different behavior: the peaks positions of the first one change slightly from point to point on the diagonal, having a behavior close to the unmounted sample, while the sample mounted without any additional pressure displays a qualitatively higher shift. The sample mounted on the ceramic substrate shows a small shift in both cases.

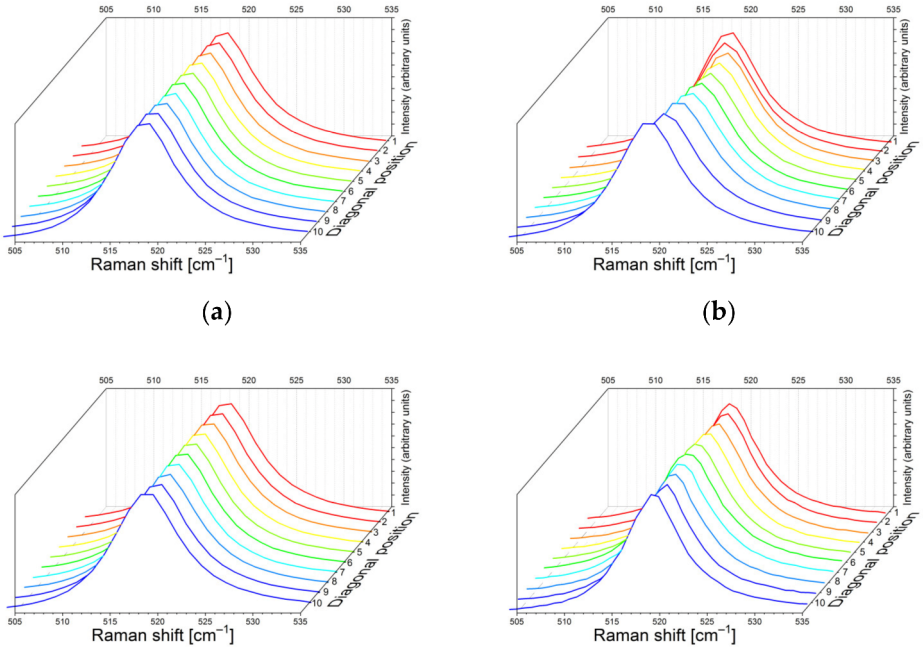


Figure 6. Raman peak, corresponding to the LO phonon mode, collected, at room temperature, along the diagonal points (from [1, 1] to [10, 10] of Figure 4b) of (**a**) the Si_Unmounted chip, (**b**) sample A_AuSn, (**c**) sample A_AuSn_p and (**d**) sample B_AuSn.

These observations can also be derived from Raman data collected from the complete mapping of the samples. The distributions of the peak positions over the area of the chips are reported on the color maps in Figure 7 and reveal an asymmetric distribution in the unmounted and mounted with pressure samples; in contrast, there is a symmetric distribution over the area of the chip mounted without pressure, with higher values in the center of the chip, with respect to the corners.

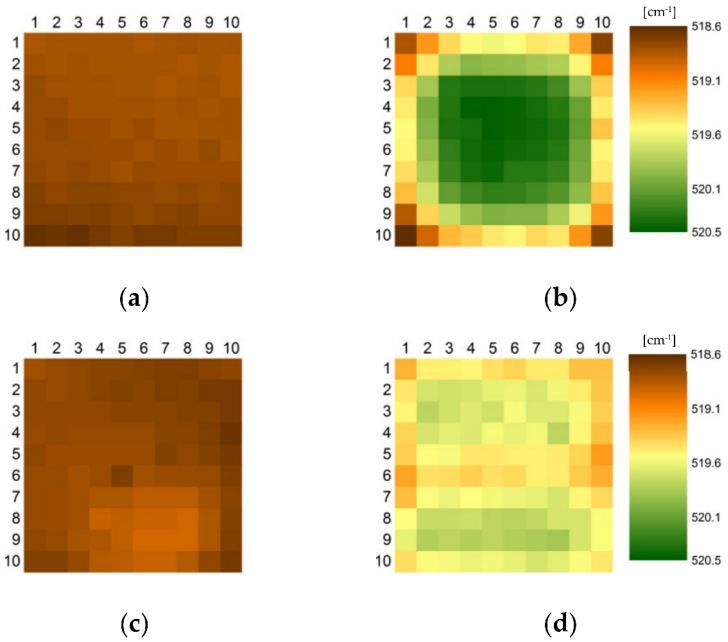


Figure 7. Raman-shift distribution at room temperature of the (**a**) Si_Unmounted chip, (**b**) A_AuSn, (**c**) A_AuSn_p, and (**d**) B_AuSn samples.

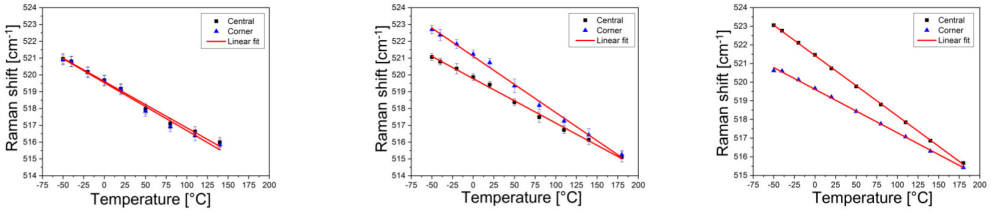
Sample B_AuSn assembled on a ceramic substrate shows a shift of the signal over the surface, with higher Raman shift values along the marginal points, as reported in Figure 7d.

3.3. Effect of Temperature on Si Samples

Raman spectra were collected at different temperatures, from −50 to 180 °C. Sample A_AuSn was measured on the diagonal, at −50, −40, −20, 0, 20, 50, 80, 110, 140, and 180 °C, at increasing and decreasing temperatures. By acting in this way, no strong differences were observed between the data collected at the same temperature during the heating and cooling process (see Table S1 in SI for details). This is clear evidence that, independently of the thermal history of the sample, the assembly has high stability between −50 and 180 °C.

The slight differences in signal position may be due to the micrometric shift of the sample inside the sample holder as the temperature changes. This fact leads to inevitable random errors due to the sampling of a chip position that is not exactly identical to the previous one.

For the Si_Unmounted, A_AuSn_p, and A_AuSn samples, the Raman-shift values of the 520 cm^{-1} peak were collected from −50 to 180 °C, at increasing temperature, in the center of the chip (position [6, 6]) and in a corner (position [1, 1]), which are the positions that typically correspond, respectively, to a more and a less stressed area of the sample [6,7,13]. These Raman shifts are reported in Figure 8 and show a linear trend with different intercept and slope values, whose values are reported in Table 3. It is evident how temperature affects the Raman shift value of all samples: as temperature increases, the Raman shift values decrease. Moreover, in the central position, there is a marked difference between Si_Unmounted and mounted samples, reaching the higher values with the A_AuSn assembly, whereas in the corners there are no marked differences in intercepts and slopes. This means that the center, the most stressed area, is more affected by thermal processes than the corner.



(**a**) (**b**) (**c**)

Figure 8. Central [6, 6] (squares) and corner (triangles) [1, 1] Raman shift recorded at temperatures from −50 to 180 °C with the Si_Unmounted chip (**a**), the A_AuSn_p sample (**b**) and the A_AuSn sample (**c**).

Table 3. Linear fit parameters of the Raman peak position signal of the chips at different temperatures.

	R^2	Intercept	Slope
Central position [6, 6]			
Si_Unmounted	0.980	519.53 ± 0.07	−0.0248 ± 0.0007
A_AuSn_p	0.997	519.78 ± 0.05	−0.0265 ± 0.0005
A_AuSn	0.999	521.43 ± 0.01	−0.0324 ± 0.0002
Corner position [1, 1]			
Si_Unmounted	0.986	519.44 ± 0.09	−0.0248 ± 0.0007
A_AuSn_p	0.996	519.69 ± 0.05	−0.0268 ± 0.0005
A_AuSn	0.996	519.61 ± 0.05	−0.0268 ± 0.0005

Additionally, the intercept values and the slopes of the fitting outline the differences between the mounted and unmounted samples.

The Raman shift values, collected on the diagonal of the chips on copper substrates, at −50 °C, 20 °C, and 180 °C are reported in Figure 9: the Raman shift values decrease at increasing temperature.

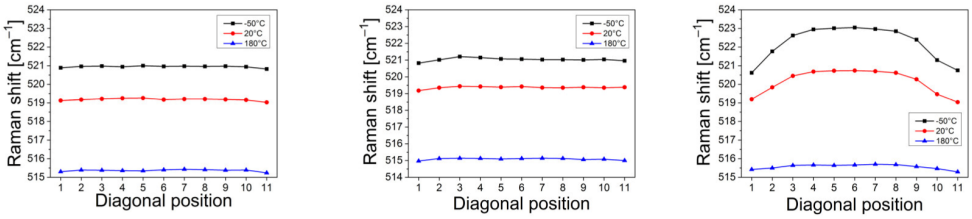


Figure 9. Raman shift distribution along the diagonal recorded at −50 (black points and lines), 20 (red points and lines) and 180 °C (blue points and lines), on (**a**) Si_Unmounted chip, (**b**) A_AuSn_p sample and (**c**) A_AuSn sample (C). Position *i* refers to the position [i,i] of Figure 4b.

The position of the peak does not change significantly along the diagonals of unmounted and mounted pressure samples when the temperature is constant: this reflects that the samples present only weak stress values. The Raman shift values along the diagonal of the sample without pressure show a variation in the shift that has a similar trend at constant temperatures: lower values at the corner positions [1, 1] and [11, 11], which increase symmetrically as the temperature moves closer to the center; moreover, it increases in absolute value with decreasing temperature, in particular in the central area.

4. Discussion

The biaxial stress values of silicon have been calculated from Raman data with the equation $(\sigma_{xx} + \sigma_{yy}) = -2.26 \times 10^5 \Delta\omega_j/\omega_0$. A Raman frequency greater than the stress-free frequency indicates compressive stress in the sample, while a Raman frequency smaller than the stress-free frequency indicates tensile stress [7,10,25].

The stress values of the Si samples evaluated along the diagonal positions at −50, 20, and 180 °C, from Raman spectra, are reported in Figure 10. To evaluate the stress values of the assembled samples, the Raman frequency of the unmounted sample is assumed as the reference value: ω_j is the Raman shift value of the j-peak of the sample, while ω_0 is chosen as the Raman shift of the unmounted sample relative to the same position on the map, in order to relate the measured stress only to the assembly process, that is, to neglect the intrinsic stresses that are inevitable in the samples. Instead, the stress of the unmounted chip is calculated by considering as a reference the internal value obtained from the average Raman shift of the entire position of the sample in the unmounted sample. The negative sign indicates compressive stress.

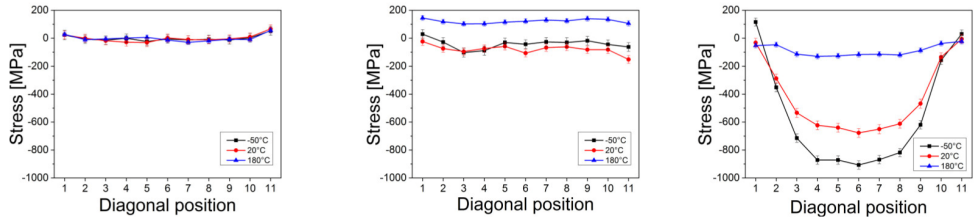


Figure 10. Stress distribution along the diagonal recorded at −50 (Black points and lines), 20 (Red points and lines) and 180 °C (Blue points and lines), on the Si_Unmounted chip (**a**), the A_AuSn_p sample (**b**) and the A_AuSn sample (**c**). Position *i* refers to the position [x, x] of Figure 4b.

The experimental data show a compressive stress, whose values vary in a range of 1 GPa when the assembly is at high temperature (180 °C) or low temperature (−50 °C).

The figure shows that the magnitude of stress in the sample prepared under pressure is much lower than in the sample prepared without the use of an additional pressure of 5 N. At first sight, the conclusion would be that the effect of the pressure during soldering of the transition AuSn layer could be helpful, because for the assembly without pressure, the Raman signal of the Si peak changes strongly, in comparison to the signal of unmounted Si. Further measurements were carried out to check the interconnections, in particular, those for the cross-section analyses of the assemblies have revealed that the Si chip was not properly soldered to the substrate, i.e., the use of the pressure of 5 N was a disadvantage on these samples. Studies in this direction are still in progress.

Similarly, the stress distribution of the different samples was determined from the Raman mapping data. Color maps, in Figure 11, report the stress values of the Si samples, determined on the entire surface of the samples, at 20 °C. A_AuSn is the most stressed sample, with a variation of 775 MPa on the surface. The stress map of the B_AuSn sample shows the highest variation on the total area equal to 329 MPa, a value that is lower compared to the corresponding sample assembled without pressure on the copper substrate.

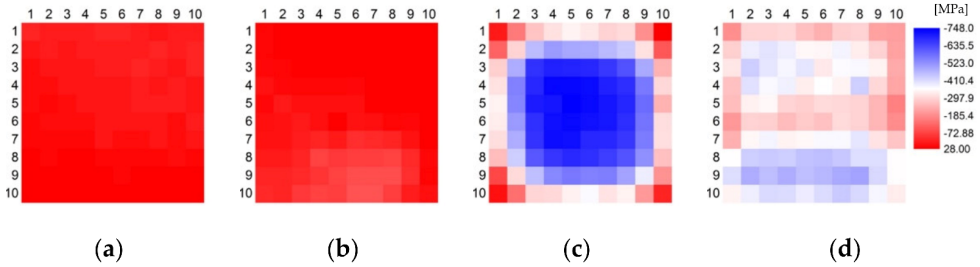


Figure 11. Stress distribution at 20 °C, on (**a**) Si_Unmounted chip, (**b**) A_AuSn_p, (**c**) A_AuS, and (**d**) B_AuSn samples.

Figures 12 and 13 report the stress values of the Si samples, on copper substrates, determined on the entire surface of the samples, at −50 and 180 °C, respectively. The maximum stress is observable at low temperature on A_AuSn: it reaches a value of −928 MPa and is highly symmetric.

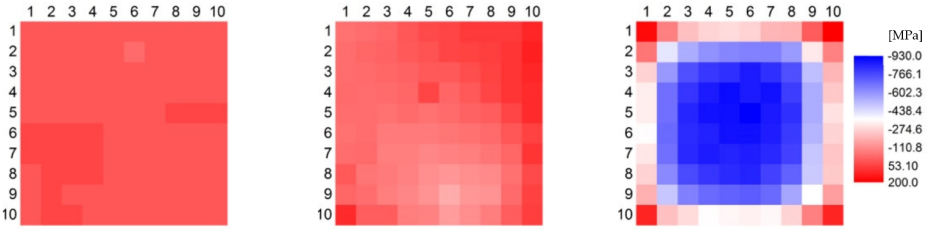


Figure 12. Stress distribution at −50 °C, on a Si_Unmounted chip (panel **a**), A_AuSn_p sample (**b**), and A_AuSn sample (**c**).

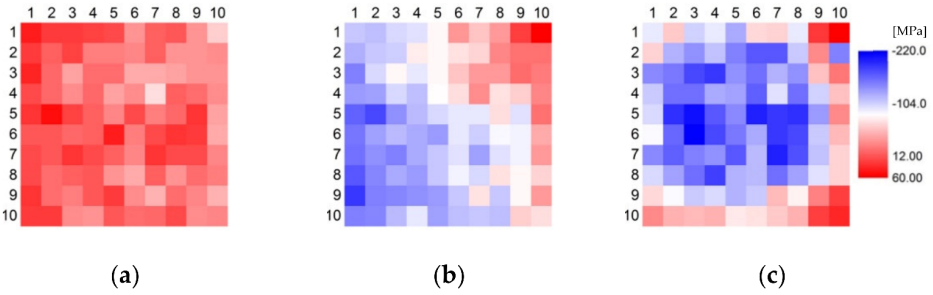


Figure 13. Stress distribution at 180 °C, on Si_Unmounted chip (**a**), A_AuSn_p sample (**b**), and A_AuSn sample (**c**).

Figures 11c, 12c and 13c show an unstable stress distribution. This can be correlated with mechanical defects after the soldering process. Cross sections of the samples confirmed the experimental results that the samples had cracks within the solder joint. An alternative method to test the integrity of the solder joint is transient thermal testing, which is a nondestructive tool [27]. It is worth also recalling that samples with cracks detected by Raman spectroscopy and confirmed by transient thermal analysis and cross section can still have functioning electric contacts, as demonstrated with high power LEDs, which passed the light-on test [28]. The Raman results of the current study suggest the high potentiality, accuracy, and precision of this optical spectroscopy to estimate the quality of samples.

These results are compared in Tables 4–6, reporting the overview of the maximum, minimum, and average values of the Raman shift and stress for each sample, at different temperatures: −50, 20, and 180 °C.

Table 4. Raman shift [cm^{-1}] and stress values [MPa] obtained for the Si_Unmounted sample.

Temperature [°C]	Maximum Value	Minimum Value	Average Value	Maximum Variation	Unit for Shift and Stress
−50	521.13 ± 0.05	521.02 ± 0.05	521.07 ± 0.05	0.11 ± 0.1	[cm^{-1}]
	27 ± 20	−28 ± 20	0 ± 1	5 ± 40	[MPa]
20	518.84 ± 0.05	518.63 ± 0.05	518.77 ± 0.05	0.21 ± 0.1	[cm^{-1}]
	71 ± 20	−36 ± 20	0 ± 2	107 ± 40	[MPa]
180	515.49 ± 0.02	515.26 ± 0.02	515.36 ± 0.02	0.23 ± 0.04	[cm^{-1}]
	52 ± 20	−63 ± 20	0 ± 2	115 ± 40	[MPa]

Table 5. Raman shift [cm^{-1}] and stress values [MPa] obtained for the A_AuSn_p sample.

Temperature [°C]	Maximum Value	Minimum Value	Average Value	Maximum Variation	Unit for Shift and Stress
−50	521.48 ± 0.05	520.78 ± 0.05	521.13 ± 0.02	0.70 ± 0.01	[cm^{-1}]
	126 ± 20	−178 ± 20	−23 ± 7	304 ± 40	[MPa]
20	518.94 ± 0.05	518.64 ± 0.05	518.77 ± 0.01	0.30 ± 0.10	[cm^{-1}]
	70 ± 20	−101 ± 20	−1 ± 4	171 ± 40	[MPa]
180	515.73 ± 0.0	515.31 ± 0.03	515.57 ± 0.01	0.42 ± 0.06	[cm^{-1}]
	70 ± 20	103 ± 20	128 ± 5	33 ± 40	[MPa]

Table 6. Raman shift [cm^{-1}] and stress values [MPa] obtained for the A_AuSn sample.

Temperature [°C]	Maximum Value	Minimum Value	Average Value	Maximum Variation	Unit for Shift and Stress
−50	523.2 ± 0.05	520.61 ± 0.05	522.31 ± 0.05	2.59 ± 0.01	[cm^{-1}]
	200 ± 20	−928 ± 20	−535 ± 30	1128 ± 40	[MPa]
20	520.51 ± 0.05	518.63 ± 0.04	519.85 ± 0.05	1.88 ± 0.09	[cm^{-1}]
	28 ± 20	−747 ± 20	−471 ± 20	775 ± 40	[MPa]
180	515.86 ± 0.03	515.31 ± 0.03	515.62 ± 0.02	0.55 ± 0.06	[cm^{-1}]
	57 ± 20	−219 ± 20	−111 ± 6	276 ± 40	[MPa]

All data are reported with their respective uncertainties obtained from the Lorentzian fit of the peaks. In all tables, the highest variation in Raman shift and stress calculated on the chip surface at the three temperatures is also reported. The errors in the stress values are obtained with the quadrature propagation method.

Considering the unmounted sample (Table 4), as expected, the position of the peak does not change significantly on the surface when the temperature is constant: this reflects that the unmounted sample presents only weak stress values, randomly distributed on the area of the chip, which fall in a range slightly higher than 100 MPa. From the calculation of the uncertainties of the stress values, it emerges that the measurements show stress values

of the same order of magnitude as the calculated errors. This fact agrees with expectations: since the unmounted samples are used as zero-stress reference materials, low-stress values around zero are expected. These values represent the starting point for calculating the stress of the other samples developed during the assembly steps.

The A_AuSn_p sample (Table 5) shows higher stress variations on the whole surface at −50 °C and at room temperature, while the A_AuSn sample (Table 6) shows the highest variations at all temperatures. In A_AuSn_p, the peak positions change slightly from point to point on the diagonal, giving asymmetric stress distributions and presenting a region of compressive stress on a side area of the chip. At room temperature, the highest variation in Raman shift on the entire surface is 0.30 cm^{-1}, which is only slightly higher than that of the unmounted sample. This value corresponds to a variation in stress of 171 MPa. The situation is different with sample A_AuSn: the Raman shift and stress variations over the surface at room temperature are higher than in the other cases: they reach values of 1.88 cm^{-1} and 775 MPa, respectively. The stress distribution developed along a diagonal clearly shows the predominance of tensile stresses, higher (in absolute value) in the center of the chip. It increases (in absolute value) with decreasing temperature, particularly in the central area.

The A_AuSn sample displays only tensile stresses (negative values); meanwhile, the A_AuSn_p shows compressive stresses (positive values) at 180 °C and tensile stresses at −50 °C and at room temperature. Further measurements to check the interconnections have revealed that the assembling process was not sufficiently efficient under the pressure of 5 N, because the Si chip was not well soldered to the substrate. Therefore, the initial considerations of the phenomena of weak stress must be reconsidered. Investigations in this direction are underway to understand the effect of applied pressure on the assembly process.

Raman shift profiles at the same sample position recorded at different temperatures show a linear trend with slightly different slope values for the three samples. Therefore, it shows that the effect of temperature has different repercussions on the samples depending on their stress values. In particular, a difference in the variations in the stress values, along the diagonal, from −50 to 180 °C is found, particularly for the A_AuSn sample. At high temperatures, the stress is significantly lower than at the other temperatures. This fact can be explained by considering the assembly process and the materials involved in the process.

The residual stresses in the mounted samples are mainly due to thermal mismatch due to the different thermal expansion coefficients, reported in Table 7, of the materials involved.

Table 7. Materials properties of investigated assemblies' components [29–31].

Material	CTE [ppm/°C]	Young's Modulus (GPa)	Poisson's Ratio
Si	2.8 at 25 °C	191	0.278
AuSn	16	68	0.4
Cu	16.4 at 25 °C	131	0.35
Al_2O_3	8.1	330	0.238

The working conditions of the soldering process reach a temperature of approximately 320 °C. At this temperature, the AuSn interconnection layer is melted and is in contact with a dilated substrate and a dilated chip. During the cooling process, the materials shrink differently according to their thermal expansion coefficients, and the further we recede from the highest process temperature, the more the effect of the different thermal expansion coefficients increases, accentuating the stress on the device. In particular, since the copper substrate has a higher thermal expansion coefficient than silicon, it contracts more than the chip, causing the chip to be more susceptible to tensile stresses.

The measurement temperature of 180 °C represents a value closer to that of the soldering, which means that the materials are characterized by geometric distortions between molecules and intramolecular forces similar to what they have during the assembly process. Furthermore, at 180 °C the Si atoms in the lattice are much more mobile and can

easily adapt to the new conditions to which the system is subjected. It results in low variations in the stress on the materials.

The pressure applied during the assembly plays a crucial role in the results: the difference in stress is clearly evident by comparing samples mounted with and without pressure and needs to be further investigated. The pressure may influence the dynamics of the interconnection layer by affecting the voids in the AuSn alloy and the compactness of the conductive layer, influencing the stress of the active layer. In any case, from these measurements it clearly emerges that Raman spectroscopy can be used as a valuable tool to understand the efficiency and quality of the interconnection process.

The results of the analysis on sample B_AuSn, consisting of a silicon chip soldered on a ceramic substrate, are reported in Table 8. They suggest a lower Raman signal shift along the sample surface than for the same sample assembled on a copper substrate. This result can be easily explained by considering the thermal effect: comparing the mismatch of the linear thermal expansion coefficients of silicon and alumina with the mismatch between silicon and copper, it is observed that for the alumina substrate it is about half as much as for copper. This means that the thermal mismatch generates only weaker stresses.

Table 8. Raman shift [cm^{-1}] and stress values [MPa] obtained for the B_AuSn sample.

Temperature [°C]	Maximum Value	Minimum Value	Average Value	Maximum Variation	Unit for Shift and Stress
20	519.87 ± 0.04 -170 ± 20	519.18 ± 0.05 -499 ± 20	519.56 ± 0.02 -345 ± 6	0.69 ± 0.09 329 ± 30	[cm^{-1}] [MPa]

5. Conclusions

A crucial point in the realization of devices with high performance, reliability, and durability is the evaluation of the mechanical properties of the materials that make up the device itself and are necessary for its assembly. Internal stresses can deform the microstructure of the device and occasionally destroy it. The aim of this work was to investigate the stresses induced in silicon devices during the assembling process as a function of the different assembly parameters, i.e., the physical–chemical characteristics of the involved materials, temperature, and pressure.

Silicon chips soldered with AuSn alloy on copper substrates demonstrated differences in stress values and distributions, depending on the experimental parameters of the assembly process. The stress distribution observed on the assembly on the copper substrate, obtained without additional pressure, depends on the temperature: at 180 °C, no stress is observable, while at 22 °C a compressive stress is developed in the center of the assembly with a maximum value of −700 MPa, which reaches −1 GPa at −50 °C. Indeed, from corner to center, a maximum variation in the Raman band of 1.8 cm^{-1} is recorded, corresponding to a maximum stress of 900 MPa. These samples present a stress distribution with a symmetric profile with respect to the central area of the chip. In contrast, the samples assembled under pressure conditions of 5 N showed very weak stress values due to inefficient interconnections.

The silicon chip assembled on a ceramic substrate without pressure turned out to be extremely interesting. Even in the absence of pressure, the sample did not show a large shift in the Raman position indicating a low stress: it reaches in the central region a compressive stress of 329 MPa, a value that is lower if compared with the corresponding sample assembled on the copper substrate.

AuSn solder, with a eutectic temperature of 280 °C, is a very promising material for the microelectronic industry, because it shows excellent shear strength and good resistance to oxidation and corrosion. Because intensive studies are ongoing to optimize lead-free soldering, the properties of AuSn solder make it useful in high-performance optoelectronics, power electronics, MEMS sensors, and other various applications. However, Raman measurements show high stress on samples assembled with this material, and this problem

must be considered to improve the mechanical reliability of the bonded joints. Studies on sintering are ongoing as an alternative to soldering.

Supplementary Materials: The following supporting information can be downloaded at https://www.mdpi.com/article/10.3390/app13042737/s1, Table S1: Comparison between results acquired at position [6,6] of the A_AuSn sample at an increasing temperature (from −50 to 180 °C) and at a decreasing temperature (from 180 to −50 °C) temperature. FWHM: full width at half maximum.

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