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Modified Design of Two-Switch Buck-Boost Converter to Improve Power Efficiency Using Fewer Conduction Components

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Abstract: In this study, a modified design of a two-switch buck-boost (TSBB) converter is proposed to improve power efficiency using fewer conduction components, and the optimal power range is measured. The proposed TSBB converter operates in three topologies: buck, boost, and buck-boost, like the conventional TSBB converter. However, the proposed converter improves the power efficiency in the buck and buck-boost topologies by decreasing conduction loss using the diode in the switch-off section while maintaining the same number of semiconductors as that in the conventional TSBB converter. The power efficiency of the buck topology improves for the power range 10–80 W in the constant voltage (CV) and constant current (CC) modes; it increases on average by 0.75–1.36% and 0.83–2.27% in the CV and CC modes, respectively. The power efficiency of the buck-boost topology step-down improves for the 10–80 W in all modes. This increases the average by 0.73–0.99% and 3.33–4.75% in the CV and CC modes, respectively. The power efficiency of the buck-boost topology step-up increases on average by 1.65–2.00% for 10–80 W in the CV mode. In the CC mode, it increases by 2.17–2.77% on average for 10–50 W.

Keywords: converter; buck-boost converter; TSBB converter; conduction loss; switching loss; metal-oxide-semiconductor field effect transistor (MOSFET); switch; diode; voltage stress

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1. Introduction

The DC–DC converter is a power conversion device that converts the received DC voltage to a DC voltage required by the system for transferring energy to the load [1]. It is used in several electronic devices for stabilizing the operation of systems; this can range from high-power applications such as solar photovoltaics, electric vehicles, and energy storage systems to low-power applications such as laptops, mobile phones, and portable batteries [2]. DC–DC converters are becoming miniaturized, and these parts are becoming denser because of the weight reduction and miniaturization of various application products [3]. DC–DC converters require high-power conversion efficiency for the reduction of energy consumption and long life [4]. Such high power-conversion efficiency is an important factor for a high-performance high-reliability DC–DC converter [5,6].

There are three topologies for non-isolated-type DC–DC converters: buck for step-down, boost for step-up, and buck-boost for both step-down and step-up. Figure 1 shows the circuit diagrams of each topology that consists of a switch, a diode, an inductor, and a capacitor. Step-down and step-up are determined by the duty ratio (d) and wiring of the semiconductors. Table 1 summarizes the current path and gain (G) of each topology based on switch operation; these topologies of the single switch type should be selected based on the input and output voltage specifications of the system; it is difficult to switch between topologies owing to the fixed element connection. Buck-boost topology with both

step-down and step-up cannot be used in applications that require an output voltage of the same polarity as the input voltage because the polarity of the output voltage is opposite to that of the input voltage. Moreover, the power conversion efficiency decreases compared to that of other topologies because the voltage stress of the switch and diode equals the sum of the input voltage V_i and output voltage V_o. Therefore, the TSBB converter that can switch to a different topology based on system requirements is used frequently [7–10].

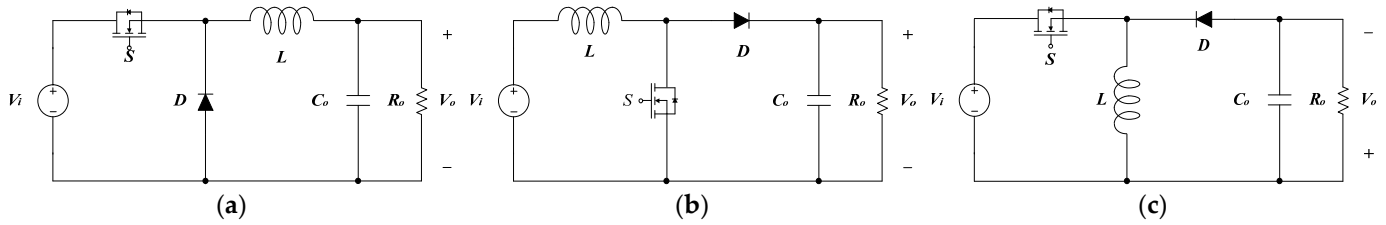

Figure 1. Circuit diagram: (**a**) buck; (**b**) boost; (**c**) buck-boost.

Table 1. Current path and gain in topologies.

Topology	Current Path		Gain (G)
	Switch ON	Switch OFF	
Buck	V_i-S-L-C_o	L-C_o-D	d
Boost	V_i-L-S	V_i-L-D-C_o	$1/(1-d)$
Buck-Boost	V_i-S-L	L-C_o-D	$d/(1-d)$

Figure 2 shows a circuit diagram of a conventional TSBB converter that comprises two switches, two diodes, an inductor, and a capacitor. This TSBB converter operates in the buck, boost, or buck-boost topology based on the operation of the switch [5–7]. Table 2 summarizes the switching operations of the conventional TSBB converter; it operates in the buck topology by the on/off switching of S_1 while S_2 is always off, and in boost topology by the on/off switching of S_2 while S_1 is always on. Further, the TSBB converter operates in the buck-boost topology by the on/off switching of both S_1 and S_2. It is easy to change the topology despite the increase in parts; the output voltage has the same polarity as the input in the buck-boost topology. Moreover, it is easy to select semiconductors because the voltage stress of the parts does not exceed the input voltage V_i and output voltage V_o [9–13].

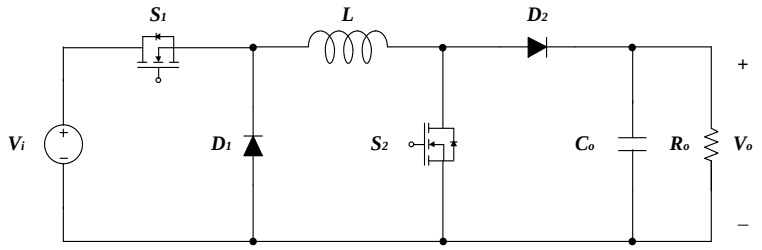

Figure 2. Circuit diagram of the conventional TSBB converter.

Table 3 presents the switching and conduction semiconductors in each topology of a single switch converter and a TSBB converter. The TSBB converter uses more parts than the single switch converter in each topology owing to the composition and wiring of the semiconductors; this increases the power loss and lowers the power efficiency. The loss of the TSBB converter increases because of the amount of the conduction loss of one diode than the single switch type in the buck topology and the amount of the conduction loss of one switch in the boost topology. Moreover, the power efficiency in the buck-boost topology decreases owing to the switching and conduction losses of one switch and one diode [5,6,10].

Table 2. Switch operation of the conventional TSBB converter.

Topology	Period	Component			
		S_1	S_2	D_1	D_2
Buck	Switch ON Switch OFF	ON OFF	Always OFF	OFF ON	Always ON
Boost	Switch ON Switch OFF	Always ON	ON OFF	Always OFF	OFF ON
Buck-Boost	Switch ON Switch OFF	ON OFF	ON OFF	OFF ON	OFF ON

Table 3. Switching and conduction semiconductors of single switch converters and the conventional TSBB converter.

Topology	Single Switch Type				Conventional TSBB			
	Switch ON		Switch OFF		Switch ON		Switch OFF	
	Switching	Conduction	Switching	Conduction	Switching	Conduction	Switching	Conduction
Buck	S	S	D	D	S_1	S_1, D_2	D_1	D_1, D_2
Boost	S	S	D	D	S_2	S_1, S_2	D_2	S_1, D_2
Buck-Boost	S	S	D	D	S_1, S_2	S_1, S_2	D_1, D_2	D_1, D_2

New circuits are suggested in [5,6] to prevent such a decrease in power efficiency. They demonstrated that power efficiency can be increased compared to those of the conventional TSBB converter by reducing the number of switching and conduction semiconductors in the current path. However, there is a trade-off between the number of semiconductors in the current path and the voltage stress. Therefore, in the new circuits of [5,6], the voltage stress of the semiconductors in the boost and buck-boost topologies increases, and it will lower power efficiency above a specific power range. The experimental results confirm the efficiency based on changes in the output current; however, it is difficult to find the optimal power range according to the changes in the input voltage and duty that influence the voltage stress of the semiconductors. To solve this problem, this study proposed a new type of TSBB converter for improving power efficiency and analyzing the optimal power range that can improve power efficiency. The proposed TSBB converter can increase power efficiency in buck and buck-boost topologies by reducing conduction loss caused by the diode in the switch-off section while using the same number of semiconductors as that of the conventional TSBB converter. Moreover, the optimal power range of each topology is analyzed by evaluating the effect of an increase in the voltage stress of semiconductors.

The contributions of this study are as follows:

- We investigated related research about the TSBB converter and proposed a modified design of the TSBB converter to improve power efficiency using fewer conduction components in the current path.
- We presented the optimal power range according to the buck, boost, and buck-boost topologies in CV and CC modes, and, in particular, divided into step-up/step-down sections in the buck-boost topology.
- We analyzed the power dissipation of the three topologies and explained why the CC mode of the buck-boost step-up is less efficient than conventional converters over a certain power range through analytic and experimental diode stress analysis.

The remainder of this paper is organized as follows. Section 2 describes the operation principle of the proposed TSBB converter. In Section 3, the power loss is compared between the proposed TSBB converter and the conventional TSBB converter in each topology by analyzing the switching and conduction losses. The experiment results are described in Section 4, and, finally, the conclusions are presented in Section 5.

2. Operation Principle

Figure 3 shows the circuit diagram of the proposed TSBB converter. Like the conventional TSBB converter, the proposed TSBB converter is composed of two switches, two diodes, an inductor, and a capacitor; further, it operates in three topologies based on the switching of S_1 and S_2, and it operates in the buck topology by the on/off switching of S_1, in the boost topology by the switching of S_2, and in the buck-boost topology by the simultaneous on/off switching of S_1 and S_2.

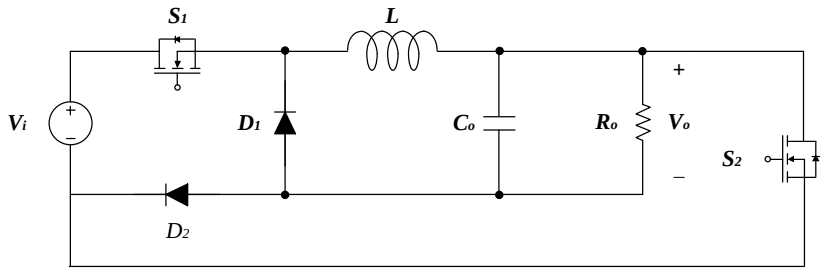

Figure 3. Circuit diagram of the proposed TSBB converter.

Table 4 summarizes the switching operations of the proposed TSBB converter. Table 4 indicates that the switching operations of S_1, S_2, and D_1 are the same as those of the conventional TSBB converter. However, D_2 performs on/off switching in the buck topology and is always off in the buck-boost topology.

Table 4. Switch operation of the proposed TSBB converter.

Topology	Period	Component			
		S_1	S_2	D_1	D_2
Buck	Switch ON Switch OFF	ON OFF	Always OFF	OFF ON	ON OFF
Boost	Switch ON Switch OFF	Always ON	ON OFF	Always OFF	OFF ON
Buck-Boost	Switch ON Switch OFF	ON OFF	ON OFF	OFF ON	Always OFF

Figure 4 presents the operation principle of the proposed TSBB converter in each topology. The switch-on/off sections are divided by the operation of the switch that transfers the energy to the inductor. The semiconductors located in the current path in each section are conduction semiconductors; the semiconductor that only operates in one of the switch-on/off sections is the switching semiconductor. Table 5 compares the switching and conduction semiconductors between the conventional and proposed TSBB converters. In comparison with the conventional TSBB converter, the proposed TSBB converter undergoes an increase in the switching loss of D_2 in the switch-on section and a decrease in the conduction loss of D_2 in the switch-off section. In the buck-boost topology, the switching and conduction losses of D_2 in the switch-off section decrease. Table 6 compares the stress between the conventional and proposed TSBB converters; they have the almost same voltage stress in buck and boost topologies, but in the buck-boost topology, the stress of D_1 increases to $V_i + V_o$.

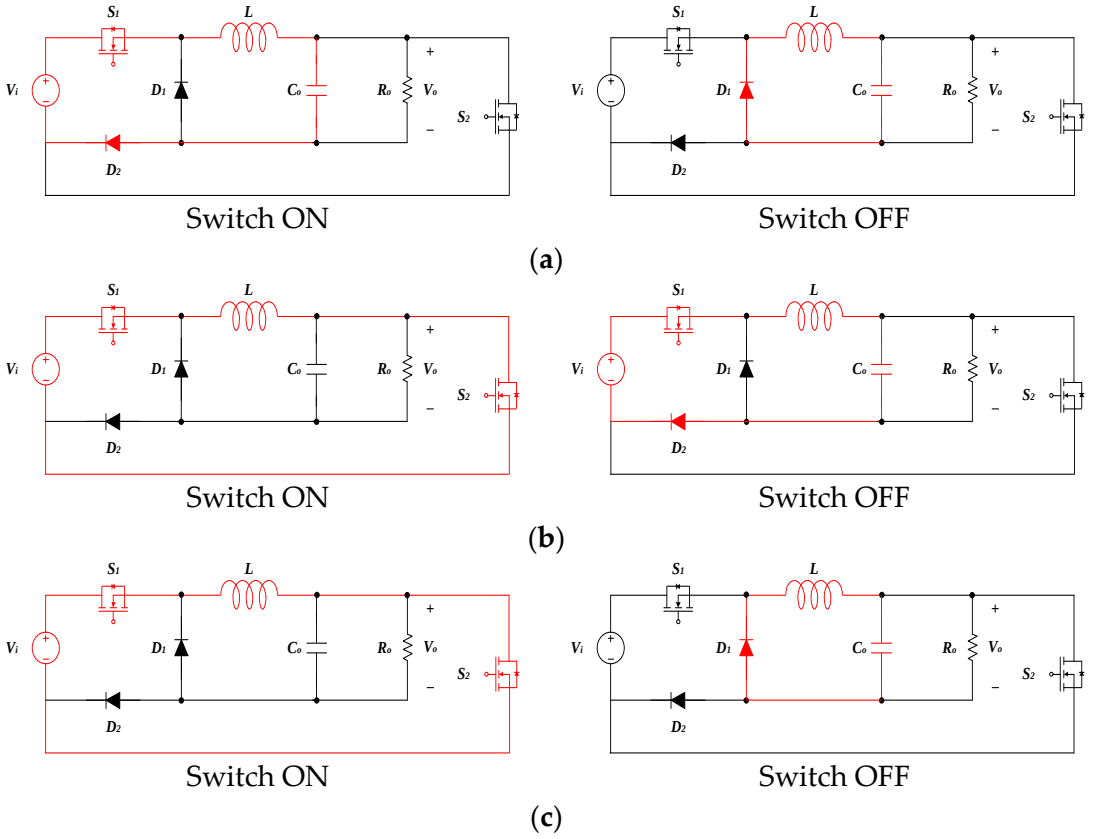

Figure 4. Operation principle of the proposed TSBB converter: (**a**) Buck; (**b**) Boost; (**c**) Buck-boost.

Table 5. Switching and conduction semiconductors of the conventional and proposed TSBB converters: (a) Switching semiconductors; (b) Conduction semiconductors.

Topology	Gain	Conventional		Ref. [5]		Proposed	
		Switch ON	Switch OFF	Switch ON	Switch OFF	Switch ON	Switch OFF
Buck	d	S_1	D_1	S_1, D_2	D_1	S_1, D_2	D_1
Boost	$1/(1-d)$	S_2	D_2	S_2	D_2	S_2	D_2
Buck-Boost	$d/(1-d)$	S_1, S_2	D_1, D_2	S_2	D_1	S_1, S_2	D_1

(a)

Topology	Gain	Conventional		Ref. [5]		Proposed	
		Switch ON	Switch OFF	Switch ON	Switch OFF	Switch ON	Switch OFF
Buck	d	S_1, D_2	D_1, D_2	S_1, D_2	D_1	S_1, D_2	D_1
Boost	$1/(1-d)$	S_1, S_2	S_1, D_2	S_2	S_1, D_2	S_1, S_2	S_1, D_2
Buck-Boost	$d/(1-d)$	S_1, S_2	D_1, D_2	S_2	D_1	S_1, S_2	D_1

(b)

Table 6. Comparison of stress in each TSBB converter: (a) Voltage stress; (b) Current stress.

Topology	Conventional			
	S_1	S_2	D_1	D_2
Buck	V_i	-	V_i	-
Boost	-	V_o	-	V_o
Buck-Boost	V_i	V_o	V_i	V_o

Table 6. *Cont.*

Topology	Ref. [5]			
	S_1	**S_2**	**D_1**	**D_2**
Buck	$\frac{C_{oss,D2}}{C_{oss,S1}+C_{oss,D2}}V_i$	-	V_i	$\frac{C_{oss,S1}}{C_{oss,S1}+C_{oss,D2}}V_i$
Boost	-	V_o	-	$\frac{C_{oss,S1}}{C_{oss,S1}+C_{oss,D2}}V_o$
Buck-Boost	$\frac{C_{oss,D2}}{C_{oss,S1}+C_{oss,D2}}V_i$ or $\frac{C_{oss,D2}}{C_{oss,S1}+C_{oss,D2}}V_o$	V_i+V_o	V_i+V_o	$\frac{C_{oss,S1}}{C_{oss,S1}+C_{oss,D2}}V_i$ or $\frac{C_{oss,S1}}{C_{oss,S1}+C_{oss,D2}}V_o$
Topology	**Proposed**			
	S_1	**S_2**	**D_1**	**D_2**
Buck	$\frac{C_{oss,D2}}{C_{oss,S1}+C_{oss,D2}}V_i(\cong V_i)$	-	V_i	$\frac{C_{oss,S1}}{C_{oss,S1}+C_{oss,D2}}V_i(\cong 0)$
Boost	-	V_o	-	V_o
Buck-Boost	$\frac{C_{oss,D2}}{C_{oss,S1}+C_{oss,D2}}V_i(\cong V_i)$	$\frac{C_{oss,D2}}{C_{oss,S2}+C_{oss,D2}}V_o(\cong V_o)$	V_i+V_o	-
(a)				
Topology	**Conventional/Proposed**			
	S_1	**S_2**	**D_1**	**D_2**
Buck	$V_o\left(\frac{1}{R^1}+\frac{1-d}{2L\cdot f_{sw}}\right)$	-	$V_o\left(\frac{1}{R^1}+\frac{1-d}{2L\cdot f_{sw}}\right)$	$V_o\left(\frac{1}{R^1}+\frac{1-d}{2L\cdot f_{sw}}\right)$
Boost	-	$V_i\left[\frac{1}{(1-d)^2\cdot R^1}+\frac{d}{2L\cdot f_{sw}}\right]$	-	$V_i\left[\frac{1}{(1-d)^2\cdot R^1}+\frac{d}{2L\cdot f_{sw}}\right]$
Buck-Boost	$V_i\left[\frac{d}{(1-d)^2\cdot R^1}+\frac{d}{2L\cdot f_{sw}}\right]$	$V_i\left[\frac{d}{(1-d)^2\cdot R^1}+\frac{d}{2L\cdot f_{sw}}\right]$	$V_i\left[\frac{d}{(1-d)^2\cdot R^1}+\frac{d}{2L\cdot f_{sw}}\right]$	-
(b)				

[1] Output resistance.

3. Analysis of Semiconductor Power Loss

The power loss of a TSBB converter includes the losses of the switch, diode, inductor, and capacitor when various parasitic components in the circuit are ignored. The power loss of the two converters is determined by the power loss of the semiconductors assuming that the losses of the inductor and capacitor are the same between the conventional and proposed TSBB converters. Therefore, the increase or decrease in power efficiency is determined by the operation of the switch and diode.

3.1. Switch and Diode Current

Figure 5 presents the switch and diode current of the proposed TSBB converter in each topology. In the buck topology, the inductor current flows through S_1 and D_2 during the switch-on section and through D_1 during the switch-off section. The inductor current I_L is the output current I_o and $\Delta I_L = \frac{V_o(1-d)}{L\cdot f_{sw}}$ by the volt-sec balance law at switching frequency f_{sw}, the inductor current I_{max}, I_{min} flowing through switch S_1 and diode D_1/D_2 can be expressed as:

$$I_{max} = I_o + \frac{\Delta I_L}{2} = V_o\left(\frac{1}{R} + \frac{1-d}{2L\cdot f_{sw}}\right) \quad (1)$$

$$I_{min} = I_o - \frac{\Delta I_L}{2} = V_o\left(\frac{1}{R} - \frac{1-d}{2L\cdot f_{sw}}\right) \quad (2)$$

The inductor current flows through S_1 and D_2 during the switch-on section and through D_1 during the switch-off section in the boost topology. Since the inductor current

I_L is $\frac{I_o}{1-d}$ and $\Delta I_L = \frac{d \cdot V_i}{L \cdot f_{sw}}$, the inductor current I_{max}, I_{min} flowing through switch S_1/S_2 and diode D_2 can be expressed as:

$$I_{max} = I_o + \frac{\Delta I_L}{2} = V_i \left[\frac{1}{(1-d)^2 \cdot R} + \frac{d}{2L \cdot f_{sw}} \right] \tag{3}$$

$$I_{min} = I_o - \frac{\Delta I_L}{2} = V_i \left[\frac{1}{(1-d)^2 \cdot R} - \frac{d}{2L \cdot f_{sw}} \right] \tag{4}$$

In buck-boost topology, the inductor current flows through S_1 and D_2 during the switch-on section and through D_1 during the switch-off section. Since the inductor current $I_L = \frac{I_o}{1-d}$ and $\Delta I_L = \frac{d \cdot V_i}{L \cdot f_{sw}}$ same as boost topology, the inductor current I_{max}, I_{min} flowing through switch S_1/S_2 and diode D_2 can be expressed as:

$$I_{max} = I_o + \frac{\Delta I_L}{2} = V_i \left[\frac{d}{(1-d)^2 \cdot R^1} + \frac{d}{2L \cdot f_{sw}} \right] \tag{5}$$

$$I_{min} = I_o - \frac{\Delta I_L}{2} = V_i \left[\frac{d}{(1-d)^2 \cdot R^1} + \frac{d}{2L \cdot f_{sw}} \right] \tag{6}$$

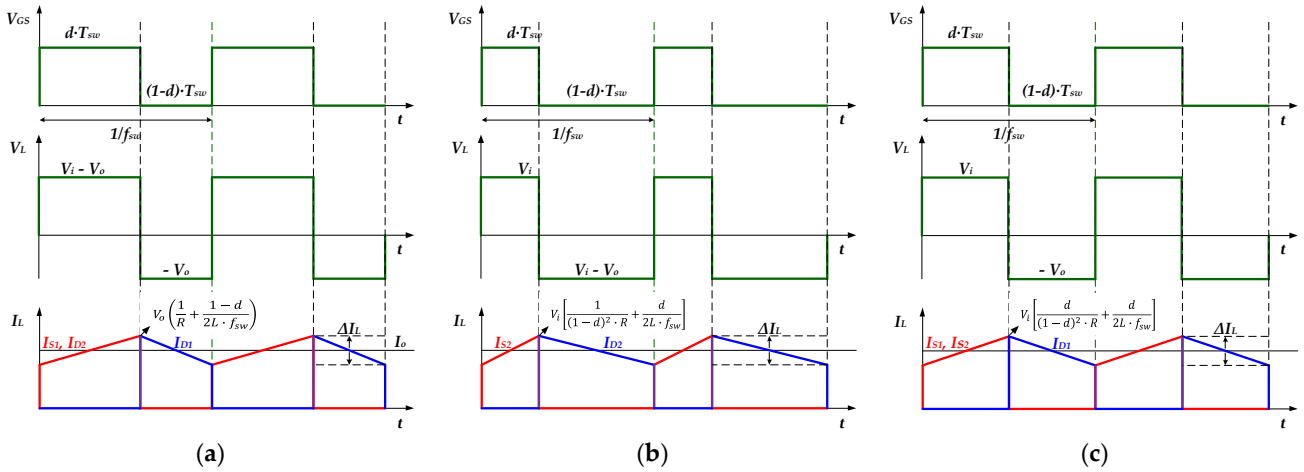

Figure 5. Switch and diode current of the proposed TSBB converter: (**a**) Buck; (**b**) Boost; (**c**) Buck-boost.

The power loss of a TSBB converter includes the losses of the switch, diode, inductor, and capacitor when various parasitic components in the circuit are ignored. The power loss of the two converters is determined by the power loss of the semiconductors assuming that the losses of the inductor and capacitor are the same between the conventional and proposed TSBB converters. Therefore, the increase or decrease in the power efficiency is determined by the operation of the switch and diode.

The losses of semiconductors are divided into switching and conduction losses. A switching loss occurs during the transient time of the switching operation. Although the switching loss is 0 in the ideal condition, it is caused by the time delay attributed to the parasitic resistance and parasitic capacitance at the time of turn-on or turn-off [14,15]. The conduction loss is caused by the current that flows by the turn-on of the semiconductor and on the resistance of the semiconductor [16–18].

3.2. Switching Loss

The switching loss of MOSFET, $P_{S,SW}$ is divided into switch turn-on loss, $P_{S,SW,ON}$ switch turn-off loss $P_{S,SW,OFF}$, and output capacitance loss $P_{S,SW,Coss}$ as [5,15,17]:

$$P_{S,SW} = P_{S,SW,ON} + P_{S,SW,OFF} + P_{S,SW,Coss} \tag{7}$$

The switch turn-on and turn-off losses are difficult to calculate because of the nonlinear characteristics of the drain-source voltage v_{DS} and drain current i_D. Therefore, they can be determined by applying linear approximation in the rising and falling sections of v_{DS} and i_D. The output capacitance loss of MOSFET can be determined by calculating the stored energy of the capacitor because the energy is charged in the output capacitance when the MOSFET turns off, and is discharged when the MOSFET turns on. The MOSFET switching loss can be represented by using the turn-on time t_{on}, turn-off time t_{off}, switching frequency f_{sw}, and output capacitance C_{oss} of the MOSFET as [5,17,18]:

$$\begin{aligned} P_{S,SW} &= \tfrac{1}{2}\cdot v_{DS}\cdot i_D\cdot t_{on}\cdot f_{sw} + \tfrac{1}{2}\cdot v_{DS}\cdot i_D\cdot t_{off}\cdot f_{sw} + \tfrac{1}{2}\cdot C_{oss}\cdot {v_{DS}}^2\cdot f_{sw} \\ &= \tfrac{1}{2}\cdot v_{DS}\cdot i_D\cdot (t_{on} + t_{off})\cdot f_{sw} + \tfrac{1}{2}\cdot C_{oss}\cdot {v_{DS}}^2\cdot f_{sw} \end{aligned} \tag{8}$$

The output capacitance of the MOSFET is several tens to hundreds of picofarads. Therefore, it is negligible compared to the switch turn-on and turn-off losses and can be represented as [5,6,17,18]:

$$P_{S,SW} = \frac{1}{2}\cdot v_{DS}\cdot i_D\cdot (t_{on} + t_{off})\cdot f_{sw} \tag{9}$$

The switching loss $P_{D,SW}$ of the diode can be divided into the switch turn-on loss $P_{D,SW,ON}$ and the switch turn-off loss $P_{D,SW,OFF}$ it is represented as:

$$P_{D,SW} = P_{D,SW,ON} + P_{D,SW,OFF} \cong P_{D,SW,OFF} \tag{10}$$

The switching loss of the diode can be approximated as the switch turn-off loss because the loss of the diode caused by the reverse recovery in the turn-off section is considerably larger than the turn-on loss [19,20].

Figure 6 shows the reverse recovery characteristic of the diode [6]. In an ideal diode, the current flows when the voltage is applied in the forward direction, and no current flows when the voltage is applied in the reverse direction. However, in an actual operation, the reverse current flows for a certain time before it reaches zero when the diode is turned off after a forward current flow. Here, the time during which the reverse current flows is referred to as the reverse recovery time (t_{rr}); the maximum value of the reverse current that flows in the diode is referred to as the repetitive peak reverse current (I_{RRM}). The turn-off loss $P_{D,SW,OFF}$ of the diode when the reverse voltage applied to the diode is V_R and the switching frequency is f_{sw} can be expressed as [21,22]:

$$P_{D,SW} = \frac{1}{2}\cdot V_R\cdot I_{RRM}\cdot t_{rr}\cdot f_{sw} \tag{11}$$

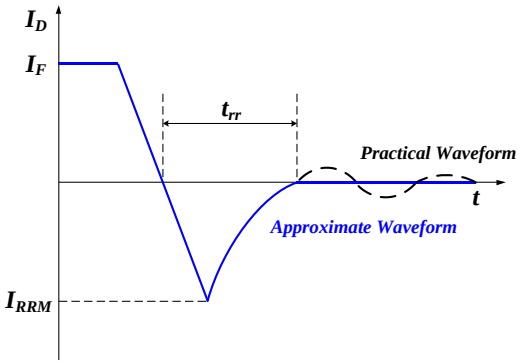

Figure 6. Diode reverse recovery characteristics.

3.3. Conduction Loss

The instantaneous value of the conduction loss of the MOSFET, $P_{S,CD}(t)$ can be expressed by $v_{DS}(t)$, $i_D(t)$, and the drain-source resistance $R_{DS(ON)}$ in the complete switch turn-off section as [6,15,16,19]:

$$P_{S,CD}(t) = v_{DS}(t) \cdot i_D(t) = {i_D}^2(t) \cdot R_{DS(ON)} \tag{12}$$

The average value can be determined by integrating Equation (6) over the switching period T_{sw} as:

$$P_{S,CD}(t) = \frac{1}{T_{sw}} \int_0^{T_{sw}} {i_D}^2(t) \cdot R_{DS(ON)} \, dt \tag{13}$$

$$P_{S,CD} = {I_{D(rms)}}^2 \cdot R_{DS(ON)} \tag{14}$$

The instantaneous value of the conduction loss of the diode $P_{D,CD}(t)$ can be expressed by the forward voltage drop $v_F(t)$, forward current $i_F(t)$, and diode resistance R_D as [5,6]:

$$P_{D,CD}(t) = v_F(t) \cdot i_F(t) + R_D \cdot {i_F}^2(t) \tag{15}$$

The average value can be determined by integrating Equation (8) over the switching period T_{sw} as [5,12,15]:

$$P_{D,CD}(t) = \frac{1}{T_{sw}} \int_0^{T_{SW}} \left\{ v_F(t) \cdot i_F(t) + R_D \cdot {i_F}^2(t) \right\} dt \tag{16}$$

$$P_{D,CD} = V_F \cdot I_{F(AVG)} + R_D \cdot {I_{F(RMS)}}^2 \tag{17}$$

4. Analysis of Power Loss in Topologies

Table 5 summarizes the switching and conduction semiconductors of the conventional and proposed TSBB converters in each topology. Table 6 presents the voltage and current stresses of the conventional and proposed TSBB converters in each topology. In each topology, the switching loss that has reflected the voltage stress and conduction loss based on the switch on/off time can be determined and compared.

4.1. Buck Topology

In Table 5, the switching semiconductors of the conventional TSBB converter are S_1/D_1, and the conducting semiconductors are $S_1/D_1/D_2$. Thus, the switching loss $P_{CON,SW}$ and conduction loss $P_{CON,CD}$ can be expressed, respectively, as:

$$P_{CON,SW} = P_{SW,S1} + P_{SW,D1} \tag{18}$$

$$P_{CON,CD} = P_{CD,S1,ON} + P_{CD,D2,ON} + P_{CD,D1,OFF} + P_{CD,D2,OFF} \tag{19}$$

The switching semiconductors of the proposed TSBB converter are $S_1/D_1/D_2$, and those of the conducting semiconductor are $S_1/D_1/D_2$. Therefore, the switching loss $P_{PRO,SW}$ and conduction loss $P_{PRO,CD}$ can be expressed as:

$$P_{PRO,SW} = P_{SW,S1}\left(\frac{C_{oss,D2}}{C_{oss,S1} + C_{oss,D2}} V_i\right) + P_{SW,D1}(V_i) + P_{SW,D2}\left(\frac{C_{oss,S1}}{C_{oss,S1} + C_{oss,D2}} V_i\right) \tag{20}$$

$$P_{PRO,CD} = P_{CD,S1,ON} + P_{CD,D2,ON} + P_{CD,D1,OFF} \tag{21}$$

The switching loss varies by the voltage stress; however, the internal voltage of semiconductors is V_i for both the conventional and proposed TSBB converters. Consequently,

the switching losses of the semiconductors are the same. Therefore, the difference in power loss between the two converters can be expressed as:

$$P_{CON} - P_{PRO} = P_{CD,D2,OFF} - P_{SW,D2}\left(\frac{C_{oss,S1}}{C_{oss,S1} + C_{oss,D2}} V_i\right) \tag{22}$$

This difference can be determined by the conduction and switching losses in the switch-off section of D_2. Since the switch-off section is $(1-d)\cdot T_{SW}$, the lower the duty ratio, the higher the efficiency of the proposed TSBB converter.

4.2. Boost Topology

In the boost topology, the switching semiconductors are S_2/D_2, and the conducting semiconductors are $S_1/S_2/D_2$. Thus, the switching loss $P_{CON,SW}$ $(= P_{PRO,SW})$ and the conduction loss $P_{CON,CD}$ $(= P_{PRO,CD})$ can be expressed as:

$$P_{CON,SW} = P_{PRO,SW} = P_{SW,S2} + P_{SW,D2} \tag{23}$$

$$P_{CON,CD} = P_{PRO,CD} = P_{CD,S1,ON} + P_{CD,S2,ON} + P_{CD,S1,OFF} + P_{CD,D2,OFF} \tag{24}$$

There is no difference in the efficiency between the conventional and proposed TSBB converters because there is no change in the operation of semiconductors.

4.3. Buck-Boost Topology

In Table 5, both the switching and conducting semiconductors of the conventional TSBB converter are $S_1/S_2/D_1/D_2$. Therefore, the switching loss $P_{CON,SW}$ and conduction loss $P_{CON,CD}$ can be expressed as:

$$P_{CON,SW} = P_{SW,S1}(V_i) + P_{SW,S2}\,(V_o) + P_{SW,D1}(V_i) + P_{SW,D2}(V_o) \tag{25}$$

$$P_{CON,CD} = P_{CD,S1,ON} + P_{CD,S2,ON} + P_{CD,D1,OFF} + P_{CD,D2,OFF} \tag{26}$$

Both the switching and conducting semiconductors of the proposed TSBB converter are $S_1/S_2/D_1$. Therefore, the switching loss $P_{PRO,SW}$ and conduction loss $P_{PRO,CD}$ can be, respectively, expressed as:

$$\begin{aligned} P_{PRO,SW} = {} & P_{SW,S1}\left(\frac{C_{oss,D2}}{C_{oss,S1}+C_{oss,D2}} V_i\right) + P_{SW,S2}\left(\frac{C_{oss,D2}}{C_{oss,S2}+C_{oss,D2}} V_o\right) \\ & + P_{SW,D1}(V_i + V_o) \end{aligned} \tag{27}$$

$$P_{PRO,CD} = P_{CD,S1,ON} + P_{CD,S2,ON} + P_{CD,D1,OFF} \tag{28}$$

The voltage stress of each semiconductor is indicated in parentheses since the switching loss varies by the voltage stress. The loss difference between the conventional and proposed TSBB converters is determined by the switching loss of D_1/D_2 and the conduction loss of D_2 in the switch-off section, and it can be expressed as:

$$P_{CON} - P_{PRO} = P_{SW,D1}(V_i) + P_{SW,D2}(V_o) + P_{CD,D2,OFF} - P_{SW,D1}(V_i + V_o) \tag{29}$$

There are no switching and conduction losses by D_2 because the proposed TSBB converter D_2 does not operate. However, the voltage stress of D_1 increases to $V_i + V_o$, the voltage stress and reverse current of the diode in a linear section are $P_{SW,D1}(V_i) + P_{SW,D2}(V_o) \cong P_{SW,D1}(V_i + V_o)$. Therefore, the loss is determined by the conduction loss of the switch-off section of D_2. The power efficiency of the proposed TSBB converter is higher than that of the conventional TSBB converter. In contrast, the switching loss by D_1, $P_{SW,D1}(V_i + V_o)$, increases in the section where the reverse current of the diode increases sharply owing to the voltage stress. Therefore, the power efficiency of the proposed TSBB converter is lower than that of the conventional TSBB converter.

5. Experimental Results

Figure 7 shows a prototype of a 100 W TSBB converter fabricated to verify the improved power efficiency. The Arduino controller generates a 5 V pulse width modulation (PWM) to control the MOSFET driver IC input; upon receiving this signal, the MOSFET driver IC converts it to an 18 V drive signal and transfers it to the gate of the MOSFET. The specifications of the components are 20% or more larger than the calculated maximum stress considering the various input/output conditions of the experiment. Table 7 summarizes the detailed specifications of the components; Table 8 presents the maximum values of the voltage stress measured in the CV/CC modes.

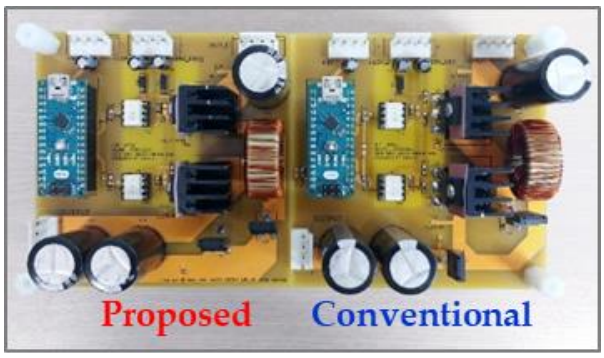

Figure 7. 100 W TSBB prototype.

Table 7. Components specifications.

Component	Part Name	Specification
PWM Generator	Arduino Nano	5 V, 16 MHz
MOSFET Driver	HCPL-J312	Output Peak Current = 2.5 A, Input Current = 7–16 mA Supply Voltage = 15–30 V, Input Capacitance = 60 pF Rise Time = 0.1 us, Fall Time = 0.1 us
MOSFET	RCX510N25	Drain-Source Voltage V_{DSS} = 250 V Gate-Source Voltage V_{GSS} = ±30 V Drain Current I_D = 51 A Static Drain-Source ON-State Resistance = 48 mΩ Output Capacitance = 350 pF Rise Time = 300 ns, Fall Time = 210 ns
Diode	RF2001T3D	Reverse voltage (DC) V_R = 300 V Forward voltage V_F = 1.3 V (at I_F = 10 A) Average Rectified Forward Current I_F = 20 A Reverse recovery time t_{rr} = 25 ns (at I_F = 0.5 A, I_R = 1 A, I_{rr} = 0.25 × I_R)
Inductor	CH270125	Cross Section = 0.654 cm^2, Path Length = 6.35 cm Window Area = 1.56 cm^2, Volume = 4.154 cm^3 AL Value = 157 nH/$Turn^2$, Permeability μ = 125 Inductance = 250 uH
Electrolytic Capacitor	100YXG820MEFC18 × 40	Rated Voltage (V_{dc}) = 100 V Rated ripple current = 2330 mA (at 100 kHz) Leakage Current = 3 μA, Impedance = 20 °C, 100 kHz Dissipation Factor(MAX) tanδ = 0.08 Capacitance = 820 uF

The experiments are conducted in the CV/CC modes of the three topologies. The experiment for the buck-boost topology is conducted separately for the step-down and step-up sections. In the CV mode, the power efficiency is measured for the output power range of 10–80 W at the switching frequency f_{sw} = 100 kHz of the output current. The

power efficiency was measured at three duty ratios to analyze the power efficiency based on the change in the duty ratio. If the input/output voltage variation ratio V_{var} is defined as the ratio of the difference between the input and output voltages to the input voltage, it can be expressed using the input voltage V_i and the output voltage V_o as:

$$V_{var}\ (\%) = \frac{|V_i - V_o|}{V_i} \times 100 \tag{30}$$

In each topology, the power efficiency was measured at the duty ratios where V_{var} was 25%, 33%, and 50%. Table 9 shows the duty ratio based on V_{var} in each topology. Figure 8a–d shows PWM waveforms of the conventional and the proposed TSBB converter in each topology implemented using Arduino Nano. Figure 8e–h presents waveforms of the inductor current, the gate-source voltage, and the output voltage of the conventional and proposed TSBB converters measured in CC mode at V_{var} = 33% (V_o ≅40 V).

Table 8. Measured maximum voltage stresses on components in CV and CC modes.

V_{var}	Device	CV								CC							
		Conventional (V_{max})				Proposed (V_{max})				Conventional (V_{max})				Proposed (V_{max})			
		Buck	Boost	Buck-Boost		Buck	Boost	Buck-Boost		Buck	Boost	Buck-Boost		Buck	Boost	Buck-Boost	
				Step-Down	Step-Up			Step-Down	Step-Up			Step-Down	Step-Up			Step-Down	Step-Up
25%	S_1	53.3	-	53.3	32.0	53.3	-	53.3	32.0	80.0	-	80.0	80.0	80.0	-	80.0	80.0
	S_2	-	41.3	46.0	45.5	-	41.6	47.5	46.8	-	104.5	67.2	114.8	-	105.2	68.9	116.9
	D_1	53.3	-	53.3	32.0	53.3	-	100.8	78.8	80.0	-	80.0	80.0	80.0	-	148.9	196.9
	D_2	-	41.3	46.0	45.5	-	41.6	-	-	-	104.5	67.2	114.8	-	105.2	-	-
33%	S_1	60.0	-	60.0	30.0	60.0	-	60.0	30.0	80.0	-	80.0	80.0	80.0	-	80.0	80.0
	S_2	-	41.3	45.9	44.9	-	41.7	47.5	46.3	-	111.9	59.0	121.0	-	112.0	60.5	123.0
	D_1	60.0	-	60.0	30.0	60.0	-	107.5	76.3	80.0	-	80.0	80.0	80.0	-	140.5	203.0
	D_2	-	41.3	45.9	44.9	-	41.7	-	-	-	111.9	59.0	121.0	-	112.0	-	-
50%	S_1	80.0	-	80.0	26.7	80.0	-	80.0	26.7	80.0	-	80.0	80.0	80.0	-	80.0	80.0
	S_2	-	41.8	46.3	45.5	-	41.7	47.9	46.9	-	126.5	43.2	138.5	-	127.3	44.6	141.2
	D_1	80.0	-	80.0	26.7	80.0	-	127.9	73.6	80.0	-	80.0	80.0	80.0	-	124.6	221.2
	D_2	-	41.8	46.3	45.5	-	41.7	-	-	-	126.5	43.2	138.5	-	127.3	-	-

Table 9. Duty ratio according to V_{var} in each topology.

V_{var}	Buck	Boost	Buck-Boost	
			Step-Down	Step-Up
25%	0.750	0.200	0.430	0.556
33%	0.667	0.250	0.400	0.571
50%	0.500	0.330	0.330	0.600

5.1. Buck Topology

Figure 9 shows the power efficiency of the buck topology in the CV and CC modes. If the power efficiency difference P_{Diff} is positive (+), it means efficiency improvement; if it is negative (-), it indicates an efficiency decline. The power efficiency improves in every condition from 10–80 W because of the removal of D_2 in the switch-off section in the CV and CC modes. P_{Diff} increases as the switch-off section becomes longer, i.e., when there is an increase in the duty ratio. In the same duty ratio condition, P_{Diff} decreases with an increase in the input voltage and output current. The improvement effect is large in the low-power region. The proposed converter can achieve a greater efficiency improvement effect in a region where the voltage conversion is large, and the output current is low.

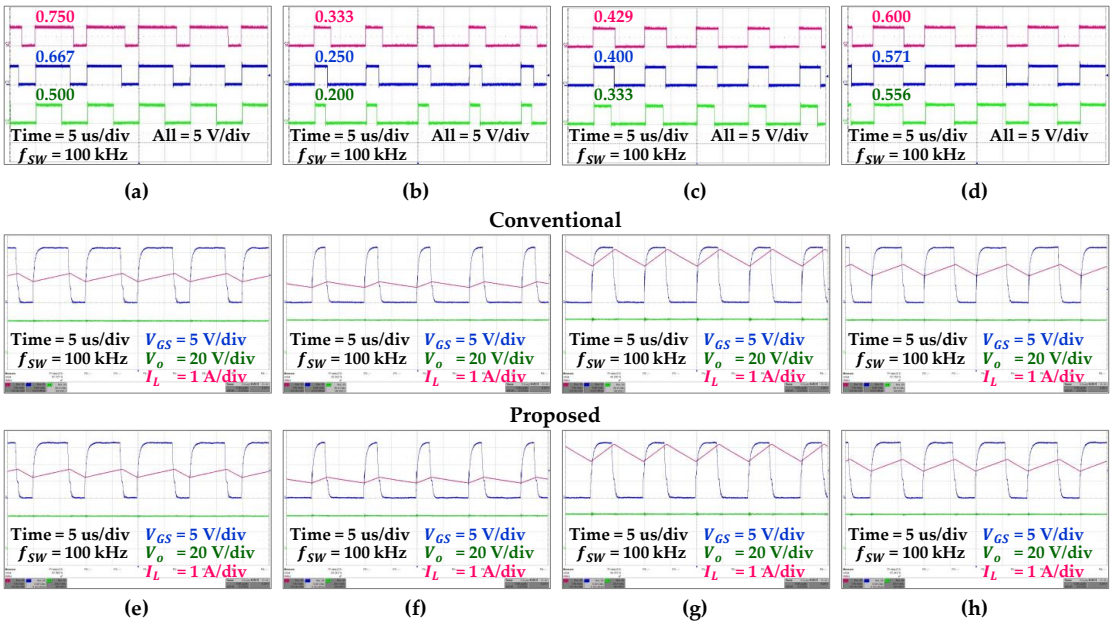

Figure 8. Waveforms of PWM, inductor current I_L, gate-source voltage V_{GS}, and output voltage V_o: PWM of (**a**) buck; (**b**) boost; (**c**) buck-boost step-down; (**d**) buck-boost step-up; I_L, V_{GS}, V_o of (**e**) buck (at d = 0.667; I_L = 1.5 A); (**f**) boost (at d = 0.250, I_L = 0.75 A); (**g**) buck-boost step-down (at d = 0.400, I_L = 1.5 A); and (**h**) buck-boost step-up (at d = 0.571, I_L = 0.75 A).

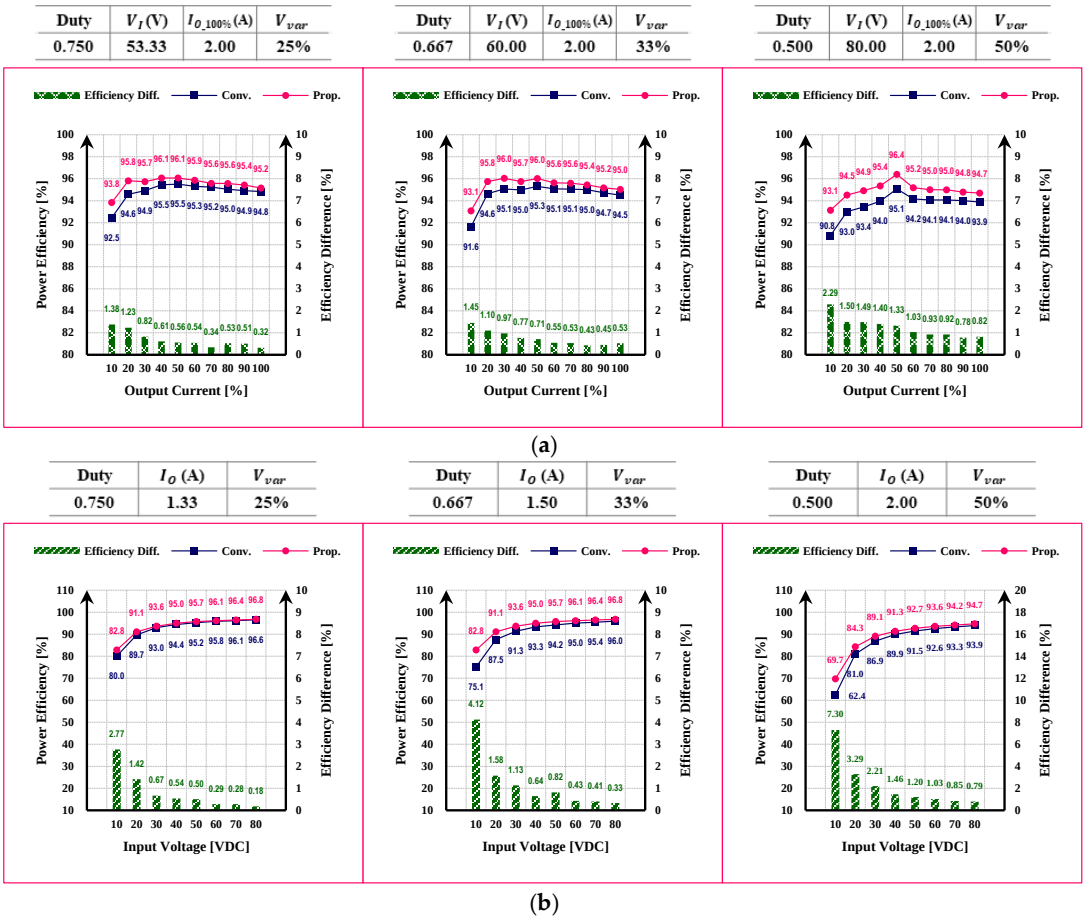

Figure 9. Power efficiency comparison of the buck topology: (**a**) CV mode; (**b**) CC mode.

5.2. Boost Topology

Figure 10 shows the power efficiency of the boost topology. The proposed converter shows the same power efficiency in the measured error range because it has the same number of semiconductors and the same stress as the conventional converter.

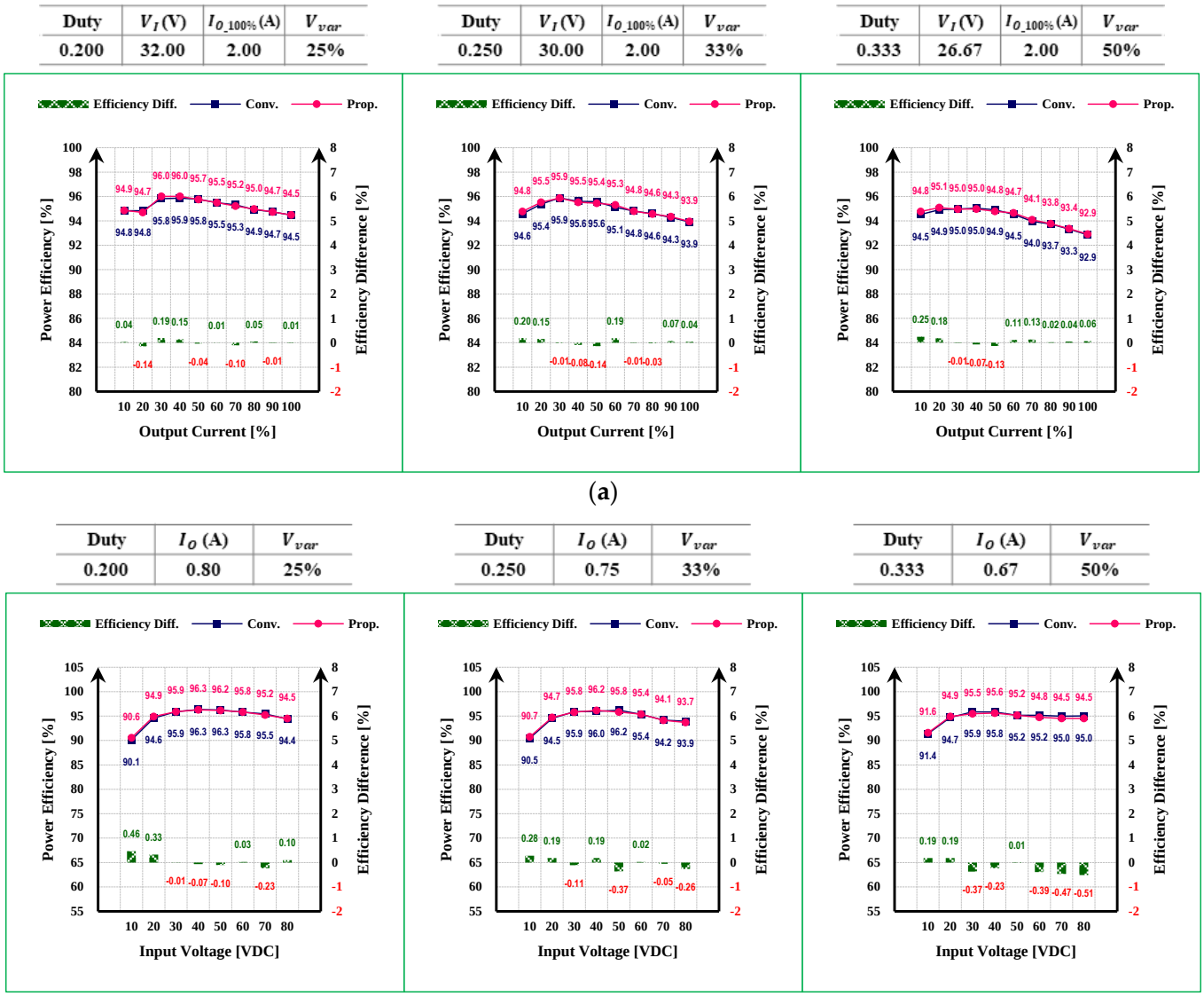

Figure 10. Power efficiency comparison of the boost topology: (**a**) CV mode; (**b**) CC mode.

5.3. Buck-Boost Topology

5.3.1. Step-Down

Figure 11 shows the power efficiency in the step-down section of the buck-boost topology in the CV and CC modes. The power efficiency is improved in every condition because of the removal of D_2 in the switch-off section. In the CV mode, the efficiency improvement becomes larger with an increase in the output current; P_{Diff} increases in the high-power region. In the CC mode, the power efficiency improves with a decrease in the input voltage, and P_{Diff} increases in the low-power region. In the same duty condition, the voltage stress of the diode D_1 increases with the input voltage; P_{Diff} decreases with an increase in loss.

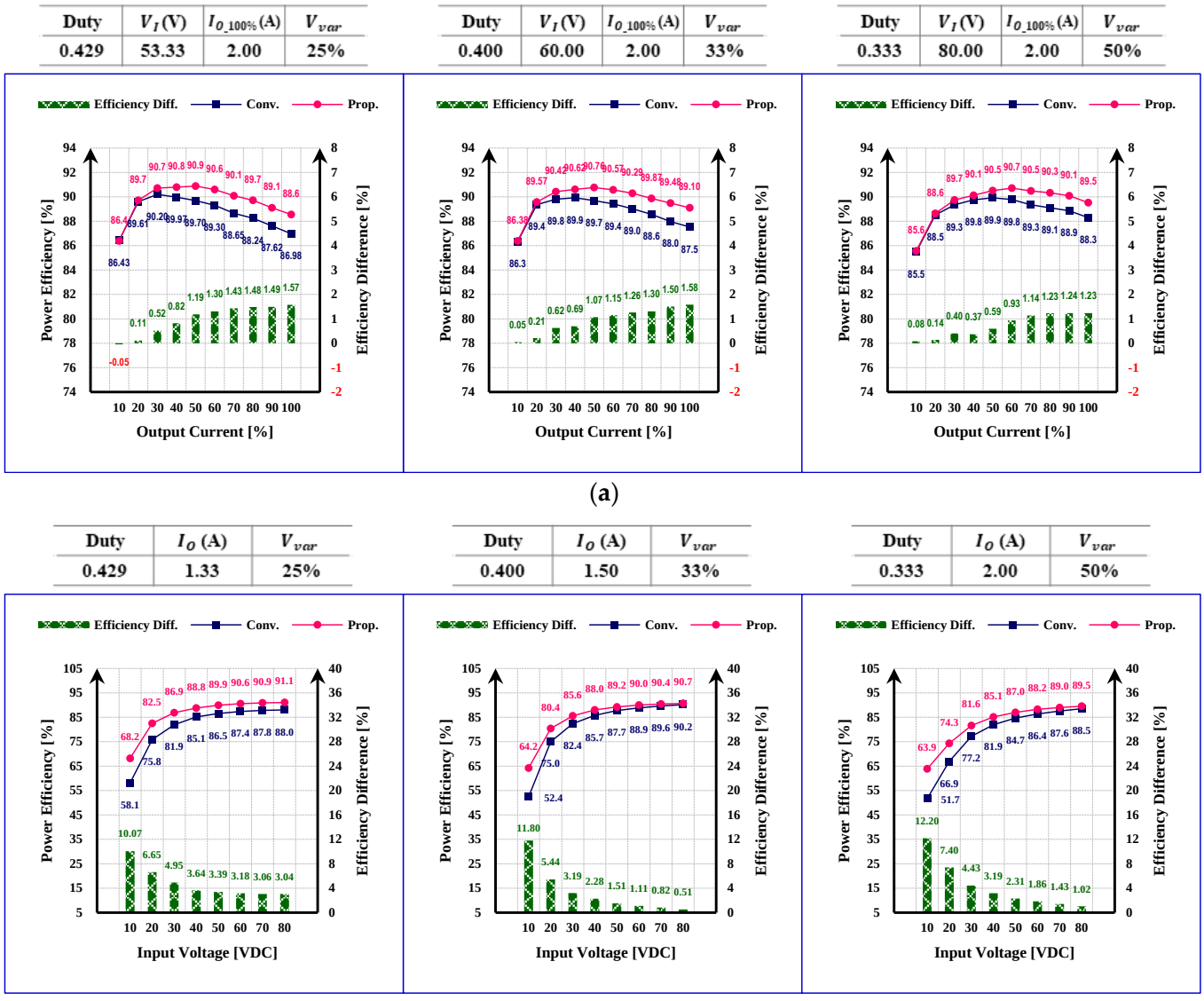

Figure 11. Power efficiency comparison of the buck-boost topology (step-down): (**a**) CV mode; (**b**) CC mode.

5.3.2. Step-Up

Figure 12 shows the power efficiency of the step-up buck-boost topology in the CV and CC modes. In the CV mode, the efficiency improves in general to 10–80 W and P_{Diff} increases in the high-power region where the output current increases. In the CC mode, P_{Diff} decreases with an increase in V_{var} and the input voltage. The power efficiency decreases more than the conventional converter at a power of 50 W or higher. In the step-up section, the output voltage increases with the input voltage, and the voltage stress of diode D_1 also increases. The efficiency decreases more than the conventional converter because the resulting diode loss exceeds the increase in the efficiency obtained by the removal of D_2 in the switch-off section. Therefore, the proposed converter is suitable for applications below 50 W in the step-up section of the buck-boost topology.

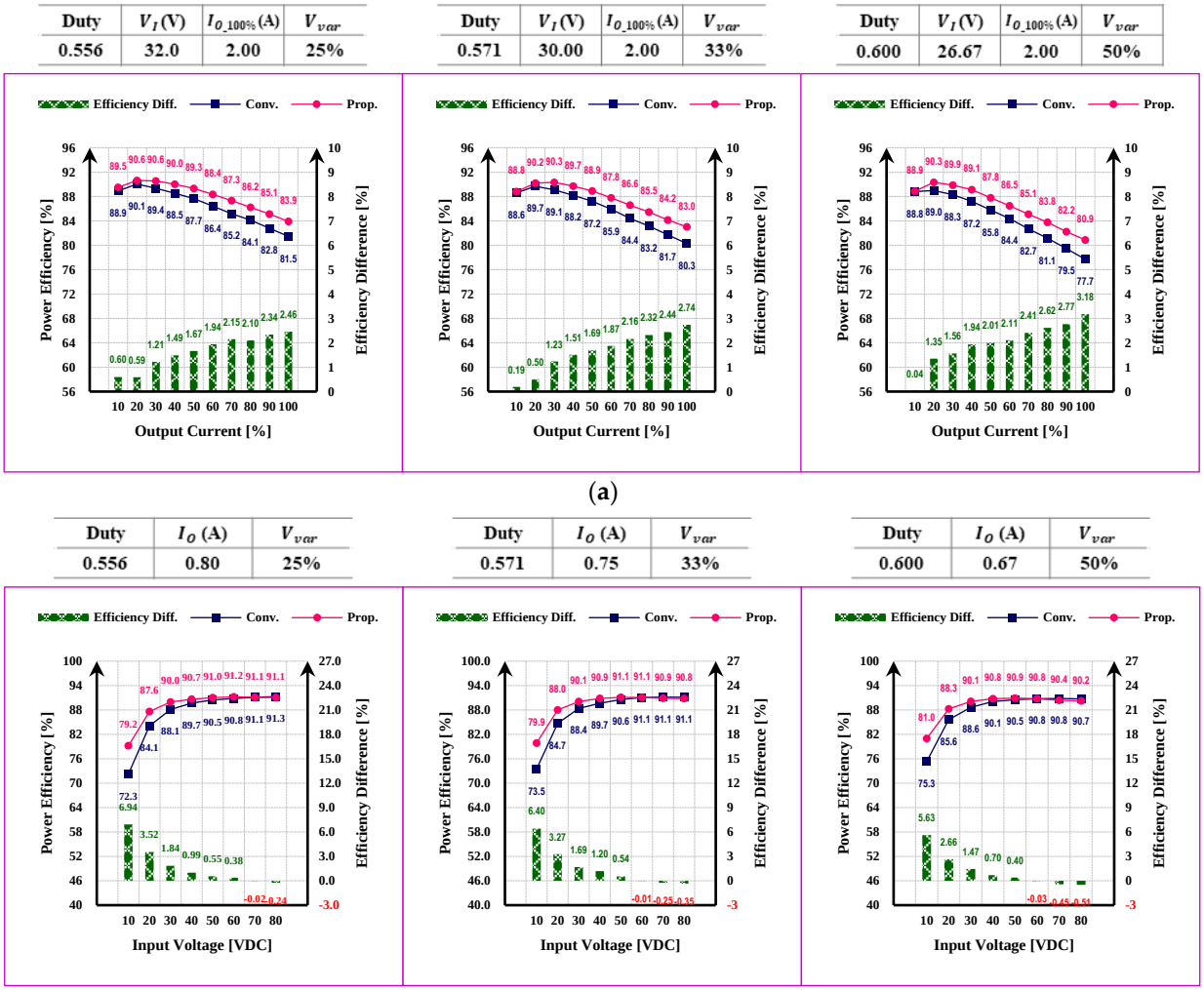

Figure 12. Power efficiency comparison of the buck-boost topology (step-up): (**a**) CV mode; (**b**) CC mode.

5.3.3. Diode Stress (Buck-Boost Step-Up, CC Mode)

Figure 13 shows the analytic and experimental diode power loss in the CC mode in the step-up section of the buck-boost topology. A positive power loss difference L_{Diff} implies that the diode loss of the proposed TSBB converter is large, whereas if it is negative, it implies a large diode loss of the conventional TSBB converter.

To calculate the diode loss, information on several parameters was referenced from the datasheet and all data are typical values at 25 degrees. Parameters not provided in the datasheet were used to calculate the diode loss with some assumptions.

- Forward voltage V_F: obtained from the V_F-I_F characteristic curve.
- Equivalent resistance R_D: obtained from the V_F-I_F characteristic curve by linear approximation under the current conditions used in the experiment.
- Reverse recovery time T_{rr} and peak reverse recovery current I_{rrm}: estimated and calculated using value 16 nsec at the forward current I_F = 1.0 A and the reverse current I_R = 0.5 A.
- Peak reverse recovery voltage V_{rrm}: assumed $\frac{dI_F}{dI_R} = 0.5$ at $V_R\left(1 + \frac{dI_F}{dI_R} / \frac{dI_F}{dI_R}\right)$ and corrected coefficient by temperature with V_R characteristic curve.
- Ignored any other parasitic factors like internal inductance, capacitance, and so on.

Due to several assumptions and uncertain parameter values, the two results are slightly different. This is expected to be due to the reverse recovery characteristics that

change exponentially with the increase in temperature and voltage stress, and also to be affected by parasitic components on the PCB and errors in measurement equipment.

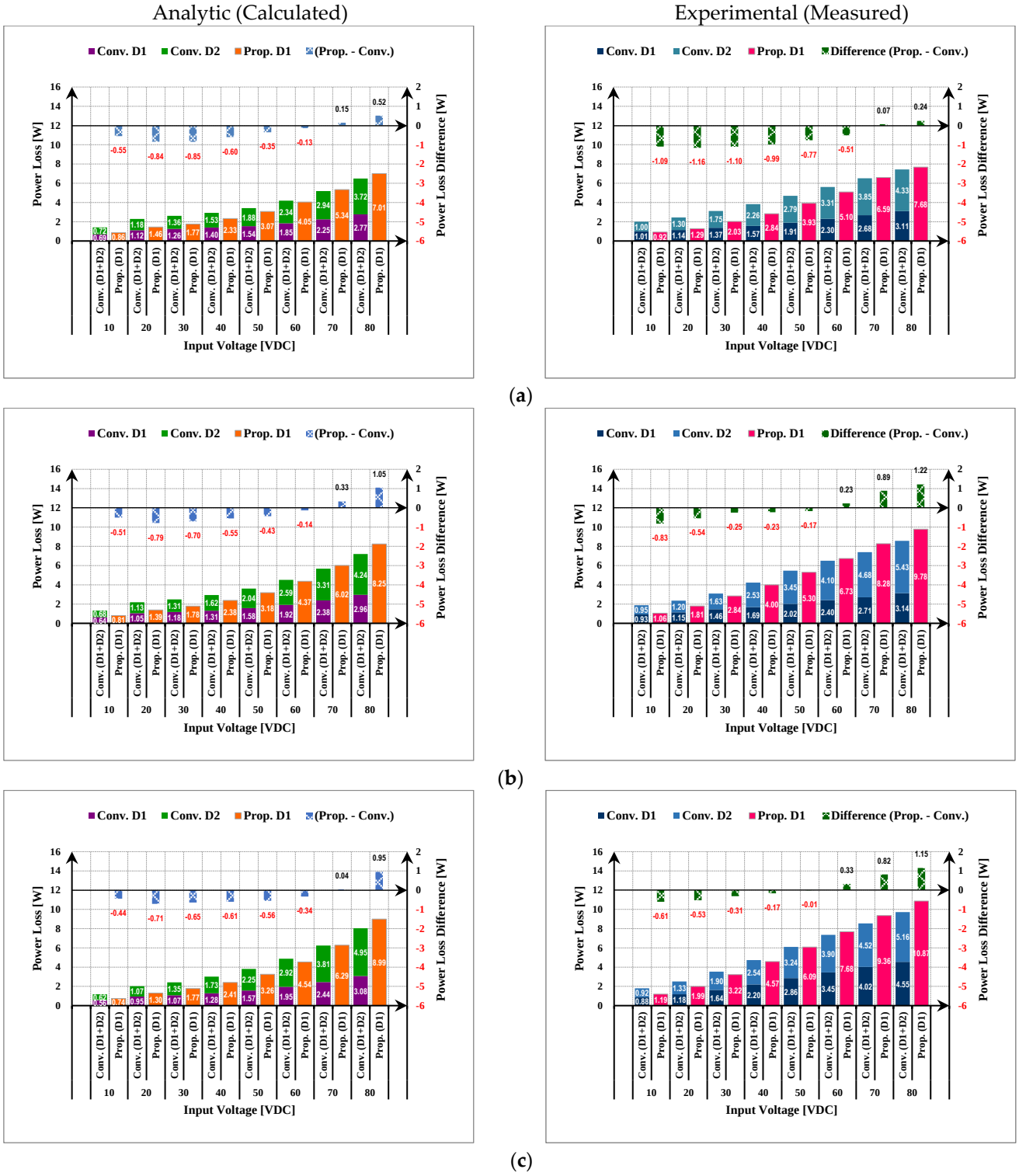

Figure 13. Analytic and experimental diode power loss of the buck-boost topology step-up period in the CC mode: (**a**) Duty = 0.556, I_O = 0.8 A; (**b**) Duty = 0.571, I_O = 0.75 A; and (**c**) Duty = 0.600, I_O = 0.667 A.

Despite these differences, both results show a similar trend in which diode losses rapidly increase with voltage stress over a certain region, thereby diode power loss of the

proposed TSBB converter is bigger than the conventional converter over a certain input voltage. The increase in the D_1 loss of the proposed TSBB converter becomes larger than the power efficiency improvement by the removal of D_2. The power efficiency is reversed at the point where the difference in diode loss changes from negative to positive (+). For the proposed TSBB converter, the power efficiency increases at 60 W or lower at the duty ratio of 0.556; the power efficiency increases at 50 W or lower at the duty ratios of 0.571 and 0.600.

6. Conclusions

This study proposed a modified design of the TSBB converter to improve power efficiency using fewer conduction components and measured the optimal output power range. The proposed TSBB converter improved power efficiency in buck and buck-boost topologies by reducing the conduction loss caused by the diode in the switch-off section power efficiency. A 100 W prototype was designed and fabricated to verify the improvement. Experiments were conducted in the CV/CC modes of three topologies, and the power efficiency was measured for 10–80 W. In the buck topology, power efficiency improved in the entire power range of 10–80 W; it increased on average by 0.75–1.36% and 0.83–2.27% in the CV and CC modes, respectively. In the buck-boost topology step-down, the power efficiency improved in the entire power range of 10–80 W; it improved on average by 0.73–0.99% and 3.33–4.75% in the CV and CC modes, respectively. In the buck-boost topology step-up, the power efficiency increased on average by 1.65–2.00% in the entire power range of 10–80 W in the CV mode, and by 2.17–2.77% in the power range of the 10–50 W in the CC mode.

In future research, we will study how to reduce the conduction and switching losses by reducing the voltage and current stress of semiconductors for efficiency improvement. In addition, we will analyze the effect on output ripple under various conditions by using inductance, capacitance, and switching frequency as design variables, and study how these parameters affect converter efficiency.

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References

1. Zhou, X.; Sheng, B.; Liu, W.; Chen, Y.; Wang, L.; Liu, Y.F.; Sen, P.C. A high-efficiency high-power-density on-board low-voltage dc–dc converter for electric vehicles application. *IEEE Trans. Power Electron.* **2021**, *36*, 12781–12794. [CrossRef]
2. Jin, F.; Nabih, A.; Chen, C.; Chen, X.; Li, Q.; Lee, F.C. A high efficiency high density dc/dc converter for battery charger applications. In Proceedings of the 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 14–17 June 2021.
3. Yang, C.; Xie, S.; Mao, L.; Zhang, Z. Efficiency improvement on two-switch buck-boost converter with coupled inductor for high-voltage applications. *IET Power Electron.* **2014**, *7*, 2846–2856. [CrossRef]
4. Sahu, B.; Rincón-Mora, G.A. A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications. *IEEE Trans. Power Electron.* **2004**, *19*, 443–452. [CrossRef]
5. Moon, B.; Jung, H.Y.; Kim, S.H.; Lee, S.H. A modified topology of two-switch buck-boost converter. *IEEE Access* **2017**, *5*, 17772–17780. [CrossRef]

6. Jung, H.Y.; Kim, S.H.; Moon, B.; Lee, S.H. A new circuit design of two-switch buck-boost converter. *IEEE Access* **2018**, *6*, 47415–47423. [CrossRef]
7. Chandran, C.; Chandran, L.R. Two switch buck boost converter for power factor correction. In Proceedings of the 2015 International Conference on Technological Advancements in Power and Energy (TAP Energy), Kollam, India, 24–26 June 2015.
8. Veerachary, M.; Khuntia, M.R. Design and analysis of two-switch-based enhanced gain buck–boost converters. *IEEE Trans. Ind. Electron.* **2021**, *69*, 3577–3587. [CrossRef]
9. Ahmad, A.A.; Abrishamifar, A. A simple current mode controller for two switches buck-boost converter for fuel cells. In Proceedings of the 2007 IEEE Canada Electrical Power Conference, Montreal, QC, Canada, 25–26 October 2007.
10. Son, H.S.; Kim, J.K.; Lee, J.B.; Moon, S.S.; Park, J.H.; Lee, S.H. A new buck–boost converter with low-voltage stress and reduced conducting components. *IEEE Trans. Ind. Electron.* **2017**, *64*, 7030–7038. [CrossRef]
11. Fan, H. Design tips for an efficient non-inverting buck-boost converter. *Analog Appl. J.* **2014**, 20–25.
12. Chen, J.; Maksimovic, D.; Erickson, R.W. Analysis and design of a low-stress buck-boost converter in universal-input PFC applications. *IEEE Trans. Power Electron.* **2006**, *21*, 320–329. [CrossRef]
13. MOSFET Power Losses and How They Affect Power-Supply Efficiency. Available online: https://www.ti.com/lit/an/slyt664/slyt664.pdf (accessed on 5 November 2022).
14. Infineon Application Note. Available online: https://application-notes.digchip.com/070/70-41484.pdf (accessed on 5 November 2022).
15. Xiong, Y.; Sun, S.; Jia, H.; Shea, P.; Shen, Z.J. New physical insights on power MOSFET switching losses. *IEEE Trans. Power Electron.* **2009**, *24*, 525–531. [CrossRef]
16. Lirio, L.E.A.; Bellar, M.D.; Neto, J.A.M.; Dos Reis, M.S.; Aredes, M. Switching losses analysis in sic power mosfet. In Proceedings of the 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), Fortaleza, Brazil, 29 February 2016.
17. Ren, Y.; Xu, M.; Zhou, J.; Lee, F.C. Analytical loss model of power MOSFET. *IEEE Trans. Power Electron.* **2006**, *21*, 310–319.
18. Power MOSFET Basics: Understanding MOSFET Characteristics Associated with the Figure of Merit. Available online: https://www.vishay.com/docs/71933/71933.pdf (accessed on 5 November 2022).
19. Shen, Z.J.; Xiong, Y.; Cheng, X.; Fu, Y.; Kumar, P. Power MOSFET switching loss analysis: A new insight. In Proceedings of the 2006 IEEE Industry Applications Conference and Forty-First IAS Annual Meeting, Tampa, FL, USA, 8–12 October 2006.
20. Rodríguez, M.; Rodríguez, A.; Miaja, P.F.; Lamar, D.G.; Zúniga, J.S. An insight into the switching process of power MOSFETs: An improved analytical losses model. *IEEE Trans. Power Electron.* **2010**, *25*, 1626–1640. [CrossRef]
21. Li, X.; Jiang, J.; Huang, A.Q.; Guo, S.; Deng, X.; Zhang, B.; She, X. A SiC power MOSFET loss model suitable for high-frequency applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8268–8276. [CrossRef]
22. Ivanovic, Z.; Blanusa, B.; Knezic, M. Power loss model for efficiency improvement of boost converter. In Proceedings of the 2011 XXIII International Symposium on Information, Communication and Automation Technologies, Sarajevo, Bosnia and Herzegovina, 27–29 October 2011.