



Article On Noise Modeling of Capacitive Feedback Transimpedance Amplifiers in CMOS

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Abstract: The work reports on the development of a detailed noise current model for a low-noise capacitive feedback transimpedance amplifier (TIA) in CMOS. The proposed TIA circuit implements the programmable-gain using an array of discretely controlled feedback capacitors and resistances in the biasing circuit and is originally designed bearing in mind low-noise requirements for optical time-domain reflectometer (OTDR) applications with the base gain of 10 k Ω at 1 GHz bandwidth and noise levels below 5.0 pA/ $\sqrt{\text{Hz}}$. The newly developed model for input-referred noise current spectral density complements the previously suggested transimpedance gain model and takes into account both the primary and secondary noise sources so far ignored in the models known in the literature. The proposed noise model consists of five terms and includes the effects caused by biasing components of the input stage and the noise shaping from the source follower. The performance of the developed noise model is evaluated using the post-layout simulation in 0.18 µm CMOS and 0.25 µm BiCMOS technologies, and a close match of the proposed model is demonstrated in the results of the post-layout simulation with the noise level below 1.8 pA/ $\sqrt{\text{Hz}}$ for the base gain configuration in CMOS. A comparison to available noise models from the literature confirms that previously known noise models for this promising TIA architecture omitted important noise components present in practical and physically realizable circuits and, therefore, resulted in underestimating the base noise level by a factor of two to three, while completely ignoring the flicker noise mapping in the low-frequency range.

Keywords: capacitive feedback; CMOS integrated circuits; low-noise amplifiers; noise modeling; optical time-domain reflectometry; transimpedance amplifiers

1. Introduction

In the last decades, numerous works have been published on developing transimpedance amplifiers (TIA) in complementary metal oxide semiconductors (CMOSs) [1]. These circuits are typically used for applications where weak signals from current-mode sensors, such as photodiodes (PD), are to be converted to the output voltage of amplitude sufficient for subsequent processing and analysis. Although mostly known for their usage in optical coupling and optical communication receivers [2,3], the TIA circuits are also widely employed in other applications, such as the readout of MEMS sensors [4–8], LIDAR processing [9], miniaturized magnetic resonance systems [10], acoustic wave and ultrasound imaging [11–14], biosensors [15–17] and other biological applications [18], spectroscopy [19,20], etc. Clearly, such a broad range of diverse applications had resulted in contradicting sets of requirements and constraints when it comes to choosing an amplifier design and topology for a particular application. For example, while optical communication systems have pushed the requirements for the amplifiers in the direction of higher-gainbandwidth products, reduced power consumption and noise are often seen as the major constraints for biological and sensor applications, while the bandwidth of such TIAs can be set as low as just several hundreds of kHz. Thus, there may be no single TIA architecture



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Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). that best fits every possible application, and different usage scenarios are likely to benefit from complementary properties of competing TIA designs [21].

The work as presented below was initially motivated by the search for a TIA design suitable for low-noise high-performance optical time-domain reflectometer (OTDR) equipment [22]. Fiber optical networks form the backbone of the modern high-speed Internet as they provide extremely high bandwidth, relatively low power, low signal distortions, and all this at low costs. With a constantly growing demand for new online services, cloud-based applications and streaming services are the drivers for new communication technologies as well as force the providers to work continuously on the ramp-up of the existing network infrastructure. However, rapid development and extension of optical communication networks also require equipment for network installation, monitoring, maintenance, fault analysis, and failure prevention. One of the most popular and commonly used instruments for the assessment of optical line quality is the OTDR instrument mentioned earlier. The operating principle of the instrument is based on the injection of a laser pulse into the fiber, where the line quality or, correspondingly, faults are assessed by performing the time-domain analysis of the recorded pulse reflections caused by the Rayleigh scattering. Similarly to other systems with current-mode sensors, here, the TIA is one of the major building blocks of the instrument's front end, and its performance essentially limits the overall sensitivity of the device. The main parameters of the TIA circuit, such as its transimpedance gain, bandwidth, and noise current, define the major characteristics of the OTDR instrument, such as its dead zone and dynamic range [23].

When designing a TIA, several main parameters of the circuit shall be taken into account. Apart from the power consumption, implementation footprint, and supply voltage, the TIA-specific parameters such as photodetector (PD) capacitance, transimpedance gain, bandwidth, and noise are of major importance. While the PD capacitance is mainly a design requirement, the noise, bandwidth, and gain form a typical set of TIA requirements and the basis for deciding whether the suggested topology fits the target application. Clearly, every meaningful design shall be accompanied by sufficiently detailed models so that the performance of the circuit could be understood without performing extensive numerical simulations. In terms of the models needed for TIA characterization, one typically ends with the requirement to have two elaborated models: the complete transimpedance gain model and the input-referred noise current spectral density model. Although a detailed model for the transimpedance gain for the capacitive feedback TIA had been proposed by us before (see [22] for further details), an equivalent and accurate model of the noise current was still missing. Even though, together with the gain models, the corresponding noise models were originally proposed by Shahdoost [24] and Keshri [5], those models, as we will see below, are very rough and ignore numerous effects which arise while designing realistic TIAs under the constraints of advanced CMOS processes. Furthermore, we believe that it is also important to develop such a noise model incrementally from the basic principles (in this case, independently considering all relevant noise sources) similarly as we performed for the gain model in [22] so that both gain and noise models are consistent with each other and are formulated following similar assumptions.

As a detailed and accurate noise model for capacitive feedback TIA seems to be missing in the literature, in this work we want to close this gap by proposing an accurate noise current model which complements our previous work on the gain model reported in [22]. With this, we ensure that all important signal components in both models are considered and evaluated in a consistent manner. This will also support our understanding of the interplay of the noise sources in practical design and form a solid foundation for the efforts toward a possible noise minimization strategy. Although the modeling will be demonstrated using a single-ended design in accordance with the gain model developed in [22], the obtained results can be easily extended for differential TIA configurations.

The rest of the paper is structured as follows. In Section 2, based on our previously published gain model, we propose a new input-referred noise current model for the suggested capacitive feedback TIA. In Section 3, the simulation results are presented, where

we analyze the suggested noise models against the results of the post-layout simulation using programmable-gain TIA implemented for OTDR applications in 0.18 μ m CMOS and 0.25 μ m BiCMOS technologies. In Section 4, we discuss the proposed noise model, compare it to the models known in the literature, and suggest further noise improvement using a cascode current source in the source-follower block. Section 5 concludes this contribution with a summary of the obtained results.

2. Analytical Methods

Although the classical resistive-feedback TIA provides a fair balance of the most important TIA parameters, it has an inherent problem with the noise performance of the feedback resistor $R_{\rm F}$ as its noise is directly added to the input-referred noise current and drastically degrades the noise figures of this well-accepted design. Although numerous works have been reported on modifications to this established TIA topology, the major issue with this design is that all major circuit characteristics depend entirely on the value of $R_{\rm F}$. Here, a larger value of $R_{\rm F}$ is needed for lower noise and an improved gain, while a smaller value is required for designs with a larger bandwidth. Finally, technological constraints are also important, as the large value of R_F may be limited by the maximum realizable on-chip resistance and parasitic capacitances [25]. Thus, by striving for a better TIA performance, it may be inevitable to introduce some structural changes to this reference TIA design in order to obtain an additional degree of freedom for balancing noise, gain, and bandwidth. On the other hand, the basic feedback structure of the TIA itself has important structural benefits as it ensures almost constant transimpedance gain in the bandwidth of interest while decreasing the sensitivity to process and temperature variations. Therefore, it may be still beneficial to keep the general feedback structure of the amplifier, while substituting the noisy feedback resistor with something which is less noisy. An intuitive candidate for such a noise-free element is a capacitor, but a direct replacement of $R_{\rm F}$ with a capacitor will result in a phase shift which requires a subsequent stage for phase correction. Such TIAs formed by an integrator and cascaded differentiator, also often called capacitive feedback TIAs, have been also reported and have their own advantages (see, e.g., [25,26] for further details). However, in this work, we follow an alternative approach where the feedback network is formed by a dedicated network of two capacitors C_1 and C_2 [24] and is shown in Figure 1 with separate blocks corresponding to the feedback circuit (a), the forward gain (b), and the source follower (c). An advantage of the proposed approach that it does not require the second-stage differentiator.



Figure 1. The general structure of the proposed capacitive feedback TIA with major blocks: (**a**) feedback block, (**b**) forward-gain block; (**c**) source-follower block (adopted with changes from [22]).

The development of the analytical noise model is provided for the programmable-gain TIA configuration as required when implementing the front-end amplifier according to OTDR requirements [22,23]. The necessity for the programmable-gain configuration is

caused by an inherent relationship between the responsivity of the PD and the specification for the dynamic range and gain of the measurement equipment. With the amplifier, which is able to support a wide range of gain-bandwidth configurations, one can effectively use the same circuit with different PDs enabling varying operating modes for the very same device. This also includes support for operations with both very weak optical signals and short optical pulses.

The mid-frequency value of the transimpedance gain R_T for a generic capacitive feedback architecture can be, in theory, approximated as [1]:

$$R_{\rm T} = \left(1 + \frac{C_1}{C_2}\right) R_2. \tag{1}$$

This expression for the transimpedance gain is valid under the assumption of an infinite gain A, and the overall gain of this TIA circuit is defined by the feedback circuit formed solely by the two feedback capacitors C_1 and C_2 . It was also recently proved that the performance of the capacitive feedback TIA in terms of Pareto frontier [27] is always greater than that of the resistive-feedback TIA, reaching four to five times for low output capacitance [28]. The simplified model from above can be used for a very rough analysis of this promising architecture; it may not be extremely helpful for predicting the performance of a real circuit in CMOS and, therefore, more accurate models are needed.

In order to develop an accurate noise current model, one shall shortly recall the gain model for the very same circuit. The capacitive feedback TIA topology was originally suggested in the seminal work of Razavi [29] and extended in the series of works of Shahdoost [2,24,30,31]. The modeling of the gain for this TIA architecture was revisited in our recent work [22] where we developed accurate gain expressions for circuits implemented under realistic CMOS and power supply constraints. The discussion below complements the original approach of [22] by developing the corresponding noise current model for the very same circuit following an approach similar to the gain model, where an elaborated model is developed incrementally bottom-up from the noise contribution of the circuit's basic components. Clearly, where relevant, for the noise components shaped through some of the blocks in the gain model, one shall recall the original gain model elaborated in [22].

The generic capacitive feedback TIA design along with the major noise sources is shown in Figure 1 and employs the voltage amplifier, the second stage with M_2 , and a capacitive feedback network formed by two capacitors, C_1 and C_2 . A corresponding circuit-level design of the proposed amplifier, including the relevant noise sources, is shown in Figure 2. Here, we followed a classical approach of using a modification of the single-stage common-source amplifier, although alternative solutions for the core voltage amplifier can also be used [15,32]. A more detailed discussion on the gain model and motivation behind particular design decisions can be found in our previous work [22].

The input-referred noise current $i_{n,TIA}$ is an important parameter when characterizing any given TIA design, as it determines the overall sensitivity of the circuit. The proper characterization of the noise of the TIA for our scenario is even more important, as the PD's current in the case of OTDR applications is very small. Below, we show how the noise model can be derived for the developed circuit and which noise sources have the most significant contribution. As we have argued before, one of the major advantages of the capacitive feedback TIA is that the feedback network itself is noiseless and contributes no noise, as opposed to the traditional resistive-feedback network. Furthermore, the current thermal noise due to R_2 will be suppressed when divided by the current gain of the circuit. Unfortunately, this only holds for the circuit operating under benign conditions, and additional significant noise sources shall be taken into account due to imperfections in biasing circuits, current mirrors, etc.

We will start the noise analysis from the classical resistor's *R* thermal noise. This can be modeled as a voltage source in series with the resistor or, equivalently, as a current source in parallel with it. The noise is generated by the thermal agitation of the charge

carriers that occurs inside any electrical conductor, and for the noise representation in the form of the voltage source, one obtains the voltage noise spectral density [33]:

$$\frac{v_{\rm nr}^2}{\Delta f} = 4k_{\rm B}TR,\tag{2}$$

where *T* is the absolute temperature, k_B is the Boltzmann constant, and *f* is frequency. The noise is white and is proportional to the product of the resistance and the temperature, but does not depend on the actual current flowing through the resistance. One can obtain an equivalent current noise spectral density as follows:



Figure 2. A circuit-level implementation of a fixed-gain capacitive feedback TIA and contributing noise sources: (1) thermal noise due to $R_{\text{bias},1}$, (2) thermal noise due to R_2 , (3) M_1 thermal noise, (4) M_1 flicker noise, and (5) M_5 flicker noise (adapted from [22]).

For the given circuit, there are several sources for the resistor's thermal noise which we may consider for the complete noise model. The first noise source is due to the resistor $R_{\text{bias},1}$ in the biasing circuit of the input stage. Differently from other works, where the performance of the biasing circuit is considered to be perfect and contributes no noise to TIA, we may not consider this noise source to be negligible in the real circuit. Thus, the noise contribution due to $R_{\text{bias},1}$ becomes

$$\frac{2}{\mathrm{nr1}}{\Delta f} = \frac{4\mathrm{k_B}T}{R_{\mathrm{bias},1}},\tag{4}$$

and is directly added to the input noise current. Additionally, we also have the noise component due to R_2 . In this case, however, the component is not directly added to the input but is suppressed by the approximate gain due to capacitive feedback:

$$\frac{\overline{i_{nr2}^2}}{\Delta f} = \frac{4k_B T R_2}{Z_T^2} \approx \frac{4k_B T}{R_2 \left(1 + \frac{C_1}{C_2}\right)^2}.$$
(5)

Even though the approximation above may not be valid in the general case, it is clear that the noise contribution due to R_2 is damped by a significant factor for the frequencies where the TIA gain is significant. Thus, the final thermal noise component consists of two contributions: noise current caused by $R_{\text{bias},1}$ in the front-end biasing circuit for M_1 , and scaled noise from R_2 :

$$\frac{\overline{i_{nr}^2}}{\Delta f} = \frac{i_{nr1}^2}{\Delta f} + \frac{i_{nr2}^2}{\Delta f} = \frac{4k_BT}{R_{bias,1}} + \frac{4k_BTR_2}{Z_T^2}.$$
(6)

There are several noise sources to be evaluated when it comes to the contribution of the metal oxide semiconductor (MOS) transistor. The two most important noise sources of the transistor are the thermal noise and the 1/f noise, if we ignore the secondary effects such as the shot noise due to the leakage current of the drain–source reverse diodes. The thermal noise of the channel can be represented by a voltage source in series with a gate and the voltage spectral density:

$$\frac{v_{\rm nt'}^2}{\Delta f} = \frac{8}{3} \frac{k_{\rm B} T g_{\rm d0}}{g_{\rm m}^2},\tag{7}$$

where g_{d0} is the zero-bias drain conductance. If we approximate g_{d0} with the transconductance g_{m} , a somewhat simpler expression can be obtained [33]:

$$\frac{\gamma_{\rm nt'}^2}{\Delta f} \approx \frac{8}{3} \frac{k_{\rm B} T}{g_{\rm m}}.$$
(8)

For the design shown in Figure 2, we may consider this noise component only for the transistor M_1 with $g_{m,1}$.

As the charge carriers move at the interface, so-called flicker noise is caused by the random trapping of the charges. This noise contribution typically varies from process to process and depends on the impurities at the oxide–silicon interface. The noise is typically modeled by a current source across the drain, with the spectral density as

$$\frac{i_{\rm nf}^2}{\Delta f} = \frac{K_{\rm f}}{f} \frac{g_{\rm m}^2}{C_{\rm ox}WL},\tag{9}$$

where W and L are, correspondingly, the width and the length of the channel, K_f is the flicker noise constant, and C_{ox} is the gate oxide capacitance per unit area. When referred as input, the noise is represented by a voltage source between gate and source with

$$\frac{\mathcal{V}_{\rm nf}^2}{\Delta f} = \frac{K_{\rm f}}{f} \frac{1}{C_{\rm ox} WL}.$$
(10)

Recall that the value of K_f of PMOS devices is an order lower than that of NMOS devices, and the former devices also exhibit less flicker noise. As this noise component has an inverse dependency on frequency, it is also often called 1/f noise (yet another name for pink noise). Similar to the case of the channel thermal noise, this noise shall be again considered at least for the input transistor M_1 . Note that in many high-frequency designs, the flicker noise component is ignored, as these noise sources are often considered nondominant and are excluded from the approximate analysis.

Summing up all the terms discussed above, we obtain a generic expression:

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{\overline{i_{nr}^2}}{\Delta f} + \frac{\overline{i_{nt',M1}^2}}{\Delta f} + \frac{\overline{i_{nf,M1}^2}}{\Delta f} = \frac{\overline{i_{nr}^2}}{\Delta f} + \frac{1}{Z_{in}^2} \left(\frac{\overline{v_{nt'}^2}}{\Delta f} + \frac{\overline{v_{nf}^2}}{\Delta f}\right).$$
(11)

With the thermal noises on both the bias resistance $R_{\text{bias},1}$ and R_2 , we obtain

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4k_BT}{R_{\text{bias},1}} + \frac{4k_BTR_2}{Z_T^2} + \frac{1}{Z_{\text{in}}^2} \left(\frac{8}{3}\frac{k_BT}{g_{\text{m},1}} + \frac{K_f}{f}\frac{1}{C_{\text{ox}}W_{\text{M1}}L_{\text{M1}}}\right).$$
(12)

The expression above already represents a fair approximation of the TIA noise in midand high-frequency ranges and captures typical 1/f flicker noise behavior of M_1 . Still, the proposed practical circuit implementation with I_{SS} implemented using M_5 may contribute an additional noise which is typically missed with an approximate noise modeling. At the node V_{s2} , the flicker noise due to M_5 becomes an additional drain current of M_2 , and after amplification with R_2 results in voltage noise at the output (here, for the noise consideration we ignore the effect of the output buffer). As the ratio of the output voltage to the input current is exactly the transimpedance gain Z_T (see [22] for the detailed structure of Z_T), we obtain

$$Z_{\rm T} = \frac{V_{\rm out1}}{I_{\rm in}}.$$

The transfer function of the M_5 noise at the node V_{s2} to the input current noise becomes

$$G_{\rm M5} = \frac{R_2}{Z_{\rm T}},\tag{13}$$

with the final noise due to M_5 :

$$\frac{i_{\rm nf,M5}^2}{\Delta f} = G_{\rm M5}^2 \frac{K_{\rm f,M5}}{f} \frac{1}{C_{\rm ox} W_{\rm M5} L_{\rm M5}}.$$
(14)

The overall noise model including the newly developed contribution from M_5 can be formed:

$$\frac{i_{n}^{2}}{\Delta f} = \frac{4k_{B}T}{R_{\text{bias},1}} + \frac{4k_{B}TR_{2}}{Z_{T}^{2}} + \frac{1}{Z_{\text{in}}^{2}} \left(\frac{8}{3}\frac{k_{B}T}{g_{m,1}} + \frac{K_{f,M1}}{f}\frac{1}{C_{\text{ox}}W_{\text{M1}}L_{\text{M1}}}\right) + G_{\text{M5}}^{2}\frac{K_{f,M5}}{f}\frac{1}{C_{\text{ox}}W_{\text{M5}}L_{\text{M5}}}.$$
(15)

For simplicity, we only consider the 1/f noise of M_5 and ignore the thermal channel noise. Recall also from the discussion of the gain in [22] that the input impedance for total input capacitance C_T is

$$Z_{\rm IN} = \frac{R_{\rm bias,1}}{1 + sR_{\rm bias,1}C_{\rm T}}.$$
(16)

For noise, however, we consider an effective input impedance:

$$Z_{\text{IN,eff}} = \frac{R_{\text{bias,1}}}{1 + sR_{\text{bias,1}}C_{\text{T,eff}}} = \frac{R_{\text{bias,1}}}{1 + sR_{\text{bias,1}}(C_{\text{T}} + C_{\text{M1}} + C_{\text{in2vs}})},$$
(17)

where the input capacitance is inflated due to transistor M_1 and input capacitance to the ground. Due to the small contribution of R_2 , the overall input-referred noise density can be effectively approximated as follows for the mid- and high-frequency ranges:

$$\frac{\overline{i_n^2}}{\Delta f} \approx \frac{4k_BT}{R_{\text{bias},1}} + \frac{1}{Z_{\text{IN,eff}}^2} \left(\frac{8}{3}\frac{k_BT}{g_{\text{m},1}} + \frac{K_{f,\text{M1}}}{fC_{\text{ox}}W_{\text{M1}}L_{\text{M1}}}\right) + \frac{K_{f,\text{M5}}G_{\text{M5}}^2}{fC_{\text{ox}}W_{\text{M5}}L_{\text{M5}}}$$

3. Mathematical and Computer Simulation Results

Below, we present the results for the noise modeling only, while the corresponding results for the gain modeling can be found in the previous work [22]. The results are demonstrated for five gain-bandwidth configurations of the programmable-gain TIA, as

developed according to the OTDR specification. Here, we shall bear in mind that we did not target the equal bandwidth design and, as expected, bandwidth decreases with the increasing gain. The obtained results also confirm that the achieved bandwidth of around 1 GHz for the base gain of 10 k Ω is close to the limit for the proposed implementation for the given gain and technological node. As we saw in the previous section, an exact gain model Z_T is important for the accuracy of the complete noise model due to its coupling in the flicker noise component of M_5 and thermal noise component due to R_2 .

Before we proceed to the noise results, let us first elaborate on how the noise model components sum up to the final noise performance and what impact each of these components has over the complete frequency range. To make the analysis more intuitive, we plot the results for all five gain configurations at once in order to observe the impact of different target gains. Let us start with the thermal noise component at the gate of the transistor M_1 :

$$\frac{\overline{i_{\rm nt'}^2}}{\Delta f} \approx \frac{1}{Z_{\rm IN\,eff}^2} \frac{8}{3} \frac{k_{\rm B}T}{g_{\rm m,1}},\tag{18}$$

and shown in Figure 3 for T = 298.15 K. The contribution is mostly responsible for the high-frequency noise, while its contribution to the noise figures in the mid- and low-frequency range is, obviously, insufficient to describe the behavior of a real circuit.



Figure 3. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component only (example case for TSMC 0.18 µm CMOS).

Next, we consider the proposed noise model for both M_1 thermal noise and the noise component due to $R_{\text{bias},1}$:

$$\frac{\overline{i_{\mathrm{nt'}}^2}}{\Delta f} + \frac{\overline{i_{\mathrm{nr1}}^2}}{\Delta f} \approx \frac{1}{Z_{\mathrm{IN,eff}}^2} \frac{8}{3} \frac{\mathbf{k}_{\mathrm{B}} T}{g_{\mathrm{m,1}}} + \frac{4\mathbf{k}_{\mathrm{B}} T}{R_{\mathrm{bias,1}}}.$$
(19)

The results are shown in Figure 4, where noise due to the bias resistor dominates in the mid- and low-frequency range and significantly pulls up the noise to the level of approximately 1 pA/ $\sqrt{\text{Hz}}$ for the base 10 k Ω gain.

Further, we extend the noise model by adding the noise contribution due to R_2 :

$$\frac{\overline{i_{\text{nt}}^2}}{\Delta f} + \frac{\overline{i_{\text{nr1}}^2}}{\Delta f} + \frac{\overline{i_{\text{nr2}}^2}}{\Delta f} \approx \frac{1}{Z_{\text{in,eff}}^2} \frac{8}{3} \frac{k_B T}{g_{\text{m,1}}} + \frac{4k_B T}{R_{\text{bias,1}}} + \frac{4k_B T R_2}{Z_T^2},$$
(20)

with the results shown in Figure 5. Although one may expect to again see the white resistor noise added to the previous results, this is not the case. As we elaborated in the previous section, the noise component i_{nr2}^2 is typically approximated in the literature as

$$\frac{\overline{i_{\rm nr2}^2}}{\Delta f} \approx \frac{4k_{\rm B}T}{R_2 \left(1 + \frac{C_1}{C_2}\right)^2}.$$
(21)



Figure 4. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component and noise due to $R_{\text{bias},1}$ (example case for TSMC 0.18 µm CMOS).



Figure 5. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component and noises due to $R_{\text{bias},1}$ and R_2 (example case for TSMC 0.18 µm CMOS).

The term represents the white noise (constant power spectral density) and its value is negligible when compared to the noise floor set by the noise component caused by $R_{\text{bias},1}$. However, this approximate expression is only valid if we assume a constant gain $Z_T \approx R_T$ over the complete frequency range. As this assumption is not valid due to the bandpass behavior of the proposed circuit, the noise due to R_2 is amplified for very low frequencies. By adding the flicker noise component for the input transistor M_1 , we obtain

$$\frac{\overline{t_{nf}^2}}{\Delta f} = \frac{1}{Z_{in,eff}^2} \frac{K_f}{f} \frac{1}{C_{ox}WL}.$$
(22)

The parameter $K_f/C_{ox}WL$ for M_1 gives us around 10 µA with the model performance containing four noise components shown in Figure 6. The impact of the flicker noise can be clearly seen in the transition region between middle and high frequencies, where the famous 1/f characteristic of the pink noise is hidden behind the shaped noise due to R_2 . The 1/f noise, due to its square-root dependency in PSD, gives the 10 dB/decade drop which is only partially seen in the transition region.



Figure 6. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component, noises due to $R_{\text{bias},1}$, R_2 and flicker noise on M_1 (example case for TSMC 0.18 µm CMOS).

We can complete the noise model by adding the last component due to the flicker noise of M_5 . The shaping filter for this noise is shown in Figure 7 and is simply the scaled inverse of our designed transimpedance Z_T . It also becomes obvious that the noise has a significant impact on extremely low frequencies only. Figure 8 shows the overall noise model.



Figure 7. Shaping filter due to G_{M5} (example case for TSMC 0.18 μ m CMOS).



Figure 8. Analytically calculated complete input-referred noise performance for programmable-gain configuration (example case for TSMC 0.18 µm CMOS).

After we demonstrated how the noise model is constructed from contributions of separate components, we are in the position to compare the proposed analytical models with the Cadence-based simulation using exactly the parameter values from the suggested design. The results for 1.8 V TSMC 0.18 µm CMOS and 2.5 V IHP 0.25 µm BiCMOS can be found in Figures 9 and 10, correspondingly. The slightly better noise performance of BiCMOS can also be partly explained by the fact that this technology employs a 2.5 V power supply and, therefore, voltage headroom problems are easier to avoid. In the case of CMOS, a relatively good fit of the analytical model and numerical simulation can be seen for both low- and high-frequency ranges, where the mismatch in the noise minimum point is below 10% at the frequency of 500 MHz for the 10 k Ω gain. Similarly, a good match can be also seen for the noise model at other gain configurations. A slight mismatch between the developed noise model can be found in the transition from the low- to mid-frequency ranges, where the post-layout simulated noise exceeds the prediction of the model. While the same is true for the BiCMOS-based implementation, the latter is also better suited to the problematic segment from the low- to mid-frequency range. Still, the mismatch in the noise minimum point is a bit larger and reaches 15% at the frequency of 500 MHz for the base gain case. Additionally to the effects discussed before, we also clearly see the famous 1/f behavior of the M_1 flicker noise in the low-frequency region. While this effect gives the 10 dB/decade drop, it is mainly responsible for the noise behavior between 10 kHz and 1 MHz, while for very low frequencies, the noise with a slope around 20 dB/decade can be seen, which cannot be explained by the flicker noise M_1 . This was a major motivation to incorporate the impact of M_5 flicker noise into the noise model.



Figure 9. Proposed analytical model for the input-referred noise current density and Cadencesimulated noise for programmable-gain TIA configuration in TSMC 0.18 μ m CMOS. Solid lines are due to Cadence simulation; dashed lines are due to the developed analytical noise model.



Figure 10. Proposed analytical model for the input-referred noise current density and Cadencesimulated noise for programmable-gain TIA configuration in IHP 0.25 μ m BiCMOS. Solid lines are due to Cadence simulation; dashed lines are due to the developed analytical noise model.

4. Discussion

Apart from the low-frequency M_5 noise, the nonideal behavior of a practical biasing (resistive) circuit was also often neglected by other authors while deriving the noise models. This was exactly followed by the author in [5], where the the noise component due to R_2 was kept while assuming a perfect biasing circuit. However, for a realistic circuit operating under voltage headroom constraint with resistive biasing, such a model would clearly result in an overoptimistic estimation for the noise level in mid-range frequencies. Note that none of the components of resistive noise was considered in the series of works of Shahdoost (see his latest work [24]). While biasing noise was similarly ignored due to transistor-based implementation and the assumption of effectively infinite resistance, the noise from R_2 was neglected due to an assumption of its minor impact. According to the author, the noise contribution was solely due to the noise of the core amplifier (our first noise component $\overline{i_{nt'}}$ presented above).

The assumption of a perfect biasing for M_1 results in yet another difference with the models so far presented in the literature. Authors typically assumed a pure reactive input impedance (see the series of works of Shahdoost and work [10]), resulting in

$$\overline{i_{n,TIA}^2} \approx \overline{v_{n,OpAmp}^2} \left[C_T + \frac{C_1}{1 + C_1/C_2} \right]^2 s^2.$$
 (23)

Technically, the model can be derived from our noise model when one assumes perfect biasing $R_{\text{bias},1} \rightarrow \infty$. Then, the model for the input impedance becomes

$$\lim_{R_{\text{bias},1}\to\infty} Z_{\text{in}} = \frac{1}{1 + s\left(C_{\text{T}} + \frac{C_{1}C_{2}}{C_{1} + C_{2}}\right)} \approx \frac{1}{1 + s(C_{\text{T}} + C_{2})} \approx \frac{1}{1 + sC_{\text{T}}}.$$
 (24)

In the capacitive network, the input impedance is formed by C_T in parallel with the series connection of C_1 and C_2 . As the C_T dominates the input impedance, one can rearrange the noise model, and since in capacitive feedback TIA holds $C_1 \gg C_2$, we obtain

$$\overline{v_{n,TIA}^{2}} \approx \overline{v_{n,OpAmp}^{2}} \left[C_{T} + \frac{C_{1}C_{2}}{C_{1} + C_{2}} \right]^{2} s^{2} \qquad (25)$$

$$\approx \overline{v_{n,OpAmp}^{2}} \left[C_{T} + \frac{C_{1}C_{2}}{C_{1}} \right]^{2} s^{2} = \overline{v_{n,OpAmp}^{2}} [C_{T} + C_{2}]^{2} s^{2},$$

and the latter expression is yet another simplified noise model, as reported by [5].

How the previously known noise model of Keshri compares to the proposed noise model can be found in Figure 11, where both models are shown for the very same set of parameters in CMOS. The comparison employs the very same set of true circuit parameters, where the simplified model of Keshri is fed with the required parameter values of the true operating CMOS circuit without any additional tuning or inflation of the parameter values. As the noise model proposed by Shahdoost is even simpler when compared to the one of Keshri (it even ignores the noise component due to R_2), it is not discussed any further. Based on Figure 11, we see that for the given valid CMOS TIA design we cannot confirm the simplified noise model to represent the dominating noise behavior as well as to correctly represent even the base noise level (compare Figures 9 and 11). The major differences are caused by the absence of both flicker noise components (correspondingly from M_1 and M_5) and missing resistor noise contribution in the biasing circuit. The latter observation is consistent with the discussion in the previous section, as the biasing circuit was often assumed to possess infinite resistance and was omitted from consideration while developing the noise models by other authors. Of importance is that our proposed noise model does not assume fixed TIA gain when scaling the noise from R_2 . As we see, the noise models that are commonly found in the literature are inadequate for estimating the noise level in realistic capacitive feedback TIA when voltage headroom constraints are applied (i.e., for realistic circuits with biasing circuits), and such models may significantly underestimate the noise level at all frequency ranges.



Figure 11. The noise model from Keshri applied for our set of circuit parameters (dashed lines) and our developed complete analytical noise model for the same set of parameters (solid lines).

One can notice here a distinct difference in the proposed TIA architecture when compared to the classical resistive-feedback approach. In simple resistive-feedback TIA, both the dominating noise source and the gain are mainly defined by the feedback resistor R_F . However, in the proposed design, the baseline noise is defined by a set of different parameters along with a more complex gain definition. We believe that it is exactly this feature of the proposed architecture that provides a better trade-off for the main amplifier parameters when compared to the classical TIA designs still widely adopted for numerous applications [28]. While in the classical resistive approach almost everything depends on a single value of R_F , in capacitive feedback, the dependency is far more complex, which provides the designer with alternative and complementary tuning knobs for circuit optimization and tuning.

A careful inspection of the previous results reveals that the gain adjustment method based on two tuning knobs ($R_{\text{bias},1}$ and C_1) may be also a weakness of the proposed schema. For the exemplary realistic CMOS configuration presented above, the passband in the middle may be not sufficiently flat, as the gain in the low-frequency range is mainly adjusted with the bias resistor of M_1 , while C_1 controls the gain adjustment at higher frequencies. In the particular example above, this leads to a drop of around 0.7 dB Ω and this may have a negative impact on the performance of the complete front-end. The small pitch or step appears in the middle of the passband and it cannot be easily tuned out by a careful selection of both tuning parameters available to the user. In practice, this means that the pitch is likely to be maintained no matter how the two tuning knobs are selected, and the flatness in the passband depends on correspondence between both values, as well as on the rest of the circuit parameters. This may make the process of the gain adjustment far less intuitive.

An idea for the solution comes from the observation that the exact position of the transition point between the frequency ranges (dominated by, correspondingly, $R_{\text{bias},1}$ and C_1) depends itself on the value of r_{DS5} . The preliminary results using the cascode in the current source with the transistor $M_{5\text{C}}$ on top of M_5 confirm that further improvement in base noise levels can be achieved (see Figures 12 and 13) along with the improved flatness of the gain plateau (not shown). The preliminary results for the cascode configuration with $Z_{\text{T}} = 10 \text{ k}\Omega$ confirm that the noise minimum decreases from approximately 1.6 pA/ $\sqrt{\text{Hz}}$ – 1.8 pA/ $\sqrt{\text{Hz}}$ in the case of non-cascode configurations. This is a significant performance improvement in terms of noise at a price of somehow larger r_{DS5} . The BiCMOS-based implementation also demonstrates constant input noise current density over a wider frequency range for the two configurations with the largest gain when compared to the

CMOS-based implementation. Although all configurations demonstrate the noise level for the base gain configuration with $Z_{\rm T} = 10 \text{ k}\Omega$ below 2.0 pA/ $\sqrt{\text{Hz}}$, further work is still needed on the development of accurate models for capacitive feedback TIA with cascode.



Figure 12. Cadence-simulated noise for programmable-gain TIA configuration with cascode I_{SS} in TSMC 0.18 µm CMOS. The horizontal gray dashed line indicates the target noise level of 5.0 pA/ $\sqrt{\text{Hz}}$.



Figure 13. Cadence-simulated noise for programmable-gain TIA configuration with cascode I_{SS} in IHP 0.25 µm BiCMOS. The horizontal gray dashed line indicates the target noise level of 5.0 pA/ $\sqrt{\text{Hz}}$.

5. Conclusions

In this paper, an improved input-referred noise current model is proposed for lownoise capacitive feedback TIA. The noise model complements the previously developed gain model for the programmable-gain TIA architecture extended to support 10 k Ω , 25 k Ω , 100 k Ω , 200 k Ω , and 500 k Ω gains using the arrays of discrete-controlled feedback capacitors and resistances in the biasing circuit. The main sources of noise present in the proposed TIA architecture were studied and their impact on the total noise current spectral density was evaluated. Analytic expressions for the respective noise components were provided along with the discussion on noise minimization strategies. A generalized mathematical model of the noise current spectral density was developed which consists of five noise terms, including those due to nonperfect biasing and flicker noise. The developed analytical model closely matches the numerical results obtained with the post-layout simulation both using 1.8 V 0.18 µm CMOS and 2.5 V 0.25 µm BiCMOS technologies, and provides the basis on which a detailed study on the TIA architecture and verification of the suggested model can be performed. The obtained results confirm that the new model allows an accurate prediction of the performance for the design, with the mismatch between analytical models and computer simulation being 10%–15% in noise current spectral density at the frequency of 500 MHz and gain $Z_T = 10 \text{ k}\Omega$ for the exemplary CMOS and BiCMOS designs. Additional improvement in the noise performance was suggested by introducing a cascode in the current source of the source-follower block. Further work is planned in developing programmable-gain control for the capacitive feedback TIA with cascode, circuit manufacturing, and experimental circuit performance validation.

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