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Accurate Efficiency and Power Densities Optimization of Output Inductor of Buck Derived Converters

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Abstract: In this article, inductor loss models are developed based on the experimental characterization of off-the-shelf components. The modelling steps and techniques are described and validated. It is shown that the model exhibits fairly good accuracy over a large range of ripple current frequency and magnitude. Then, these models are used, as an illustration, in order to present the possible optimization process of the tradeoff between switching frequency-current ripple magnitude and output inductors value in the case of a Buck-derived converter. This optimization has shown that a large current ripple may lead to minimized losses in some cases. The developed modelling technique aims to represent Joules and iron losses, as well as DC and AC losses of inductors. It is not based on physical behaviour description but on mathematical equations based on a set of experimental characterizations. The modelling technique is not suitable for designing the component itself but is useful for selecting the best component value in the manufacturer's series of components. Since it remains difficult with the manufacturer datasheet to estimate AC losses accurately with respect to frequency and ripple current magnitude, a specific characterization is carried out to complement the available data.

Keywords: power electronics; design method; characterization method; ripple current; switching frequency; power density; efficiency; design tradeoffs; off-the-shelf components

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1. Introduction

Power converters are key players toward decarbonation of our modern societies contributing, for example, to the effective usage of electrical energy in most motor drive applications such as mobility, air conditioning, home appliances ... For many years, research and developments are focused on increasing the efficiency, power density and reliability of power converters, working on materials, components, topologies and control strategies. Nowadays, most power converters have reached excellent efficiency levels such as in PV applications with converter efficiency ranging from 96 to 98% [1–3]. Also, converters with very high-power densities are available. For example, three-phase Voltage Source Inverters (VSI) have power densities above 30 kW/L [4]. Nonetheless, the quest to improve further the tradeoff between efficiency and power density remains a specification driver for the domain.

It is well admitted that the power density of power converters is mostly impacted by cooling needs as well as energy storage needs. On one side, cooling is required to remove the generated heat produced by the power converter under operation. The higher the efficiency and/or the maximum operating temperature of components, the smaller the cooling needs. The recent great progress on active devices, with the introduction of Wide-Band Gap (WBG) materials and components, has introduced a shift toward higher Figure Of Merits (FOM) and higher maximum operating temperature, opening the door for drastic cooling needs reduction, even at higher switching frequencies [5,6]. On the other side, energy storage in power converters is necessary to smooth and filter the voltage and current waveforms chopped by the switching cells to pattern the power flow. Regarding

passive components, if significant progress has been reached toward better design, materials and manufacturing technologies, a disruptive shift has still not been identified since the introduction of ferrite materials.

It is well known that a key driver to increasing power density is to increase the apparent switching frequencies of power converters. This can be obtained thanks to multicell interleaved converters such as in [7,8]. Or it can be obtained more classically by increasing the switching frequency of the power converter. If, with the introduction of WBG devices, the increase in switching frequency can be performed at no cost in terms of extra switching losses, on the passive components side, the quest for increasing the switching frequency is not always a success in terms of efficiency. This is mostly due to skin effects that increase Joules losses as well as extra core/iron losses as described in Section 3 of [9]. The impact of the frequency on the extra losses to be produced remains a difficult issue to be precisely estimated during the design process. Indeed, the design methodologies have a limited ability to estimate precisely the impact of switching frequency increase on passive component losses. For power electronics (PE) converter designers, optimizing the switching frequency with respect to efficiency remains a difficult task since no accurate data or model, made available from the component manufacturers, is able to deliver a representative estimate of the magnetic device losses with respect to the actual signal shape and frequency applied to the component. As a consequence, many designers are reluctant to increase switching frequency and/or the ripple voltage and current applied to passive components because their high-frequency behaviour is not easy to forecast. In buck-derived converters such as the chopper or the voltage source inverter (VSI) illustrated in Figure 1, this may lead to a large value and size for the output inductor(s).

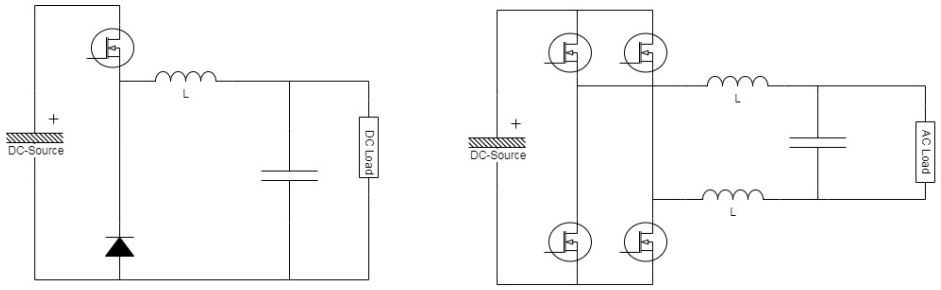

Figure 1. Classical Buck-derived converter topologies. (**Left**) a buck chopper and (**right**) a voltage source inverter.

This paper is investigating the relevance to consider the design procedure only from existing parts, trying to develop a full set of data and models directly from experiments and characterization. Starting from "standardized" off-the-shelf components, the paper is developing a modelling and design approach based on pre-characterized magnetic component series, allowing estimating their total losses properly for any switching frequency and consequently any ripple current. For this purpose, the modelling technique is based on experimental loss characterization on numerous components. From a set of measures, completed with datasheets, a generic mathematical model is derived to express an equivalent series resistance for each component with respect to a set of fitted parameters. This work is applied to an inductor series that is, first of all, studied to extend our knowledge of their characteristics. In order to develop an accurate model, the step-by-step modelling technique leads to a final characterization approach based on representative current waveforms applied to the device under test (DUT). In particular, large signals under variable frequencies are applied in order, to sum up all possible losses induced in the DUT. For this purpose, a particular set-up has been developed in order to measure the losses inside the DUT in these conditions. All losses are then represented by their series equivalent resistance which is parametrized with respect to the inductor value and the operating switching frequency of the converter. The generic mathematical models are then applied

and implemented in the following parts of the paper to outline its benefits and to validate, in real conditions its effectiveness.

In a second time, the paper describes the design optimization that can be carried out thanks to the proposed modelling technique. The objective is to look for the optimal trade-off between efficiency and power density, not only based on component value but also on their actual behaviour. Existing series of components, sharing the same volume, the same materials and the same technologies open up the opportunity to carry on a precise and effective converter design benchmark, looking for the best compromise. Thanks to the modelling technique numerous components and operating points are tested, looking for the best component, minimizing losses and volume. For this purpose, at first, complementary models are introduced in order to define the design and optimization framework. It is then investigated which component is offering the best compromise, in terms of power density versus efficiency from the modelling point of view. The ability to estimate inductor losses accurately for any frequency and current ripple magnitude opens up the relevance to look for the optimal device, leaving free to optimize the switching frequency and consequently the inductor current ripple magnitude. In particular, it is made possible to explore a wider range of design parameters, in a tentative to minimize chopper output inductor losses at fixed volume, material and technology. For this purpose, a special care is given to compare the designs with respect to a set of comparable specifications, including conducted EMI constraints. The last section of the paper is dedicated to the experimental validation of the approach, with efficiency measurements, based on the opposition method, in real conditions for a set of optimal designs.

2. Data Acquisition and Model Construction

L	Main inductor, main inductor value
R_{dc}	Parasitic resistance of L (DC mode)
R_{lr}	Parasitic equivalent AC resistance of L (measured at low current ripple)
R_{hr}	Parasitic equivalent AC resistance of L (measured at high current ripple)
I_{sat}	Saturation current (at 10% inductance decrease)
P_{calc}	Calculated losses
P_{measur}	Measured losses

2.1. Quest for Magnetic Component Size Reduction

Single winding inductors are made out of two main parts, the magnetic core and the winding. In power electronics, for high switching frequency operation, the magnetic cores are mostly realized in ferrite materials while the windings are mostly made out of copper wires. Under operation, both parts are producing losses, which have been widely investigated and modelled in the literature [9–13]. Among them, the impact of the ripple current, its frequency, its shape and its magnitude have drawn a significant interest [14]. Nonetheless, it remains today difficult to forecast properly what the losses are in magnetic devices, especially the ones induced by the high-frequency part of the applied signals. In most design procedures, the switching frequency and the ripple current are selected first to keep reasonable AC losses. Then, the value for the inductor is derived from converter specifications. Prototypes are then manufactured and characterized, based on allowed volume and total losses. Nonetheless, using "reasonable" to qualify inductor losses is never satisfactory for an engineer.

In the proposed approach, we are considering only off-the-shelf magnetic components, pre-designed, optimized and manufactured in volume. Manufacturers are producing component series in which power electronics engineers can select the component they prefer. However, several important data are missing in most manufacturer datasheets, making difficult the selection of the best device. In particular, component loss abacus or equivalent models are missing. In this part, we are considering building a set of data and models, from existing inductor series. These data will be later on used in converters' design optimization.

The characterization and modelling work has been carried out on three series of inductors from Coilcraft manufacturers. Their datasheets are recalled in [15–17]. Some

relevant parameters are summarized in Table 1 below. These three series were chosen for their advanced features such as low ESR, high-frequency working capacity, low volume and their wide range of use. A wide range of inductance values can be seen in each series. They are also declared by the manufacturer as using their most advanced technology.

Table 1. The main characteristics of the three inductor series considered in this work [15–17].

Manufacturer Reference	Volume (mm^3)	Weight (g)	Inductor Value Range (µH)	DC Resistor Range (mΩ)	Frequency Range (MHz)
MSS1210	1353	5.1–6.2	10–10,000	14–7390	4–0.2
MSS1260	777	2.8–3.3	1–1000	5.8–1295	>10–0.6
XGL6060	274	1.41–1.56	0.22–47	1.1–97	50–2

The three series pictured in Figure 2 are mapping a wide range of high-frequency inductor values and current saturation as illustrated in the plot in Figure 3. With this set of components, the power electronics designer has in its hands many options to design power converters in the range of a few tens of volts and amps, leading to converters from tens to hundreds of watts. Maximum energy density can be derived with Equations (1) and (2). In the selected series, the volume energy density ranges from 0.2 kJ/L up to 0.35 kJ/L.

$$Ev = L \times I_{sat}2/V \quad [\mathrm{J/L}] \tag{1}$$

$$Ew = L \times I_{sat}2/W \quad [\mathrm{J/kg}] \tag{2}$$

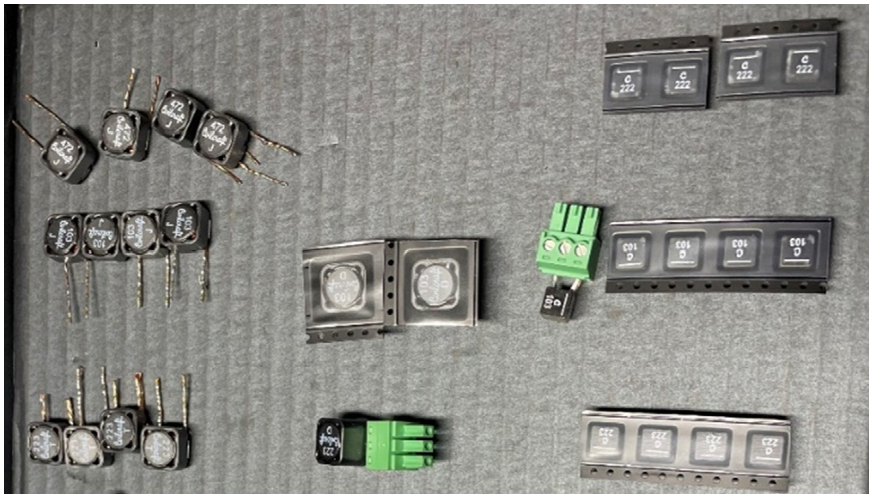

Figure 2. Picture of the 3 inductor series considered in this work [15–17].

Looking at plots Figure 3, one can see that, globally, the maximum stored energy (in mJ) is quite stable within a component series respectively 80, 180 and 500 mJ for series MSS1210, MSS1260 and XGL6060. This points out that each device is individually designed and optimized in a similar way for given material and technology. Also, it confirms that energy density is quite dependent on the component volume of a given material and technology. In other words, for a given series, defined by a volume, a material and a technology, the value of the inductor is inversely proportional to the square of the saturation current. Regarding the energy density itself, one can see that the two series exhibits similar densities while the bigger series exhibits a fairly higher energy density. This might come from a different material or technology or a different proportion between copper and core material.

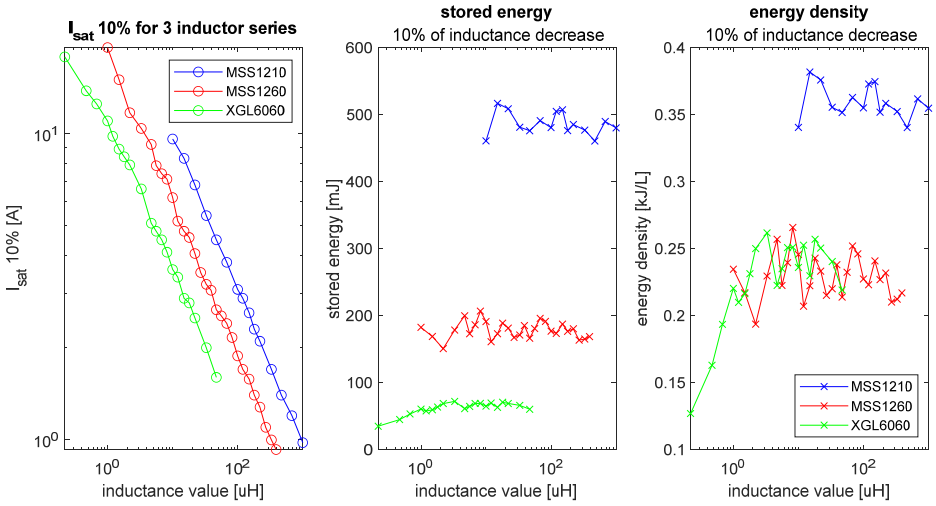

Figure 3. Saturation current (at 90% nominal inductor value) versus inductor value for three Coilcraft moulded inductor series. All data are extracted from [15–17].

Another important parameter made available by the manufacturer is the R_{DC}, the winding resistance in DC. Figure 4 below is providing a logarithm plot to present the evolution of the R_{DC} with respect to the inductor value for the three inductor series.

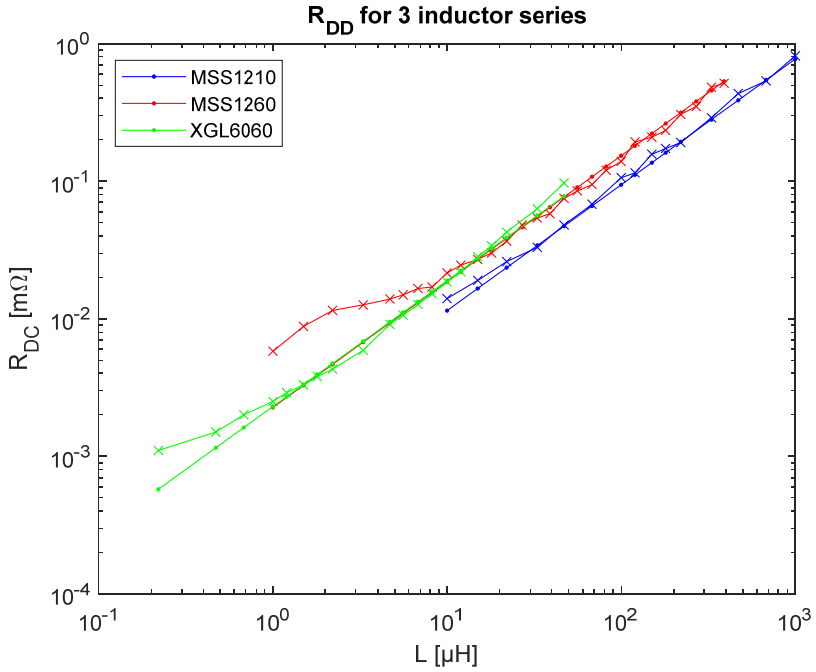

Figure 4. Evolution of the R_{DC} series resistance of the inductors with respect to inductor value for the three studied inductor series [15–17]. Also linearized R_{DC} curves for each inductor series with respect to inductor value.

In Figure 4, it is interesting to see that, no matter the component series, a relation may be found between the series resistance R_{DC} and the inductor value. A simple relationship can be defined to link the DC series resistance of each inductor with its value as (3).

$$R_{DC} = K_l \times L^{P_l} \tag{3}$$

Looking at the evolution of the DC series resistance with respect to inductor value, it is highly desirable to reduce the value of L, in a tentative to reduce the losses of the inductor

under operation. However, reducing the value of L without changing the switching frequency induces an increase in the current ripple magnitude that may produce extra AC losses in the windings and the core as it will be underlined later. To account for this, important knowledge is missing, the evolution of equivalent series resistance of the inductors with respect to the frequency and the magnitude of the ripple current. It is, therefore, necessary to build this complimentary knowledge in order to identify for which component series and for which inductor value, the power electronics designer will get the best compromise in a converter design optimization.

2.2. Inductor Series Resistance Characterization and Modelling

The simplest model to represent magnetic component losses is based on the addition of a series resistance with the inductor. Well parametrized, this series resistance is able to represent the losses in the inductor with respect to the current flowing through the device. In this part, we aim to identify a relationship between the series resistance of the inductor and the inductor value itself. If this generic representation is possible at the inductor scale, it will be possible to use it in the inductor component series. Considering the curves in Figure 4, the value of R_{DC}, can easily be derived with respect to L for any device of the three series, applying linear regression. But it is well k-own that this DC resistance is not representative of the actual resistor of the inductor for high-frequency currents. Skin effects as well as proximity effects are affecting the current distribution in the wire, increasing the apparent resistance. Also, core/iron losses are also generated when AC signals are applied to the magnetic devices. In order to account for it, additional characterization must be performed. The goal of the characterization test bench is to record the power losses into the DUT with respect to realistic and/or representative current waveforms applied to it. To do this, several characterization steps are considered. A first option can be to measure the frequency dependence of the inductor resistance with an impedance analyser. A second option can be to measure the actual losses in the inductor, applying a variable ripple current over a wide frequency range and magnitude, more representative of the actual large signals usually applied to the DUT while implemented in PE converters. The following parts are investigating these two techniques, showing that the first one is not sufficient to describe the characteristics of the tested inductor. It is shown that the most accurate approach to characterize and model the inductor losses is based on a combination of the two methods. Figure 5 presents the characterization and modelling approach used to determine the mathematical model and parameters of the inductor losses. The characteristic factors: R_{DC}, R_{lr} and R_{hr} are going to be presented in the following parts.

2.2.1. Small Signal Loss Characterization and Modelling

A first characterization is made with an impedance analyser (Keysight E4990A + Keysight 16047E from Keysight, Santa Rosa, CA, USA). A first frequency-dependent characteristic of the equivalent series resistance is obtained and depicted in Figure 6. Since the characterization method with the impedance analyser is based on applying low-magnitude HF currents, the obtained characteristic for the equivalent series resistance accounts mainly for the winding resistance. The evolution of the series resistance of the characterized inductor with respect to the frequency is representative of the skin effects as well as the proximity effects in the wire. If the skin effect is to be the major part of the frequency-dependent resistor, this resistance is expected to evolve with the square root of the switching frequency, as explained chapter 5.2 of [10]. As it can be seen in Figure 6, the evolution of the series resistance appears not to be proportional to the square root of the frequency as it would be the case if only skin effects were taken into account. This difference highlights the difficulty to rely only on theoretical models to represent the behaviour of the inductor resistance accurately with respect to the frequency. From this characterization, an equivalent inductor value and frequency dependent resistor model R_{lr} can be derived by fitting the two parameters k_{lr} and P_{lr} in Equation (4). In these parameters, "lr" accounts for "a low ripple" current. This fit can be made by applying common exponential regression on the second

part of the curve. For the characterized inductor, the values for parameters k_{lr} and P_{lr} are respectively 210 and 1.5. As the principal factor frequency dependence in inductors are skin effect and core losses, evolving respectively with the square root of the frequency [10,18] and a power factor between one and two [11,12]. This resistance is a combination of several physical effects with respect to the frequency, it is difficult to represent with theoretical modelling technique without materials and winding knowledge.

$$R_{lr}(f) = L \times k_{lr} \times f^{p_{lr}} \tag{4}$$

$$R_{total} = R_0 + L \times k_{lr} f^{P_{lr}} \tag{5}$$

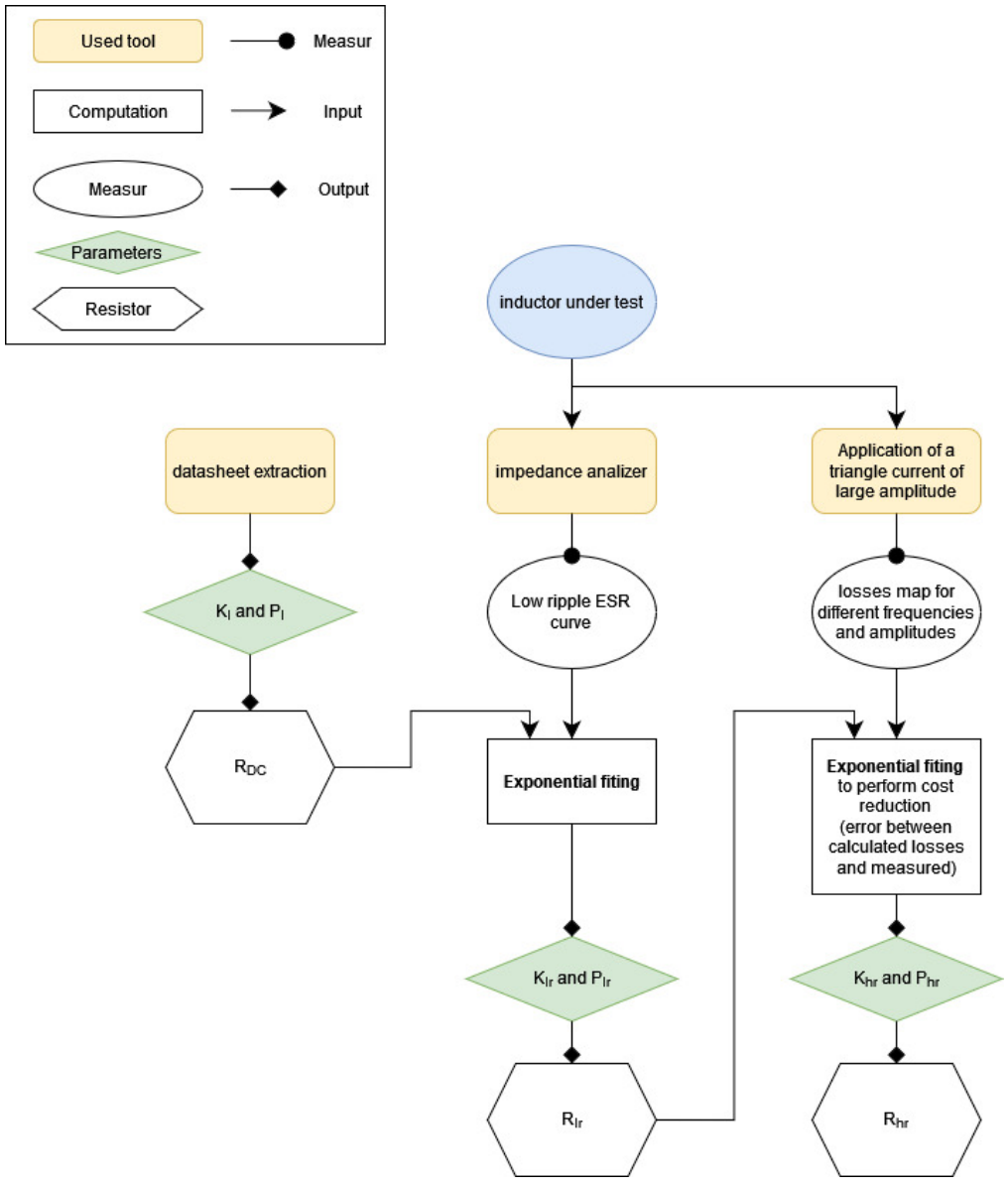

Figure 5. Characterization and modelling approach to derive the generic mathematical inductor losses model and corresponding parameters with respect to inductor value.

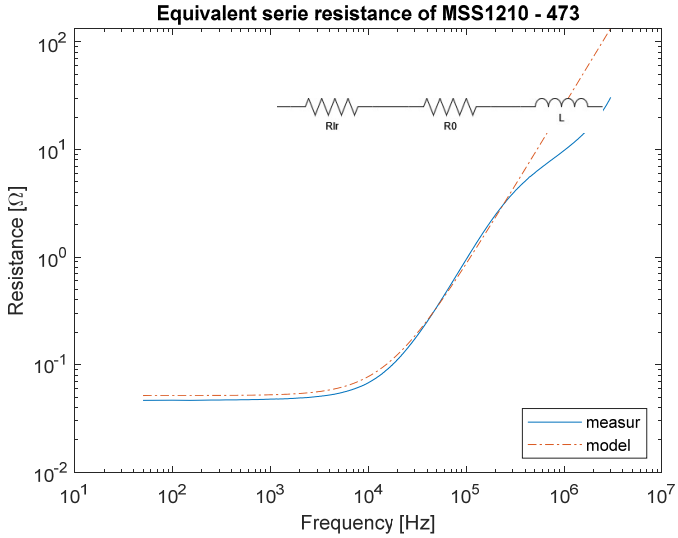

Figure 6. Evolution of the series resistance of the MSS1210-473 47 µH inductor with respect to frequency. Practical characterization in blue and equivalent model in dashed red.

2.2.2. Large Signal Loss Characterization and Modelling

In order to account for the impact of large signals on inductor losses, another type of characterization is necessary. The objective is to apply a large current ripple to the inductors to be characterized, with variable magnitude and frequency. Measuring the induced losses will help derive a more representative model for the total losses taking place in the device under high ripple current magnitude and variable frequency. For this purpose, the inductor is now connected to a full-bridge inverter as depicted in Figure 7. This test bench configuration is offering the opportunity to apply a voltage square wave to the Device Under Test (DUT) that will in turns produce of triangular current waveform, very similar to the one taking place in real conditions. If the applied voltage square wave is a pure AC signal, the resulting triangular waveform will also be an AC signal with no DC part.

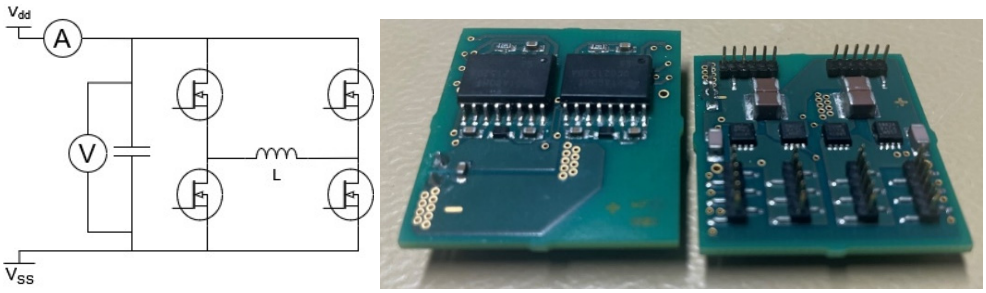

Figure 7. Bench topology for the inductor AC losses measurement under high ripple current and variable frequency. (**Left**) the schematic, (**Right**) the low voltage "high" current full-bridge inverter (30 V up to 5 A).

In fact, this test bench is producing an energy flow from the DC capacitor to the AC inductor and vice versa. No power is dissipated by a load, except for the losses produced by the circulation of power in the components. In this test bench, the total DC power required to supply the full bridge inverter is measured, considering that most losses are dissipated in the inductor. For this, the full-bridge inverter is always operating in Zero Voltage Switching (ZVS) to minimize switching losses while active devices are oversized to minimize conduction losses. Also, they are driven by gate drivers and a control board that is supplied externally. In such a way, the measured losses are mainly the ones taking place in the DUT.

In Figure 8a below, the blue curve with cross presents on the left the evolution of the measured losses inside the inductor for a 1A ripple current over a frequency range from 50 kHz to 150 kHz. In the same plot, the red curve with dots represents the losses estimated with the equivalent series resistance obtained from the previous characterization method. As it can be seen in Figure 8a, taking into account the measured equivalent series resistance from Figure 5, it is not possible to derive the same amount of losses dissipated in the inductor while performing the characterization test depicted in Figure 7. Indeed, in the left of Figure 8 it appears that the inductor losses are significantly underestimated with the model derived from the impedance analyser characterization. To take into account the extra AC losses produced by the high ripple current with respect to the frequency, there is a need to add an additional resistance to the model. For this purpose, the loss curve is fitted by action on the two additional parameters k_{hr} and P_{hr} in the Equation (6). The resulting equivalent resistance is set to produce the same amount of losses with respect to the frequency as is it shown in Figure 7, right. The total inductor resistance is now fully described in Equation (7), also illustrated in Figure 8b.

$$R_{hr}(f) = L \times k_{hr} \times f^{p_{hr}} \tag{6}$$

$$R_{total} = R_0 + L \times k_{lr} f^{P_{lr}} + L \times k_{hr} f^{P_{hr}} \tag{7}$$

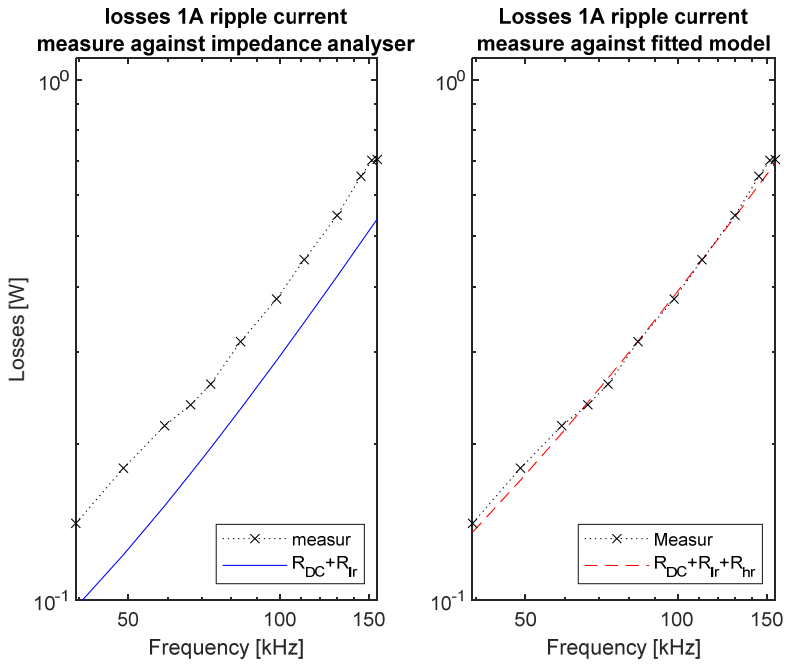

Figure 8. (**a**) Evolution of the power losses in the inductor under test for a frequency range from 50 kHz to 150 kHz. Left, comparison of the losses between the AC losses measure and the model described with Equation (5). Right comparison of the losses between the measure and the model described in Equation (7). (**b**) Equivalent impedance model of the inductor under test.

k_{hr} and P_{hr} are obtained by cost function minimization coded in MATLAB with the cost function calculated as $\sum (P_{measur} - P_{calc})^2$. To calculate the Power losses P_{calc}, the losses caused by each individual harmonics are calculated independently and summed as in Equation (8).

$$P_{calc} = P_{calc} = \sum_{f=f_{sw}}^{N*f_{sw}} \hat{I}_L\,(f)^2 * R_{total}(f) \tag{8}$$

In order to check the validity of the model with respect to the ripple current magnitude, another set of measures is conducted at 100 kHz frequency for ripple current ranging from 0.2 up to 2A. Figure 9 provides a set of curves showing in black the measured AC losses, in blue the losses estimated with the impedance analyser modelling technique and in red the model derived from the AC losses measurements. The bottom plot presents the relative errors between the models. It is possible to see that the model derived from the AC losses measurements is robust to ripple current frequency and magnitude variations. At low ripple current magnitudes, the modelling errors are significant. This is certainly due to the fact that losses are low and harder to measure accurately.

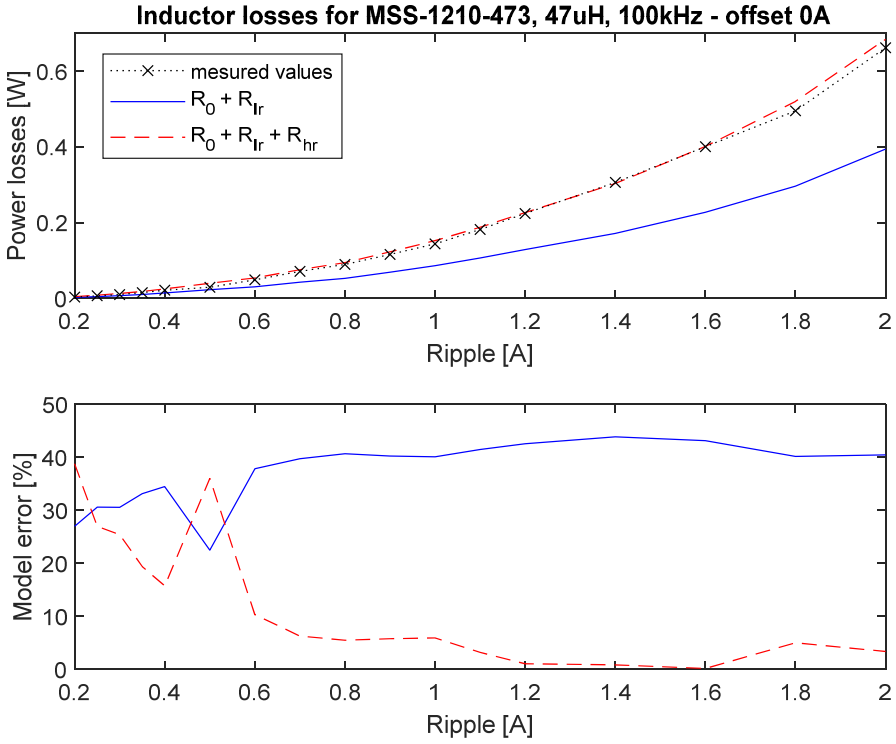

Figure 9. Evolution of losses into an MSS1210-473 47 µH inductor at 100 kHz over a ripple current magnitude from 0.2 up to 2 A. The upper curve represents the losses into the inductor measured and calculated with models of Equation (4) in blue and (6) in red. The bottom curves present the absolute relative errors between the impedance analyser model and the AC loss model.

With this model, there is still a risk to make an estimation error since we did not characterize the inductor losses when a strong DC current is applied in addition to the ripple current. Indeed, the addition of the DC current plus the ripple current magnitudes may exceed the saturation current magnitude. In this case, the inductor behaviour is no more linear. In this paper, we are considering that the inductor is kept used in its linear region, away from the saturation current. In this case, it is possible to consider that the extra losses coming from the DC part of the current will only produce extra Joules losses from the DC resistance of the inductor.

From this characterization procedure, it is now possible to extend it to the entire inductor series from the selected manufacturer in order to develop models that can represent

the evolution of the losses of any inductor with respect to the applied frequency and ripple current magnitude.

2.3. Characterization and Modelling Extension to Inductor Series

This characterization and modelling methods have been applied to three Coilcraft inductor series named MSS1210, MSS1260 and XGL6060. The curves in Figure 10 show the characterization results for a set of inductor values in each series. Red dashed lines are presenting the modelled curves with the extraction of parameters listed in Table 2 hereafter. The parameters K_{lr} and P_{lr} are equivalent and comparable to the logic shown in [11] as the K_{lr} (k_i in [11]) is high for material that accepts low frequency as N87 and lower for high-frequency materials. As well, P_{lr} (α in [11]) is close to two for high frequency material. These factors show that HF materials will brutally lose their interest at a given frequency (when R_{lr} became predominant in front of R_{hr}).

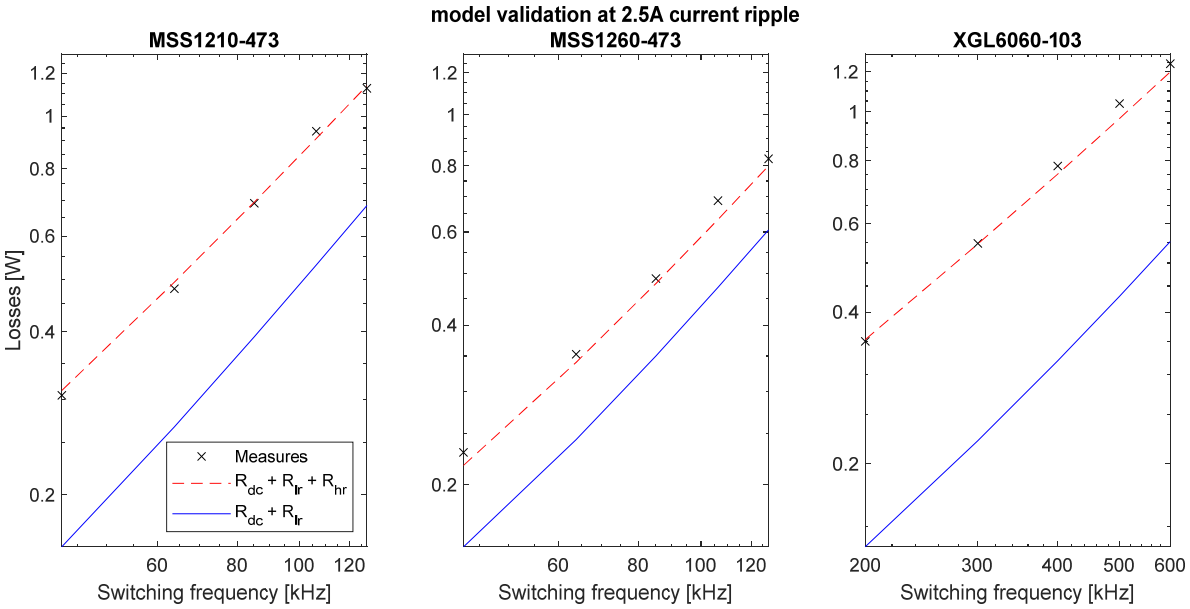

Figure 10. Evolution of the losses produced by three inductors under test. Validation of the $R_{dc} + R_{lr} + R_{hr}$ model.

Table 2. Series resistance model parameters for the three manufacturer inductor series.

Inductor Series		Factor	MSS1210	MSS1260	XGL6060
Volume (mm^3)		1	1353	777	274
$R_{DC} = K_l * L^{P_l}$	K_l	1	430	700	710
	P_l	1	0.915	0.915	0.915
$R_{lr} = L * K_{lr} * f^{P_{lr}}$	K_{lr}	1×10^{-3}	210	88	0.3
	P_{lr}	1	1.5	1.55	1.9
$R_{hr} = L * K_{hr} * f^{P_{hr}}$	K_{hr}	1	67	45	134
	P_{hr}	1	1.049	1.089	1.028

The produced models are now ready to be used in converter design optimization. It is important to notice that this model offers the possibility to identify the origins of losses. By taking into account R_{dc} the part of the losses due to RMS currents is identified. Moreover, with R_{lr} and R_{hr} the losses due to the high-frequen ripple current are extracted. This will allow comparing and optimising inductor value, switching frequency, and ripple amplitude into converters to minimize total losses.

2.4. Limits of the Model

This model is developed to assist designers in their choice of a magnetic component inside a predefined, preselected series of components. Since it requires significant characterization work, the selection of component series must be performed prior to its detailed characterization. This is the reason why the modelling technique developed here is mostly applied in the paper to carry component value selection rather than component technology selection. Of course, one can still explore and compare component technologies with this modelling technique. Also, at this stage of the modelling development, this model does not consider exceeding saturation limits nor the maximum frequency range, each time it has an effect on the inductor value, out of the linear region. The more the inductor will be used under the condition that exceeds linearity, the less the model will be efficient. J. Kaiser & T. Dürbaum [19] presented an overview of the uses of saturable inductors. It is complementary to this work as it relates results out of its scope.

3. Complementary Model Description

C_{x1}, C_{x2}	Values of the filtering capacitor
$E_{C_{oss}}$, E_{Ciss}	stored energy into parasitic capacitors
I_{sw}	Switched current
I_L	Current flowing through L
L	Value of the main inductors
L_{filter}	Value of the filtering inductors considered as 1 inductor
$R_{lisn_{100}}$	Total output resistance of the LISN (100 Ω)
t_{dt}	Dead time
V_{drop}	Voltage drop due to body diode
V_{DS}	Drain-Source voltage
V_{lisn}	Voltage measured on one LISN resistor (50 Ω)

3.1. Design Frame Considerations

As introduced in Section 2, during power converter design, the selection of the optimal inductor value relies on the operating conditions and the design specifications in terms of targeted power density and efficiency. Playing with switching frequency and current ripple magnitudes impacts on many other elements of the design. It is well known that increasing the switching frequency may induce extra switching losses in active devices. Also, increasing current ripples will increase RMS current, which in turn, will produce extra conduction losses in all devices, including active devices. Nonetheless, as mentioned in the introduction, it is believed here that thanks to the introduction of WBG devices, it is today possible to increase RMS current and switching frequency without producing extra losses in active devices compared to the state-of-the-art silicon-based active devices. Nonetheless, for the purpose of validation and illustration, active device switching and conduction losses must be taken into consideration in the design and optimization process of a power converter. For this, a simple model is proposed in the following part.

Second, increasing switching frequency and inductor current ripples will have an impact on the converter conducted EMI. In particular, differential mode conducted EMI is strongly dependent on the input inductor size in most Buck-derived topologies such as the well-known Voltage Source Inverter (VSI). It is therefore important to consider in this work a max value for the current ripple exiting the converter. In other words, if the optimization process of the inductor leads to a large ripple current, way above reasonable limits, an extra-filtering stage will have to be considered and added to the comparison. An important part is provided below to settle properly how EMI constraints are taken into account for the selection of the optimal inductor value.

These design considerations are going now to be developed in order to be taken into account for the selection of the optimal inductor value and then designing a buck-based power converter.

3.2. Active Device Losses in the Converter

The losses of active components are partially frequency-dependent. These are called switching losses. There are a lot of complex models able to describe switching losses [8,20–22]. For silicon MOSFET power devices operating under a very fast switching transition, a simple one is to consider the switching losses with respect to the stored energy into parasitic capacitor Coss. Since Coss is a nonlinear capacitor, special care must be paid to estimate the energy stored in the Coss. From MOSFET manufacturer datasheets, one can derive the total energy stored in Coss, using Equation (9). Considering that each time the transistor switches ON, the entire energy stored into Coss is dissipated through the channel of the device [20,22], then switching losses can be derived thanks to Equation (9) below. This switching loss modelling technique is valid only if the MOSFET is switching very fast. The transistor used to make the test bench being (SIS862DN-T1-GE3), the stored energy in Coss can be extracted from the datasheet according to the curve pasted in Figure 11. Parameters in Equation (12) are derived to fit Coss versus Vds. Transistor gate drivers are also dissipating the loss function of the switching frequency. In the transistor datasheet, the stored charge can be easily derived from tables and abacus. For hard switching operation, both losses must be taken into consideration. For soft switching, only driver losses must be considered.

Additional losses must be taken into consideration. When MOSFET-MOSFET switching transitions are considered, a short deadtime is nonetheless necessary to avoid short circuit operation [20]. At each switching time, a dead time of 100 ns is applied between off and on. This dead Time is necessary to prevent cross commutation in hard switch and allows ZVS switching but causes body diode conduction [23,24] making extra losses. These losses are considered in Equation (11).

$$E_{C_{oss}} = \int_0^{V_{max}} C_{oss}(v_{DS}) v_{DS}\, dv_{DS} \tag{9}$$

$$E_{C_{iss}} = Q_{iss} \times v_{GS} \tag{10}$$

$$E_{body} = t_{dt} \times V_{drop} \times I_{sw} \tag{11}$$

$$C_{oss}(V_{DS}) = 760 - V_{DS}\frac{760-400}{760} + \exp^{-(V_{DS}*0.17-6.7)} \tag{12}$$

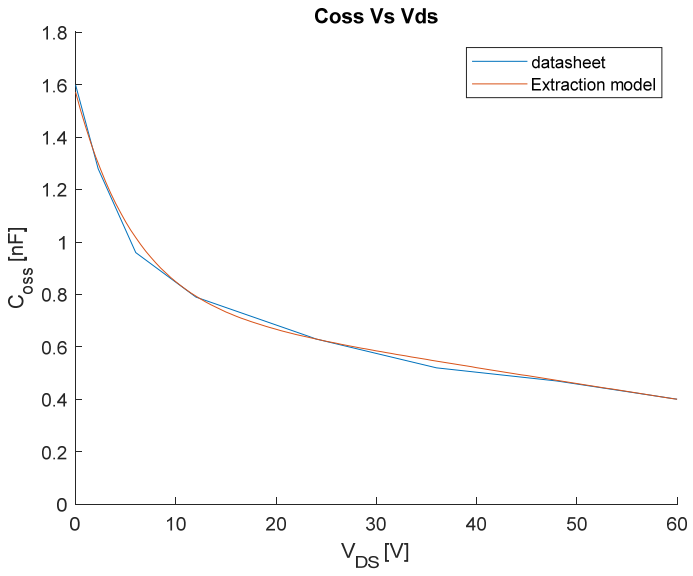

Figure 11. C_{oss} of the transistor SIS862DN-T1-GE3 versus Drain-source Voltage from Equation (12) in red and from component datasheet [25] in bleu.

Equation (12) is a mathematical representation of the non-linear capacitor C_{oss}, following its evolution with respect to Drain Source voltage across the MOSFET. It is illustrated in Figure 11 below.

3.3. Setting the EMI Constraints

As mentioned above, a clear design frame must be defined in order to take into account the impact of frequency and inductor ripple magnitude on conducted EMI. For this purpose, it is defined that the output ripple current going out from the converter must not exceed some limits. Taking into consideration conducted EMI regulations [26,27], in a tentative to make it clear and simple to use in the inductor value selection process, it has been defined that the current harmonics are going out of the power converter, flowing into the two 50Ω resistors of a conducted EMI testing equipment, should not exceed 60 dBµV no matter the frequency considered. These choices are slightly different from the regulations. Nonetheless, they are offering a realistic reference that eases the design and optimization process. Figure 12 below presents the schematic of a typical differential mode (DM) input filter circuit inserted between the converter itself and the LISN (Line Impedance Stabilization Network) testing equipment considered for conducted EMI compliance.

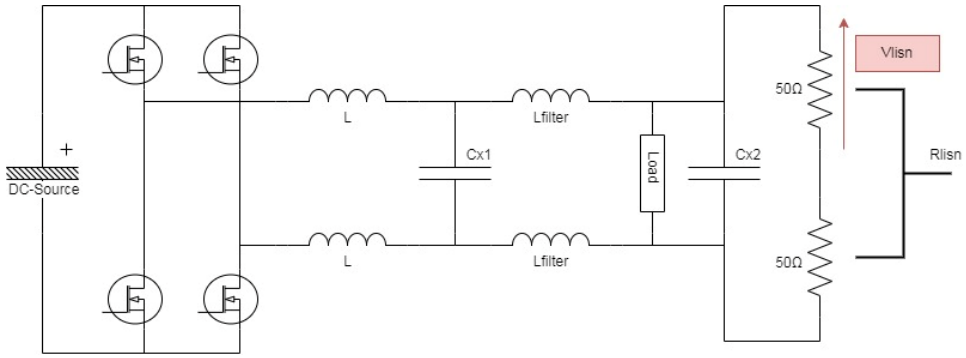

Figure 12. Schematic of a VSI + its differential mode input filter for conducted EMI compliance + the LISN resistors (LISN simplified representation in high frequency range).

In this schematic, a traditional differential mode filter topology is considered, with symmetric input inductors L (one on the phase and one on the neutral) together with Cx1 and Cx2 capacitors for DM current ripple filtering, between the converter and the LISN, used for normative tests. In the upper-frequency range, above 100 kHz, the LISN looks similar to a set of two 50 Ω resistors, from which, one can measure the current flowing through. Setting the limit at 60 dBµV across each LISN resistor means that the maximum current ripple harmonic must not exceed 2µA. If the input inductor current ripple magnitude is higher, the C_{x1} and C_{x2} capacitors will have to be adjusted to filter the current harmonics. If the C_x capacitor value exceeds 20 µF, extra L_{filter} filtering inductors will have to be inserted between C_{x1} and C_{x2} in order to increase the global filter order as shown in Figure 13. A limit for C_x has been introduced because large C_x capacitors have low resonant frequencies, preventing them from a satisfactory filtering over a large frequency range.

The Equation (13) below presents the ideal attenuation with respect to the frequency offered by a C_x capacitor filter topology, considering C_x equals $C_{x1} + C_{x2}$.

$$\frac{V_{lsin}}{I_L} = \frac{(R_{lisn_{100}}/2)}{1 + Cx \times R_{lisn_{100}} \times j\omega} \tag{13}$$

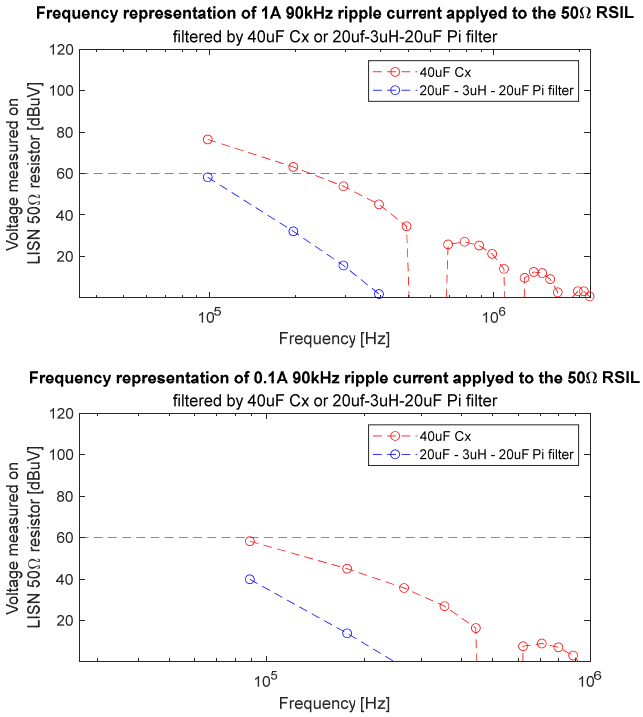

Figure 13. Frequency domain representation of 1A magnitude at 83% duty cycle filtered by a Cx capacitor of 40 µF or by a $C_{x1} - L - C_{x2}$ filter (C_{x1} = 20 µF, L = 3 µH, C_{x2} = 20 µF) to meet the 60 dBµV limits using Equation (15) to calculate the value of L.

Please note that the LISN total resistor is 100 Ω, the sum of two 50 Ω resistors. However, the probe is inserted across one of the two resistors, justifying the factor 2 in Equation (13) above. Also, in Equations (13) and (14), I_L is the current flowing in the inductors of the chopper.

Equation (14) below presents the ideal attenuation with respect to the frequency offered by a $C_{x1} - L_{filter} - C_{x2}$ filter topology. The operation to select the minimum inductor value for this filter is described in the following Section 3.3.2.

$$\frac{V_{lsin}}{I_L} = \frac{(R_{lisn_{100}}/2)}{1 + j\omega\left(R_{lisn100}C_{x1} + R_{lisn_{100}}C_{x2}\right) - \omega^2\left(L_{filter}C_{x2}\right) - j\omega^3\left(R_{lisn_{100}}L_{filter}C_{x1}C_{x2}\right)} \tag{14}$$

3.3.1. Values of Filtering Components and Design Considerations

To be able to compare the different design optimization choices (frequency and ripple associated with an input inductor) it has been chosen to use a 2 × 20 µF C_x capacitor filter when sufficient or a 20 µF − X µH − 20 µF for higher ripple current. The extra losses and volume produced by the addition of L_{filter} inductors will be taken into account during design optimization.

3.3.2. Modelling of Additional Losses Resulting from Filtering

The implementation of the DM filter induces additional losses due to current flow through additional capacitors and inductors. These passive components can also be represented by equivalent series resistance (ESR) to account for extra losses. Due to the evolution of the filter depending on the frequency and the amplitude of the current ripple, it is necessary to estimate these additional losses for each case. The current flowing through the filtering inductors L_{filter} is the full current filtered as described in Equation (15).

$$\frac{I_{Lfilter}}{I_L} = \frac{1}{1 + \frac{C_{x1}}{C_{x2}} - \omega^2 L_{filter}C_{x1}} \tag{15}$$

The minimal standard value of L matching the condition of switching frequency first harmonic under 60 dBµV on two RSIL resistors from Equation (16) is then selected:

$$L_{filter} > \left| \frac{\frac{I_L \times R}{2V_{max}(1+i\omega_{sw} \times R \times C_{x2})} + 2}{-\omega_{sw}^2 \times C_{x2}} \right| \quad (16)$$

With V_{max} = 1 mV = 60 dBµV.

The losses due to these components are calculated using the same process as the one used for the output inductors L developed in Section 2.

3.3.3. Filtering Capacitor Losses Modelling

Filtering capacitors are usually high-quality components, with fairly low equivalent series resistance (ESR). Nonetheless, large ripple currents may flow in these components making it necessary to estimate their losses accurately. For this purpose, manufacturers provide ESR of their capacitors. From their characteristics, it is possible to derive a representative ESR model. In our experiments, we are using ceramic capacitors from the manufacturer Murata. Murata is providing accurate ESR curve for all its components from a web application [28]. In Figure 14 below are plotted a set of ceramic capacitors ESR versus frequency.

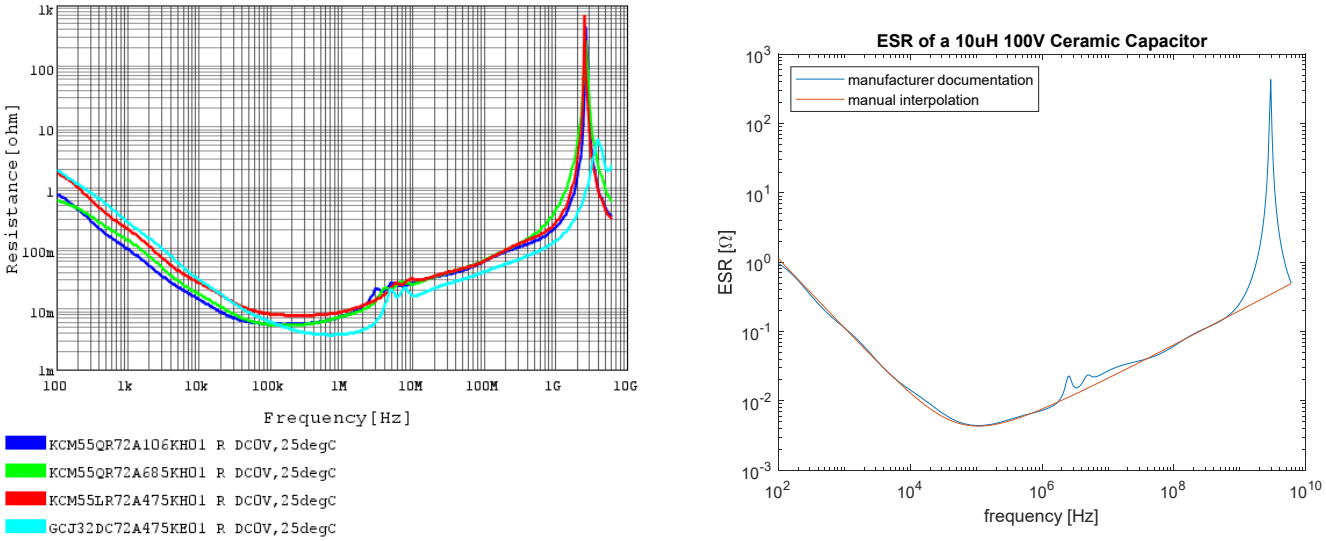

Figure 14. Ceramic capacitor equivalent series resistance with respect to frequency. (**Left**), manufacturer data, (**right**), equivalent model representation for the series resistance with respect to frequency.

Since the various ceramic capacitors have a comparable ESR, the model considered here, will be the same for all capacitor values.

The chosen interpolation curve (in red) follows the mathematical variation of Equation (17) below. This curve has been manually fitted with $R_{c0} = 0.0012$; $k_{c1} = 112$; $k_{c2} = 160E3$. With k_{c1} and k_{c2} fixed to match the elbow.

$$ESR(f) = R_{c0} + \frac{\sqrt{f}}{k_{c1}} + \frac{k_{c2}}{f} \quad (17)$$

In order to derive losses in C_x capacitors, the RMS current in each component must be derived. If no L_{filter} is inserted, the current flowing through the capacitors C_{x1} and C_{x2} is the one flowing inside inductors L. Therefore $I_L = I_{C1}$. If L_{filter} are inserted, the currents flowing inside C_{x1}, C_{x2} and L_{filter} must be derived. $I_{Lfilter}$ is derived thanks to Equations (18)

and (19). C_{x1} capacitor current is the difference between I_L and $I_{Lfilter}$. As well, C_{x2} current is expected to be the same as $I_{Lfilter}$. These Equations are supposing an open output load.

$$\frac{I_{c1}}{I_L} = \frac{\frac{C_1}{C_2} - \omega^2 LC_1}{1 + \frac{C_1}{C_2} - \omega^2 LC_1} \tag{18}$$

$$\frac{I_{c2}}{I_L} = \frac{1}{1 + \frac{C_{x1}}{C_{x2}} - \omega^2 LC_{x1}} \tag{19}$$

3.4. DC Resistance of the Converter

Due to the modularity of our test bench, there are a total of 10 connector's contacts in series with the main current way causing a not negligible DC resistivity. A measure of this total resistor has been made in DC with a shorted output at 3 A. the parasitic series resistor has been measured as 60 mΩ (180 mV). Considering the 2 × 10 mΩ due to the transistor (SIS862DN-T1-GE3) commended with a grid at 6.5 V. It is undoubtedly that the conception of the test bench, by adding 40 mΩ, will result to overestimate the losses due to RSM-current in regard to an optimal full soldered design.

3.5. Limits of the Models Considered in the Optimization Loop

The scalability of the models is discussed in this paragraph. Regarding the modelling technique of inductors, its scalability is possible as long as the component usage remains in the linear region with respect to inductor value. This means that the model will need to be improved if the devices are used in the saturation region or with high switching frequencies that significantly impact its behaviour. Regarding the other models considered in the optimization loop, it was not our purpose to propose a universal modelling technique for all components. In particular, our aim was mainly to implement and illustrate how useful and effective the proposed modelling technique is for inductors. In this respect, the simplicity of the loss model used for active components is not going without strong limits. It is used here under specific conditions. The switching time in hard switch mode is considered under 10 ns keeping switching losses low. When the DC supply voltage becomes higher, it is rarely possible to force the switching time to be this low due to higher grid capacitor and EMI considerations. To be able to use a complete model of converter losses at a higher voltage or with cheaper components, the user should use a more accurate model for active components [21,29].

4. Theoretical Optimization of Converter Inductor

Thanks to accurate losses modelling of inductor series together with input filter components, it is now possible to look for the optimal trade-off in terms of switching frequency and current ripples in the inductor while designing a buck-derived power converter. It is a partial design optimization since only input inductors + input DM filter are considered and selected in this paper. Nevertheless, it will be shown that it provides interesting optimization results. Also, this design optimization procedure may take part in a more global converter optimization work.

4.1. Frequency and Ripple Optimization for One Inductor Value

With the models that have been established in Sections 2 and 3 based on characterizations, a theoretical optimization of a symmetric DC to DC converters (two interleaved choppers) is presented in this part. This optimization aims to minimizthe e losses at input inductors + filter stage while keeping volume minimal. For this purpose, considered losses include losses in inductors L, in C_{x1} and C_{x2} capacitors and in L_{filter} inductors when applicable. As the losses due to C_{x2} are not dominating (<<1%) and these losses should not become significant no matter the frequency and current ripple in the inductor L, the losses will be considered as if the converters were not interleaved. Also losses in the converter

due to transistors DC resistance, as well as switching losses due to hard switch modes and transistors gates losses will be considered as described in Section 3. These losses will be calculated for each combination of ripple current amplitude and switching frequency.

4.1.1. Losses in the Main Inductors

The following operating point is considered for the design optimization: V_{in} = 30 V, V_{out} = 20 V, $\langle I_{out} \rangle$= 2.5 A. For a given inductor value of 47 µH, the losses in the output inductors with respect to frequency are provided in Figure 15 below. One can see in the plots the losses due to the DC current (left), the losses due to HF current harmonics (centre) and the total losses in the inductors (right). It appears that no matter the type of losses, they all decrease with respect to the frequency. Indeed, increasing the switching frequency reduces the ripple current magnitude, which in turn reduces the RMS current value. This has a direct impact on the DC losses. Looking at HF losses, on one side, increasing the switching frequency increases ESR resistance (representing core losses and skin effects) but it also reduces the magnitude of the current harmonics. All in all, the higher the switching frequency, the lower the HF losses. Total losses are therefore decreasing with respect to switching frequency.

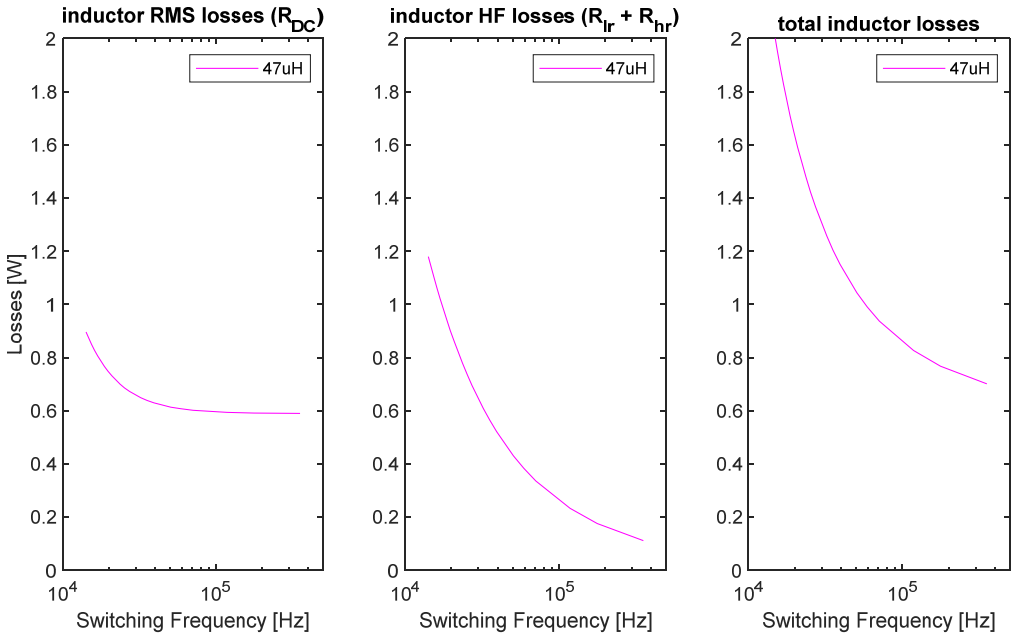

Figure 15. Inductor losses calculated for the two MSS1210 inductors of bidirectional full bridge converter working under 30 V input with 20 V output at 2.5 A.

4.1.2. Active Device Losses in the Converter

Considering Section 3.4, the energy of transistors switching has been extracted from the datasheet of the transistors as illustrated in Table 3. This model might be quite simple but is not subject to important variation and produces representative results as long as the assumptions introduced in Section 3 are valid. At each switching period, this energy is lost twice. Because at each commutation there are two switching events.

Table 3. Energies lost at each commutation due to C_{oss}, C_{iss} and body diode conduction.

Parasitic Capacitor	C_{oss}	C_{iss}	Transistor Body Diode
Voltage	30 V	6.5 V	0.7 V
Stored energy	287 nJ	81 nJ	$70 * Isw$ nJ

Figure 16 presents the switching losses into the active devices caused by these three factors in the case where a 47 µH inductor has been chosen. As expected, in the curve in Figure 16, the active device losses are increasing with increasing switching frequency.

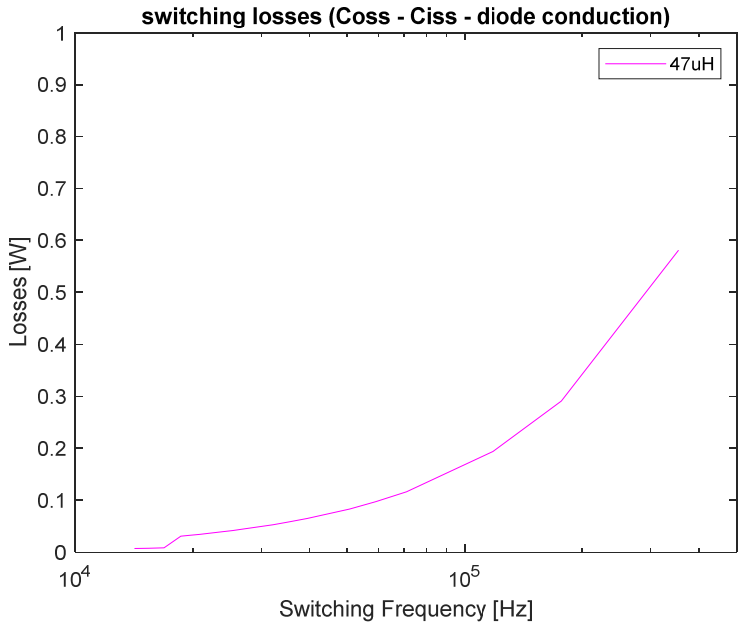

Figure 16. Switching losses made by the four transistors depending on the switching frequency in a converter using two 47 uH main inductors.

4.1.3. Losses in the Differential Mode Filter

In Section 3 the modelling technique to derive the losses in the differential mode filter with and without L_{filter} was introduced. L_{filter} inductor values are chosen for the XGL6060 component series and capacitors are paralleled 10 µF ceramic capacitors. In order to account for capacitor derating with respect to the voltage rating, six 10 µF ceramic capacitors are used to implement a 20 µF C_x capacitor (at 20 V). Figure 17 below presents the evolution of the losses inside the DM filter with respect to the frequency for the operating point defined above and for main inductor values L = 47 µH. In this particular case, the value for the filter inductor L_{filter} is adapted with respect to the ripple current flowing across the main inductor L. This is the reason why there are different slopes in Figure 17. As can be observed in Figure 17, the filter losses are also decreasing with respect to the frequency.

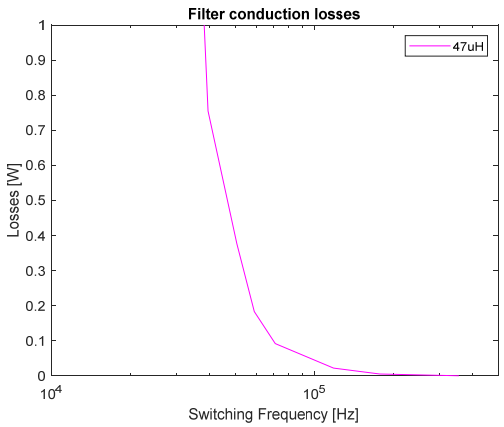

Figure 17. Losses caused by the two filtering inductors depending on the switching frequency in a converter which 2 × 47 µH main inductors.

Increasing the frequency leads to reduced ripple current which in turn leads to reduced HF losses in the filter.

4.1.4. Optimal Switching Frequency for the Specific Inductor

To finalize the design optimization with the operating point defined above and the 47uH inductor considered as a first example, all losses are computed. Figure 18 is presenting the resulting total losses with respect to the frequency and the ripple current magnitude. As expected, the losses are reducing with respect to the switching frequency up to a minimum value. Then losses are rising again with respect to switching frequency. We can see that for this specific inductor value the optimal operating point is a little bit over 1 A of current ripples (>40% of the DC current in the example).

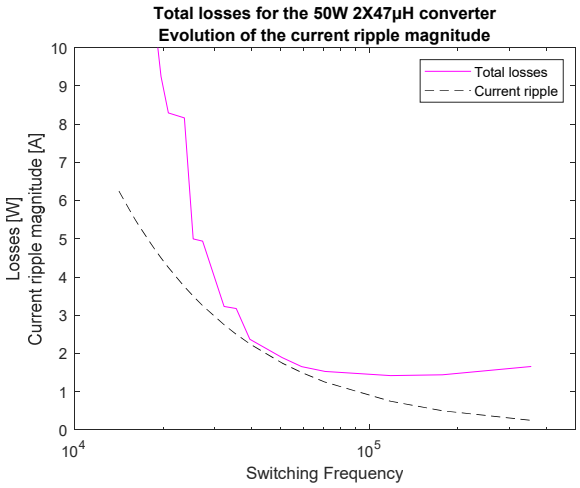

Figure 18. Calculated total losses into the full-bridge converter considering all losses modelled in Section 3. These losses are considered for a 30 V to 20 V, 50 W converter equipped with 2 × 47 µH main inductors.

From this first result, it appears that reducing the ripple current would lead to minimum losses. It is interesting to notice that quite reduced ripple current may not lead to minimum losses in this particular case. Nonetheless, it is important to keep in mind that the differences are not very important and could come from uncertainties. Let us now investigate what design optimization we can reach if an entire inductor series is considered.

4.2. Application to the Three Sets of Inductors

With the example of a switching frequency optimization made with one specific 47 µH inductor from Coilcarft MSS1210 series, it is now possible to apply this work to the three series of inductors considered in this paperwork. This part will propose an optimization result of the F-R-Oi (Frequency Ripple Output inductor) for the losses into the bidirectional 50 W, 30 V to 20 V converter.

4.2.1. Losses in the Main Inductors

Similar to Section 4.1.1, the losses in the main inductors have been calculated for each series and are presented in Figure 19 with respect to switching frequency. Purple curves represent the 47 µH values (as in Section 4.1). These curves show that due to the rising of R_{lr} *and* R_{hr} with the frequency, there is a rise in the losses at low switching frequencies (left side of each curve). The losses for each inductors value will decrease with the frequency increase (leading to a reduction of the ripple current) down to losses due to R_{DC} These results are comparable to [18] as it shows the equilibrium between skin effect and losses due to current ripples. However, the interesting part of each value is where the loss into the inductor is lightly dependent on the Frequency-Ripple-Output inductor (F-R-Oi).

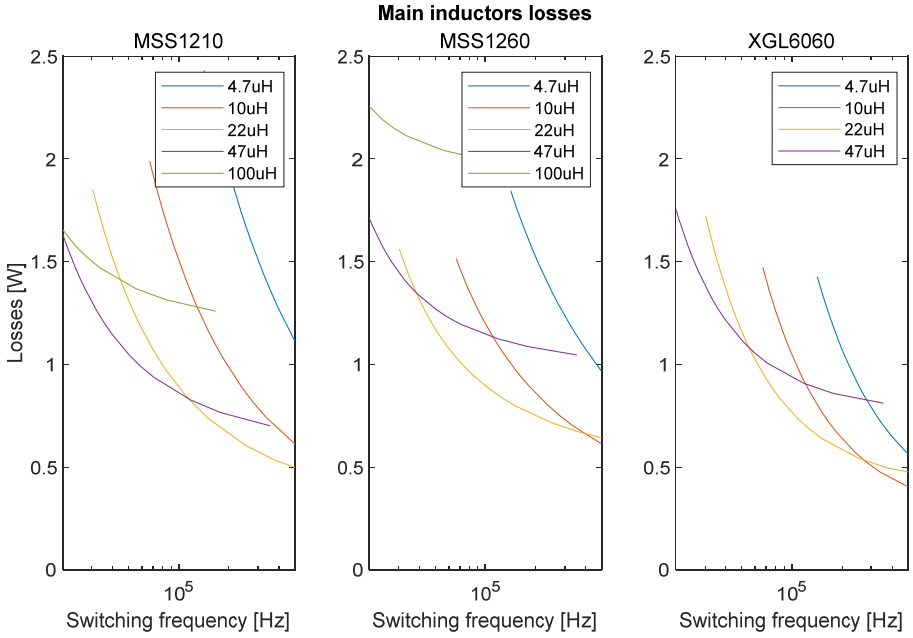

Figure 19. Losses into the main inductors, for multiple inductor values in the three series.

Decreasing the inductor value will decrease the losses at the same frequency if the losses due to $R_{hr} + R_{lr}$ are not prevalent.

4.2.2. Active Device Losses

As presented in Section 3, the active device losses are dependent on the switching frequency. It grows higher with the frequency (with the exception of full ZVS mode). For each inductor value, a step due to ZVS mode is placed at a different frequency (see Figure 20), it is explained by the fact that the ZVS appear at iso-ripple and not iso frequency. The rising of the frequency will be opposed to the benefit of the F-R-Oi shown in Section 4.2.1.

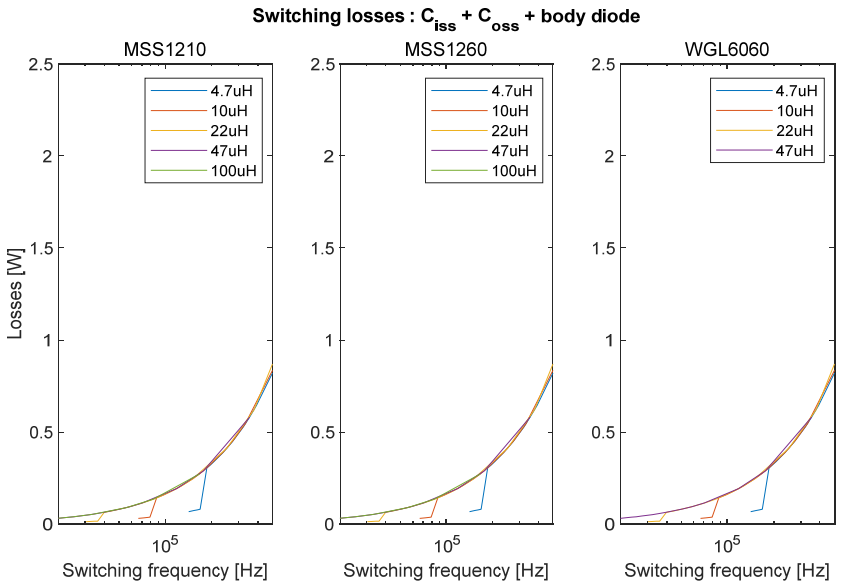

Figure 20. Active device switching losses for a 50 W–30 V to 20 V converter with respect to the main inductor value and the switching frequency.

4.2.3. Losses in the Input Filter

As presented in Section 3.3, the minimum filtering inductor value needed to comply with the 60 dBµV has been calculated for each F-R-Oi value. Losses due to this filter have been calculated accordingly. Thanks to the high quality of ceramic capacitors and their low relative ESR, the prevalent part of the losses in the π filter is due to the R_{DC} part of the filtering inductors' ESR. The estimated losses inside the filter are presented in Figure 21. The steps on each curve are the result of a decrease in value implying a decrease of R_{DC}. While at the same ripple, the value of the main inductor is low, the frequency is high. This means that the value of the filtering inductor is lower, lowering the global losses. However, for an iso-frequency, the lower the main inductor value is, the higher the value for the filter inductor.

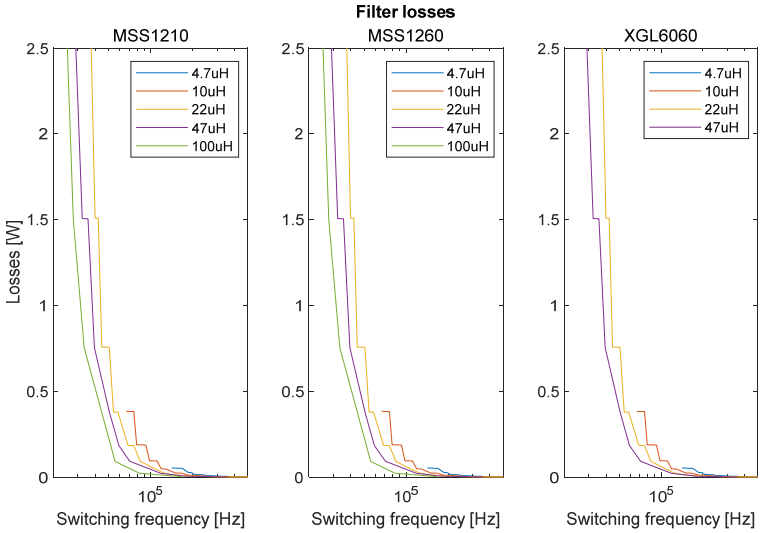

Figure 21. Losses in the output filter depending on the main inductor values (coloured curves) with respect to the switching frequency. The filtering inductor values are the minimum discrete standard values complying with the 60 dBµV limits at LSIN resistors as proposed in Section 4.1.

4.2.4. Optimal F-R-Oi

From the three previous Sections 4.2.1–4.2.3 and according to Section 4.1.4, it is then possible to calculate the total losses in the converter processing 50 W from 30 V to 20 V. It includes the losses in the main inductors, the active components, the output filtering stage and the parasitic DC resistance of the converter. With the values shown on Figure 22, it is possible to conclude the theoretical optimal Frequency-Ripple-Output Inductor (F-R-Oi) and compare the different off-the-shelf inductors and select the one that would offer the best compromise.

Although the different series have different volumes, it is interesting to note that the losses on the optimum are around the same value for the three inductors series. But the lower the volume is, the lower the optimal inductor value is, and the higher the ripple current is. The optimum can be found around a switching frequency of 100 kHz. Figure 23 presents the same result as the frequency is linked to the ripple current by the inductor value. As the optimum switching frequency is around 100 kHz, the optimum ripple current magnitude is around 1.25 A for an average current of 2.5A. Therefore, the optimal ripple current magnitude seems to be located at about 50% of the average current in this particular design case study. This is significantly higher than what the power electronic design engineer considers, usually more in the range of 10 to 25%. It is even above the standard recommendation of 20 to 40% proposed by manufacturers as in [30–32]. With these considerations, for each series, an optimal working point has been found with a pair of 22 µH inductors and losses extracted in Table 4.

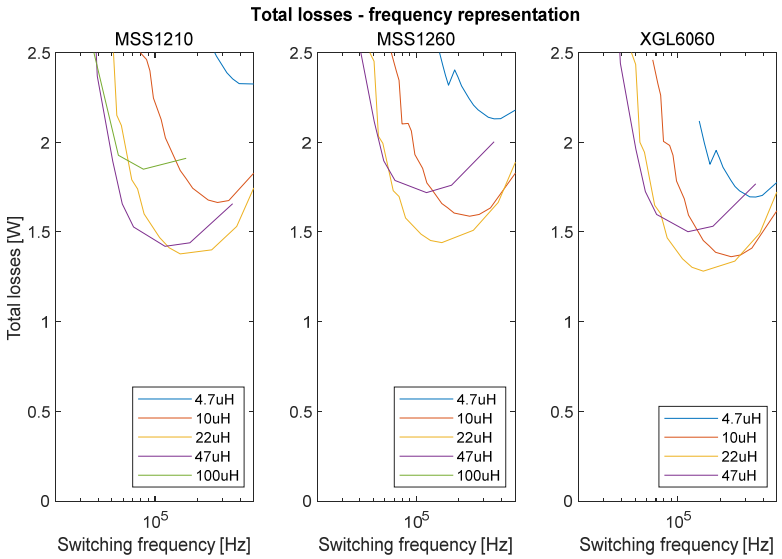

Figure 22. Total mosses modelling results for the three inductor families. Total losses are represented as a function of the switching frequency and the inductor values.

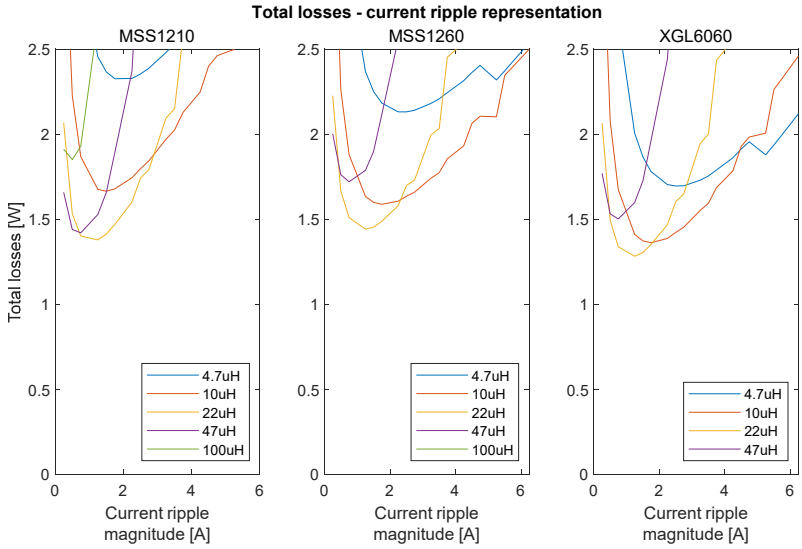

Figure 23. Model results for the three inductor families. Total losses are represented as a function of the Current Ripple and the inductor values.

Table 4. Calculated losses at global optimums for each series and individual main inductor losses at these optimums.

Serie	MSS1210	MSS1260	XGL6060
Optimal total losses	1.38 W	1.44 W	1.28 W
Main inductor losses	2 × 0.37 W	2 × 0.40 W	2 × 0.32 W

Before concluding this design and selection process, it is needed to check if the selected inductor is able to handle the heat that will be produced under operation. For this purpose, it is needed to check if, from a thermal point of view, the design compromise is feasible.

4.3. Thermal Considerations

Another dimensioning factor of magnetic devices is the thermal behaviour of the component during operation. It is important to check that even if the design optimization tends to minimize the losses in the components, still the produced heat does not induce an operating temperature above limits. For this purpose, the Coilcraft® datasheet has been analysed further in order to extract an approximation of the thermal resistance of each inductor series. The link between DC current magnitude, the DC resistance of the component and component temperature increase is used to estimate the thermal resistance of each component. Figure 24 below presents the evolution of the DC losses with respect to the value of the inductor for a temperature rise of 20 °C and 40 °C based on datasheets. The curves are flat, validating that the total amount of allowed losses per inductor shape (per inductor series) is constant. From these plots, one can derive the equivalent thermal resistance using Equation (20) below easily. These thermal resistances are listed in Table 5.

$$R_{th} = \frac{\Delta T}{(I^2 \times R_{dc})} \tag{20}$$

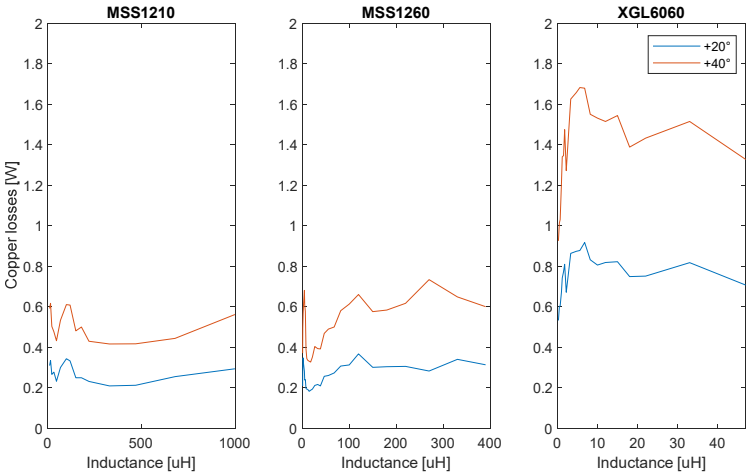

Figure 24. Maximum losses allowed in the inductor for various inductor values and for two temperature rises. Data extracted from datasheets [15–17].

Table 5. Median thermal resistance of copper to the core in MSS1210, MSS1260 and XGL6060 series.

Series	MSS1210	MSS1260	MSS6060
Median of the thermal resistance R_{th}(°C/W) at +20°	75	79	26
Median of the thermal resistance R_{th}(°C/W) at +40°	80	83	29

It is interesting to note that the inductor series with the largest dimensions seems to have a higher thermal resistance than the two others. This is somewhat strange and we were not able to provide a justification for this.

With these thermal characteristics, it is possible to verify the thermal behaviour of the magnetic component under the stress caused by the converter action. Under optimal configuration, for the 50 W converter, each inductor's power loss and thermal rising are presented in Table 6. These temperatures being under the manufacturer's limits, there is no reason to dismiss one of these technologies during the optimization process.

Table 6. Thermal rising of a 22 µH selected during optimization process of the 50 W converter.

Series	MSS1210	MSS1260	MSS6060
Inductor losses (W)	0.37	0.40	0.32
Thermal rising (°C)	27.8 to 29.6	31.6 to 33.2	8.3 to 9.3

To conclude this third part, the inductor model was successfully used to select the best inductor value, together with the converter switching frequency in order to minimize the overall losses. It was shown that, in the particular design and optimization case study considered here, the selected inductor and switching frequency may lead to significant current ripple magnitude in the inductors. This conclusion needs now to be validated with experiments.

5. Experimental Validation, Using Power-Cycling Converters

In this last part, the design optimization made in Section 4 will be illustrated and analysed with an experimental test bench where the measures of the losses of a full converter will be acquired and the search for the optimal operating point and design compared to the model optimization results. Some configurations will be tested to discretize the result and verify that the losses are in range with the calculation. Moreover, consolidated local and global optimum configurations will be checked throughout the experimental results.

5.1. Validation Setup Presentation

5.1.1. Opposition Method

The test bench that will be used for the experimental validation of the design optimization is based on the opposition method. It is made out of two equivalent converters, one feeding the other as illustrated in Figure 25. The first conversion unit is a DC to DC step down converter with energy flowing from the source to the central capacitor. The second one works as a step up converter sending back the energy from the central capacitor to the source. Tow DM filters are also inserted between the two converter stages in order to take the corresponding losses into account. A voltage source is used to supply power losses, to maintain the voltage at the right level. Thanks to this test bench, measuring the power delivered by the DC source and measuring the power transferred to the middle point DC link, it is possible to derive the global efficiency of the two converters and from this to derive the efficiency and the losses of each of them, making the assumption that the losses are equally shared between the two conversion stages. A picture of the test bench is given in Figure 26. For these study cases, the main inductors L are the ones named over each result cur. Each C_x capacitors are 20 µF ceramic capacitores, and each filtering inductor is taken from the XGL6060 series, chosen with Equation (16).

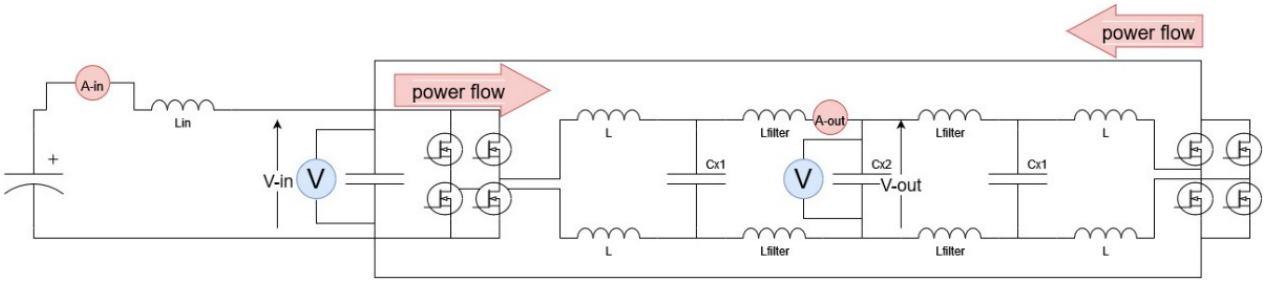

Figure 25. Schematic of the opposition method to characterize converter losses.

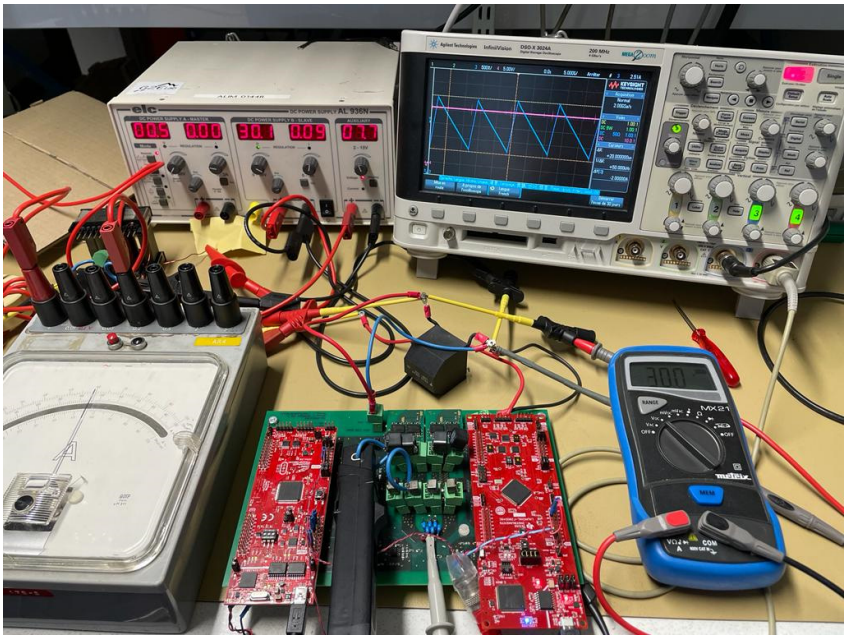

Figure 26. Picture of the test bench with the two TI controllers, one for each converter and in between the two converters, one feeding the other.

5.1.2. Losses Measurement

To measure the losses, the source voltage is measured across the input capacitor terminals noted V-in on the schematic Figure 25. the current consumption is measured filtered by a second order filter to measure only the DC current as it represents the losses dissipated in the converters under test. Regarding the measurement of the power flow, the V_{out} DC voltage of the C_{x2} capacitor is measured with a voltmeter and the current flowing into the filtering inductor (on the left in the schematic Figure 25) is measured continuously with an accurate ampere meter.

5.2. Experimental Losses Measure

A set of Frequency-Ripple-Output-Inductor (F-R-Oi) operating points have been defined and characterized by the opposition method in order to check if they are actually optimal. Losses have been measured for these points and are presented in Figures 27 and 28. Figure 27 represents converter losses curves for the following operating point: step down 30 V to 20 V under <2.5 A> output current for various inductor values. These values have been chosen to be compliant with the bench limits (switching frequency) and the limits of inductors (saturation). These inputs have been validated by the simulation results as Figure 28 presents the same curves for <1 A> output current. The model calculations and measures are plotted and compared with respect to current ripples, keeping in mind that for the same inductor value, frequency and ripple are linked. In the plots, dashed curves with circles are coming from measurements whereas full lines are modelling results coming from previous parts. Not all inductors have been measured since this is representing a lot of operating points and measurement set-up.

These measures are highly sensitive to the output DC current level. This variable can hardly be measured with better precision than 2% (50 mA in our case) and made it difficult to set precisely the operating point. Combined with high R_{DC}, this lack of precision is the weakest spot of the measurement process. Nonetheless, the results provide that the model calculations are in satisfactory accordance with the experimental results. Also, the different curves prove the ability of the modelling and design optimization method to identify the best inductor value and the minimum total losses with respect to ripple current magnitude since both theoretical and experimental curves are pointing to the same optimal point.

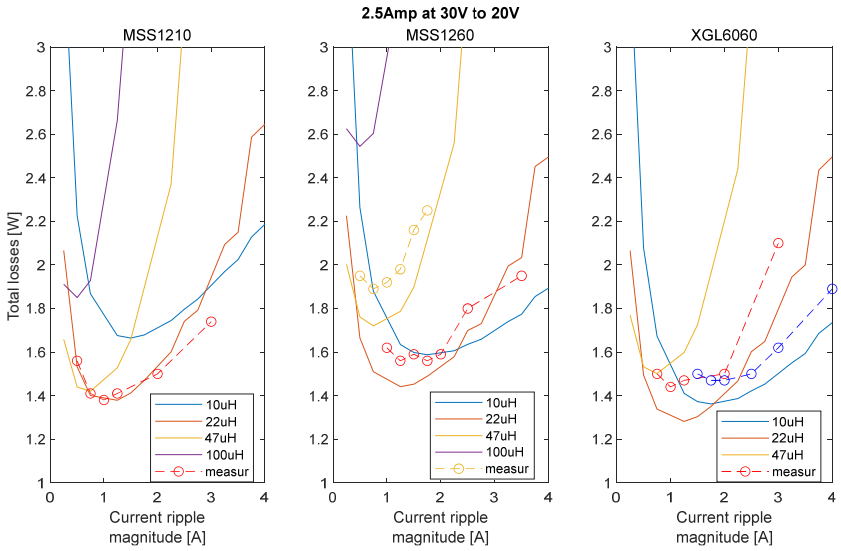

Figure 27. Optimization results compared with experimental measurements (curves with circles). For one converter processing, 50 W from 30 V to 20 V. Measure are carried out with back-to-back method. The results are plotted with respect to current ripples into the main inductors.

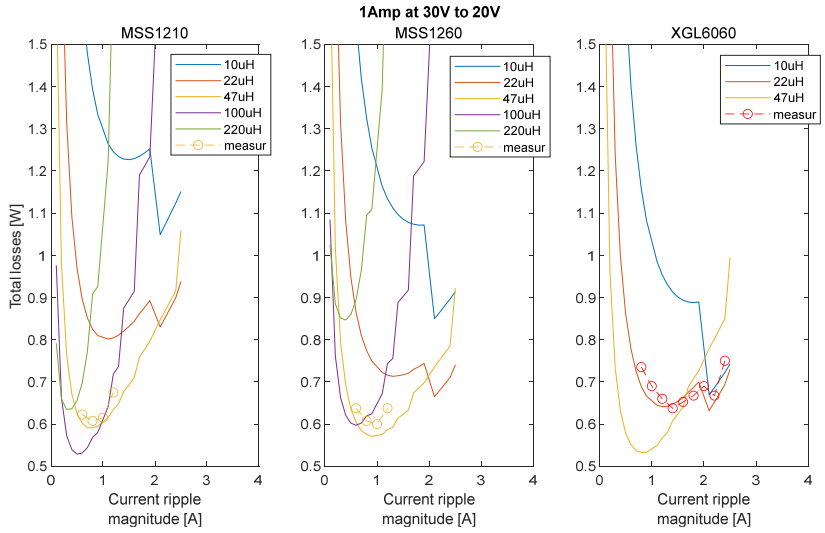

Figure 28. Optimization results compared with experimental measurements (curves with circles). For one converter processing, 20 W from 30 V to 20 V. Measures are carried out with the back-to-back method. The results are plotted with respect to the current ripple magnitude into the main inductors.

In Figure 27, it appears clearly in the plot for XGL6060 that lowering the value for the main inductor down to 10 µH, with a ripple current magnitude of about 80% of the average output current is almost leading to the minimum total losses in the converter. In addition to being the smaller component series, the smallest component in the series appears to be the best compromise in terms of volume and total losses, keeping in mind that the output filter has been taken into account.

Again, in Figure 27, it is clearly visible that there is always an inductor value which is optimal for a significant ripple current magnitude, more in the range of 40 to 80%, significantly larger than the ripple current magnitude usually considered in best practice designs. This clearly outlines the interest to add knowledge on the inductor characteristics in order to really explore the solution space and look for the best compromises. Using an

off-the-shelf component series. Implementing AC loss characterizations is a useful generic work in order to later carry on multiple design optimizations.

In Figure 28, with a lower average output current, it is still possible to see that large ripple currents are leading to optimal tradeoff for each component series. Also for this specific operating point, the optimal design leads to large inductor values, one can still see that XGL6060 components, which are the smallest, are leading to minimal total losses with large ripple current magnitudes, in the range of 100% of the average output current. These numerous experiments are validating the interest of the modelling method and the interest of the design engineer to extend the knowledge of components from experiments in order to carry on optimal design and tradeoffs.

The limits of the model are seen between Figures 27 and 28. As in Figure 28 the losses are accurately modelled. However, due to the high DC current bias, in Figure 27, saturation presses begin to appear. Therefore, the losses are lightly underestimated in this condition. The more the saturation process is advanced the more the error is important, as it can be seen comparing MSS1260-47 in yellow against MSS1260-22 in red.

5.3. Future Applications

This work has been fulfilled in order to be applied to the team's actual development. It will have a direct interest in the development of DC-AC standard conversion cells (CSC) for Power Converter Arrays (PCA) [33]. This optimisation method will help in selecting the optimal AC side input inductors in multilevel converters. It can also be used in combination with the analysis of different control strategies as zero voltage or current switching where large di/dt is usually required as illustrated in [34–36]. Also, as mentioned above, it will help to compare inductors technologies for future development. We expect that with more accurate active component models, the scope of the work could be extended to a higher-voltage converter. Finally, a high-frequency test bench will be necessary to extend the proposed model to wide-bandgap converters as we expect small standardized parts will gain in popularity with increased switching frequencies, and multicell conversion techniques [37–39].

6. Conclusions

In this paper, two complementary parts have been developed in order to outline the methodology to select the optimal inductor value from off-the-shelf component series. The first part was dedicated to enlarging the knowledge available to carry on the inductor value selection. For this purpose, a simple modelling method was proposed to derive a generic and accurate mathematical model of the inductor total losses. It is based on the definition of an equivalent series resistance, parametrized with respect to the inductor value and the switching frequency of the converter. All parameters were derived using experimental characterizations. The modelling technique was first introduced, step-by-step and then applied to manufacturer components series. The second part of the paper was dedicated to implementing this modelling technique, together with state-of-the-art models for the other components, in order to carry on the selection of the best inductor value in a representative case study. Thanks to the generic modelling approach and the parameters derivation technique, the numerous inductor option, coming from three components series were benchmarked. The best inductor value could be identified, leading to minimum losses and minimum volume. An interesting conclusion came out of the design, related to the ripple current magnitude, significantly above best practices. The model accuracy was helpful in investigating design options with large ripple currents. The last part of the paper was dedicated to the full validation of the modelling and design approach. Based on opposition technique, the case study was implemented and total losses were characterized. The measurement results were found in good accordance with the modelling results, confirming that the modelling technique was accurate. Also, the whole modelling and design approach has shown that a large ripple current magnitude can lead to optimal designs in terms of efficiency and power density at the inductor level.

All in all, this paper, which is quite long, is presenting a full modelling and design approach to select the best inductor value for buck-derived converter applications. It is shown how the acquisition of complementary data from off-the-shelf components may help in looking for the best component over a large panel of components and operating conditions. The two parts in this paper are helping the reader to understand how powerful the proposed modelling technique could be when applied in a design process, as well as how a few extra parameters, made available by manufacturers, could help greatly in representing the performances of their devices accurately.

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