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Editorial

Special Issue on Design of Fault-Tolerant Digital Circuits and Systems

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As technology scales down, the speed and power efficiency of digital circuits become greatly enhanced. On the other hand, the transistors become highly vulnerable to variability in process, voltage, and temperature, which leads the circuit to fail more easily. In addition, the increased current and power densities due to high density make transistors and interconnects wear out far earlier. Thus, the electrical characteristics of circuits are significantly changed, which results in unrecoverable damage. Although the circuits can be designed conservatively, such as using large-scale devices and wires, they unavoidably incur power, performance, and area overhead. Moreover, the circuit can fail due to high-energy particles in the atmosphere as the particles can shock the electric circuit and accidentally inject charge and change the voltage states, normally referred to as a soft error.

Therefore, designing digital circuits and systems to have fault tolerance is highly important. The present special session covers how digital circuits or systems can be configured or designed to have fault tolerance. There are various circuit techniques that tackle this issue. For example, whether the error occurs during the circuit operation can be detected with special sensing circuitry so that the error can be corrected instantly by the compensation circuits. There are many circuits or systems that adaptively allocate resources (using more bits, applying high supply voltage, or reducing frequency) to prevent operating failure while minimizing costs. Moreover, there are various novel circuit techniques and structures that can fix circuit operation failure. It is no doubt that the papers included in this Special Issue will have a great impact on how future digital circuits and systems are designed.

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