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Brief Report

High-Temperature Annealing Effects on Atomically Thin Tungsten Diselenide Field-Effect Transistor

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Abstract: Two-dimensional (2D) material-based devices are expected to operate under high temperatures induced by Joule heating and environmental conditions when integrated into compact integrated circuits for practical applications. However, the behavior of these materials at high operating temperatures is obscure as most studies emphasize only room temperature or low-temperature operation. Here, the high-temperature electrical response of the tungsten diselenide (WSe_2) field-effect transistor was studied. It is revealed that 350 K is the optimal annealing temperature for the WSe_2 transistor, and annealing at this temperature improves on-current, field-effect mobility and on/off ratio around three times. Annealing beyond this temperature (360 K to 670 K) adversely affects the device performance attributed to the partial oxidation of WSe_2 at higher temperatures. An increase in hysteresis also confirms the formation of new traps as the device is annealed beyond 350 K. These findings explicate the thermal stability of WSe_2 and can help design 2D materials-based durable devices for high-temperature practical applications.

Keywords: annealing; 2D materials; WSe_2; mobility; field-effect transistor; thermal stability

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1. Introduction

Since the invention of the transistor in 1947, silicon has become the material of choice for electronics [1–4] and photonics applications [5–8]. For the last few decades, enormous efforts have been made by the scientific community to find an alternative to silicon as a material of choice for future electronics [9–11]. It has been long appreciated that carbon nanotubes (CNTs) possess the required potential to be an ideal electronics material [12–16]. However, the challenges that arise from the non-uniform and imperfect growth of CNTs could not be resolved [12]. Since the discovery of graphene in 2004, 2D materials have emerged as a strong candidate for future high-speed and low-power electronics [17–20]. Two-dimensional materials possess several intrinsic properties like quantum confinement, a reasonable large bandgap, ease of fabrication, strong light–matter interaction, ability to form heterostructures and strong gate modulation, making them a suitable material for future electronics as well as photonics applications [21–24]. Among the 2D materials family, transition metal dichalcogenides (TMDs) are particularly of interest. WSe_2 is a prominent member of TMDs because of its ambipolar behavior, large spin–orbit coupling and optical properties [25]. Studies showed the application of WSe_2 not only in electronic applications such as inverters and Schottky diodes [26] but also in photonic applications such as photodetectors, single-photon emitters and light-emitting diodes [27].

Until now, most of the studies have investigated the properties of WSe_2 at either room temperature or cryogenic temperatures [28]. While these studies were successful in understanding the intrinsic properties of the materials, there have been very few studies investigating the behavior of the material at high temperatures. For practical applications, 2D materials are expected to operate under high thermal stress caused by Joule heating in integrated circuits or local heating due to incident light in photonic applications [29–31].

Further, due to low thermal conductivity and heat capacity as well as high surface area, these materials are expected to endure temperatures higher than bulk materials such as Si and GaAs [32–36]. Therefore, it is essential to test the WSe_2 devices at high operating temperatures and monitor their performance under these conditions.

In this work, we designed an experimental setup to investigate the changes in the electrical behavior of the WSe_2 device after being exposed to high annealing temperatures. The investigation was carried out using a homemade probe station that can also anneal the devices in a nitrogen environment so that there is no need to take out the device after annealing. The device was annealed to temperatures ranging from 300 K to 670 K (step size: 10 K), and the electrical characterization of the device was performed at 300 K after each cycle of annealing. It was found that 350 K is the optimal annealing temperature for WSe_2, which improves the device performance by eliminating the adsorbed species and chemical residue. Annealing at temperatures higher than 350 K adversely affects the device performance. The effects of annealing on the transfer characteristic curve, on/off ratio, field-effect mobility and hysteresis were investigated.

2. Materials and Methods

Figure 1a,c shows the schematic drawing and optical microscope image of the WSe_2 device. In order to fabricate this device, thin WSe_2 flakes were produced from the bulk WSe_2 crystal by the standard exfoliation method using scotch tape. The flakes were then transferred on a silicon substrate capped with 300 nm SiO_2. An optical microscope was used to scan the substrate and identify suitable flakes, followed by Raman spectroscopy and atomic force microscopy (AFM). The back gated devices were prepared by electron beam lithography followed by metal deposition in an electron beam evaporation chamber. Electron beam lithography was used to make contact patterns on the selected WSe_2 flake. Titanium/gold (Ti/Au) with a thickness of 10/40 nm were chosen as contact materials as Ti forms Ohmic-like contacts with WSe_2. The metal deposition was carried out in an electron beam evaporation chamber, followed by the lift-off in acetone.

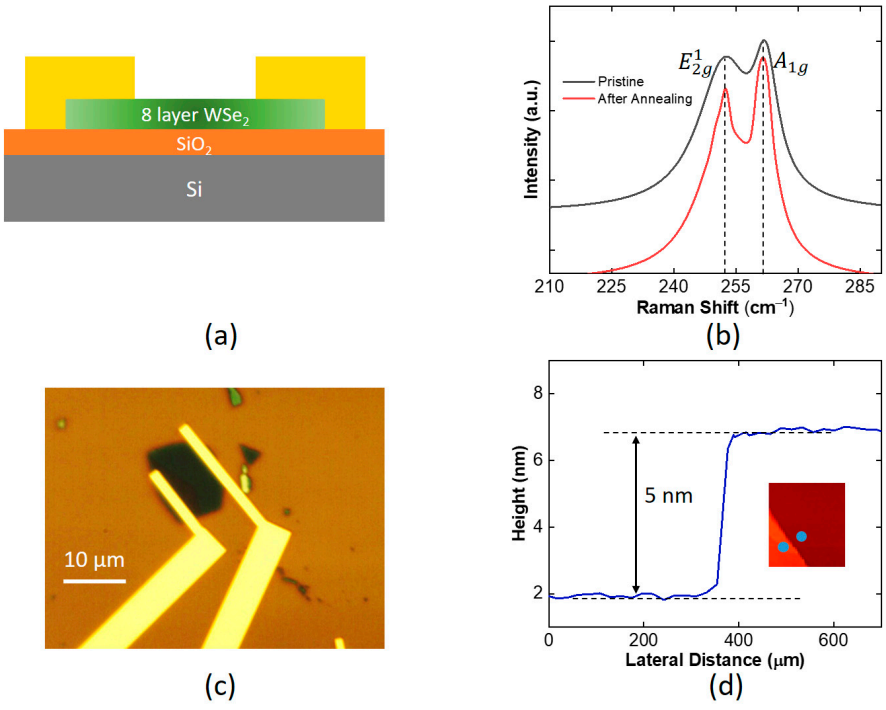

Figure 1. (**a**) Schematic of the WSe_2 device. (**b**) Raman spectrum of the WSe_2 before and after annealing. (**c**) Optical microscope image of the device. (**d**) AFM image and height profile of the WSe_2 layer.

3. Results and Discussion

Figure 1b illustrates the Raman spectrum of the device taken by a 532 nm laser. The signature WSe_2 Raman peaks, $E^1{}_{2g}$ and A_{1g}, can be seen at 252 cm^{-1} and 261cm^{-1}, respectively [37,38]. The presence of these two peaks not only confirms the material to be WSe_2 but also indicates that the flake thickness is more than four layers [22,23]. The Rama n spectroscopy was performed after annealing at 673 K as well. The comparison of the Raman spectrum before and after annealing is discussed in the later part. In order to accurately determine the WSe_2 thickness, atomic force microscopy (AFM) was carried out. Figure 1d presents the AFM image of the WSe_2 flake as well as the line profile between the two points shown in Figure 1d. It can be seen that the flake thickness is 5 nm, which corresponds to eight layers of WSe_2.

The transfer characteristics curves of the device at a constant source-drain voltage of 1 V measured at 300 K after annealing at different temperatures is shown in Figure 2. The influence of annealing on the device properties was systematically investigated by annealing the device at a target temperature for 30 min in a Nitrogen environment and then measuring its transfer characteristics curve at 300 K. The process was repeated for temperatures ranging from 310 K to 670 K with a step size of 10 K. In Figure 2, however, for better visibility, transfer curves are shown for selected annealing temperatures only. It can be seen that the device exhibits ambipolar behavior with hole-dominated transport for negative gate voltages and electron-dominated transport for positive gate voltages. After annealing at 310 K, the electron current is almost an order of magnitude higher than the hole current. In most studies, WSe_2 exhibit p-dominant transport; however, in the present study, n-dominant transport can be attributed to the Ti contacts. As shown in the schematic band diagram in Figure 2d, Ti has a work function of 4.3 eV, which is closer to the conduction band of WSe_2 [39,40]. Therefore, Ti can facilitate the injection of electrons in the conduction band of WSe_2 by forming good Ohmic-like contacts. At the same time, Ti forms a large Schottky barrier with the valence band of WSe_2. This Schottky barrier results in electron transport being more prominent than the hole current. The inset of Figure 2a represents the output curve (I_d–V_d) of the WSe_2 device, and Ohmic-like linear characteristics can be seen there.

For the positive gate region (electron transport), as the annealing temperature is increased up to 350 K, an increase in the drain current as well as on/off ratio (ratio of on current to the off current of the device) is observed. As annealing temperature increases from 300 K to 350 K, the on/off ratio increases from 8000 to 22,000, whereas maximum on current increases from 14 μA to 37 μA. This observation of enhanced device performance after annealing is consistent with the previous studies in the literature [41]. The annealing improves the device's performance by removing the contaminants, adsorbed moisture and chemical residues from the surface of WSe_2 [41]. Two-dimensional materials possess a high surface-to-volume ratio and are extremely sensitive to the changes at the interface; therefore, annealing can drastically improve the device's performance. However, as the annealing temperature is increased beyond 350 K, the device performance gradually deteriorates. Overall, a decrease in device current as well as on/off ratio can be seen when the annealing temperature exceeds 350 K. The maximum current reduces from 37 μA to 1.5 μA, and the on/off ratio reduces from 22,000 to 1000 as the annealing temperature is gradually increased from 350 K to 590 K. Previous studies reported that WSe_2 oxidizes to WO_x at high temperatures [42,43]. The oxidation of 2D materials differs from bulk materials as these materials show higher reactivity at the edges and defect sites only. The effects of oxidation on the electrical characteristics of the WSe_2 device can be seen in this temperature range (350 K to 590 K), where not only the on/off ratio and total current reduced but a decrease in the subthreshold swing can also be observed. It is safe to say that higher thermal and electrical stress has induced structural and chemical changes in the $WSe_{2,}$ which is further explained in the latter part. From 590 K to 670 K, the device behavior changes from semiconducting to fully conducting with very little gate control. The on/off ratio in the region is less than 10, and the off current has increased several orders of magnitude. In

order to obtain further insight into the device behavior, we extracted field-effect mobility and hysteresis of the device.

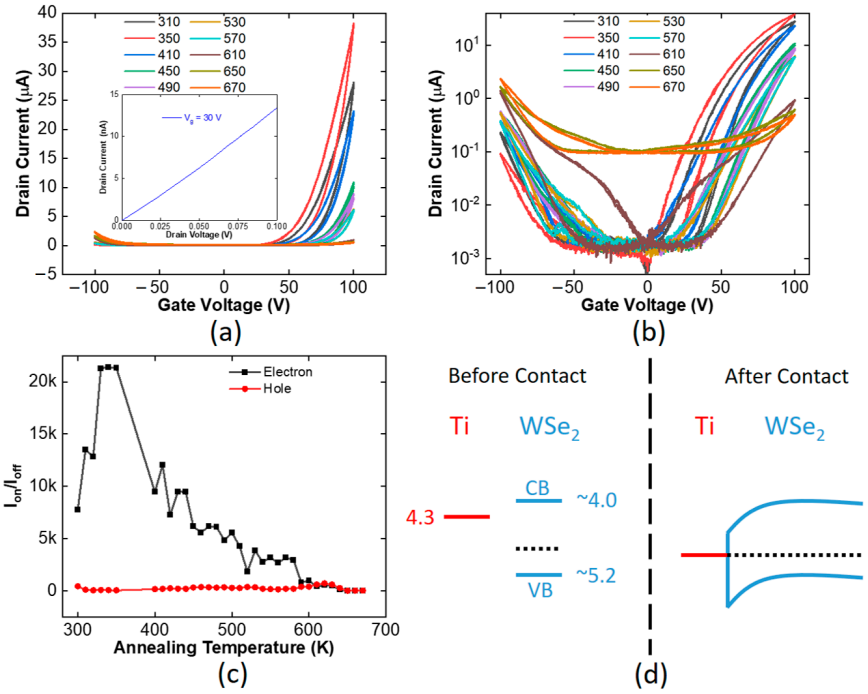

Figure 2. (**a**) Transfer characteristics curve of the WSe_2 device measured at 300 K after annealing at different temperatures on a linear scale (legend shows the annealing temperature in Kelvin, and inset represents the I_d–V_d curve of the device). (**b**) Transfer characteristics curve of the WSe_2 device measured at 300 K after annealing at different temperatures on a semi-logarithmic scale (legend shows the annealing temperature in Kelvin). (**c**) The ratio of on current to the off current of the device as a function of annealing temperatures. (**d**) Schematic band diagram showing Ti and WSe_2 before and after contact.

Figure 3 illustrates the field effect mobility as well as hysteresis as a function of annealing temperature. The field-effect mobility was extracted for electrons as well as holes using the following equation:

$$\mu = \frac{L}{W}\frac{g_m}{C_{ox}V_d}$$

In this equation, L and W are the total channel length and width, respectively, and C_{ox} is the back gate silicon dioxide capacitance per unit area, calculated by $C_{ox} = \varepsilon_0 \cdot \varepsilon_r / d$. Here, $\varepsilon_0 = 8.85 \times 10^{-12}$ Fm^{-1} is the permittivity of free space, and $\varepsilon_r = 3.9$ is the relative permittivity of SiO_2 and d is SiO_2 thickness (300 nm). g_m is the trans-conductance obtained from the slope of each transfer curve, V_d is the applied drain voltage and μ is the field effect mobility. A similar trend for electron mobility can also be seen in Figure 3, where initially, electron mobility increases from 4 $cm^2/V.s$ to 9 $cm^2/V{\cdot}s$ as the annealing temperature is increased from 300 to 350 K. The mobility in 2D materials is limited by the scattering, and an improvement in mobility indicates a reduction in scattering. All the measurements were performed at 300 K, so it was safe to rule out any change in phonon scattering. Therefore, the increase in electron mobility can be attributed to a cleaner WSe_2 surface enabled by thermal annealing. As observed previously, in the temperature range of 360 K to 590 K, a consistent drop in electron mobility can be seen. One can also observe three distinct regions in the mobility curve: the mobility increases from 300 K to 350 K and from 350 K to 590 K, mobility gradually reduces from 9 $cm^2/V.s$ to 2.5 $cm^2/V.s$ and it reaches 0.1 $cm^2/V{\cdot}s$ at 670 K. This trend of mobility and device current reflects that 350 K is the optimal annealing temperature for WSe_2. Until this temperature, annealing improves the

device's performance by removing the contaminants, adsorbed moisture and chemical residues from the surface of WSe_2 [41]. Beyond 350 K, the high temperature starts to oxidize WSe_2 and alter its chemical composition. As WSe_2 becomes oxidized to WO_x, new traps are created at the WSe_2-WO_x interface, which results in a reduction in electron mobility [42,43]. The presence of hysteresis in the transfer curve is an indicator of charge traps in a device, so we investigated the hysteresis behavior of our device, as shown in Figure 3b. It is defined as the threshold voltage difference between the forward and reverse gate voltage sweep. Three distinct regions are also visible here; from 300 K to 350 K, hysteresis reduces, indicating the removal of traps and surface contaminants from WSe_2. It gradually increases from 350 K to 590 K and increases exponentially from there onwards. Since hysteresis is an indicator of traps, it can be said that as WSe_2 becomes oxidized beyond 350 K, new traps are created, which degrade device performance by causing a reduction in electron mobility and on/off ratio. Figure 3c presents the off current as a function of annealing, which remains almost constant except at temperatures beyond 630 K, where chemical changes in WSe_2 result in complete loss of gate control. The comparison of Raman (Figure 1d) and AFM measurements (Figure 3d) before and after the annealing give insight into the chemical changes induced by the thermal stress. In the Raman spectrum, the quenching of Raman peaks after annealing points to partial oxidation of WSe_2 and the formation of new traps [44]. The average surface roughness before annealing was 320 pm, which was increased to 450 pm after annealing. The increased surface roughness in AFM measurement also corresponds to the formation of new traps. The observations such as quenching in the Raman spectrum, increased overall conductivity of WSe_2, an increase in p-type behavior and an increase in surface roughness can be attributed to partial oxidation of WSe_2 to WO_x as reported in previous studies [43–48]. Based on these observations, it can be assumed that in our WSe_2 device, the WSe_2 became oxidized during high-temperature annealing. However, this could be one of the reasons, and the exact nature of chemical changes still needs to be established.

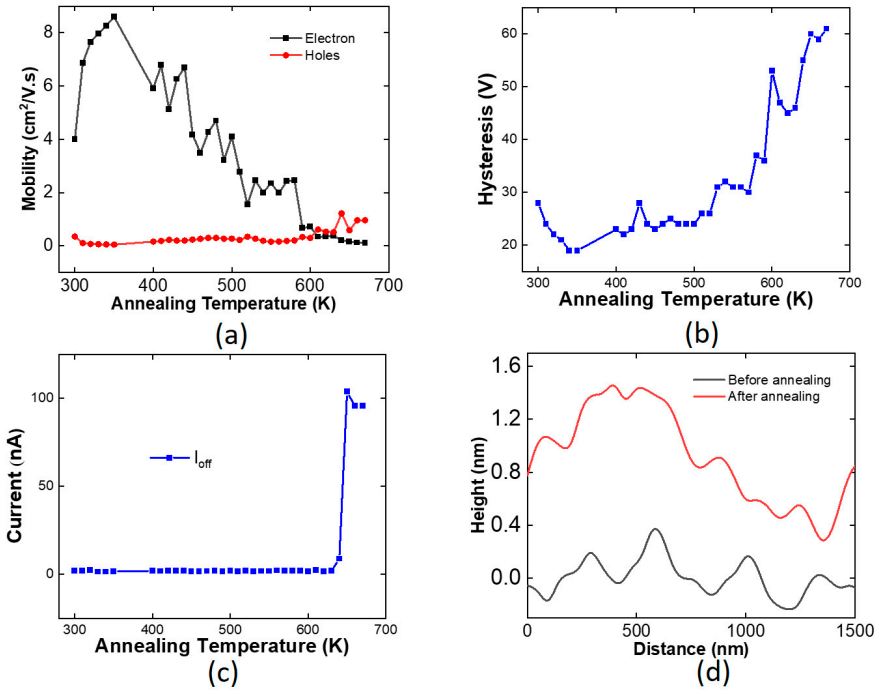

Figure 3. (**a**) The field-effect mobility of the WSe_2 device as a function of annealing temperature. (**b**) The hysteresis of the device as a function of annealing temperature. (**c**) The off current of the device as a function of annealing temperature. (**d**) Surface roughness of WSe_2 as measured by AFM before and after annealing.

Thus far, we have discussed the positive gate region of Figures 2 and 3 mostly. For the negative region, the mobility and on/off ratio do not vary substantially with the annealing indicating that the hole transport is not limited by the channel imperfections. As shown in Figure 2, the bottleneck in hole transport is the Schottky contacts. Ti is used as a contact metal that can form a relatively large Schottky barrier with the valence band of WSe_2, thus limiting the hole transport. This Schottky barrier results in low mobility and low current in the negative gate region and cannot be improved with annealing. Therefore, annealing does not affect the hole transport other than at temperatures beyond 590 K, where chemical changes in WSe_2 result in the channel becoming accumulated with the carriers completely and also results in a reduction in the effective Schottky barrier. This reduction results in enhanced hole current and hole mobility, as seen in Figure 3.

4. Conclusions

In conclusion, we systematically investigated the thermal stability of the WSe_2 transistor by annealing it in a nitrogen environment at different temperatures. The effects of annealing on transfer curve, field-effect mobility and hysteresis were investigated. It was found that 350 K is the optimal annealing temperature that significantly improves the electrical characteristics of the WSe_2 transistor. Annealing beyond this temperature adversely affects the device's performance by oxidizing WSe_2 and permanently changing its electrical properties. Our findings elucidate the thermal stability of WSe_2 and can be useful to design 2D materials-based practical and durable devices to be operated at moderate or high temperatures.

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