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Design of a Single-Stage Transformerless Buck–Boost Inverter for Electric Vehicle Chargers

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Abstract: This paper details the design and implementation of a single-stage transformerless buck–boost inverter for electric vehicle (EV) chargers. Being different from conventional H-bridge inverters, the proposed inverter operates like buck–boost dc/dc converters instead of buck dc/dc converters. As a consequence, the advantages of a buck–boost dc/dc converter, i.e., the arbitrary relationships between its input voltage and output voltage, are still applicable to the proposed inverter. Specifically, it remains in normal operation even when the peak ac output voltage is higher than the dc-link voltage. Simulation results are finally presented to illustrate its effectiveness.

Keywords: electric vehicle (EV); buck–boost; inverter; power electronics; single-stage; transformerless

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1. Introduction

Dc/ac power electronic converters, i.e., inverters, have found widespread applications in the areas of renewable generation [1–5], power conditioning [6–9], energy storage systems [10], and electric vehicles (EVs) [11,12]. Generally, buck-type inverters, such as the well-known H-bridge inverters, are employed to achieve the objective of dc to ac power conversion [1–10]. However, due to the inherent voltage step-down characteristic of buck converters [13], the peak ac output voltage for the buck-type inverter should always be lower than its input dc-link voltage. This requirement imposes several limitations on the design and operation of buck-type inverters. For example, in applications where the input dc voltage is equivalent to or lower than the output ac voltage, one additional stage of dc/dc power converter is necessary to boost up the dc-link voltage. Otherwise, the undesirable over modulation of buck-type inverters may occur, which will disrupt the system from normal operation [6].

Although the adoption of another dc/dc converter into the dc/ac power conversion system with low dc-link voltages, e.g., photovoltaic generation [1], is a feasible and widely used solution, this approach will inevitably increase the system cost and complexity. It is therefore highly desirable that the inverter can operate without any limitations on the relationships between its dc voltage and ac voltage. As an interesting attempt, Peng F. proposed a novel inverter, named the z-source inverter, which simultaneously achieves the objectives of dc to ac conversion and voltage boost [14]. Nevertheless, it necessitates extra filter components and complicated control algorithms.

As an alternative simple solution, a single-stage transformerless buck–boost inverter is proposed in this paper. By directly extending the operating principles of dc/dc buck–boost converter into dc/ac applications, the proposed inverter can be designed and operated in a straight-forward way, as will be discussed in the following sections.

2. System Schematic

Figure 1 shows a schematic diagram of the proposed single-stage transformerless buck–boost inverter system, where the dc-link voltage V_{dc} is maintained as a constant V_{dc}

by a dc power supply. Through operating the semiconductor switches S_1–S_4, the inductor L_f can be charged from both directions, and then it will be discharged to supply the filter capacitor C_f and the load R_o so long as switch S_5 or S_6 are turned-on. In Figure 1, i_L, i_R, and v_c denote the inductor current, load current, and capacitor voltage, respectively.

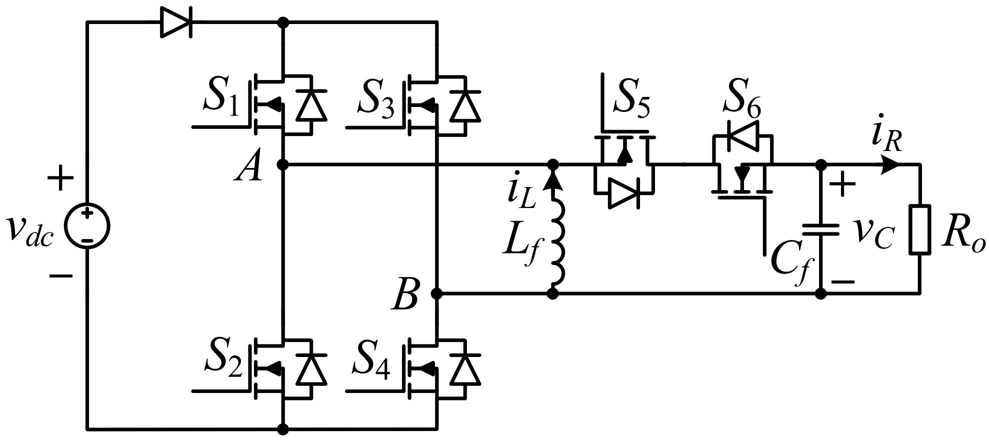


Figure 1. Schematic diagram of the proposed single-stage transformerless buck–boost inverter system.

3. Operation Principle

The operation principle of the proposed buck–boost inverter can be explained well by the switching patterns illustrated in Figures 2 and 3. Assuming that the desirable waveform of the output voltage v_c is a sinusoid, which pulsates at fundamental frequency. Under this assumption, the operation of semiconductor devices will be dependent on the sign of v_c. For the case of a positive half-wave of v_c, S_1 and S_4 remain in the off-state, as shown in Figure 2. As it can be observed from Figure 2a, when S_2 and S_3 turn on, the dc power supply charges the inductor L_f, and hence, the inductor current i_L increases linearly. Meanwhile, S_6 remains in the off-state and the capacitor C_f releases its energy to supply the load R_o. In contrast, it is clear from Figure 2b that the inductor L_f transforms its energy to the capacitor C_f and load R_o when S_2 and S_3 turn-off, together with S_6 switched on. For the case of a negative v_c, the operations of S_2, S_3, and S_6 are replaced by S_4, S_1, and S_5, respectively. From the above analysis, the proposed buck–boost inverter operates very similar to the conventional dc/dc buck–boost inverter, except for its bipolar output voltage. As a consequence, it enables both the operation of voltage step-down and boost.

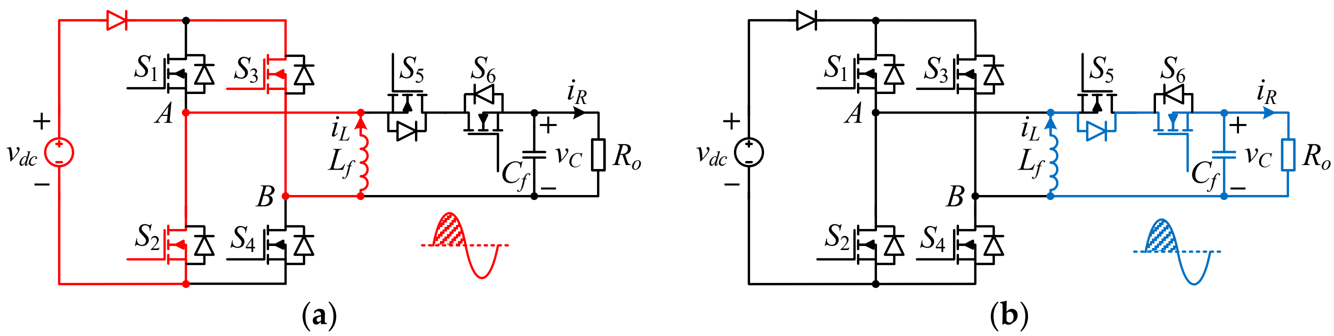


Figure 2. Switching patterns for the positive half-wave of v_c: (**a**) Inductor charged, (**b**) Inductor discharged.

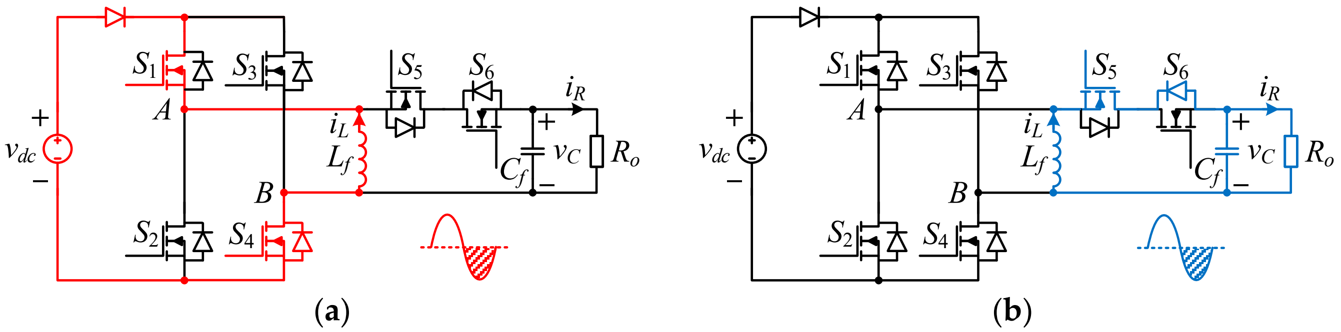


Figure 3. Switching patterns for the negative half-wave of v_c: (**a**) Inductor charged, (**b**) Inductor discharged.

4. Mathematic Model

Let T_s denote the switching period, T_{on} represent the switching-on time of S_2 and S_3 or S_1 and S_4 in each switching cycle, T_{off} stand for the switching-on time of S_5 or S_6 in each switching cycle, and $d_o = T_{on}/T_s$ designate the duty cycle. The state equation description of the proposed buck–boost inverter can be derived from Figure 2 as follows:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{R_o C_f} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix} v_{dc}, \tag{1}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_f} \\ \frac{1}{C_f} & \frac{-1}{R_o C_f} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{dc} \tag{2}$$

where (1) and (2) represent the equations for switching-on and switching-off, respectively. The state space average model of the proposed inverter can be further derived through adding (1) and (2) with their respective weighted coefficients of d_o and 1-d_o as follows:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-d_o)}{L_f} \\ \frac{1-d_o}{C_f} & \frac{-1}{R_o C_f} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{d_o}{L_f} \\ 0 \end{bmatrix} v_{dc}. \tag{3}$$

Based on (3), the transfer functions from the dc-link v_{dc} to the inductor current i_L and capacitor voltage v_c can be derived as:

$$\frac{i_L(s)}{v_{dc}(s)} = \frac{d_o(C_f R_o s + 1)}{C_f L_f R_o s^2 + L_f s + R_o(1-d_o)^2}, \tag{4}$$

$$\frac{v_C(s)}{v_{dc}(s)} = \frac{R_o d_o(1-d_o)}{C_f L_f R_o s^2 + L_f s + R_o(1-d_o)^2}. \tag{5}$$

In steady-state, (4) and (5) can be reorganized as:

$$\frac{I_L}{V_{dc}} = \frac{d_o}{R_o(1-d_o)^2}, \tag{6}$$

$$\frac{V_C}{V_{dc}} = \frac{d_o}{1-d_o}. \tag{7}$$

It should be noted that (1)–(7) are only applicable to the case of positive output voltages (see Figure 2). In the case of negative output voltages, as shown in Figure 3, the v_{dc} in (1)–(7) should be replaced by $-v_{dc}$. This nonlinear behavior will bring in additional concerns to controller design. In order to address this problem, the absolute value of duty cycle *do* is used instead of its actual value. Furthermore, when the reference duty cycle crosses zero from a positive value to a negative value, the driving pulses of S_2 and S_3 are shifted to S_1 and S_4, and vice versa. Through this approach, the sign of the output voltage v_c can always be regulated to follow the sign of its reference, and (1)–(7) are applicable to $|v_c|$.

5. Controller Design

5.1. Open-Loop Control

It is obvious from (7) that the duty cycle for a desirable sinusoidal output voltage $v_c = V_{Cp}\sin(\omega t)$ can be expressed as:

$$d_o = \frac{|V_{Cp}\sin(\omega t)|}{V_{dc} + |V_{Cp}\sin(\omega t)|}. \tag{8}$$

5.2. Closed-Loop Control

A typical double-loop controller, i.e., an outer voltage-loop and an inner current-loop controller [15,16], is incorporated to regulate the proposed buck–boost inverter. Its relevant control block diagram is shown in Figure 4, where K_{pwm} denotes the gain of the pulse-width modulator (PWM), z^{-1} represents one sampling period time delay, and ZOH stands for the mathematical model of the zero-order-hold behavior of the pulse-width generator [7]. It should be mentioned that the proposed controller is implemented by a digital controller, and hence, the transfer functions of the controllers are expressed in the discrete z-domain. In contrast, the system plant model, which is described by (3), is represented in the continuous s-domain. Additionally, a control block denoted as $G_d(z)$ is employed in the current controller to effectively dampen the resonant peak introduced by the LC-filter. Moreover, taking the varying loads into consideration, the load current $i_R(s)$ is treated as a disturbance here.

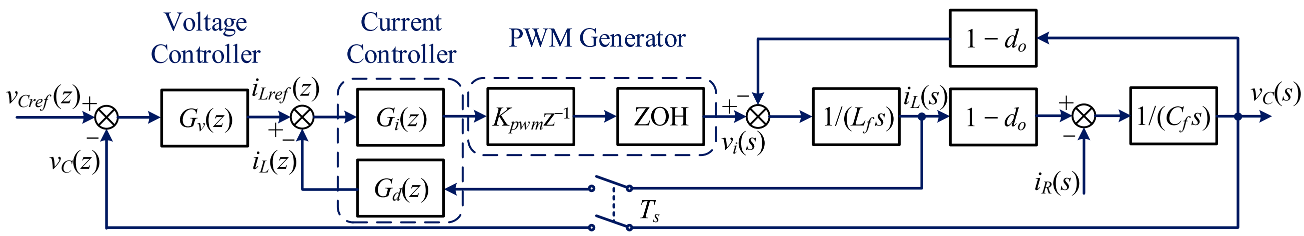


Figure 4. Overall control block diagram of the proposed buck–boost inverter.

The transfer function from the output of PWM generator to the inductor current $i_L(s)$ can be derived from Figure 4 as follows:

$$T_{vi\_iL}(s) = \frac{i_L(s)}{v_i(s)} = \frac{C_f s}{C_f L_f s^2 + (1-d_o)^2}. \tag{9}$$

In addition, the transfer function from the output of PWM generator to the output voltage v_c (s) can be derived as:

$$T_{vi\_vC}(s) = \frac{v_C(s)}{v_i(s)} = \frac{1-d_o}{C_f L_f s^2 + (1-d_o)^2}. \tag{10}$$

Applying the z-transformation with ZOH into (9) and (10), the relevant discrete expressions can be obtained as:

$$\begin{aligned} T_{vi\_iL}(z) &= Z\left[(1-z^{-1})\cdot\frac{T_{vi\_iL}(s)}{s}\right] \\ &= \frac{(z-1)\cdot\sin[(1-d_o)\omega_r T_s]}{(1-d_o)L_f\omega_r\cdot\{z^2-2z\cos[(1-d_o)\omega_r T_s]+1\}}, \end{aligned} \tag{11}$$

$$T_{vi\_vC}(z) = Z\left[(1-z^{-1}) \cdot \frac{T_{vi\_vC}(s)}{s}\right] = \frac{(z+1)\cdot\{1-\cos[(1-d_o)\omega_r T_s]\}}{(1-d_o)\cdot\left\{z^2-2z\cos[(1-d_o)\omega_r T_s]+1\right\}} \quad (12)$$

where $\omega_r = 1/(L_f C_f)^{1/2}$ denotes the resonance frequency of the LC-filter. After the derivation of (11) and (12), the simplified control block diagram of the proposed buck–boost inverter is illustrated in Figure 5, where all the transfer functions are expressed in the z-domain. The system and control parameter values are tabulated in TABLE I. It should be mentioned that the proportional gains G_i and G_d are used for the current controller, while a proportional-resonant (PR) controller with its proportional gain denoted as G_{vp} and resonant gain denoted as G_{vr} is employed as the voltage controller.

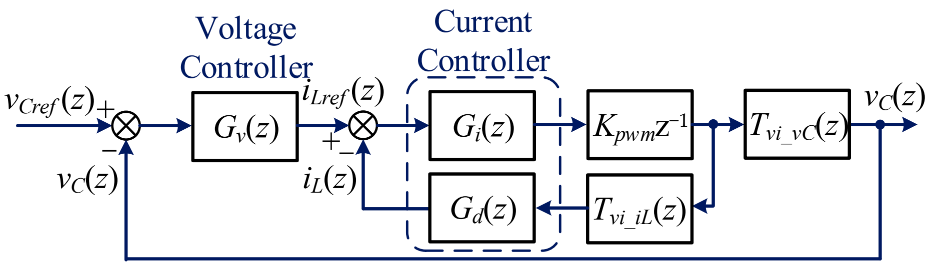
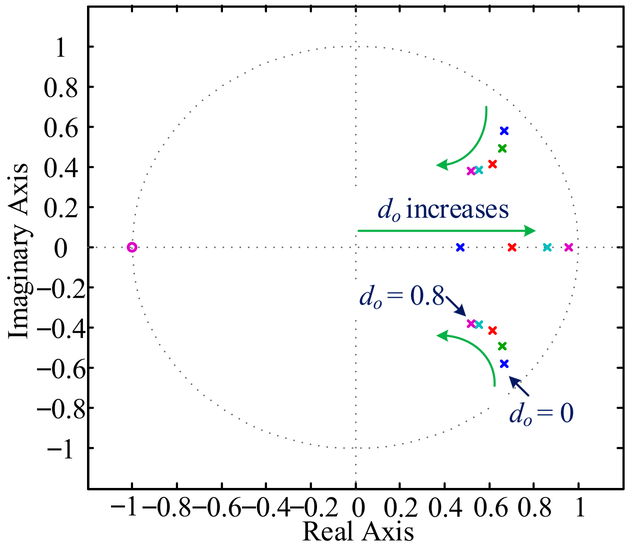


Figure 5. Simplified control block diagram of the proposed buck–boost inverter.

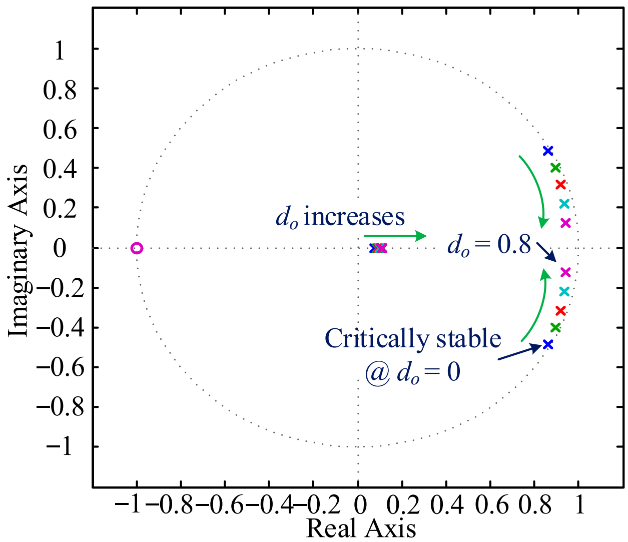
Based on Figure 5 and the system parameter values listed in Table 1, the pole-zero map of the closed-loop voltage control is illustrated in Figure 6, where the zeros are represented as circles while the poles are denoted as crosses. The effectiveness of the proposed damping control block $G_d(z)$ can be clearly observed by comparing Figure 6a,b. As seen, the system poles are located much closer to the center of the unit circle after the carefully designed $G_d(z)$ is enabled. It should be highlighted that the variation in the duty cycle will influence the stability of the proposed inverter, while the stability of conventional H-bridge inverters is independent of d_o. As a consequence, all the closed-loop poles should always stay within the unit cycle as the duty cycle varies. In order to ensure the system stability, the maximum value of the output voltage v_c should be given first, and then the maximum d_o can be derived according to (8). Next, the variation range of d_o can be obtained. Finally, the map of the closed-loop poles can be drawn to validate whether the system poles are always inside the unit cycle. As it can be seen from Figure 6a, the system can be stable even when the duty cycle is as high as 0.8, which corresponds to an output voltage of 400 V.

Table 1. System and Control Parameter Values.

Description	Symbol	Value
Dc-link voltage	V_{dc}	100 V
Filter inductor	L_f	1 mH
Filter capacitor	C_f	50 µF
Load resistor	R_o	10 Ω
Output voltage	V_C	50–150 V
Current controller	G_i/G_d	1/4
Voltage controller	G_{vp}/G_{vr}	0.2/100
Fundamental frequency	f_o	50 Hz
Switching frequency	f_s	10 kHz
Sampling frequency		
Rated power	P_o	1 kW



(**a**)



(**b**)

Figure 6. Pole-zero map of the closed-loop voltage control: (**a**) With damping controller ($G_d(z)$ = 4), (**b**) Without damping controller ($G_d(z)$ = 1).

6. Simulation Results

Simulations models were built in Matlab/Simulink software based on the system parameter values listed in Table 1 and the schematic diagram shown in Figure 1. The simulation waveforms of capacitor voltage v_c and inductor current i_L under two cases, where the peak ac voltages (50 V and 150 V) are lower than and higher than the dc-link voltage, are demonstrated in Figures 7 and 8. For these two cases, the dc-link voltage v_{dc} is maintained as a constant 100 V. As observed, the proposed inverter enables the operations of both buck-type and boost-type inverters. As mentioned, the switching patterns are changed while the system structure remains fixed. These results are consistent with the theoretical analysis.

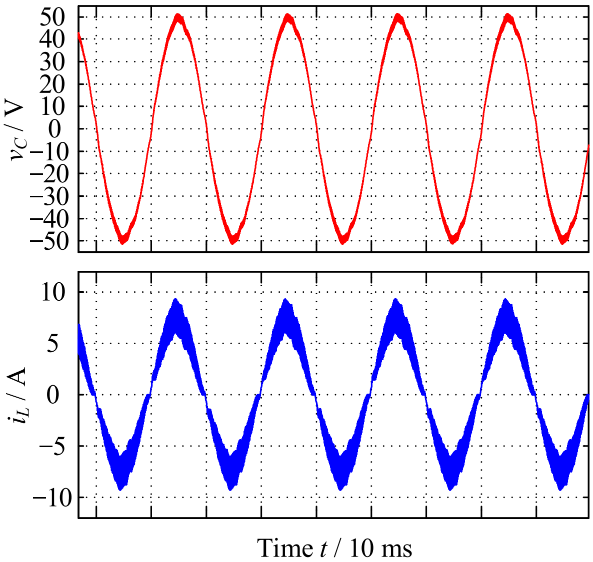


Figure 7. Simulation results of the proposed buck–boost inverter working as buck-type inverter.

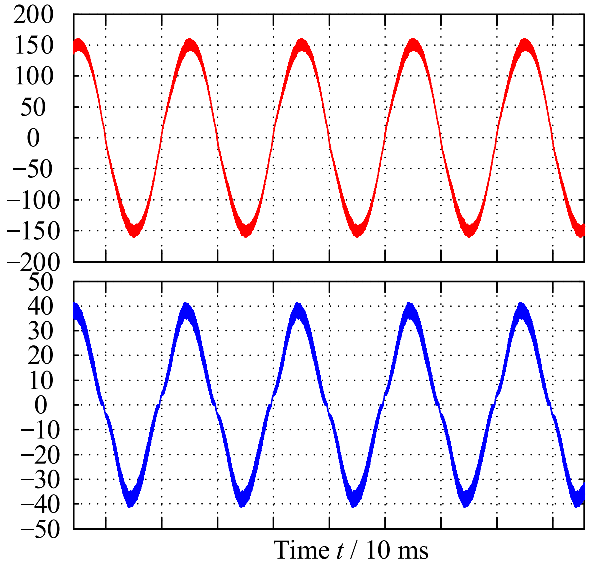


Figure 8. Simulation results of the proposed buck–boost inverter working as boost-type inverter.

7. Conclusions

In this paper, a single-stage transformerless buck–boost inverter has been proposed to directly achieve dc to ac conversion regardless of the relationships between its dc-link voltage and peak ac output voltage. The proposed inverter is an equivalent replacement of a conventional boost converter cascaded with an inverter, while the former features simpler circuit structure, lower cost, smaller volume, and straight-forward implementation. The analysis based on its state space average model indicates that the stability of the proposed inverter is dependent on the value of its duty cycle. Fortunately, this issue can be addressed by a well-designed outer voltage-loop plus inner current-loop controller. Simulation results are presented to validate its effectiveness.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Blaabjerg, F.; Teodorescu, R.; Liserre, M.; Timbus, A.V. Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1398–1409. [CrossRef]
2. Fang, J.; Li, H.; Tang, Y. A magnetic integrated *LLCL* filter for grid-connected voltage-source converters. *IEEE Trans. Power Electron.* **2017**, *32*, 1725–1730. [CrossRef]
3. Li, X.; Wu, X.; Geng, Y.; Yuan, X.; Xia, C.; Zhang, X. Wide damping region for *LCL*-type grid-connected inverter with an improved capacitor-current-feedback method. *IEEE Trans. Power Electron.* **2015**, *30*, 5247–5259. [CrossRef]
4. Fang, J.; Li, X.; Yang, X.; Tang, Y. An integrated trap-*LCL* filter with reduced current harmonics for grid-connected converters under weak grid conditions. *IEEE Trans. Power Electron.* **2017**, *32*, 8446–8457. [CrossRef]
5. Li, X.; Fang, J.; Tang, Y.; WU, X.; Geng, Y. Capacitor voltage feedforward with full delay compensation to improve weak grids adaptability of *LCL*-filtered grid-connected converters for distributed generation systems. *IEEE Trans. Power Electron.* **2018**, *33*, 749–764. [CrossRef]
6. Tang, Y.; Loh, P.C.; Wang, P.; Choo, F.H.; Gao, F.; Blaabjerg, F. Generalized design of high performance shunt active power filter with output *LCL* filter. *IEEE Trans. Ind. Electron.* **2012**, *59*, 1443–1452. [CrossRef]
7. Fang, J.; Xiao, G.; Yang, X.; Tang, Y. Parameter design of a novel series-parallel-resonant *LCL* filter for single-phase half-bridge active power filters. *IEEE Trans. Power Electron.* **2017**, *32*, 200–217. [CrossRef]
8. Fang, J.; Li, X.; Tang, Y. A novel *LCL*-filtered single-phase half-bridge distributed static compensator with dc-link filter capacitors and reduced passive component parameters. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 3279–3285.
9. Yang, S.; Wang, P.; Tang, Y.; Zhang, L. Explicit phase lead filter design in repetitive control for voltage harmonic mitigation of VSI-based islanded microgrids. *IEEE Trans. Ind. Electron.* **2017**, *64*, 817–826. [CrossRef]
10. Delille, G.; Francois, B.; Malarange, G. Dynamic frequency control support by energy storage to reduce the impact of wind and solar generation on isolated power system's inertia. *IEEE Trans. Sustain. Energy* **2012**, *3*, 931–939. [CrossRef]
11. Emadi, A.; Williamson, S.S.; Khaligh, A. Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems. *IEEE Trans. Power Electron.* **2006**, *21*, 567–577. [CrossRef]
12. Yilmaz, M.; Krein, P.T. Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles. *IEEE Trans. Power Electron.* **2013**, *28*, 2151–2169. [CrossRef]
13. Fang, J.; Xiao, G.; Xu, Y.; Tang, Y. An optimal digital pulse-width-modulated dither technique to enhance the resolution of high frequency power converters. *IEEE Trans. Power Electron.* **2017**, *32*, 7222–7232. [CrossRef]
14. Peng, F. Z-source inverter. *IEEE Trans. Ind. Appl.* **2003**, *39*, 504–510. [CrossRef]
15. Fang, J.; Xiao, G.; Zhang, Y. An LCCL filter and its application to a half-bridge APF. In Proceedings of the 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, Korea, 1–5 June 2015; pp. 2566–2573.
16. Fang, J.; Li, X.; Tang, Y. A review of passive power filters for voltage-source converters. In Proceedings of the 2016 Asian Conference on Energy, Power and Transportation Electrification (ACEPT), Singapore, 25–27 October 2016.