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Two-Terminal Electronic Circuits with Controllable Linear NDR Region and Their Applications

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Abstract: Negative differential resistance (NDR) is inherent in many electronic devices, in which, over a specific voltage range, the current decreases with increasing voltage. Semiconductor structures with NDR have several unique properties that stimulate the search for technological and circuitry solutions in developing new semiconductor devices and circuits experiencing NDR features. This study considers two-terminal NDR electronic circuits based on multiple-output current mirrors, such as cascode, Wilson, and improved Wilson, combined with a field-effect transistor. The undoubted advantages of the proposed electronic circuits are the linearity of the current-voltage characteristics in the NDR region and the ability to regulate the value of negative resistance by changing the number of mirrored current sources. We derive equations for each proposed circuit to calculate the NDR region's total current and differential resistance. We consider applications of NDR circuits for designing microwave single frequency oscillators and voltage-controlled oscillators. The problem of choosing the optimal oscillator topology is examined. We show that the designed oscillators based on NDR circuits with Wilson and improved Wilson multiple-output current mirrors have high efficiency and extremely low phase noise. For a single frequency oscillator consuming 33.9 mW, the phase noise is −154.6 dBc/Hz at a 100 kHz offset from a 1.310 GHz carrier. The resulting figure of merit is −221.6 dBc/Hz. The implemented oscillator prototype confirms the theoretical achievements.

Keywords: controllable negative differential resistance; cascode current mirror; Wilson current mirror; oscillator; voltage-controlled oscillator; phase noise; power consumption; the figure of merit

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Citation: Ulansky, V.; Raza, A.; Milke, D. Two-Terminal Electronic Circuits with Controllable Linear NDR Region and Their Applications. *Appl. Sci.* **2021**, *11*, 9815. https://doi.org/10.3390/app11219815

Academic Editors: Paolo Visconti, Antonio Facchetti and Manijeh Razeghi

Received: 16 August 2021
Accepted: 16 October 2021
Published: 20 October 2021

1. Introduction

Negative differential resistance is a property of nonlinear semiconductor devices or special electronic circuits. An increase in the voltage drop across them results in a decrease in the flowing current.

Electronic devices with NDR are widely used in electronic and radio engineering systems of the broadest use, not only as of the main elements of amplifying [1], oscillating [2,3], multiplexing [4], static-random-access-memory (SRAM) [5], and switching circuits [6]. Recently, very promising is the use of NDR devices in radar [7], communication [8] and info-communication [9] circuits, analog-to-digital converters [10], and neural network circuits [11] due to the significant simplification of many circuitry solutions. Other possible applications of NDR devices can be found in the comprehensive overview by Reference [12].

Generally, we can divide NDR devices into N and Λ current-voltage characteristics devices and S characteristics devices. Since the article's main content is N-type NDR devices, we will analyze previously published studies for electronic structures with N- and Λ-type characteristics.

One of the main characteristics of any NDR circuit is the peak-to-valley current ratio (PVCR), which is the ratio of the peak to the valley current. In many practical tasks, it is necessary to be able to control the PVCR. For example, in oscillators, the PVCR determines the slope of the current-voltage characteristic in the NDR region, hence the value of the differential resistance at the operating point. In turn, the self-excitation of the oscillator depends on the value of the differential resistance.

The literature review (see Section 2) shows that it is impossible to control PVCR in the NDR circuits of most published studies. In studies where it is possible, the maximum current level lies in the nA or µA range.

This study proposes new two-terminal NDR circuits that combine a field-effect transistor (FET) with a multiple-output cascode, Wilson, or improved Wilson current mirror (CM). Possible types of FETs include a junction field-effect transistor (JFET), metal-semiconductor field-effect transistor (MESFET), high-electron-mobility transistor (HEMT), or pseudomorphic high-electron-mobility transistor (PHEMT). In the analyzed circuits, we control PVCR by changing the number of mirrored currents. Here, we show that one could set the PVCR to any desired value. There are several advantages of the proposed method of controlling PVCR. Firstly, the power supply voltage keeps constant. Secondly, the peak point and valley point voltages are not changed with increasing the number of mirrored currents. Thirdly, the types of transistors are also not changed. Fourthly, the current-voltage characteristics in the NDR region are almost linear. Fifthly, the output resistance of the CM is exceptionally high, which is a valuable property for oscillator applications. The mathematical modeling of the total current in the NDR region has been conducted for all NDR circuits using JFET and PHEMT as a FET for Shockley and Curtice drain current equations. We consider the applications of the proposed NDR circuits for microwave oscillators and voltage-controlled oscillators (VCOs).

The simulation results show that the circuit with multiple-output improved Wilson CM (MIWCM) has the highest slope of the current-voltage curve in the NDR region. The oscillators built on the proposed NDR circuits have extremely low phase noise and are superior in efficiency to most oscillators. The microwave oscillator with multiple-output Wilson CM (MWCM) has the lowest phase noise and the best figure of merit (FOM) when the load is 50 Ω. The VCO with MIWCM has the best FOM.

2. Review

N- and Λ-type characteristics can be obtained both through special semiconductor devices and electronic circuits. Let us consider the most prominent studies related to both groups of NDR structures. Esaki [13,14] and Gunn [15] were the pioneers of N-type NDR devices developing the tunnel and Gunn diodes, respectively, in 1957 and 1962. Stanley and Ager [16] proposed a two-terminal N-type NDR circuit based on one JFET and one bipolar junction transistor (BJT). Sharma and Dutta Roy [17] considered a versatile N-type NDR circuit comprising two BJTs and four resistors. One resistor can control the slope of the current-voltage characteristics in the NDR region. Chung Wu and Ching Wu [18] developed a theory of FET-like NDR devices. The proposed NDR devices include two or three FETs. Some circuits also comprise one BJT. Chua et al. [19] considered several NDR circuits based on the special connection of BJT, JFET, and metal-oxide-semiconductor FET (MOSFET). The authors developed an algorithm to generate a device with N-type current-voltage characteristics. Chen et al. [5] considered the NDR structure of the source-coupled n-channel metal-oxide-semiconductor (nMOS) and p-channel metal-oxide-semiconductor (pMOS) transistors exhibiting ultrahigh PVCR. Such a device can be a building element of SRAM. Trajković and Willson [20] considered two-terminal circuits with N-type current-voltage characteristics using a special connection of two BJTs and three resistors. Jung et al. [21] reported fabricating an N-type double-NDR device using a 3D hybrid structure that includes two 2D vdW/organic heterojunctions and one organic resistor. Kobashi et al. [22] proposed a new NDR transistor based on a p-n heterojunction of organic semiconductors with well-balanced carrier transport through the junction. Lv et al. [23] reported tunneling

FET (TFET) based on a BP/InSe heterostructure in contact with graphene electrodes and covered with an hBN layer. In TFET, the tunneling current and the NDR region strongly depend on electrostatic gating. Qiu et al. [24] considered a graphene-based NDR device based on intrinsic armchair-edged nanoribbons with uniform widths. The device provides a sharp current peak of 1.2 μA at bias 0.8 V and a PVCR of 2.7. Kheirabadi et al. [25] considered armchair graphene nanoribbons for creating the NDR effect, which could have applications in nanoelectronics and nanosensors. Yang and Hwu [26] analyzed the tunable NDR characteristics of metal-insulator-semiconductor-insulator-metal tunnel diodes structure where the PVCR can be over 100. The NDR voltage interval exceeds 1 V. Xiong et al. [27] reported a four-terminal NDR device made from a 2D BP/Al_2O_3/BP sandwich structure with the PVCR exceeding 100 at room temperature. Kim et al. [28] considered an m-NDR device based on a BP/(ReS_2 + HfS_2) type-III double-heterostructure and its application to a ternary latch circuit capable of storing three logic states. Liang et al. [29] proposed a Λ-type NDR circuit based on a particular connection of three nMOS transistors with the same length and different widths of the channel. Gan et al. [30] considered a MOS-heterojunction bipolar transistor (HBT) N-type NDR circuit based on three n-channel MOS and one SiGe HBT device with two power supplies. At specific supply voltages, the NDR circuit provides the PVCR of about 8. Chung et al. [31] reported a three-terminal Si-based NDR device by epitaxially growing a resonant interband tunnel diode atop the emitter of a Si/SiGe HBT on a silicon substrate. The device provides an adjustable PVCR. Semenov [32] proposed a Λ-type NDR BJT-metal–oxide–semiconductor FET (MOSFET) circuit applied to periodic and chaotic mode oscillators. Gan et al. [33] considered a novel NDR circuit comprising nMOS transistors and HBT with application to inverter design based on 0.35 μm SiGe technology. Ulansky et al. [34] presented five electronic circuits of NDR VCOs based on a GaAs transistor and single-output BJT CM. Ulansky et al. [35] considered an NDR circuit comprising a FET and a simple BJT CM with multiple outputs that control the slope of the current-voltage curve by changing the number of CM outputs. Yang [36] investigated a resonant tunneling electronic circuit with reactance elements having high and multiple peak-to-valley current density ratios displayed in the NDR curve. Kadioglu [37] considered a monolayer structure based on vanadium phosphide with a current-voltage characteristic having the NDR region. Rathi et al. [38] observed an NDR region in the current-voltage curve in graphene oxide two-terminal device with precise control of carbon-oxygen ratio. The fabricated novel electronic device can find application in switches and oscillators. Sharma et al. [39] synthesized graphene oxide quantum dots based on graphene oxide, cysteine, and H_2O_2 having N-type current-voltage characteristics with PVCR of 4.7. Shim et al. [40] demonstrated an NDR device on the base of a phosphorene/rhenium disulfide (BP/ReS_2) heterojunction. It has a high PVCR of 4.2 at room temperature. The peak and valley currents are 3 and 0.7 nA, respectively.

We can draw the following conclusions from the review of published studies:

1. Considerable attention is paid to developing new NDR devices [21–28,30,31,33,36–39], indicating the research topic's relevance.
2. Most NDR devices and circuits use one, two, or even three power supplies. Such devices have two [14–20,34,35,38,39], three [18,29,31–33], or four [27] terminals.
3. In most of the published studies, there is no possibility of controlling the PVCR. The PVCR control is available in the NDR devices considered in the studies [26,27,31,39], but the maximum current levels are in the nA and μA ranges. In the NDR circuit [17], the control of PVCR is possible in the mA range by changing the value of one of the resistors.

3. Two-Terminal NDR Circuits

Figure 1 shows a two-terminal electronic circuit with a controllable NDR region. The circuit comprises a voltage divider R_c, R_d, an n-channel FET T_0, a current mirror with m (m = 0, 1, 2, . . .) additional outputs (mirrored current sources), and a power supply $V_{1,2}$.

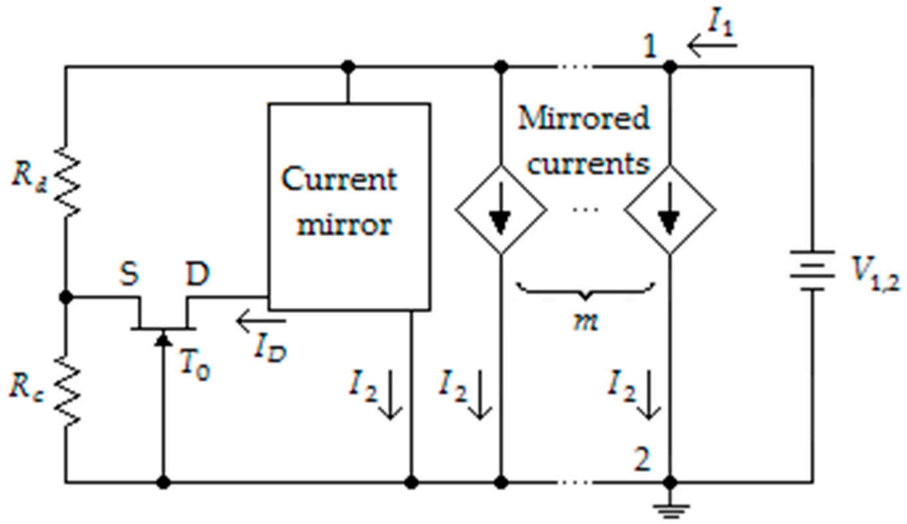

Figure 1. General two-terminal NDR circuit with multiple-output current mirror.

The circuit of Figure 1 has N-type current-voltage characteristics between nodes 1 and 2, as shown in Figure 2. The slope of the NDR region in the current-voltage characteristics depends on the number (m) of the additional mirrored current sources I_2. In Figure 2, the green curve corresponds to $m = 0$, the blue curve to $m = 1$, and the red curve to $m = 2$. As seen in Figure 2, the current-voltage characteristics have four regions. In the first $(0, V_X)$ and fourth (V_Z, ∞) regions, the current I_1 depends only on the voltage $V_{1,2}$. In these regions, all transistors are off. In the second region (V_X, V_Y), all transistors are on. Transistor T_0 operates in the ohmic region, and current I_1 increases. We should also note that the voltage V_Y does not depend on the value of m, i.e., $V_{Yi} = V_Y$, $i = 0, 1, \ldots, m$. In the third region (V_Y, V_Z), transistor T_0 operates in the saturation region and current I_1 decreases due to a decrease in the gate-source voltage.

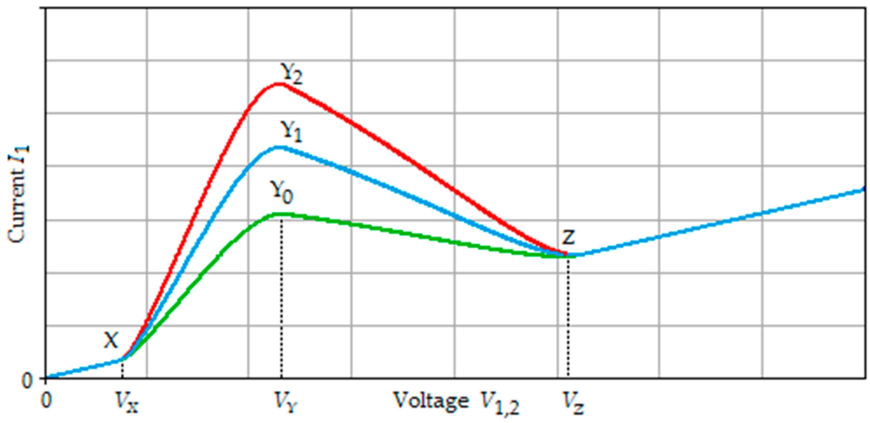

Figure 2. Current-voltage characteristics of a two-terminal NDR circuit with multiple-output current mirror; $m = 0$—green curve, $m = 1$—blue curve, $m = 2$—red curve.

The current I_1 consists of two currents in the NDR region: the current through resistor R_c and $m + 1$ currents I_2. The current through resistor R_c is due to power supply $V_{1,2}$ and the drain-current I_D of transistor T_0. Thus, the current I_1 is given by

$$I_1 = (m+1)I_2 + \frac{I_D R_d}{R_c + R_d} + \frac{V_{1,2}}{R_c + R_d}. \quad (1)$$

Outside the region (V_X, V_Z), the current I_1 is only due to the power supply voltage $V_{1,2}$.

Further, we assume the matching of all transistors in the multiple-output CMs. As is well-known [40], for large transistor dc gain h_{FE}, the currents I_2 and I_D are approximately identical. The magnitude of the difference in currents I_2 and I_D depends on the selected CM.

Figure 3 shows a two-terminal NDR circuit with the multiple-output cascode CM (MCCM). The following relation links currents I_2 and I_D [41]:

$$I_2 = I_D\left(1 - \frac{4h_{FE} + 2}{h_{FE}^2 + 4h_{FE} + 2}\right). \tag{2}$$

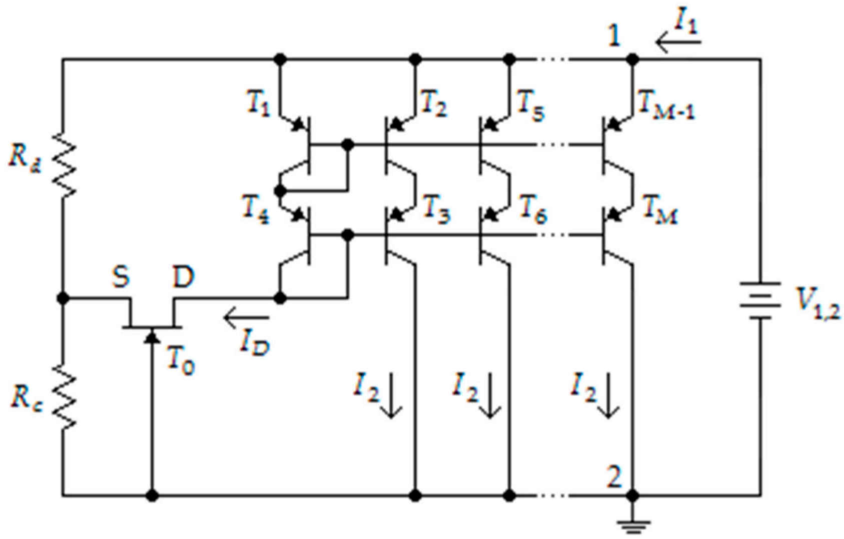

Figure 3. Two-terminal NDR circuit with multiple-output cascode current mirror.

By substitution (2) to (1), we obtain the total current in the NDR region:

$$I_1 = I_D\left[\frac{(m+1)}{1 + 4/h_{FE} + 2/h_{FE}^2} + \frac{R_d}{R_c + R_d}\right] + \frac{V_{1,2}}{R_c + R_d}. \tag{3}$$

The advantage of using cascode CM in the two-terminal NDR circuit is its high output resistance. The disadvantage is a mismatch between currents I_2 and I_D.

Figure 4 shows a two-terminal NDR circuit using MWCM. With finite Early voltage V_A, the currents I_2 and I_D are related as follows [41]:

$$I_2 = I_D\left(1 - \frac{2}{h_{FE}^2 + 2h_{FE} + 2}\right)\left(1 - \frac{V_{EB3}}{V_A}\right), \tag{4}$$

where V_{EB3} is the emitter-base voltage of transistor T_3.

Substituting (4) to (1) gives the following equation for the total current in the NDR region:

$$I_1 = I_D\left[(m+1)\left(1 - \frac{2}{h_{FE}^2 + 2h_{FE} + 2}\right)\left(1 - \frac{V_{EB3}}{V_A}\right) + \frac{R_d}{R_c + R_d}\right] + \frac{V_{1,2}}{R_c + R_d}. \tag{5}$$

The advantage of using MWCM in the NDR circuit of Figure 1 is high output resistance and a slight mismatch between master branch current (I_D) and slave branch current (I_2). The disadvantage is the difference in collector-emitter voltages V_{EC1} and V_{EC2}, which is equal to voltage V_{EB3}.

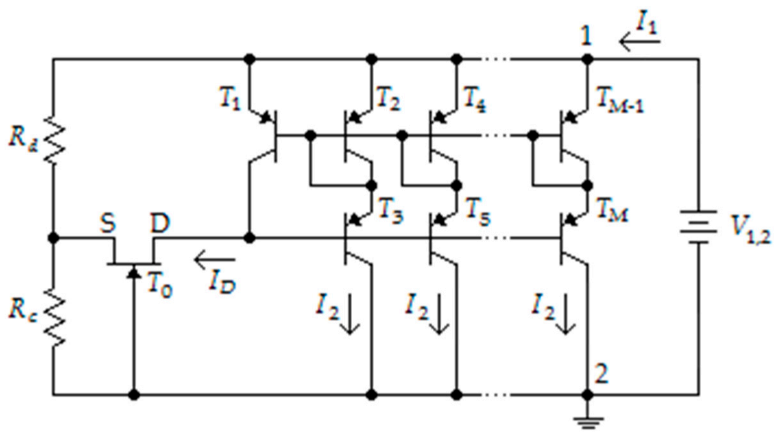

Figure 4. Two-terminal NDR circuit with multiple-output Wilson current mirror.

Figure 5 shows a two-terminal NDR circuit with MIWCM. The improved Wilson CM introduces a diode-connected transistor T_4 equalizing the collector-emitter voltages of transistors T_1 and T_2. Therefore, Equation (4) is reduced to [41]

$$I_2 = I_D\left(1 - \frac{2}{h_{FE}^2 + 2h_{FE} + 2}\right). \tag{6}$$

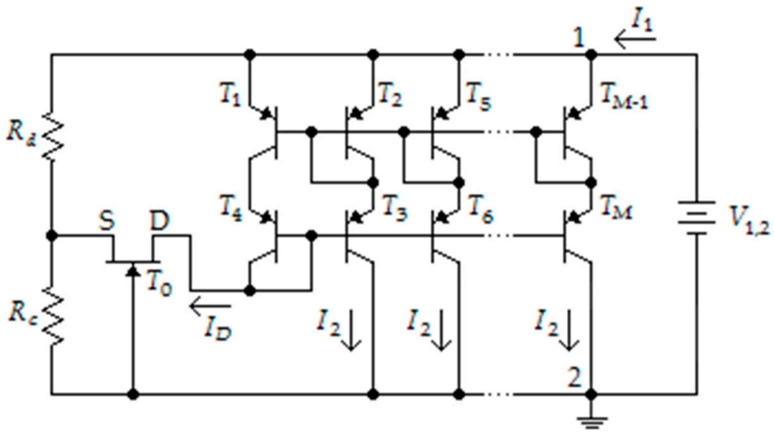

Figure 5. Two-terminal NDR circuit with multiple-output improved Wilson current mirror.

Substituting (6) to (1), we obtain an equation for the total current in the NDR region:

$$I_1 = I_D\left[(m+1)\left(1 - \frac{2}{h_{FE}^2 + 2h_{FE} + 2}\right) + \frac{R_d}{R_c + R_d}\right] + \frac{V_{1,2}}{R_c + R_d}. \tag{7}$$

Analysis of (3), (5), and (7) shows that the total current I_1 in the NDR region is a function of the drain current of transistor T_0, which is an n-channel FET. For the existence of the NDR region, the transistor T_0 must have a negative threshold voltage. Therefore, suitable types of transistors are JFET, depletion metal-oxide-semiconductor FET (DMOSFET), MESFET, HEMT, and PHEMT. As shown in Reference [35], the two-terminal NDR circuit with a multiple-output simple CM has an NDR effect when transistor T_0 is in saturation mode. In the circuits presented by Figures 3–5, transistor T_0 should also operate in the saturation mode in the NDR region. Thus, to calculate the current I_1, it is necessary to model the current I_D for the selected type of transistor T_0.

4. Modeling the Drain Current of Transistor T_0

As we can see from (3), (5), and (7), to calculate the total current I_1 in the NDR region, we should know the drain current I_D of the transistor T_0. The modeling of current I_D depends on the type of transistor T_0.

If transistor T_0 is a JFET, the Shockley equation well represents the drain current in the saturation region:

$$I_D = \frac{I_{DSS}}{V_P^2}(V_P - V_{GS})^2, \tag{8}$$

where I_{DSS} is the drain current of transistor T_0 at zero bias, V_P is the negative pinch-off voltage, and V_{GS} is the gate-source voltage.

The voltage between gate and source of transistor T_0 is negative and consists of two parts: the voltage due to voltage divider R_c, R_d:

$$\frac{R_c V_{1,2}}{R_c + R_d}, \tag{9}$$

and the voltage drop across resistor R_c because of the current through this resistor, i.e.,

$$\frac{I_D R_d}{R_c + R_d} R_c. \tag{10}$$

Combining (9) and (10) gives

$$V_{GS} = -\frac{R_c V_{1,2}}{R_c + R_d} - I_D(R_c \| R_d). \tag{11}$$

Substituting (11) to (8) and providing some mathematical manipulations, we obtain the following quadratic equation for determining the value of the current I_D:

$$(R_c\|R_d)^2 I_D^2 + \left[2\left(V_P + \frac{V_{1,2}R_c}{R_c + R_d}\right)(R_c\|R_d) - \frac{V_P^2}{I_{DSS}}\right] I_D + \left(V_P + \frac{V_{1,2}R_c}{R_c + R_d}\right)^2 = 0. \tag{12}$$

If transistor T_0 is a MESFET, we can model the current I_D by one of the nonlinear large-signal models [42–44]. For example, the popular Curtice model in the saturation region is as follows [42]:

$$I_D = b(V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tanh(\alpha V_{DS}), \tag{13}$$

where b is the transconductance, λ is the channel length modulation coefficient, α is the coefficient of the hyperbolic tangent function, V_{DS} is the drain-source voltage, and V_{TH} is the threshold voltage.

The voltage V_{DS} we find by applying Kirchhoff's voltage law to the circuit of Figure 1.

$$V_{1,2} - (V_{1,2} - V_D) - V_{DS} + V_{GS} = 0, \tag{14}$$

where V_D is the voltage at the drain of transistor T_0.

Substituting V_{GS} from (11) into (14), we obtain

$$V_{DS} = \frac{R_d V_{1,2}}{R_c + R_d} - I_D(R_c\|R_d) - (V_{1,2} - V_D). \tag{15}$$

It is evident that, for all circuits in Figures 3–5, the voltage $(V_{1,2} - V_D)$ is equal to

$$V_{1,2} - V_D = 2V_{EB}, \tag{16}$$

where V_{EB} is the emitter-base voltage of BJT used in the current mirror.

Substituting (11) and (15) into (13), we obtain the following nonlinear equation for determining the value of the current I_D:

$$\begin{gathered}\left[(R_c\|R_d)^2 I_D^2 + 2\left(V_{TH} + \tfrac{V_{1,2}R_c}{R_c+R_d}\right)(R_c\|R_d)I_D + \left(V_{TH} + \tfrac{V_{1,2}R_c}{R_c+R_d}\right)^2\right]\times \\ \left\{\lambda\left[-(R_c\|R_d)I_D + \tfrac{V_{1,2}R_d}{R_c+R_d} - (V_{1,2}-V_D)\right]+1\right\}\times \\ \tanh\left\{\alpha\left[-(R_c\|R_d)I_D + \tfrac{V_{1,2}R_d}{R_c+R_d} - (V_{1,2}-V_D)\right]\right\} - I_D/b = 0.\end{gathered} \tag{17}$$

Solving Equation (17), we can find the value of I_D for the selected two-terminal NDR circuit. Then, by substitution of I_D into (3), (5), or (7), we can calculate the total current I_1.

The large-signal modeling of HEMT and PHEMT is quite similar to MESFET modeling [45].

5. Modeling the Negative Differential Resistance

We find the NDR at the operating point as follows:

$$R_{diff} = \left(\frac{dI_1}{dV_{1,2}}\right)^{-1}. \tag{18}$$

Let us determine R_{diff} for the two-terminal NDR circuits shown in Figures 3–5. Substituting current I_1 from (3), (5), and (7) into (18) and taking the first derivative of function I_1 concerning variable $V_{1,2}$, we obtain the following equations for the NDR:

for the two-terminal NDR circuit with an MCCM,

$$R_{diff} = \left[\frac{dI_D}{dV_{1,2}}\left(\frac{(m+1)}{1+4/h_{FE}+2/h_{FE}^2} + \frac{R_d}{R_c+R_d}\right) + \frac{1}{R_c+R_d}\right]^{-1}, \tag{19}$$

for the two-terminal NDR circuit with an MWCM,

$$R_{diff} = \left\{\frac{dI_D}{dV_{1,2}}\left[(m+1)\left(1-\frac{2}{h_{FE}^2+2h_{FE}+2}\right)\left(1+\frac{V_{CE2}-V_{CE1}}{V_A}\right) + \frac{R_d}{R_c+R_d}\right] + \frac{1}{R_c+R_d}\right\}^{-1}, \tag{20}$$

and, for the two-terminal NDR circuit with a MIWCM,

$$R_{diff} = \left\{\frac{dI_D}{dV_{1,2}}\left[(m+1)\left(1-\frac{2}{h_{FE}^2+2h_{FE}+2}\right) + \frac{R_d}{R_c+R_d}\right] + \frac{1}{R_c+R_d}\right\}^{-1}. \tag{21}$$

The derivative $dI_D/dV_{1,2}$ in (19)–(21) cannot be derived analytically. Therefore, we can replace this derivative with the ratio of $\Delta I_D/\Delta V_{1,2}$ in the vicinity of the operating point. Then, calculate the increment of current ΔI_D by (12) for a JFET and by (17) for a MESFET, HEMT, or PHEMT.

6. Applications

6.1. Negative Differential Resistance Oscillators

The two-terminal circuits shown in Figures 3–5 can be used for constructing single-frequency NDR oscillators. Figures 6–8 show the NDR oscillators based on MCCM, MWCM, and MIWCM.

In the oscillator circuits of Figures 6–8, capacitors C_1, C_2, and inductor L establish a resonant tank circuit. Capacitor C_a is a feedback element used to improve the start-up of the oscillator. Capacitor C_b serves as a noise killer at the drain of transistor T_0.

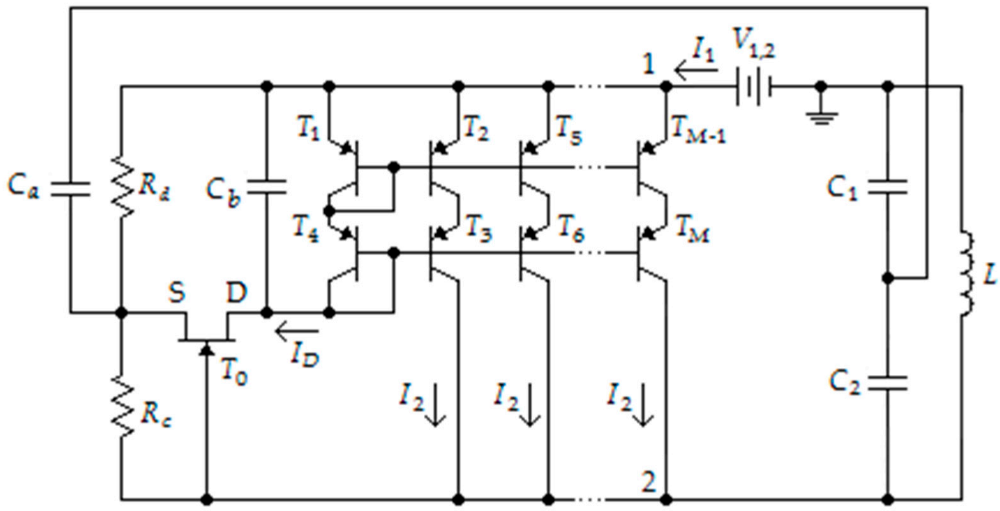

Figure 6. NDR oscillator with multiple-output cascode current mirror.

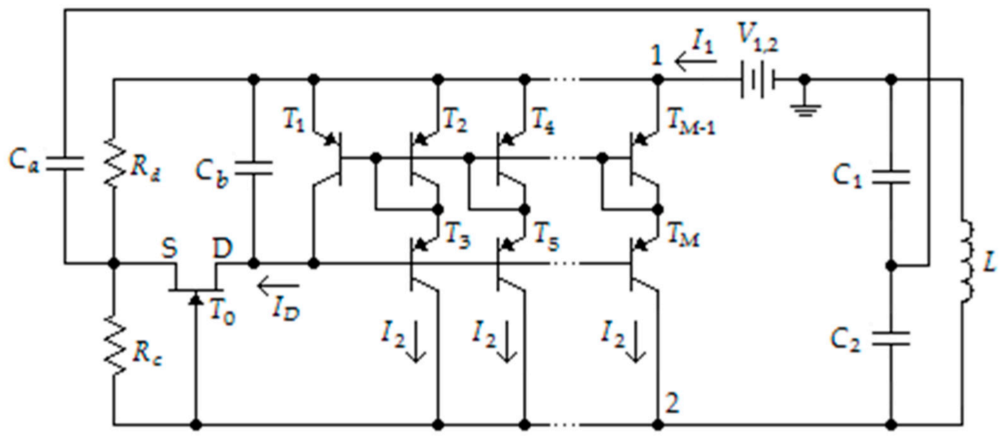

Figure 7. NDR oscillator with multiple-output Wilson current mirror.

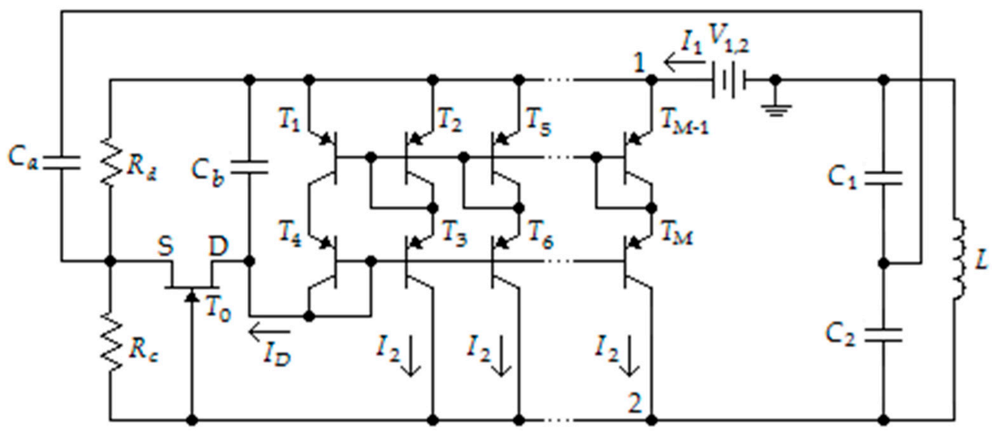

Figure 8. NDR oscillator with multiple-output improved Wilson current mirror.

We show later that the NDR oscillator performance depends on the selected CM and the number of additional current sources I_2.

The main characteristics of oscillators are frequency of operation, phase noise, harmonic distortions, and power consumption. Designers use several merit figures combining some or all of the key features to compare different oscillators [46,47].

The most common figure of merit (FOM) is given by [48]

$$FOM\left(f_{of}\right) = PN\left(f_{of}\right)_{dBc} - 20\log\left(f_c/f_{of}\right) + 10\log(P_{dis}/1\text{mW}), \tag{22}$$

where f_{of} is the offset frequency from the carrier frequency f_c, $PN(f_{of})$ is the oscillator phase noise at offset frequency f_{of}, and P_{dis} is the oscillator dissipation power. The second term allows us to compare oscillators operating at different frequencies. Thus, this criterion is invariant to the oscillator frequency.

According to (22), the less FOM, the more efficient oscillator.

For self-excitation of the oscillator, it is necessary to compensate for the tank circuit's losses. Negative differential resistance of the oscillator's electronic circuit carries such compensation for the tank circuit losses. Therefore, the condition for self-excitation of the NDR oscillator has the following form [49]:

$$\left|R_{diff}\right| < R_Q, \tag{23}$$

where $|R_{diff}|$ is the absolute value of the NDR at the operating point calculated by (19)–(21), and R_Q is the loaded tank circuit resistance at the resonance.

The loaded tank circuit resistance at resonance is [50] (p. 905)

$$R_Q = \rho Q_l, \tag{24}$$

where ρ is the characteristic impedance of the tank circuit, and Q_l is the loaded quality factor of the tank circuit.

6.2. Negative Differential Resistance Voltage-Controlled Oscillators

Voltage-controlled oscillators are crucial elements of modern instrumentation, communication, navigation, and radar systems. We can classify VCOs as negative impedance (NI) and NDR oscillators. In the NI VCOs, the real part of the input impedance has a negative sign [51,52]. This negative resistance compensates for the losses in the tank circuit. In the NDR VCOs, a negative resistance induced into the tank circuit neutralizes the tank circuit losses; this resistance is inversely proportional to the absolute value of R_{diff} [53].

The two-terminal circuits of Figures 3–5 can be the base of NDR VCOs. Figures 9–11 show the NDR VCOs based on MCCM, MWCM, and MIWCM. In the VCO circuits, instead of capacitors C_1 and C_2, two oppositely connected varactors, Var_1 and Var_2, are used. A voltage source V_{var} applies dc voltage to the cathodes of varactors. Resistor R_0 is linked with the voltage source V_{var}, preventing the parallel tank circuit's shunting.

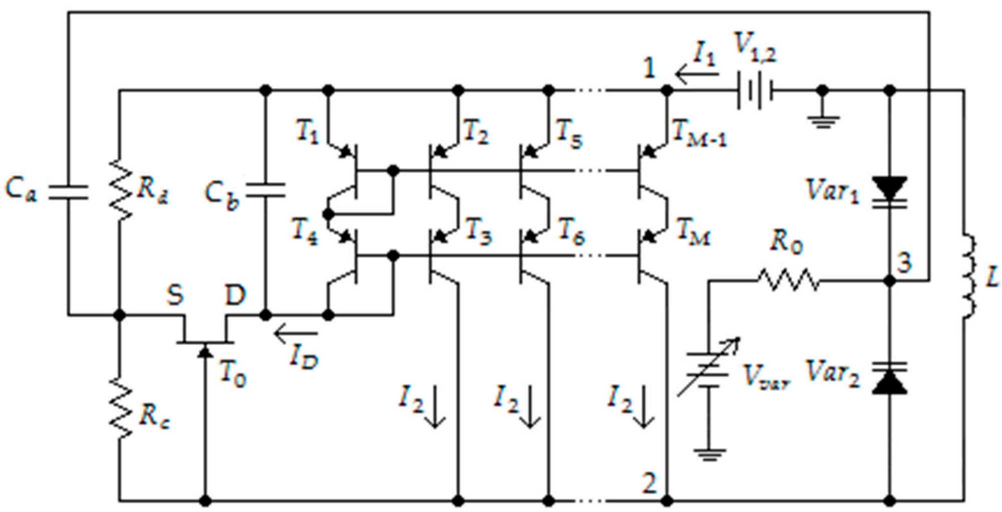

Figure 9. Voltage-controlled oscillator with multiple-output cascode current mirror.

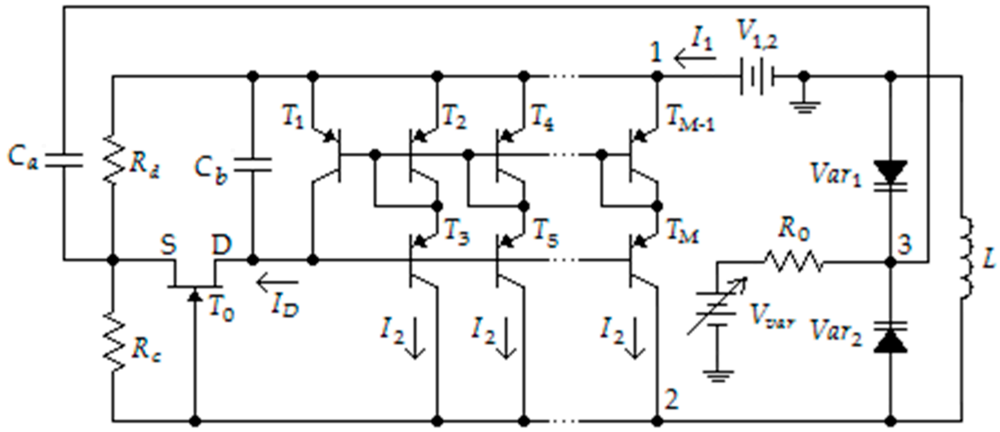

Figure 10. Voltage-controlled oscillator with multiple-output Wilson current mirror.

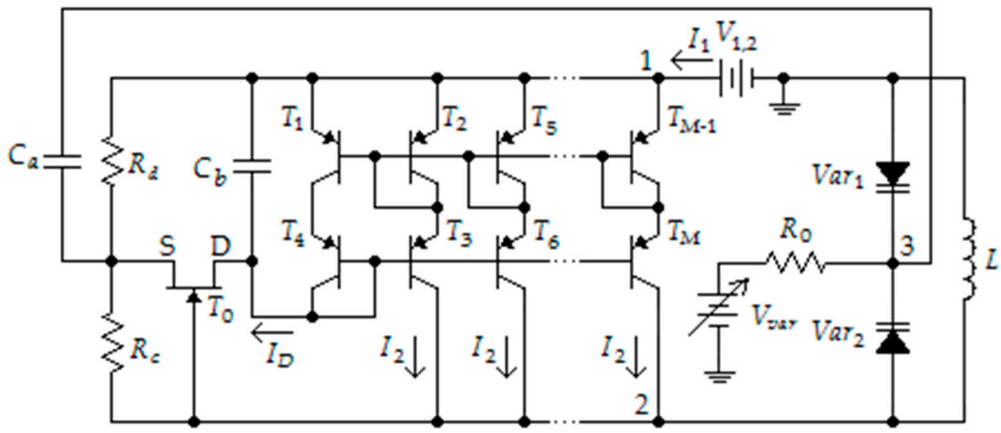

Figure 11. Voltage-controlled oscillator with multiple-output improved Wilson current mirror.

Further, we use FOM (22) to compare VCO circuits shown in Figures 9–11.

7. Results and Discussion

7.1. Simulation and Calculation of Current-Voltage Characteristics

Let us simulate the current-voltage characteristics for two-terminal NDR circuits presented in Figures 3–5 by Multisim 14.0. As transistor T_0, we use MMBFU310LT1 and BFT92W as transistors in current mirrors. We select the following resistor values: R_c = 1 kΩ and R_d = 2 kΩ.

Figures 12–14 show the current-voltage characteristics for the two-terminal NDR circuits with different multiple-output CMs. Table 1 shows the values of voltages and currents at the breakpoints of the curves. Analysis of current-voltage characteristics in Figures 12–14 and data in Table 1 leads to the following conclusions: all two-terminal NDR circuits have the same voltages V_X, V_Y, and V_Z and currents I_X and I_Z for any value of m, two-terminal NDR circuit with MCCM has the smallest value of current I_Y for any value of m, two-terminal NDR circuit with MIWCM has the most considerable value of current I_Y for any value of m, and two-terminal NDR circuits with MCCM, MWCM, and MIWCM have almost linear dependence of current on voltage in the NDR region.

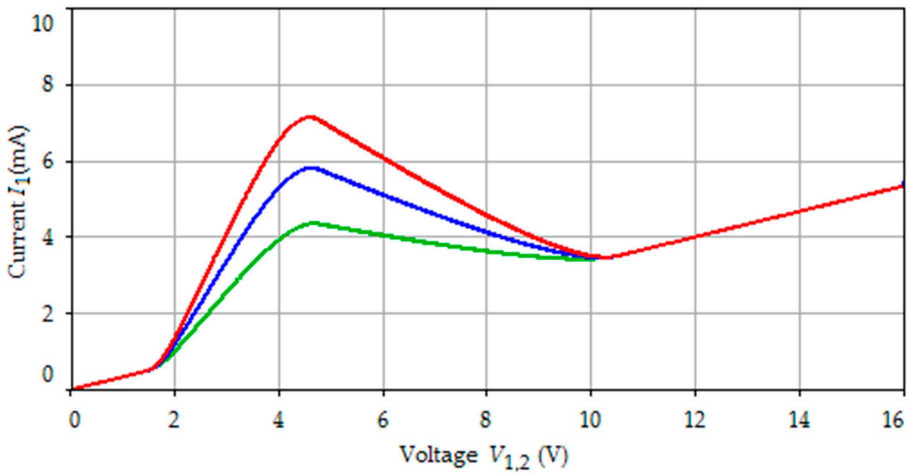

Figure 12. Current-voltage characteristics of the two-terminal NDR circuit with multiple-output cascode current mirror; m = 0—green curve, m = 1—blue curve, m = 2—red curve.

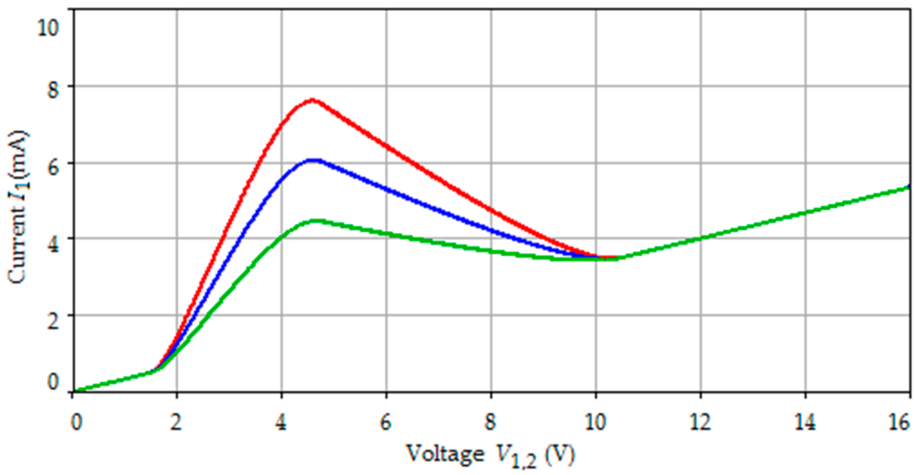

Figure 13. Current-voltage characteristics of the two-terminal NDR circuit with multiple-output Wilson current mirror; m = 0—green curve, m = 1—blue curve, m = 2—red curve.

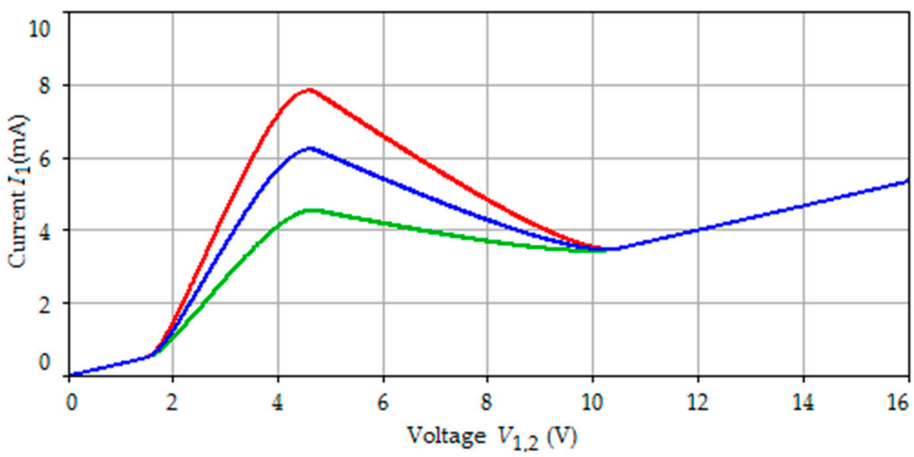

Figure 14. Current-voltage characteristics of the two-terminal NDR circuit with multiple-output improved Wilson current mirror; m = 0—green curve, m = 1—blue curve, m = 2—red curve.

Table 1. Simulated parameters of current-voltage characteristics for different two-terminal NDR circuits (T_0—JFET).

Type of NDR Circuit $\rightarrow$	**NDR Circuit with Multiple-Output**		
Parameter of I–V Characteristics $\downarrow$	**Cascode Current Mirror**	**Wilson Current Mirror**	**Improved Wilson Current Mirror**
V_X (V)	1.46	1.46	1.46
I_X (mA)	0.5	0.5	0.5
V_Y (V)	4.6	4.6	4.6
I_Y (mA) $m = 0$	4.3	4.4	4.5
I_Y (mA) $m = 1$	5.8	6.1	6.2
I_Y (mA) $m = 2$	7.1	7.6	7.8
V_Z (V)	10.2	10.2	10.2
I_Z (mA)	3.5	3.5	3.5

Since current I_Z is the same for all two-terminal NDR circuits, and current I_Y is different, the slope of the current-voltage characteristics in the NDR region is higher for the greater value of current I_Y. Therefore, we can order the absolute negative resistance values of various two-terminal NDR circuits according to the following inequality:

$$\left|R_{diff}^{C}\right| > \left|R_{diff}^{W}\right| > \left|R_{diff}^{IW}\right|, \tag{25}$$

where $\left|R_{diff}^{C}\right|$, $\left|R_{diff}^{W}\right|$, and $\left|R_{diff}^{IW}\right|$ are, respectively, the absolute values of NDR in the two-terminal circuits with cascode, Wilson, and improved Wilson CM.

Thus, inequalities (23) and (25) indicate that the oscillator with multiple-output improved Wilson CM has the most considerable self-excitation ability. In addition, the oscillator with multiple-output cascode CM has the least self-excitation ability.

For comparison with the simulation results, we calculate the current I_1 using (3), (5), and (7) with the following data of transistors MMBFU310LT1 and BFT92W: I_{DSS} = 50 mA, V_P = –3.5 V, V_A = 11 V, and V_{EB3} = 0.6 V. We use the same values of resistors R_c and R_d as in the simulation.

Figures 15 and 16 show the calculated dependences of current-voltage characteristics in the NDR region for different two-terminal circuits. Tables 2 and 3 show the calculated currents I_Y and I_Z and the relative accuracy of the I_Y current calculation ΔI_Y %, where ΔI_Y % is given by

$$\delta I_Y\% = \frac{I_Y(\text{calculated}) - I_Y(\text{simulated})}{I_Y(\text{calculated})} \times 100\%. \tag{26}$$

As shown in Table 3, the highest accuracy of current I_Y calculation when m = 0 belongs to Equations (5) and (7) for the two-terminal NDR circuit with an MWCM and MIWCM. The highest accuracy of the current I_Y calculation when m = 1, 2 has Equation (5) for the two-terminal NDR circuit with an MWCM. The worst accuracy of the current I_Y calculation when m = 0, 1, 2 has Equation (3) for the two-terminal NDR circuit with an MCCM.

In general, we should note that the worst accuracy does not exceed 12.3%, which indicates a sufficient engineering accuracy for calculating the current I_Y. A practically zero error exists in calculating the current I_Z.

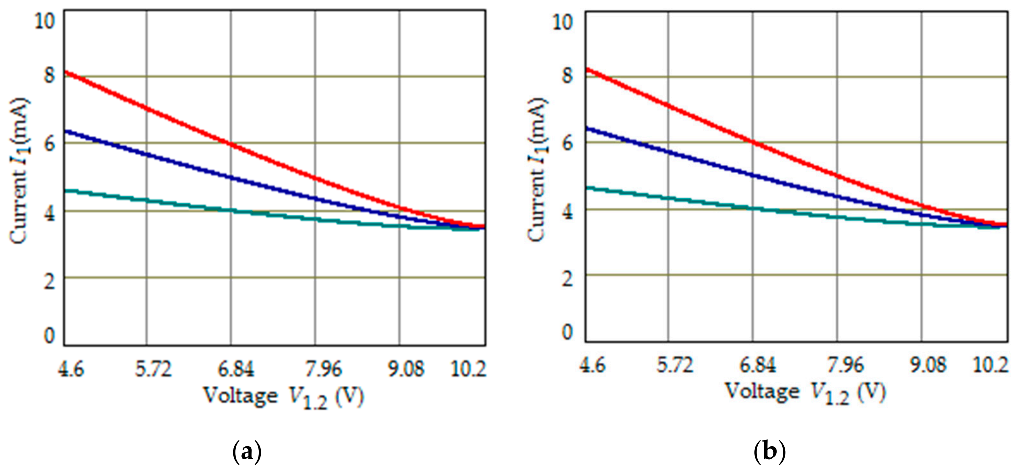

Figure 15. (**a**) Calculated current-voltage characteristics of the NDR circuit with multiple-output cascode current mirror in the NDR region; m = 0—green curve, m = 1—blue curve, m = 2—red curve. (**b**) Calculated current-voltage characteristics of the NDR circuit with multiple-output Wilson current mirror in the NDR region; m = 0—green curve, m = 1—blue curve, m = 2—red curve.

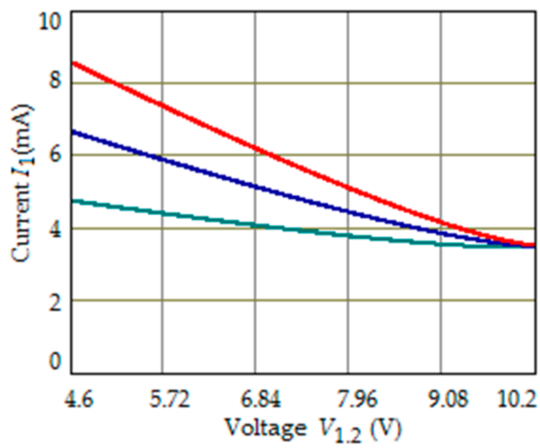

Figure 16. Calculated current-voltage characteristics of the NDR circuit with multiple-output improved Wilson current mirror in the NDR region; m = 0—green curve, m = 1—blue curve, m = 2—red curve.

Table 2. Calculated parameters of current-voltage characteristics for different two-terminal NDR circuits (T_0—JFET).

Type of NDR Circuit →	**Two-Terminal NDR Circuit with Multiple-Output**		
Parameter of I–V Characteristics ↓	**Cascode Current Mirror**	**Wilson Current Mirror**	**Improved Wilson Current Mirror**
V_Y (V)	4.6	4.6	4.6
I_Y (mA) $m = 0$	4.6	4.6	4.7
I_Y (mA) $m = 1$	6.4	6.4	6.7
I_Y (mA) $m = 2$	8.1	8.2	8.6
V_Z (V)	10.2	10.2	10.2
I_Z (mA)	3.5	3.5	3.5

Table 3. The relative accuracy of the I_Y current calculation for different two-terminal NDR circuits (T_0—JFET).

Type of NDR Circuit →	Two-Terminal NDR Circuit with Multiple-Output		
The Relative Accuracy of the I_Y Current Calculation ↓	Cascode Current Mirror	Wilson Current Mirror	Improved Wilson Current Mirror
ΔI_Y % $m = 0$	6.5%	4.3%	4.3%
ΔI_Y % $m = 1$	9.4%	4.7%	7.5%
ΔI_Y % $m = 2$	12.3%	7.3%	9.3%

Now, let us simulate the current-voltage characteristics for two-terminal NDR circuits presented in Figures 3–5 when transistor T_0 is a PHEMT. We select ATF34143 as transistor T_0 and MRFC521 as transistors in BJT CM and choose the following resistor values: $R_c = 300\ \Omega$ and $R_d = 4\ \text{k}\Omega$.

Figures 17–19 show the current-voltage characteristics for the PHEMT based two-terminal NDR circuits with different multiple-output CM. Table 4 shows the values of voltages and currents at the breakpoints of characteristics. From the analysis of Table 4, the same conclusions follow as from the study of Table 1. As in using JFET, the PHEMT based two-terminal circuits also have a linear current dependence on voltage in the NDR region.

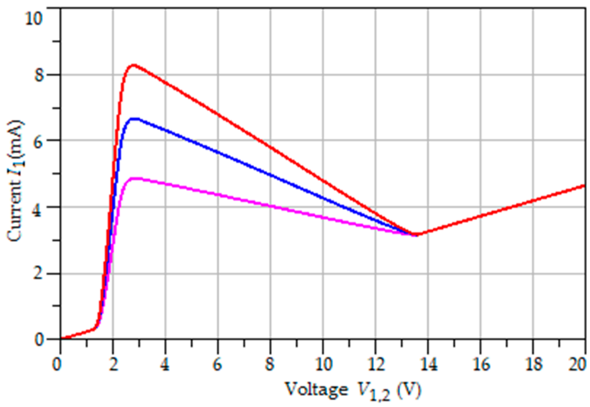

Figure 17. Current-voltage characteristics of the NDR circuit with multiple-output cascode current mirror; $m = 0$—purple curve, $m = 1$—blue curve, $m = 2$—red curve.

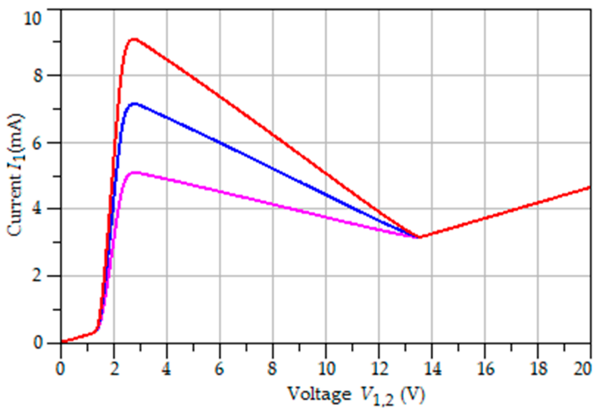

Figure 18. Current-voltage characteristics of the NDR circuit with multiple-output Wilson current mirror; $m = 0$—purple curve, $m = 1$—blue curve, $m = 2$—red curve.

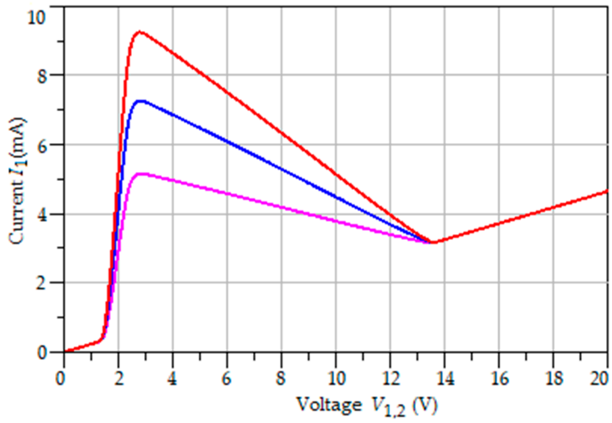

Figure 19. Current-voltage characteristics of the NDR circuit with multiple-output improved Wilson current mirror; m = 0—purple curve, m = 1—blue curve, m = 2—red curve.

Table 4. Simulated parameters of current-voltage characteristics for different two-terminal NDR circuits (T_0—PHEMT).

Type of NDR Circuit →	Two-Terminal NDR Circuit with Multiple-Output		
Parameter of I–V Characteristic ↓	**Cascode Current Mirror**	**Wilson Current Mirror**	**Improved Wilson Current Mirror**
V_X (V)	1.2	1.2	1.2
I_X (mA)	0.3	0.3	0.3
V_Y (V)	2.8	2.8	2.8
I_Y (mA), m = 0	4.9	5.1	5.2
I_Y (mA), m = 1	6.7	7.2	7.3
I_Y (mA), m = 2	8.3	9.1	9.3
V_Z (V)	13.6	13.6	13.6
I_Z (mA)	3.2	3.2	3.2

We also calculate the current I_1 at voltages V_X, V_Y, and V_Z using Equations (3), (5) and (7) with the following data of transistors ATF34143 [54] and MRFC521: b = 0.24 A/V^2, V_{TH} = –0.95 V, α = 4 V^{-1}, λ = 0.09 V^{-1}, h_{FE} = 50, V_A = 15 V, V_{EB3} = 0.7 V. The values of resistors R_c and R_d are similar to those used in simulation.

Tables 5 and 6 show the calculated currents I_Y and I_Z and the relative accuracy of the I_Y current calculation ΔI_Y %. The conclusions concerning the accuracy of the current I_Y calculation for Table 6 are the same as those for Table 3.

We should note that the accuracy of calculating the current I_D by Formula (17) is quite high. Indeed, for all two-terminal NDR circuits at V_Y = 2.8 V, the current I_D(simulated) = 2.79 mA, and the current I_D(calculated) = 2.67 mA. Therefore, ΔI_D % = –4.5 %, where ΔI_D % is the relative accuracy of calculating the current I_D by formula

$$\delta I_D\% = \frac{I_D(\text{calculated}) - I_D(\text{simulated})}{I_D(\text{calculated})} \times 100\%. \tag{27}$$

Table 5. Simulated parameters of current-voltage characteristics for different two-terminal NDR circuits (T_0—PHEMT).

Type of NDR Circuit →	**Two-Terminal NDR Circuit with Multiple-Output**		
Parameter of I–V Characteristic ↓	**Cascode Current Mirror**	**Wilson Current Mirror**	**Improved Wilson Current Mirror**
V_Y (V)	2.8	2.8	2.8
I_Y (mA), $m = 0$	5.6	5.7	5.8
I_Y (mA), $m = 1$	8.1	8.2	8.5
I_Y (mA), $m = 2$	10.5	10.8	11.1
V_Z (V)	13.6	13.6	13.6
I_Z (mA)	3.2	3.2	3.2

Table 6. The relative accuracy of the I_Y current calculation for different two-terminal NDR circuits (T_0—PHEMT).

Type of NDR Circuit →	**Two-Terminal NDR Circuit with Multiple-Output**		
The Relative Accuracy of the I_Y Current Calculation ↓	**Cascode Current Mirror**	**Wilson Current Mirror**	**Improved Wilson Current Mirror**
ΔI_Y %, $m = 0$	12.5%	10.5%	10.3%
ΔI_Y %, $m = 1$	17.3%	12.2%	14.1%
ΔI_Y %, $m = 2$	20.9%	15.7%	16.2%

7.2. Simulation of Negative Differential Resistance

By inequality (23), the steepness of the current-voltage characteristics in the vicinity of the operating point significantly affects the self-excitation of an oscillator. The less the absolute value of the differential resistance, the greater is the probability of self-excitation of the oscillator.

Table 7 shows the simulation results of the differential resistance at the operating point $V_{1,2} = 4$ V for two-terminal NDR circuits shown in Figures 3–5 using the same input data as Table 4. As shown in Table 7, the smallest absolute value of NDR at the operating point has a two-terminal NDR circuit with an improved Wilson CM. The NDR circuit with a Wilson CM has a little greater absolute value of NDR. The circuit with a cascode CM has the most considerable absolute value of NDR for any m. Thus, the improved Wilson and Wilson CM oscillators have the best start-up conditions due to inequality (23).

Table 7. Simulated negative differential resistance for different two-terminal NDR circuits (T_0—PHEMT).

Type of NDR Circuit →	**Two-Terminal NDR Circuit with Multiple-Output**		
Negative Differential Resistance R_{diff} (kΩ) ↓	**Cascode Current Mirror**	**Wilson Current Mirror**	**Improved Wilson Current Mirror**
$m = 0$	−6.25	−5.56	−5.41
$m = 1$	−3.07	−2.70	−2.67
$m = 2$	−2.63	−1.85	−1.80

7.3. Simulation of Oscillator Characteristics

Let us simulate the characteristics for oscillators presented in Figures 6–8 by ADS2020. As transistor T_0, we use ATF34143 and MRFC521 as transistors in BJT CM. We select chip inductor 0604HQ-1N1XJR (1.15 nH), and C_1 = C_2 = 1 pF, R_c = 300 Ω, R_d = 4 kΩ, C_b = 300 nF, and $V_{1,2}$ = 4 V for all oscillators. We selected the value of capacitance C_a from the condition of minimizing the phase noise of each oscillator.

We use FOM (22) to compare oscillators shown in Figures 6–8. Table 8 shows the results of the oscillators' simulation under the assumption that load resistance (R_L) is infinite.

Table 8. Simulated characteristics of different NDR oscillators when $R_L = \infty$.

Type of Oscillator	**Capacitance, C_a (pF)**	**Oscillator Characteristics**			
		Frequency of Operation, *f* (MHz)	**Phase Noise at an Offset Frequency of 10^5 Hz, *PN* (dBc/Hz)**	**Power of Dissipation, P_{dis} (mW)**	**The Figure of Merit, *FOM* (dBc/Hz)**
MCCM (m = 0)	8	2019	−125.4	18.8	−198.8
MCCM (m = 1)	8	1627	−104.4	25.2	−174.6
MCCM (m = 2)	25	1412	−104.7	31.0	−172.8
MWCM (m = 0)	1	1958	−150.7	19.6	−223.6
MWCM (m = 1)	1	1556	−151.1	27.0	−220.6
MWCM (m = 2)	3	1335	−159.9	33.9	−227.1
MIWCM (m = 0)	3	1951	−145.0	19.8	−217.8
MIWCM (m = 1)	1	1554	−152.0	27.4	−221.5
MIWCM (m = 2)	2	1333	−152.6	34.5	−219.7

As shown in Table 8, oscillators with MCCM, MWCM, and MIWCM have the best FOM value when m is 0, 2, and 1, respectively. Among all oscillators, the best FOM of −227.1 dBc/Hz has the one with MWCM when m = 2. For each value of m in Table 8, oscillators with MWCM and MIWCM have significantly better FOM than the oscillator with MCCM. For each value of m, the oscillator with MCCM has the highest oscillation frequency, the lowest power of dissipation, and the worst phase noise.

Figure 20 shows the dependence of phase noise versus offset frequency for the oscillator with MWCM. As shown in Figure 20, the best value of phase noise of −159.9 dBc/Hz at an offset frequency of 100 kHz is the case when m = 2 and C_a = 3 pF.

Figure 21 shows the dependence of phase noise versus capacitance C_b for the oscillator with multiple-output Wilson CM. We can see from Figure 21 that oscillator phase noise significantly depends on the value of C_b. Indeed, when capacitance C_b varies from 3 to 300 nF, phase noise decreases from −125.5 to −159.9 dBc/Hz. We can explain such a decrease in phase noise by reducing noise spectral density at the drain of transistor T_0 where capacitor C_b is connected.

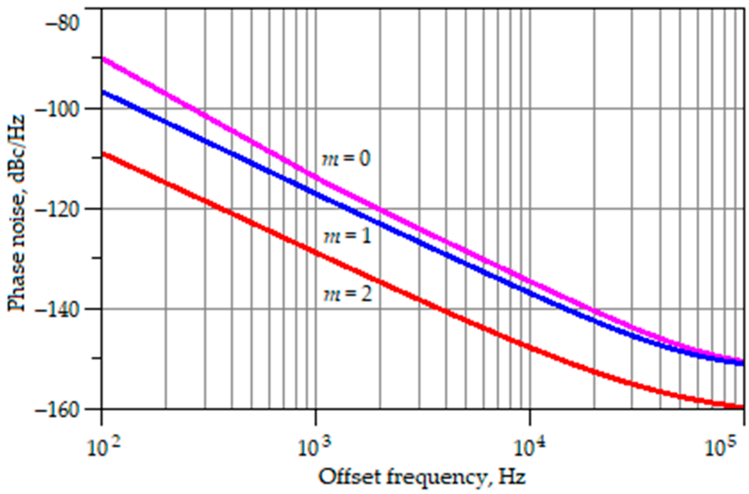

Figure 20. Phase noise versus offset frequency for the oscillator with multiple-output Wilson current mirror when $R_L = \infty$; $m = 0$—purple curve, $m = 1$—blue curve, $m = 2$—red curve.

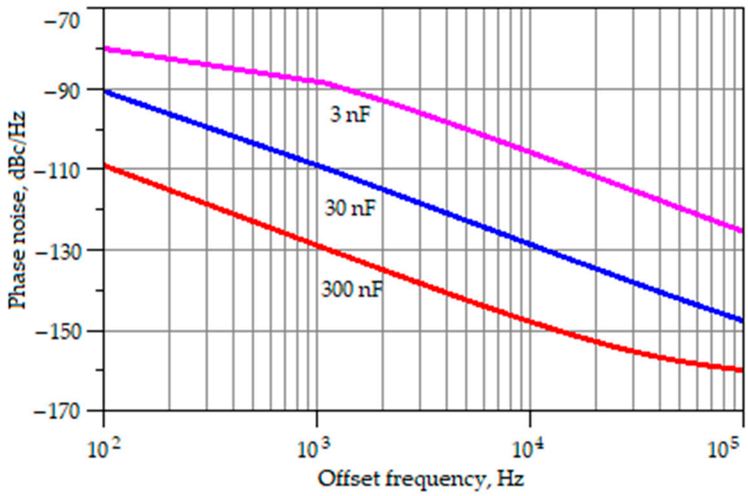

Figure 21. Phase noise versus offset frequency for the oscillator with multiple-output Wilson current mirror when $R_L = \infty$; $C_b = 300$ nF—red curve, $C_b = 30$ nF—blue curve, $C_b = 3$ nF—purple curve.

Let us now consider the case when a load R_L is connected through the capacitive divider to an oscillator output, as shown in Figure 22. Assume that $R_L = 50\ \Omega$ and $C_{CD1} = C_{CD2} = 0.5$ pF for the oscillators with MIWCM ($m = 0, 1, 2$) and MWCM ($m = 0$). For the oscillators with MCCM ($m = 0, 1, 2$) and MWCM ($m = 1, 2$), we selected $C_{CD1} = C_{CD2} = 0.25$ pF.

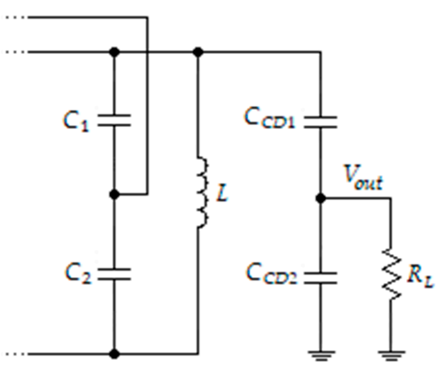

Figure 22. A capacitive divider with load resistance R_L at the oscillator output.

Using FOM (22), we compare oscillators shown in Figures 6–8 when R_L = 50 Ω. Table 9 shows the results of the oscillators' simulation. As shown in Table 9, the best FOM values correspond to the same m sequence (0, 2, 1) as when $R_L = \infty$ for oscillators with MCCM, MWCM, and MIWCM.

Table 9. Simulated characteristics of different NDR oscillators when R_L = 50 Ω.

Type of Oscillator	Capacitance, C_a (pF)	Oscillator Characteristics			
		Frequency of Operation, f (MHz)	Phase Noise at an Offset Frequency of 10^5 Hz, PN (dBc/Hz)	Power of Dissipation, P_{dis} (mW)	The Figure of Merit, FOM (dBc/Hz)
MCCM (m = 0)	28	1925	−116.1	18.8	−189.1
MCCM (m = 1)	15	1582	−103.9	25.2	−173.9
MCCM (m = 2)	25	1384	−90.0	31.0	−157.9
MWCM (m = 0)	15	1800	−143.1	19.6	−215.3
MWCM (m = 1)	3	1519	−149.8	27.0	−219.1
MWCM (m = 2)	7	1310	−154.6	33.9	−221.6
MIWCM (m = 0)	7	1800	−144.9	19.8	−217.0
MIWCM (m = 1)	5	1483	−150.8	27.4	−219.8
MIWCM (m = 2)	2	1294	−148.3	34.5	−215.2

Table 10 shows the performance comparison of oscillators with MCCM, MWCM, and MIWCM for $R_L = \infty$ and R_L = 50 Ω.

Table 10. Performance comparison of oscillators with different loads.

Oscillator Load, R_L (Ω)	The Figure of Merit (dBc/Hz)		
	Type of Oscillator		
	MCCM	MWCM	MIWCM
∞	−198.8	−227.1	−221.5
50	−189.1	−221.6	−219.8

As we can see in Table 10, the performance of each oscillator reduces when a 50 Ω load is connected to its output. The oscillator's performance with MICCM decreases to the greatest extent, and the oscillator's performance with MIWCM drops to the least. The absolute FOM value decreases by 4.9% and 0.8% in relative units, respectively, i.e., not critical.

7.4. Simulation of VCO Characteristics

Let us now simulate the characteristics for VCOs presented in Figures 9–11 by using the same transistors, resistor values of R_c and R_d, inductor type of L, and power supply voltage as in Section 7.3 when $R_L = \infty$. We select varactors SMV1104-33. The tuning voltage

V_d is varied from 2 to 12 V for each VCO. Capacitance C_b = 50 nF for VCOs with MCCM and C_b = 300 nF for VCOs with MWCM and MIWCM.

As in Section 7.3, we select the value of capacitance C_a from the condition of minimizing the phase noise of each VCO.

Figures 23 and 24 show the dependence of phase noise versus offset frequency for VCOs with MIWCM at V_d = 2 V and V_d = 12 V. The best value of phase noise of −137.9 dBc/Hz at an offset frequency of 100 kHz and V_d = 2 V has VCO with MIWCM when m = 2 (see Figure 23). The best value of phase noise of −152.5 dBc/Hz at an offset frequency of 100 kHz and V_d = 12 V also has VCO with MIWCM but when m = 1 (see Figure 24).

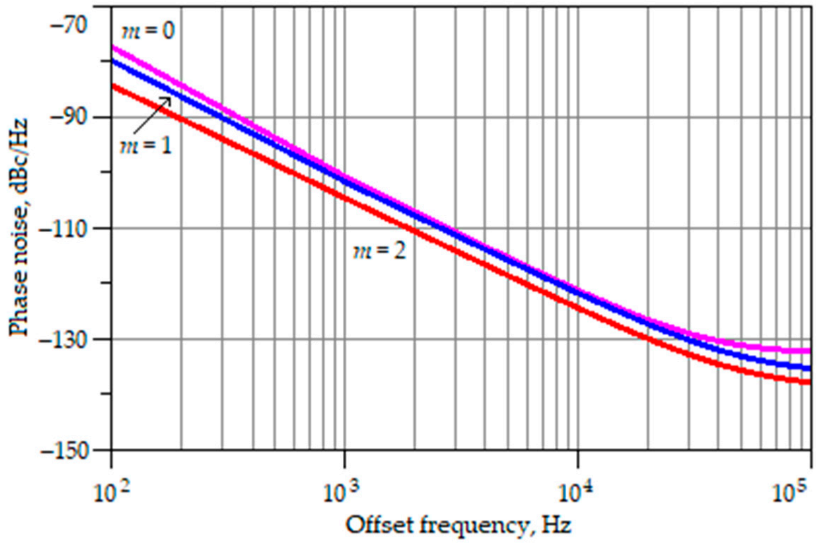

Figure 23. Phase noise versus offset frequency for VCO with multiple-output improved Wilson current mirror when V_d = 2 V, R_L = ∞; m = 0—purple curve (C_a = 10 pF), m = 1—blue curve (C_a = 7 pF), m = 2—red curve (C_a = 6 pF).

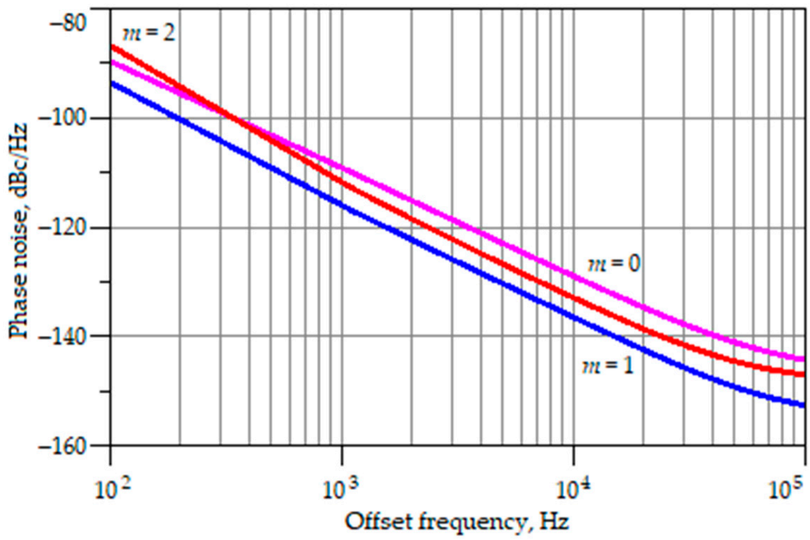

Figure 24. Phase noise versus offset frequency for VCO with multiple-output improved Wilson current mirror when V_d = 12 V, R_L = ∞; m = 0—purple curve (C_a = 10 pF), m = 1—blue curve (C_a = 7 pF), m = 2—red curve (C_a = 6 pF).

Interestingly, at V_d = 2 V, the phase noise improvement occurs in the sequence of m = 0, 1, 2, i.e., the more mirrored currents, the lower the phase noise (see Figure 23). However, at V_d = 12 V, the phase noise improvement occurs in m = 0, 2, 1, i.e., the highest phase noise occurs at m = 0, and the lowest at m = 1 (see Figure 24). The phase noise curve at m = 2 occupies an intermediate position.

Table 11 shows the simulated characteristics of different VCOs when $R_L = \infty$, where f_{min} and f_{max} are the minimum and maximum frequency of VCO operation. As shown in Table 11, the VCO with MCCM has the best performance when m = 0. The VCO with MWCM achieves the best performance when m = 2 and VCO with MIWCM—when m = 1. For each value of m in Table 11, VCO with MWCM and MIWCM have significantly lower (i.e., better) FOM than VCO with MCCM. The broadest tuning frequency range, Δf = 370 MHz, has VCO with MCCM when m = 0. The lowest power consumption, P_{dis} = 18.8 mW, also has VCO with MCCM when m = 0.

Table 11. Simulated characteristics of different NDR VCOs when $R_L = \infty$.

Type of VCO	Capacitance, C_a (pF)	VCO Characteristics				
		f_{min}, f_{max} V_d = 2 V, 12 V (MHz)	Δf (MHz)	*PN* ($f_{of} = 10^5$ Hz) V_d = 2 V, 12 V (dBc/Hz)	P_{dis} (mW)	*FOM* V_d = 2 V, 12 V (dBc/Hz)
MCCM (m = 0)	5	1616, 1986	370	−99.2, −139.1	18.8	−170.6, −212.3
MCCM (m = 1)	12	1408, 1631	223	−97.6, −100.4	25.2	−166.6, −170.6
MCCM (m = 2)	12	1262, 1410	148	−96.8, −90.4	31.0	−163.9, −158.5
MWCM (m = 0)	10	1571, 1912	341	−132.5, −143.2	19.6	−203.5, −215.9
MWCM (m = 1)	7	1366, 1556	190	−135.3, −151.2	27.0	−203.7, −220.7
MWCM (m = 2)	7	1222, 1339	117	−137.8, −148.1	33.9	−204.2, −215.3
MIWCM (m = 0)	10	1569, 1911	342	−132.4, −144.2	19.8	−203.3, −216.8
MIWCM (m = 1)	7	1364, 1554	190	−136.7, −152.5	27.4	−205.0, −222.0
MIWCM (m = 2)	6	1222, 1337	115	−137.9, −146.9	34.5	−204.3, −214.0

Figures 25 and 26 illustrate the dependence of phase noise versus capacitance C_b for VCO with multiple-output improved Wilson CM at V_d = 2 V and V_d = 12 V, respectively. We can see from Figures 25 and 26 that VCO phase noise significantly depends on the value of capacitor C_b. Indeed, when capacitance C_b varies from 3 to 300 nF, phase noise decreases from −95.3 to −137.9 dBc/Hz at V_d = 2 V and from −110.9 to −146.9 dBc/Hz at V_d = 12 V. We can explain such a decrease in phase noise by reducing noise spectral density at the drain of transistor T_0.

Table 12 shows the simulated characteristics of different VCOs when a 50 Ω load through a capacitive divider (see Figure 22) is connected to the output of VCOs shown in Figures 9–11.

We select $C_{CD1} = C_{CD2}$ = 0.5 pF for the VCOs with MWCM (m = 0, 1, 2), and MIWCM (m = 1, 2), and $C_{CD1} = C_{CD2}$ = 0.25 pF for the VCOs with MCCM (m = 0, 1, 2) and MIWCM (m = 0).

As shown in Table 12, the VCO with MCCM has the best performance when $m = 0$ and $C_a = 30$ pF. The VCO with MWCM achieves the best performance when $m = 1$ and $C_a = 20$ pF, and the VCO with MIWCM—when $m = 2$ and $C_a = 9$ pF.

As in the case of $R_L = \infty$ (see Table 11), for each value of m in Table 12, VCOs with MWCM and MIWCM have significantly lower FOM than VCO with MCCM.

Figures 27 and 28 show the dependence of phase noise versus offset frequency for VCOs with MIWCM at $V_d = 2$ V and $V_d = 12$ V when $R_L = 50\ \Omega$. The best value of phase noise of -139.0 dBc/Hz at an offset frequency of 100 kHz and $V_d = 2$ V has VCO when $m = 2$ (see Figure 27).

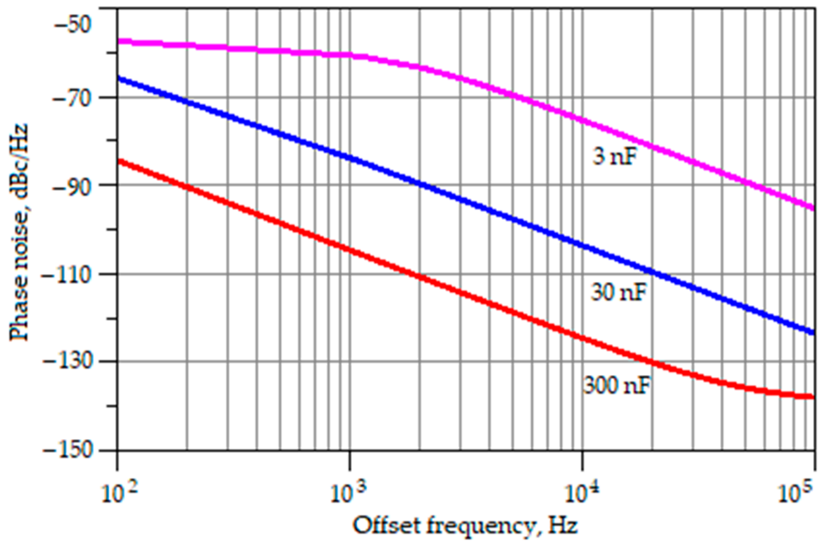

Figure 25. Phase noise versus offset frequency for the VCO with multiple-output improved Wilson current mirror when $V_d = 2$ V, $R_L = \infty$, and $C_a = 6$ pF; $C_b = 3$ nF—purple curve, $C_b = 30$ nF—blue curve, $C_b = 300$ nF—red curve.

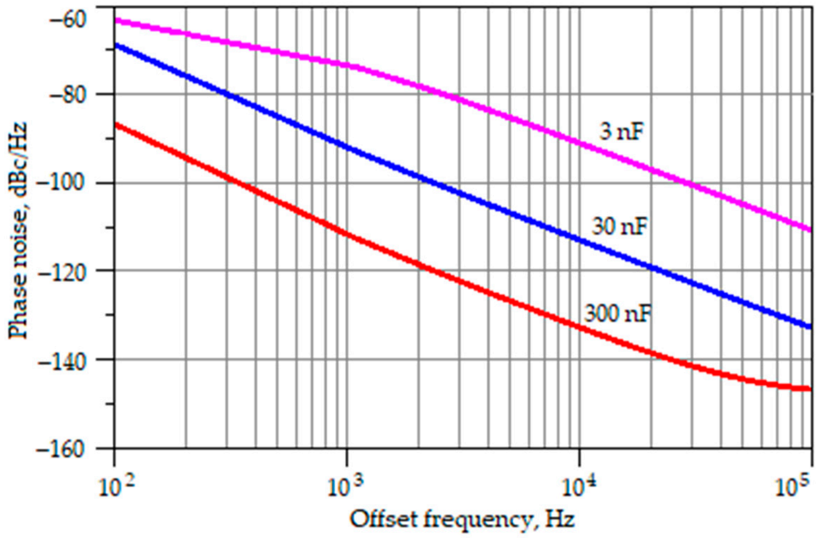

Figure 26. Phase noise versus offset frequency for the VCO with multiple-output improved Wilson current mirror when $V_d = 12$ V, $R_L = \infty$, and $C_a = 6$ pF; $C_b = 3$ nF—purple curve, $C_b = 30$ nF—blue curve, $C_b = 300$ nF—red curve.

Table 12. Simulated characteristics of different NDR VCOs when R_L = 50 Ω.

Type of Oscillator	Capacitance, C_a (pF)	VCO Characteristics				
		f_{min}, f_{max} V_d = 2 V, 12 V (MHz)	Δf (MHz)	PN (f_{of} = 10^5 Hz) V_d = 2 V, 12 V (dBc/Hz)	Power of Dissipation, P_{dis} (mW)	FOM V_d = 2 V, 12 V (dBc/Hz)
MCCM (m = 0)	30	1555, 1915	360	−99.0, −98.3	18.8	−170.1, −171.2
MCCM (m = 1)	15	1376, 1586	210	−97.3, −88.2	25.2	−166.1, −158.2
MCCM (m = 2)	30	1235, 1380	145	−97.8, −88.8	31.0	−164.7, −156.7
MWCM (m = 0)	12	1510, 1791	281	−111.7, −134.6	19.6	−182.4, −206.7
MWCM (m = 1)	20	1325, 1480	245	−134.7, −141.9	27.0	−202.8, −211.0
MWCM (m = 2)	18	1191, 1298	107	−144.0, −128.4	33.9	−210.2, −195.4
MIWCM (m = 0)	13	1532, 1841	309	−130.4, −138.4	19.8	−201.1, −210.7
MIWCM (m = 1)	12	1325, 1478	153	−135.6, −136.1	27.4	−203.7, −205.1
MIWCM (m = 2)	9	1191, 1295	104	−139.0, −137.0	34.5	−205.1, −203.9

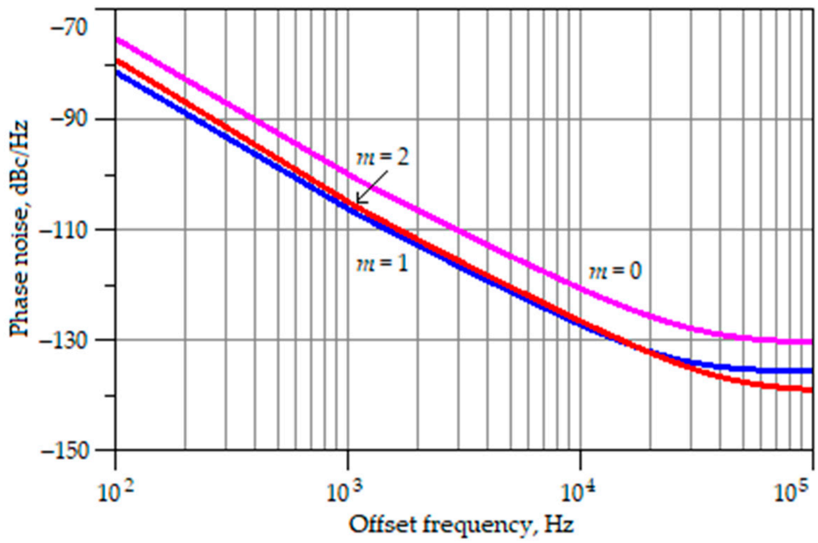

Figure 27. Phase noise versus offset frequency for VCO with multiple-output improved Wilson current mirror when V_d = 2 V, R_L = 50 Ω; m = 0—purple curve (C_a = 13 pF), m = 1—blue curve (C_a = 12 pF), m = 2—red curve (C_a = 9 pF).

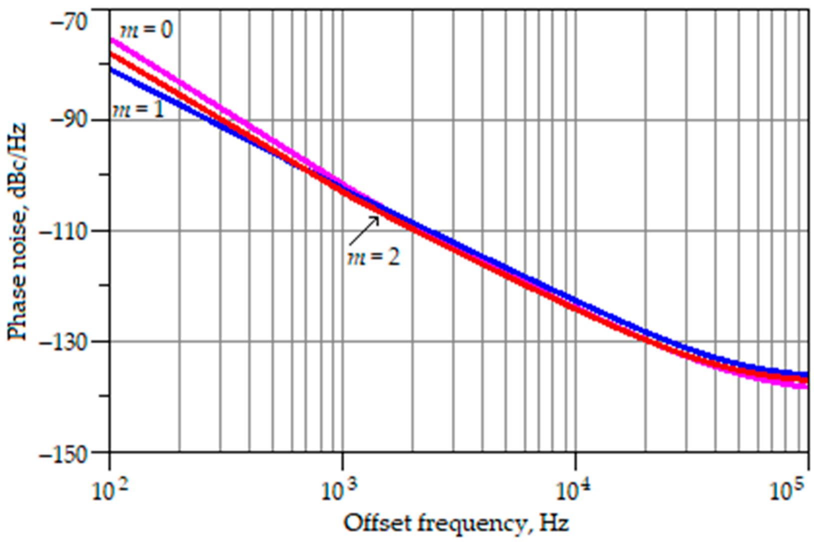

Figure 28. Phase noise versus offset frequency for VCO with multiple-output improved Wilson current mirror when V_d = 12 V, R_L = 50 Ω; m = 0—purple curve (C_a = 9 pF), m = 1—blue curve (C_a = 12 pF), m = 2—red curve (C_a = 13 pF).

The best value of phase noise of −138.4 dBc/Hz at an offset frequency of 100 kHz and V_d = 12 V corresponds to m = 0 (see Figure 28).

Table 13 compares the performance of VCOs with MCCM, MWCM, and MIWCM for R_L = ∞ and R_L = 50 Ω.

Table 13. Performance comparison of VCOs with different loads.

Oscillator Load, R_L (Ω)	The Figure of Merit (dBc/Hz)		
	Type of Oscillator		
	MCCM	MWCM	MIWCM
∞	−170.6, −212.3	−204.2, −215.3	−205.0, −222.0
50	−170.1, −171.2	−202.8, −211.0	−205.1, −203.9

As shown in Table 13, the highest (i.e., the worst) in-band value of the FOM insignificantly increases when connecting a 50 Ω load to the VCO output. Indeed, the absolute FOM value decreases by 0.5 dBc/Hz for VCO with MICCM, by 1.6 dBc/Hz for VCO with MWCM, and by 1.1 dBc/Hz for VCO with MIWCM. However, the lowest (i.e., the best) in-band FOM value changes more substantially, namely by 41.1 dBc/Hz for VCO with MCCM, by 4.3 dBc/Hz for VCO with MWCM, and by 16.9 dBc/Hz for VCO with MIWCM. Since, when comparing the VCOs, the worst in-band FOM value is considered, we can conclude that this value changes insignificantly (maximum 0.7 %) when connecting a 50 Ω load to the VCO output.

Tables 12 and 13 show that the best VCO when R_L = 50 is the VCO with MIWCM (m = 2).

Table 14 compares the performance characteristics of the recently published and developed in this article VCOs and oscillators. We can draw the following conclusions from Table 14. The oscillator with MWCM (m = 2, R_L = 50 Ω) designed in this study has the lowest phase noise (−154.6 dBc/Hz at 0.1 MHz offset) and the best FOM (−221.6 dBc/Hz) among all oscillators. The latter is an indisputable advantage of the developed oscillator since CMOS oscillators have a much lower power consumption and usually have a significant advantage over GaN and GaAs oscillators in terms of the FOM value.

Table 14. Comparison of designed and some recently published microwave oscillators.

Oscillator (VCO)	Technology	Oscillation Frequency (GHz)	Offset Frequency (MHz)	Phase Noise (dBc/Hz)	Dissipation Power (mW)	Figure of Merit (dBc/Hz)
[55]	GaN HEMT	7.9	1	−135	1456	−181.3
[56]	GaN HEMT	6.45 ÷ 7.55	1	−132	198	−185.9
[57]	GaN HEMT	5.2	1	−125.7	16	−188
[58]	GaAs PHEMT	37.608	1	−112.31	130	−182.7
[59]	GaN HEMT	1.93	1	−149	400	−189
[60]	GaN HEMT	7.26	1	−122.48	18.33	−187
[61]	GaN HEMT	8.8	1	−124.55	21.6	−190.1
[62]	SiGe	8.99	0.1	−120.05	18	−206.58
[63]	GaN HEMT	4.95	1	−143	320	−191.84
[64]	InGaP HBT	5.05 ÷ 6.35	0.1	−103, −95	350	−171.6, −165.6
[65]	CMOS	1.36 ÷ 1.86	0.1	−121	2.7	−202
[66]	CMOS	8	1	−134.3	6.6	−204
[67]	CMOS	7.4 ÷ 8.4	10	−151.5	29	−194.3, −195.6
[68]	CMOS	2.28 ÷ 2.59	0.1	−103.6, −125.5	1.9	−188, −211
[69]	CMOS	14 ÷ 18	1	−113, −110	24	−−182.1, −181.3
[70]	BiCMOS	15	1	−124	70	−189
[71]	BiCMOS	29.6 ÷ 36.5	1	−97	20	−180
This work	GaAs PHEMT, BJT	1.31	0.1	−154.6	33.9	−221.6
This work	GaAs PHEMT, BJT	1.367 ÷ 1.556	0.1	−139.0, −137.0	34.5	−205.1, −203.9

The designed VCO with MIWCM (m = 2, R_L = 50 Ω) also has very low phase noise (−139.0, −137.0 dBc/Hz at 0.1 MHz offset) and is one of the best FOM (−205.1, −203.9 dBc/Hz at 0.1 MHz offset) in the tuning range. Thus, we can successfully use the proposed two-terminal circuits with NDR for constructing highly efficient microwave oscillators and VCOs.

8. Experimental Results

We tested the oscillator circuit with MIWCM (see Figure 8) on a breadboard and printed circuit board (PCB) assembly. Table 15 shows part numbers and nominal values of the breadboard oscillator elements.

Table 15. Circuit elements used in the oscillator with MIWCM assembled on a solderless breadboard.

Circuit Elements	Part Numbers and Nominal Values
Transistor T_0	BF245B
Transistors $\overline{T_1, T_M}$	2N3906
Inductor L	1 µH
Capacitor C_a	200 pF
Capacitor C_b	10 nF
Capacitors C_1, C_2	60 pF
Resistor R_c	1 kΩ
Resistor R_d	4 kΩ

In the oscillator circuit with MIWCM of Figure 8, the value of m is equal to 1. At the operating point, $V_{1,2}$ = 6 V and I_1 = 2.7 mA. Figure 29 shows the measured oscillator output spectrum at the fundamental frequency of 18.7 MHz with an output power of −14.8 dBm. We used a spectrum analyzer USB-SA44B (Battle Ground, WA, USA) and an Auburn P-20A RF probe (Auburn, WA, USA) with a 10:1 voltage ratio.

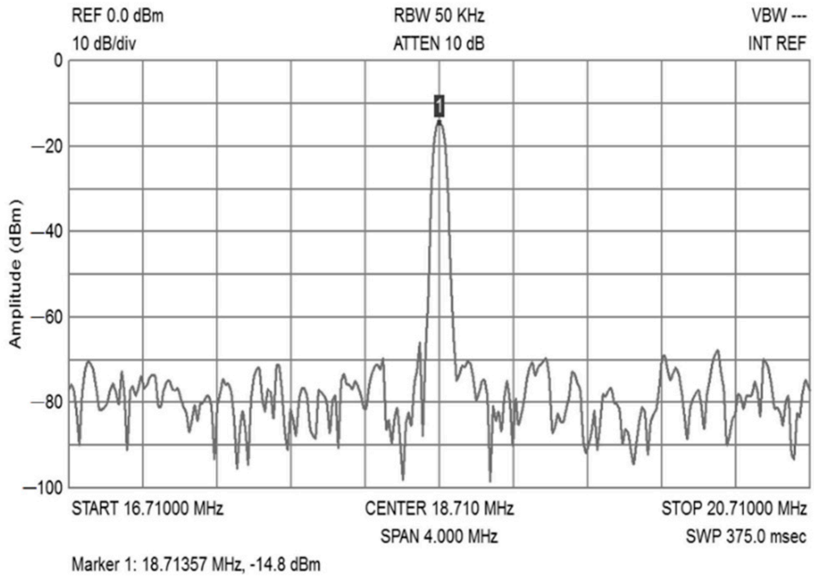

Figure 29. The output spectrum of the prototype oscillator with multiple-output improved Wilson current mirror (m = 1).

Figure 30 shows the PCB assembly of the oscillator with MIWCM (m =0). Table 16 indicates part numbers and nominal values of components assembled on PCB. We also used the USB-SA44B spectrum analyzer with Auburn P-20A RF probe to measure the oscillator output spectrum (see Figure 31) at $V_{1,2}$ = 9 V and RBW = 100 kHz. As shown in Figure 31, the oscillation frequency is 944.4 MHz, and the power level of the output signal is −40.2 dBm. In estimating the actual power level, we should consider that the attenuation provided by the P-20A RF probe is 20 dB, and an insertion loss of the buffer amplifier is 2.2 dB.

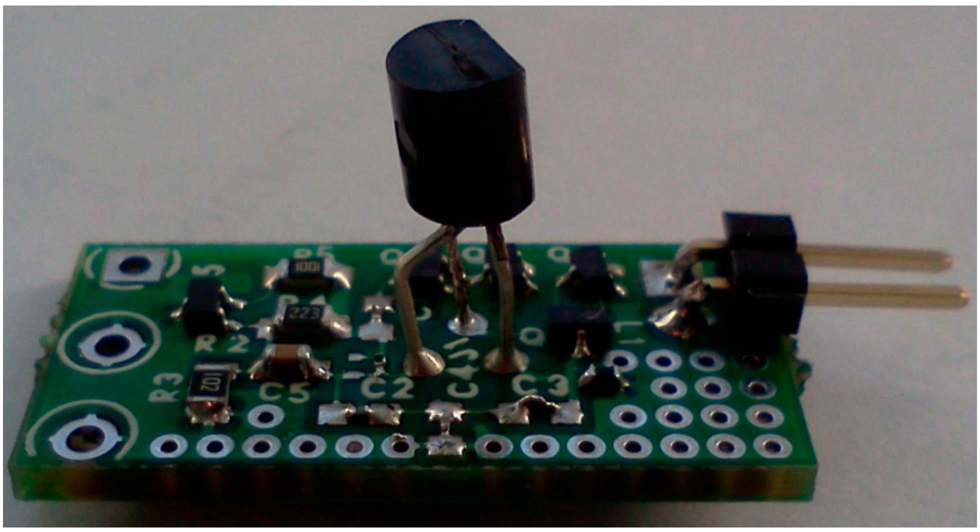

Figure 30. Printed circuit board assembly of the oscillator with multiple-output improved Wilson current mirror (m = 0).

Table 16. Circuit elements used in the oscillator with MIWCM assembled on a printed circuit board.

Circuit Elements	Part Numbers and Nominal Values
Transistor T_0	BF245B
Transistors $\overline{T_1, T_M}$	BFT92W
Inductor L	ELJQF8N2 (8.2 nH)
Capacitor C_a	C0603C0G1E100D (10 pF)
Capacitor C_b	C0603Y5V1C103Z (10 nF)
Capacitors C_1, C_2	C0603C0G1E0R5C (0.5 pF)
Resistor R_c	ERJ1GEJ102 (1 kΩ)
Resistor R_d	ERJ1GEJ392 (3.9 kΩ)

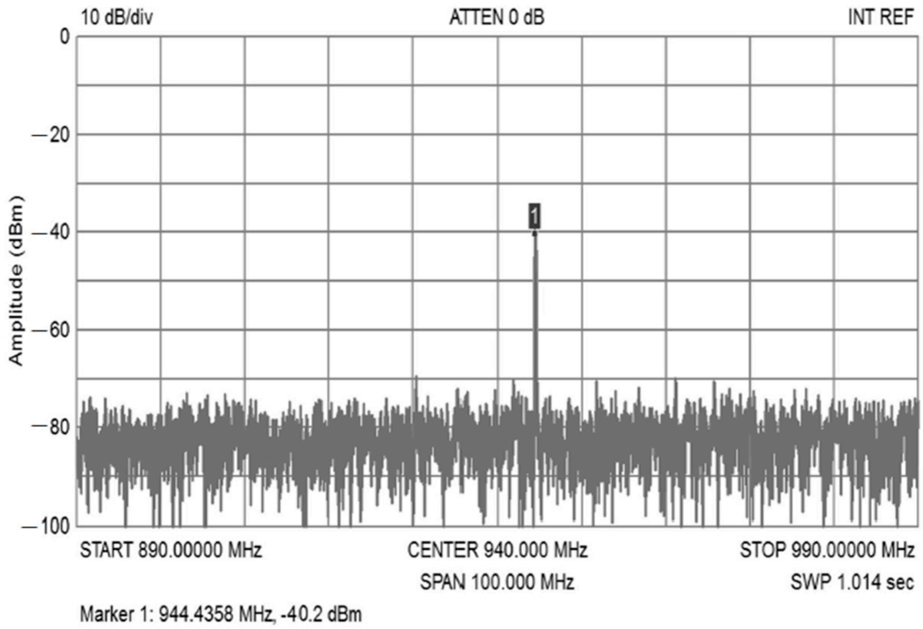

Figure 31. The output spectrum of the oscillator with multiple-output improved Wilson current mirror (m = 0).

9. Conclusions

In this article, we have demonstrated new two-terminal NDR circuits based on a combination of a field-effect transistor and multiple-output cascode, Wilson, and improved Wilson BJT current mirrors. The proposed circuits allow controlling the slope of the current-voltage characteristics in the NDR region by changing the number of mirrored currents, thus setting the peak-to-valley current ratio to any desired value. We have conducted modeling total current in the NDR region when the FET is a JFET and MESFET, HEMT, or PHEMT; the obtained current equations calculate the negative resistance at the operating point. We considered possible applications of the proposed two-terminal NDR circuits as oscillators and VCOs. We found that the NDR circuit with multiple-output improved Wilson current mirror has the smallest absolute value of negative resistance, which means that the NDR oscillator based on this circuit has the best conditions for self-excitation. We analyzed the effect of loading on the performance characteristics of the oscillators and VCOs. We found that a 50-ohm load reduces, in comparison to infinite load, the performance of the oscillators and VCOs by a maximum of 4.9% and 0.7 %, respectively. By simulation, we show that the microwave oscillator based on multiple-output improved Wilson current mirror has the lowest phase noise (−154.6 dBc/Hz at offset 100 kHz) and the best figure of merit (−221.6 dBc/Hz) compared to other considered oscillators. We also show that the VCO with multiple-output improved Wilson current mirror has the best FOM in the tuning range (−205.1, −203.9 dBc/Hz). Comparison of the developed oscillators and those previously published showed that the oscillators based on the proposed two-terminal NDR circuits are superior to the well-known GaN and GaAs HEMT oscillators by 10–20 dB with respect to the commonly used figure of merit. It is also interesting to note that the proposed oscillator circuits are higher in effectiveness than even CMOS oscillators, despite the much lower power consumption of the latter. This advantage is due to the low level of phase noise in the designed oscillators.

Our future work will focus on developing and studying two-terminal NDR circuits, in which the multiple-output current mirrors consist of MOS transistors.

Author Contributions: Conceptualization, V.U.; methodology, V.U. and A.R.; software, D.M.; validation, V.U., A.R. and D.M.; formal analysis, V.U.; investigation, V.U., A.R. and D.M.; data curation, V.U. and D.M.; writing—original draft preparation, V.U. and A.R.; writing—review and editing, V.U.; visualization, V.U. and D.M.; supervision, V.U.; project administration, A.R. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors express thanks to engineer E. Meshcheryakov for technical support.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations exist in the manuscript:

BJT	Bipolar junction transistor
CM	Current mirror
CMOS	Complementary metal-oxide-semiconductor
FET	Field-effect transistor
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility transistor
JFET	Junction field-effect transistor
MCCM	Multiple-output cascode current mirror
MESFET	Metal-semiconductor field-effect transistor
MIWCM	Multiple-output improved Wilson current mirror
MOSFET	Metal-oxide-semiconductor field-effect transistor
MWCM	Multiple-output Wilson current mirror
NDR	Negative differential resistance
NI	Negative impedance
nMOS	n-channel metal-oxide semiconductor
PCB	Printed circuit board
PHEMT	Pseudomorphic high-electron-mobility transistor
pMOS	p-channel metal-oxide semiconductor
PVCR	Peak-to-valley current ratio
RBW	Resolution bandwidth
RF	Radio frequency
SiGe	Silicon-Germanium
SRAM	Static random-access memory
TFET	Tunnel field-effect transistor
VCO	Voltage-controlled oscillator

Nomenclature

α	Coefficient of the hyperbolic tangent function
b	Transconductance
f_{of}	Offset frequency
FOM	Figure of merit
h_{FE}	Bipolar transistor dc current gain
I_1	Total dc current of the NDR circuit
I_2	Mirrored current
I_D	Current in the master branch of CM
I_{DSS}	Zero-gate-voltage drain current of JFET
I_X	Total dc current of the NDR circuit at point X
I_Y	Total dc current of the NDR circuit at point Y
I_Z	Total dc current of the NDR circuit at point Z
λ	Channel length modulation coefficient
m	Number of additional current sources (mirrored currents)
M	Number of BJTs in multiple-output current mirror
P_{dis}	Oscillator dissipation power
PN	Oscillator phase noise
Q_l	Loaded quality factor of the tank circuit
ρ	Characteristic impedance of the tank circuit
R_{diff}	Differential resistance
R^C_{diff}	Differential resistance of the NDR circuit with multiple-output cascode current mirror
R^{IW}_{diff}	Differential resistance of the NDR circuit with multiple-output improved Wilson current mirror
R^W_{diff}	Differential resistance of the NDR circuit with multiple-output Wilson current mirror
R_c, R_d	Resistive voltage divider
R_Q	Loaded tank circuit resistance at resonance
T_0	Field-effect transistor in NDR circuits
$\overline{T_1, T_M}$	Bipolar junction transistors in multiple-output current mirror
$V_{1,2}$	Voltage between terminals 1 and 2 in NDR circuits
V_A	Early voltage of a BJT in the current mirror
V_{CE1}, V_{CE2}	Collector-emitter voltages of transistors T_1 and T_2 in the multiple-output Wilson current mirror
V_D	Drain voltage of transistor T_0
V_{DS}	Drain-source voltage of transistor T_0
V_{EB}	Emitter-base voltage
V_{EB3}	Emitter-base voltage of transistor T_3 in the multiple-output Wilson current mirror
V_{GS}	Gate-source voltage of transistor T_0
V_P	Pinch-off voltage of JFET T_0
V_{TH}	Threshold voltage of transistor T_0 (MESFET, HEMT, or PHEMT)
V_X	Voltage between terminals 1 and 2 at point X
V_Y	Voltage between terminals 1 and 2 at point Y
V_Z	Voltage between terminals 1 and 2 at point Z
ΔI_Y %	Relative accuracy of calculating current I_Y
ΔI_D %	Relative accuracy of calculating current I_D

References

1. Gumber, K.; Dejous, C.; Hemour, S. Harmonic reflection amplifier for widespread backscatter Internet-of-Things. *IEEE Trans. Microw. Theory Tech.* **2021**, *69*, 774–785. [CrossRef]
2. Islam, M.T.; Kogut, A.; Yahya, I.; Dolia, R. On the Possibility of Use of Planar Dielectric Resonators for Solving the Problems of Frequency Stabilization of Millimeter Waves Oscillators. In Proceedings of the 2019 IEEE Asia-Pacific Conference on Applied Electromagnetics, Melacca, Malaysia, 25–27 November 2019. [CrossRef]
3. Semenov, A.; Osadchuk, O.; Semenova, O.; Koval, K.; Baraban, S.; Savytskyi, A. A Deterministic Chaos Ring Oscillator Based on a MOS Transistor Structure with Negative Differential Resistance. In Proceedings of the 2019 IEEE International Scientific-Practical Conference Problems of Infocommunications, Science and Technology, Kyiv, Ukraine, 8–11 October 2019. [CrossRef]
4. Choi, S.; Jeong, Y.; Lee, J.; Yang, K. A novel high-speed multiplexing IC based on resonant tunneling diodes. *IEEE Trans. Nanotechnol.* **2009**, *8*, 482–486. [CrossRef]

5. Chen, S.L.; Griffin, P.B.; Plummer, J.D. Negative differential resistance circuit design and memory applications. *IEEE Trans. Electron Devices* **2009**, *56*, 634–640. [CrossRef]
6. Kastalsky, A.; Luryi, S.; Gossard, A.C.; Chan, W.K. Switching in NERFET circuits. *IEEE Electron Device Lett.* **1985**, *6*, 347–349. [CrossRef]
7. Semenov, A.; Semenova, O.; Rudyk, A.; Voznyak, O.; Pinaiev, B.; Kulias, R. Mathematical Model of Microwave Devices on Resonant Tunneling Diodes for Practical Application in Radar and Electronic Systems. In Proceedings of the 2020 IEEE Ukrainian Microwave Week, Kyiv, Ukraine, 21–25 September 2020. [CrossRef]
8. Gumber, K.; Amato, F.; Dejous, C.; Hemour, S. Nonlinear Negative Resistance-based Harmonic Backscatter. In Proceedings of the 2020 IEEE/MTT-S International Microwave Symposium, Los Angeles, CA, USA, 4–6 August 2020. [CrossRef]
9. Semenov, A.; Semenova, O.; Osadchuk, O.; Osadchuk, I.; Baraban, S.; Rudyk, A.; Safonyk, A.; Voznyak, O. Van der Pol Oscillators Based on Transistor Structures with Negative Differential Resistance for Infocommunication System Facilities. In *Data-Centric Business and Applications. Lecture Notes on Data Engineering and Communications Technologies*; Ageyev, D., Radivilova, T., Kryvinska, N., Eds.; Springer: Cham, Switzerland, 2021; Volume 69, pp. 43–78. [CrossRef]
10. Broekaert, T.P.; Brar, B.; van der Wagt, J.P.; Seabaugh, A.C.; Morris, F.J.; Moise, T.S.; Beam, E.A.; Frazier, G.A. A monolithic 4-bit 2-Gsps resonant tunneling analog-to-digital converter. *IEEE J. Solid State Circuits* **1998**, *33*, 1342–1349. [CrossRef]
11. Boriskov, P.P.; Velichko, A.A. Inductively coupled burst oscillators in neural network information processing systems. *J. Phys. Conf. Ser.* **2019**, *1399*, 033051. [CrossRef]
12. Berger, P.R.; Ramesh, A. Negative differential resistance devices and circuits. In *Comprehensive Semiconductor Science and Technology*; Bhattacharya, P., Fornari, R., Kamimura, H., Eds.; Elsevier: Amsterdam, The Netherlands, 2011; Volume 5, pp. 176–241.
13. Esaki, L. New phenomenon in narrow germanium p−n junctions. *Phys. Rev.* **1958**, *109*, 603–604. [CrossRef]
14. Esaki, L. Discovery of the tunnel diode. *IEEE Trans. Electron Devices* **1976**, *23*, 644–647. [CrossRef]
15. Gunn, J.B. Microwave oscillations of current in III–V semiconductors. *Solid State Commun.* **1963**, *1*, 88–91. [CrossRef]
16. Stanley, I.W.; Ager, D.J. Two-terminal negative dynamic resistance. *Electron. Lett.* **1970**, *6*, 1–2. [CrossRef]
17. Sharma, C.K.; Dutta Roy, S.C. A versatile design giving both N-type and S-type of negative-resistances. *Microelectron. Reliab.* **1972**, *11*, 499–504. [CrossRef]
18. Wu, C.Y.; Wu, C.Y. The new general realization theory of FET-like integrated voltage-controlled negative differential resistance devices. *IEEE Trans. Circuits Syst.* **1981**, *28*, 382–390.
19. Chua, L.; Yu, J.; Yu, Y. Bipolar-JFET-MOSFET negative resistance devices. *IEEE Trans. Circuits Syst.* **1985**, *32*, 46–61. [CrossRef]
20. Trajković, L.; Willson, A. Negative Differential Resistance in Two-transistor One-ports with no Internal Sources. In Proceedings of the IEEE International Symposium on Circuits and Systems, Espooo, Finland, 7–9 June 1988. [CrossRef]
21. Jung, K.S.; Heo, K.; Kim, M.J.; Andreev, M.; Seo, S.; Kim, J.O.; Lim, J.H.; Kim, K.H.; Kim, S.; Kim, K.S.; et al. Double negative differential resistance device based on Hafnium Disulfide/Pentacene hybrid structure. *Adv. Sci.* **2020**, *7*, 2000991. [CrossRef]
22. Kobashi, K.; Hayakawa, R.; Chikyow, T.; Wakayama, Y. Negative differential resistance transistor with organic p-n heterojunction. *Adv. Electron. Mater.* **2017**, *3*, 1700106. [CrossRef]
23. Lv, Q.; Yan, F.; Mori, N.; Zhu, W.; Hu, C.; Kudrynskyi, Z.R.; Kovalyuk, Z.D.; Patanè, A.; Wang, K. Interlayer band-to-band tunneling and negative differential resistance in van der Waals BP/InSe field-effect transistors. *Adv. Funct. Mater.* **2020**, *30*, 1910713. [CrossRef]
24. Qiu, W.; Nguyen, P.D.; Skafidasa, E. Graphene nanopores as negative differential resistance devices. *J. Appl. Phys.* **2015**, *117*, 054306. [CrossRef]
25. Kheirabadi, S.J.; Ghayour, R.; Sanaeeb, M. Negative differential resistance effect in different structures of armchair graphene nanoribbon. *Diam. Relat. Mater.* **2020**, *108*, 107970. [CrossRef]
26. Yang, C.F.; Hwu, J.G. Tunable negative differential resistance in MISIM tunnel diodes structure with concentric circular electrodes controlled by designed substrate bias. *IEEE Trans. Electron Devices* **2017**, *64*, 5230–5235. [CrossRef]
27. Xiong, X.; Huang, M.; Hu, B.; Li, X.; Liu, F.; Li, S.; Tian, M.; Li, T.; Song, J.; Wu, Y. A transverse tunneling field-effect transistor made from a van der Waals heterostructure. *Nat. Electron.* **2020**, *3*, 106–112. [CrossRef]
28. Kim, K.H.; Park, H.Y.; Shim, J.; Shin, G.; Andreev, M.; Koo, J.; Yoo, G.; Jung, K.; Heo, K.; Lee, Y.; et al. A multiple negative differential resistance heterojunction device and its circuit application to ternary static random access memory. *Nanoscale Horiz.* **2020**, *5*, 654–662. [CrossRef]
29. Liang, D.S.; Gan, K.J.; Hsiao, C.C.; Tsai, C.S.; Chen, Y.H.; Wane, S.Y.; Kuo, S.H.; Chiang, F.C.; Su, L.X. Novel voltage-controlled oscillator design by MOS-NDR devices and circuits. In Proceedings of the IEEE Fifth International Workshop on System-on-Chip for Real-Time Applications, Banff, AB, Canada, 20–24 July 2005. [CrossRef]
30. Gan, K.J.; Lub, J.J.; Yeh, W.K. Multiple-valued logic design based on the multiple-peak BiCMOS-NDR circuits. *Eng. Sci. Technol. Int. J.* **2016**, *19*, 888–893. [CrossRef]
31. Chung, S.Y.; Jin, N.; Berger, P.R.; Yu, R.; Thompson, P.E.; Lake, R.; Rommel, S.L.; Kurinec, S.K. Three-terminal Si-based negative differential resistance circuit element with adjustable peak-to-valley current ratios using a monolithic vertical integration. *Appl. Phys. Lett.* **2004**, *84*, 2688–2690. [CrossRef]
32. Semenov, A. Mathematical model of the microelectronic oscillator based on the BJT-MOSFET structure with negative differential resistance. In Proceedings of the 2017 IEEE 37th International Conference on Electronics and Nanotechnology (ELNANO), Kyiv, Ukraine, 18–20 April 2017. [CrossRef]

33. Gan, K.J.; Tsai, C.S.; Sun, W.L. Fabrication and application of MOS-HBT-NDR circuit using standard SiGe process. *Electron. Lett.* **2007**, *43*, 516–517. [CrossRef]
34. Ulansky, V.V.; Ben Suleiman, S.F.; Elsherif, H.M.; Abusaid, M.F. Optimization of NDR VCOs for microwave applications. In Proceedings of the 2016 IEEE 36th International Conference on Electronics and Nanotechnology (ELNANO), Kyiv, Ukraine, 19–21 April 2016. [CrossRef]
35. Ulansky, V.; Raza, A.; Oun, H. Electronic circuit with controllable negative differential resistance and its applications. *Electronics* **2019**, *8*, 409. [CrossRef]
36. Yang, C.C. Influence of parasitic effects in negative differential resistance characteristics of resonant tunneling. *Electronics* **2019**, *8*, 673. [CrossRef]
37. Kadioglu, Y. Ballistic transport and optical properties of a new half-metallic monolayer: Vanadium phosphide. *Mater. Sci. Eng. B* **2021**, *268*, 115111. [CrossRef]
38. Rathi, S.; Lee, I.; Kang, M.; Lim, D.; Lee, Y.; Yamacli, S.; Joh, H.I.; Kim, S.; Kim, S.W.; Yun, S.J.; et al. Observation of negative differential resistance in mesoscopic graphene oxide devices. *Sci. Rep.* **2018**, *8*, 7144. [CrossRef]
39. Sharma, S.; Cheng, C.A.; Santiago, S.R.; Feria, D.N.; Yuan, C.T.; Chang, S.H.; Lin, T.Y.; Shen, J.L. Aggregation-induced negative differential resistance in graphene oxide quantum dots. *Phys. Chem. Chem. Phys.* **2021**, *23*, 16909–16914. [CrossRef]
40. Shim, J.; Oh, S.; Kang, D.H.; Jo, S.H.; Ali, M.H.; Choi, W.Y.; Heo, K.; Jeon, J.; Lee, S.; Kim, M.; et al. Phosphorene/rhenium disulfide heterojunction-based negative differential resistance device for multi-valued logic. *Nat. Commun.* **2016**, *7*, 13413. [CrossRef]
41. Gray, P.R.; Hurst, P.J.; Lewis, S.H.; Meyer, R.G. *Analysis and Design of Analog Integrated Circuits*, 5th ed.; Wiley: New York, NY, USA, 2009; pp. 253–277.
42. Curtice, W.R. A MESFET model for use in the design of GaAs integrated circuits. *IEEE Trans. Microw. Theory Tech.* **1980**, *28*, 448–456. [CrossRef]
43. Statz, H.; Newman, P.; Smith, I.W.; Pucel, R.A.; Haus, H.A. GaAs FET device and circuit simulation in Spice. *IEEE Trans. Electron Devices* **1987**, *34*, 160–169. [CrossRef]
44. McCamant, A.J.; McCormack, G.D.; Smith, D.H. An improved MESFET model for Spice. *IEEE Trans. Microw. Theory Tech.* **1990**, *38*, 822–824. [CrossRef]
45. Suarez, A.; Fernandez, T. RF devices: Characteristics and modelling. In *Microwave Devices, Circuits and Subsystems for Communications Engineering*; Glover, I.A., Pennock, S.R., Shepherd, P.R., Eds.; John Wiley & Sons Ltd.: Chichester, UK, 2005; p. 79.
46. Sato, T.; Okada, K.; Matsuzawa, A. A new figure of merit of LC oscillators considering frequency tuning range. In Proceedings of the 2011 9th IEEE International Conference on ASIC, Xiamen, China, 25–28 October 2011. [CrossRef]
47. Van der Tang, J.; Kasperkovitz, D. Oscillator design efficiency: A new figure of merit for oscillator benchmarking. In Proceedings of the 2000 IEEE International Symposium on Circuits and Systems (ISCAS), Geneva, Switzerland, 28–31 May 2000. [CrossRef]
48. Hegazi, E.; Sjoland, H.; Abidi, A. A filtering technique to lower LC oscillator phase noise. *IEEE J. Solid State Circuits* **2001**, *36*, 1921–1930. [CrossRef]
49. Ulanski, V.V.; Elsherif, H.M.; Machalin, I.A. Analysis and design of voltage-controlled negative resistance oscillators based on simple current mirrors. *Electron. Control. Syst.* **2005**, *3*, 134–140.
50. Boylestad, R.L. *Introductory Circuit Analysis*, 10th ed.; Pearson Education: London, UK, 2002; pp. 901–918.
51. Ulansky, V.V.; Fituri, M.S.; Machalin, I.A. Mathematical modeling of voltage-controlled oscillators with the Colpitts and Clapp topology. *Electron. Control. Syst.* **2009**, *1*, 82–90. [CrossRef]
52. Nguyen, D.A.; Seo, C. A novel varactorless tuning technique for Clapp VCO design using tunable negative capacitor to increase frequency-tuning range. *IEEE Access* **2021**, *9*, 99562–99570. [CrossRef]
53. Ulansky, V.V.; Ben Suleiman, S.F. Negative differential resistance based voltage-controlled oscillator for VHF band. In Proceedings of the 2013 IEEE XXXIII International Scientific Conference Electronics and Nanotechnology (ELNANO), Kyiv, Ukraine, 16–19 April 2013. [CrossRef]
54. Semiconductor Products. ATF-34 Series PHEMT Model. Available online: http://www.hp.woodshot.com/hprfhelp/design/SPICE/fets.htm#ATF34 (accessed on 1 October 1999).
55. Liu, H.; Zhu, X.; Boon, C.C. Design of ultra-low phase noise and high power integrated oscillator in 0.25 µm GaN-on-SiC HEMT technology. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 120–122. [CrossRef]
56. Thi Do, T.N.; Szhau Lai, S.; Horberg, M. A MMIC GaN HEMT voltage-controlled-oscillator with high tuning linearity and low phase noise. In Proceedings of the IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), New Orleans, LA, USA, 11–14 October 2015; pp. 1–4. [CrossRef]
57. Lai, W.-C.; Jang, S.-L.; Chen, Y.-W. Dual-feedback GaN HEMT oscillator. In Proceedings of the 2019 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Nanjing, China, 28–30 August 2019. [CrossRef]
58. Chang, C.-L.; Tseng, C.-H.; Chang, H.-Y. A new monolithic Ka-band filter-based voltage-controlled oscillator using 0.15 µm GaAs pHEMT technology. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 111–113. [CrossRef]
59. Lai, S.; Kuylenstierna, D.; Özen, M.; Hörberg, M.; Rorsman, N.; Angelov, I.; Zirath, H. Low phase noise GaN HEMT oscillators with excellent figures of merit. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 412–414. [CrossRef]
60. Jang, S.-L.; Chang, Y.-H.; Lai, W.-C. A feedback GaN HEMT oscillator. In Proceedings of the 2018 IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT), Chengdu, China, 7–11 May 2018. [CrossRef]

61. Lai, W.; Jang, S. An X-band GaN HEMT oscillator with four-path inductors. *Appl. Comput. Electromagn. Soc. J.* **2020**, *35*, 1059–1063. [CrossRef]
62. Xu, J.; Yang, X.; Chen, Y.; Cao, Y.; Xiao, F. Low phase noise microwave oscillator with greater than 60 dB second-harmonic suppression. *IET Microw. Antennas Propag.* **2021**, *15*, 675–682. [CrossRef]
63. Liu, H.; Zhu, X.; Boon, C.C.; Yi, X. Design of an oscillator with low phase noise and medium output power in a 0.25 μm GaN-on-SiC high electron-mobility transistors technology. *IET Microw. Antennas Propag.* **2015**, *9*, 795–801. [CrossRef]
64. Lai, S. Oscillator Design in III-V Technologies. Ph.D. Thesis, Chalmers University of Technology, Gothenburg, Sweden, 2014.
65. Cai, H.L.; Yang, Y.; Qi, N.; Chen, X.; Tian, H.; Song, Z.; Xu, Y.; Zhou, C.J.; Zhan, J.; Wang, A.; et al. A 2.7-mW 1.36–1.86-GHz LC-VCO with a FOM of 202 dBc/Hz enabled by a 26%-size-reduced nano-particle-magnetic-enhanced inductor. *IEEE Trans. Microw. Theory Tech.* **2014**, *62*, 1221–1228. [CrossRef]
66. Zailer, E.; Belostotski, L.; Plume, R. 8-GHz, 6.6-mW LC-VCO with small die area and FOM of 204 dBc/Hz at 1-MHz offset. *IEEE Microw. Wirel. Compon. Lett.* **2016**, *26*, 936–938. [CrossRef]
67. Garampazzi, M.; Mendes, P.M.; Codega, N. Analysis and design of a 195.6 dBc/Hz peak FoM P-N class-B oscillator with transformer-based tail filtering. *IEEE J. Solid State Circuits* **2015**, *50*, 1657–1668. [CrossRef]
68. Niaboli-Guilani, M.; Saberkari, A.; Meshkin, R. A low power low phase noise CMOS voltage-controlled oscillator. In Proceedings of the 2010 17th IEEE International Conference on Electronics, Circuits and Systems, Athens, Greece, 12–15 December 2010. [CrossRef]
69. Hejazi, A.; Pu, Y.G.; Lee, K.-Y. A Design of wide-range and low phase noise linear transconductance VCO with 193.76 dBc/Hz FoMT for mm-wave 5G transceivers. *Electronics* **2020**, *9*, 935. [CrossRef]
70. Padovan, F.; Quadrelli, F.; Bassi, M.; Tiebout, M.; Bevilacqua, A. A quad-core 15GHz BiCMOS VCO with −124dBc/Hz phase noise at 1MHz offset, −189dBc/Hz FOM, and robust to multimode concurrent oscillations. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 11–15 February 2018. [CrossRef]
71. Kucharski, M.; Herzel, F.; Ng, H.J.; Kissinger, D. A Ka-band BiCMOS LC-VCO with Wide Tuning Range and Low Phase Noise Using Switched Coupled Inductors. In Proceedings of the 2016 11th European Microwave Integrated Circuits Conference (EuMIC), London, UK, 3–4 October 2016. [CrossRef]