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A Low-Power, Low-Noise, Resistive-Bridge Microsensor Readout Circuit with Chopper-Stabilized Recycling Folded Cascode Instrumentation Amplifier

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Abstract: In this paper, a low-power and low-noise readout circuit for resistive-bridge microsensors is presented. The chopper-stabilized, recycling folded cascode current-feedback instrumentation amplifier (IA) is proposed to achieve the low-power, low-noise, and high-input impedance. The chopper-stabilized, recycling folded cascode topology (with a Monticelli-style, class-AB output stage) can enhance the overall noise characteristic, gain, and slew rate. The readout circuit consists of a chopper-stabilized, recycling folded cascode IA, low-pass filter (LPF), ADC driving buffer, and 12-bit successive-approximation-register (SAR) analog-to-digital converter (ADC). The prototype readout circuit is implemented in a standard 0.18 μm CMOS process, with an active area of 12.5 mm^2. The measured input-referred noise at 1 Hz is 86.6 nV/$\sqrt{Hz}$ and the noise efficiency factor (NEF) is 4.94, respectively. The total current consumption is 2.23 μA, with a 1.8 V power supply.

Keywords: low-noise; resistive microsensor; sensor readout circuit; chopper stabilization; recycling folded cascode instrumentation amplifier

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1. Introduction

The resistive micro-electro-mechanical system (MEMS) sensors are widely used to detect information, such as pressure, temperature, humidity, and biological signals [1–4]. Resistive MEMS sensors have advantages, such as low price, high linearity, and simple structure. Resistive MEMS sensors are mainly implemented with the Wheatstone bridge structure, which converts the resistance change into a voltage change with several mV. The converted voltage is too small to process resistive sensor applications. For this reason, a readout integrated circuit (ROIC), for resistive sensor signal processing, is required. The amplification stage in the ROIC is usually implemented with an instrumentation amplifier (IA). For high precision signal processing, the IA should have low-input noise and high-input impedance. Since the input signal has only a few of mV, low-frequency noise, such as flicker noise, can distort the baseline of input signal. Additionally, with the low-input impedance of IA, the effect of the mismatch with sensor electrode can be large, resulting in high-input offset and low CMRR of IA. In addition, for portable battery-powered systems, low-power implementation is required for longer operating hours.

While maintaining low-power consumption, the performances for high, open-loop gain, fast slew rate, large-output swing, and low-noise characteristics should be achieved for high precision signal aquation. The folded cascode (FC) topology is widely used for gain stage in the amplifier, as shown in Figure 1a. However, as shown in Figure 1a, the role of transistors *MN*1 and *MN*2 is only limited to providing the small-signal input current to the folding node. To overcome this inefficiency, a modified FC was presented, replacing the

current source with active current mirrors, as shown in Figure 1b, called recycling folded cascode (RFC) [5].

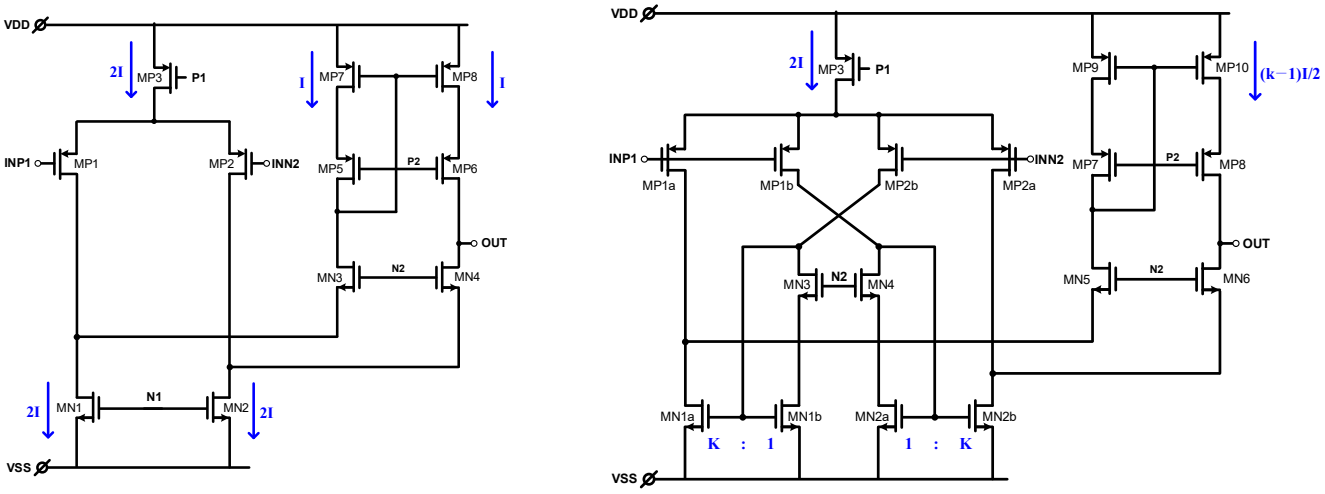


Figure 1. (**a**) conventional folded cascode; (**b**) recycling folded cascode.

Many studies have been also reported using RFC structures to enhance power efficiency [6–8]. The current mirror with a 1:*K* ratio increases transconductance, and the cross-over connections keeps the small-signal currents, added at the sources of *MN*5 and *MN*6, in phase. The resulting transconductance and gain bandwidth (GBW) of the RFC are:

$$G_{mRFC} = g_{mPM1a}(1 + K) \tag{1}$$

$$GBW_{RFC} = \frac{g_{mMP1a}(1 + K)}{2\pi C_L} \tag{2}$$

With g_{mPM1a}, the transconductance of the transistor *MP*1*a* and C_L the load capacitor is shown at the output node, OUT. For the same area and power consumption, the RFC delivers wider bandwidth, higher gain, and higher slew rate than the FC topology.

For resistive-bridge sensor readout, the resistance-to-voltage conversion has an advantage of relatively large dynamic range; however, nonlinear outputs, due to the effects of noise and the nonzero offset by the readout circuit, can occur. To minimize those nonlinearity error components, a precise sensor readout circuit, with low noise and offset, is required. The chopper stabilization scheme can reduce low-frequency noises, achieving the required low-noise specification [9]. Figure 2 shows the well-known chopping principle, with chopped amplifier and its ideal time domain waveforms. The input voltage in the DC band, V_{in}, is modulated by a chopper CH1, with clock frequency f_{ch}, and it is converted to a modulated AC signal. Next, the modulated AC signal and input offset are amplified together with amplifier gain, *A*. Then the output chopper, CH2, demodulates the amplified AC modulated signal back to DC signal. The offset to the odd harmonics of f_{ch}, modulated by the CH2, can be filtered out after passing the LPF. Thus, the thermal-noise limited signal-to-noise ratio (SNR) can be achieved.

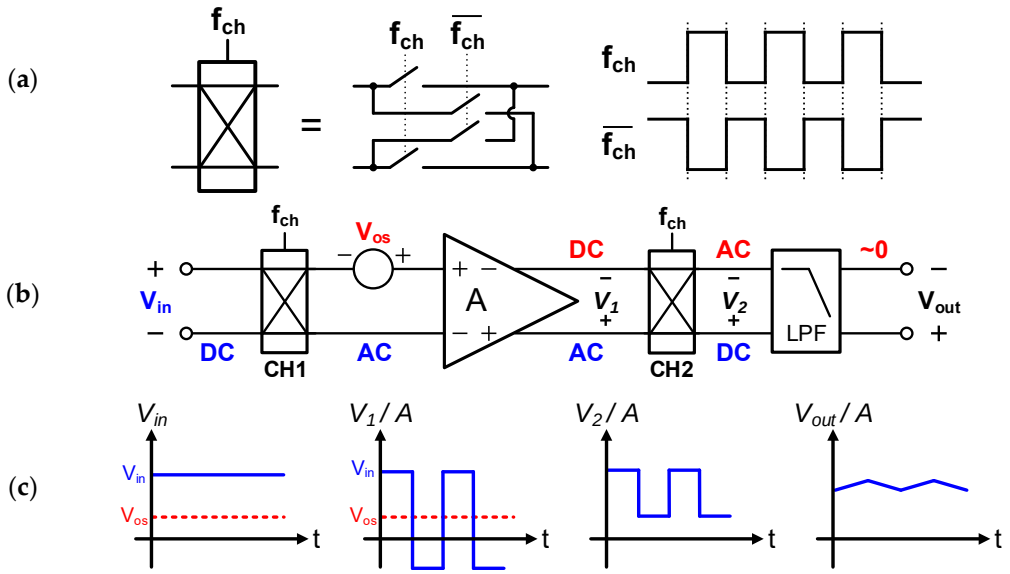


Figure 2. Chopping principle in the time domain (**a**) chopper; (**b**) amplifier with chopper; (**c**) ideal time domain signal waveforms. Adapted from [9].

In this paper, we propose a low-noise, low-power, and high-input impedance readout IC for resistive microsensors. To overcome the power–noise tradeoff, the chopper-stabilized, current-feedback instrumentation amplifier (CFIA), with RFC topology, is proposed. High-current, efficient operational transconductance amplifier (OTA) using RFC topologies have been extensively investigated; however, CFIA using RFC topologies, which has two input differential pairs and acts as differential difference amplifier, are rarely considered. To the author's best knowledge, CFIA based on RFC has not been reported. The chopper stabilization technique is an effective way to reduce low-frequency noise and is widely used in various instrumentation amplifiers. The RFC topology can reduce power consumption under the same desired bandwidth. Moreover, the high-input impedance with the tens femtofarads of small gate capacitance can be achieved with the proposed IA scheme.

This paper consists of the following order. In Section 2, the proposed resistive-bridge sensor ROIC with chopper-stabilized RFC CFIA is explained with simulation results. Section 3 describes experimental results and summarized performance of the proposed ROIC. Additional discussion and conclusions are presented in Section 4.

2. Proposed Resistive-Bridge Readout Integrated Circuit

This section discusses a proposed low-power and low-noise resistive-bridge microsensor ROIC with chopper-stabilized RFC IA. Section 2.1 discusses the top architecture and sub-blocks of the proposed resistive-bridge microsensor ROIC. Section 2.2 explains the schematic and operating principles of a chopper-stabilized RFC IA. Section 2.3 explains the AOCL, LPF, ADC driving buffer, and 12-bit SAR ADC, briefly.

2.1. Top Architecture of the Proposed Resistive-Bridge Microsensor ROIC

Three types of the IAs are mainly utilized: the capacitively-coupled, conventional 3-opamp, and current feedback IAs. To prevent signal distortion, high-input impedance is an important parameter. In Figure 3a, showing the capacitive-coupled instrumentation amplifier (CCIA) scheme, the input impedance at the input node of the amplifier is reduced, owing to the shunt–shunt feedback. The input impedance of the CCIA can be expressed as:

$$Z_{IN(CCIA)} = \left| \frac{2}{sC_{in}} \right| = \left| \frac{2}{2\pi f_{CH} C_{in}} \right| \quad (3)$$

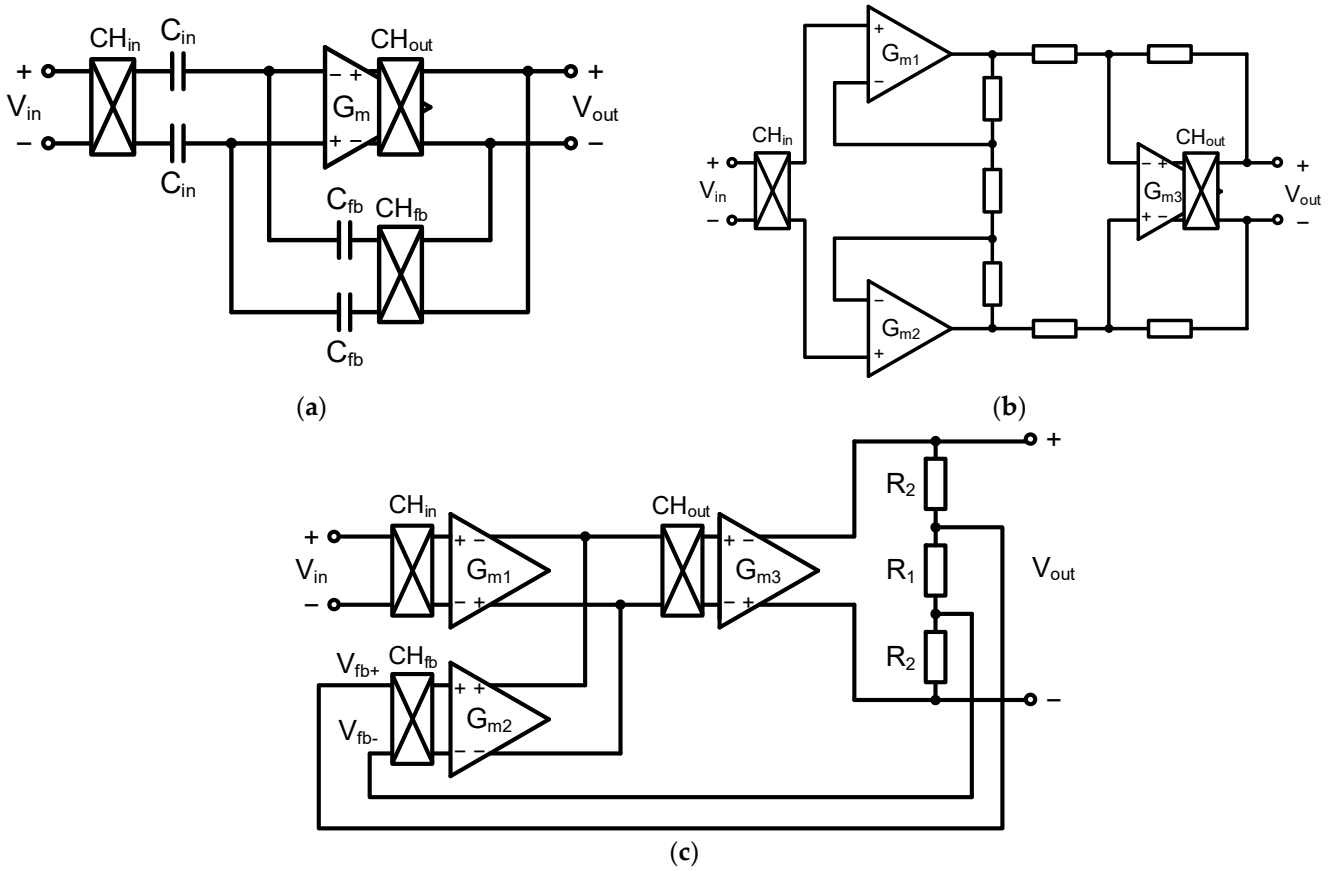


Figure 3. (**a**) Instrumentation amplifier topologies: (**a**) block diagram of CCIA; (**b**) 3-operational amplifier IA; (**c**) block diagram of a CFIA.

Its input impedance is typically in the order from several hundred kΩ to several MΩ, determined by the impedance of the input capacitors and the chopping frequency. To increase the input impedance, the input impedance boosting schemes, using positive feedback or input pre-charge techniques, are used; however, the complexity of the stability and circuits are drawbacks [10,11]. As shown in Figure 3b,c, the 3-opamp IA and the CFIA receive input signals directly from the gate input node of the amplifier, and only the small gate input capacitances are only shown at the input node; thus, much higher input impedance can be achieved than with the CCIA.

The input impedance of the 3-opamp IA and CFIA can be expressed as (4):

$$Z_{IN(3-opamp,CFIA)} = \left|\frac{2}{sC_g}\right| = \left|\frac{2}{2\pi f_{CH} C_g}\right| \quad (4)$$

where C_g is the gate input capacitance of input transconductance, G_{m1}. In this design, the gate capacitance, C_g, is simulated to 272.8 fF, which is total gate capacitance (c_{gg}). From the power consumption perspective, the CFIA is more efficient than 3-opamp IA because the output stages are shared. Moreover, by converting the input differential voltage signal through the input transconductance, G_{m1}, to differential current, the input common-mode and the feedback common-mode can be separated, thus CFIA achieve the higher CMRR, compared to 3-opamp IA [12,13].

The top block diagram of the proposed resistive-bridge microsensor ROIC is shown in Figure 4. It consists of a chopper-stabilized CFIA, low-pass filter (LPF), ADC driving buffer, and 12-bit successive-approximation-register (SAR) analog-to-digital converter (ADC). First, the resistive sensor converts the resistance to the voltage signal, the input signal is amplified through the first stage (which is the proposed, fully differential CFIA). The gain of proposed CFIA is determined by the feedback resistors R_f and R_c, and the gain can be

adjusted to 4-bits (*DIN<3:0>*) via the programmable resistance, R_c, through the SPI. The gain of the proposed CFIA can be expressed as:

$$gain = 1 + 2 \cdot \frac{R_f}{R_c} \tag{5}$$

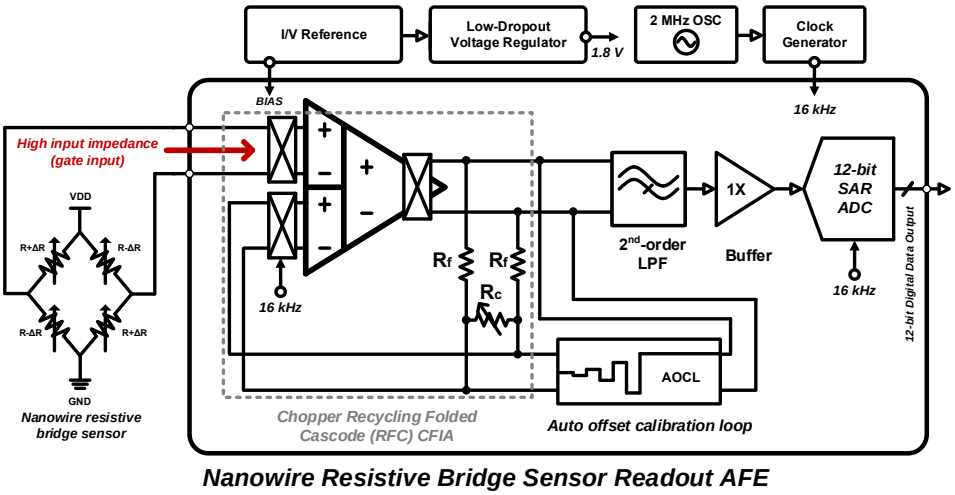


Figure 4. Top block diagram of the proposed resistive-bridge microsensor readout IC.

Figure 5 shows the transfer function of the CFIA, in which the gain is adjusted from 70.6 (*DIN<3:0>* = 1111) to 220.3 (*DIN<3:0>* = 0000). The amplified signal goes through the 2nd-order LPF, with 500 Hz cutoff frequency and buffer, and finally converts to the digital signal through the 12-bit SAR ADC.

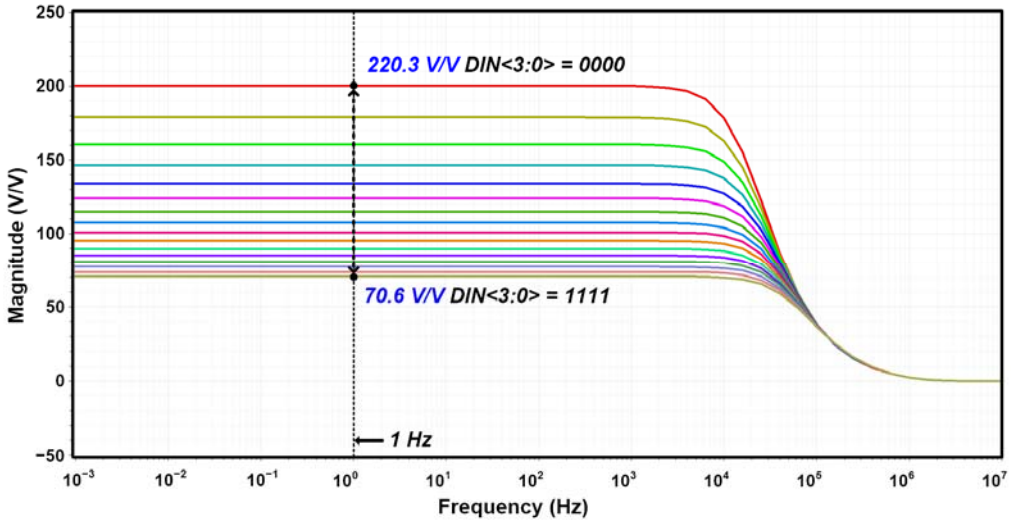


Figure 5. Simulated transfer function of the proposed CFIA.

2.2. Circuit Implementation of a Chopper-Stabilized, Recycling Folded Cascode Instrumentaation Amplifier

Figure 6 shows the schematic of the proposed chopper-stabilized RFC IA. To reduce low-frequency noise, the choppers are added to the input stage and the folded cascode stage. For using fully differential CFIA topology, the differential difference amplifier (DDA)-style input stages are needed. The PMOS differential pairs, *MP*1–*MP*4, form the recycling folded

cascode input stage, and *MP*5–*MP*8 forms the feedback input stage. *MN*1–*MN*4 work as driving transistors, with a ratio of 5:6, as shown in (6).

$$MN2 : MN1 = MN3 : MN4 = 5 : 6 \tag{6}$$

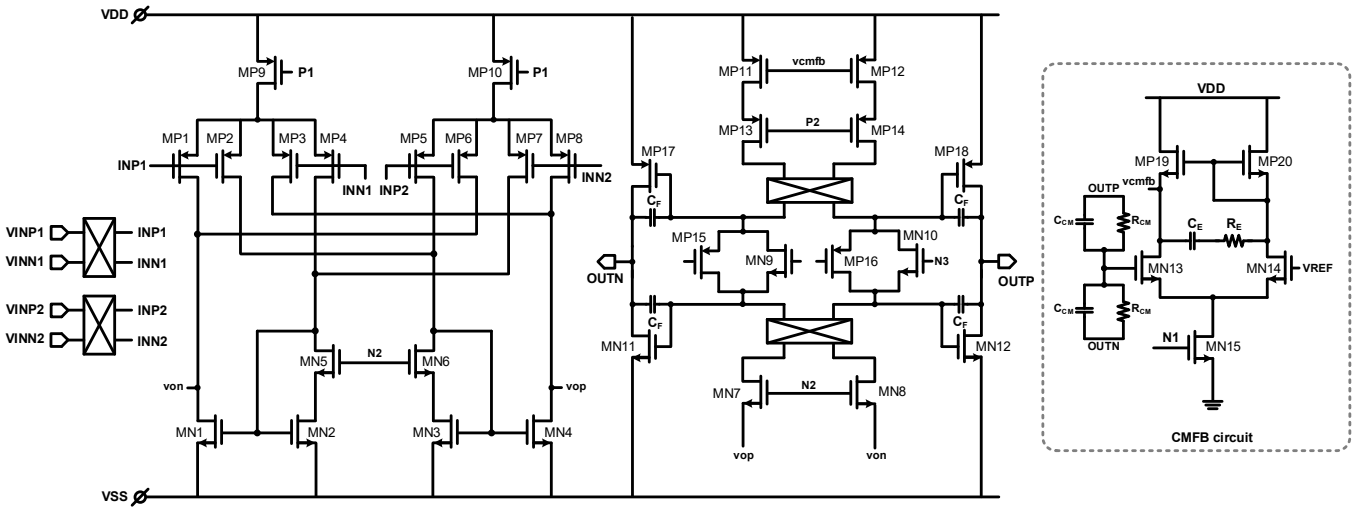


Figure 6. Schematic of the proposed chopper-stabilized RFC.

The cross-over connections of these current mirrors keep the small-signal input currents added at the sources of *MN*7 and *MN*8, in phase. The Monticelli-style, floating class-AB control units are implemented using *MP*15, *MN*9, *MP*16, and *MN*10. By implementing class-AB output stage, G_m and GBW of the RFC can be increased.

The compensation capacitors, C_Fs, are connected between the output nodes and gate of the output common source stage in a Miller compensation manner to compensate for the frequency response. The R_{CM}s and C_{CM}s detect the output common-mode voltage. The error amplifier for common-mode feedback consists of *MP*19, *MP*20, *MN*13, *MN*14, and *MN*15 to generate the control voltage *vcmfb*, which controls the bias current of the cascode stages. The W/L values of the transistors and passive components (in the proposed RFC's fully differential difference amplifier) are shown in Tables 1 and 2, respectively.

Table 1. Values of transistors in proposed RFC FDDA.

Transistor	Size (*W*/*L*) (μm)	Transistor	Size (*W*/*L*) (μm)
*MP*1–*MP*8	32/4	*MN*1, *MN*4	0.6/10
*MP*9, *MP*10	2/1.5	*MN*2, *MN*3	0.5/10
*MP*11, *MP*12	4/10	*MN*5, *MN*6	8/1
*MP*13, *MP*14	4/10	*MN*7, *MN*8	40/12
*MP*15, *MP*16	1/10	*MN*9, *MN*10	1/18
*MP*17, *MP*18	2/10	*MN*11, *MN*12	1/10
*MP*19, *MP*20	2/2	*MN*13, *MN*14	1/16
-	-	*MN*15	0.5/12

Table 2. Values of passive components in proposed RFC FDDA.

Component	Value
C_F	200 fF
C_E	16.6 pF
R_E	466 kΩ
C_{CM}	400 fF
R_{CM}	11 MΩ

The transconductance of the 1st-stage can be increased by 11/5, according to expression (1) and can be expressed as (7). The gain bandwidth can be determined by the G_{mRFC} and compensation capacitor, C_F, as (8).

$$G_{mRFC(1st-stage)} = \frac{11}{5} g_{mPM1a} \tag{7}$$

$$GBW_{RFC} = \frac{G_{mRFC}}{2\pi C_F} \tag{8}$$

The simulated input–output characteristics of the RFC CFIA are shown in Figure 7. The coefficient of the determination R^2 was calculated to be 0.9999, within the resistance variation (ΔR) range of −380Ω~380Ω. Figure 8 shows the closed-loop gain of the proposed RFC CFIA, based on corner simulation. The closed-loop gain varies from 100.0026 V/V (at the FF 125 °C) to 100.9353 V/V (at the TT 29 °C). Figure 9 shows the input-referred noise, with corner simulation results, when the chopper is enabled and disabled. The input-referred, low-frequency noise at 1 Hz is reduced from 1.49 μV/$\sqrt{}$Hz (when the chopper is disabled) to 80 nV/$\sqrt{}$Hz (TT 27 °C) (when the chopper is enabled). The input-referred noise is reduced to 1/18.6 times with the chopper operation. The corner simulation results of the CMRR and PSRR are shown in Figure 10. The value of the CMRR and PSRR at 100 Hz varies from 237 dB to 267 dB and 165 dB to 199 dB, respectively. With the Monte Carlo simulations, the high CMRR and PSRR were obtained as shown in Figure 11. The mean values of the CMRR and PSRR at 100 Hz, with mismatch, are 176.6 dB and 119 dB, respectively. The simulations were performed with the default feedback gain configuration (*DIN<3:0>* = 1000, gain = 100 V/V).

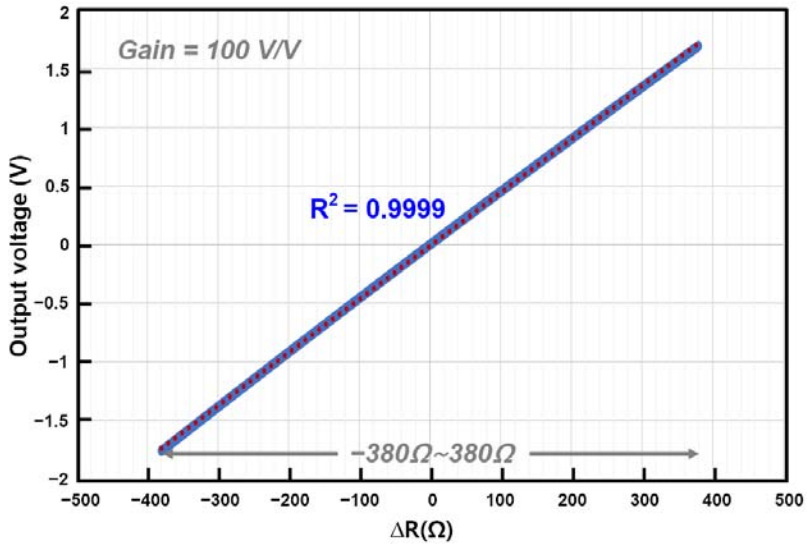


Figure 7. Simulated input–output characteristics.

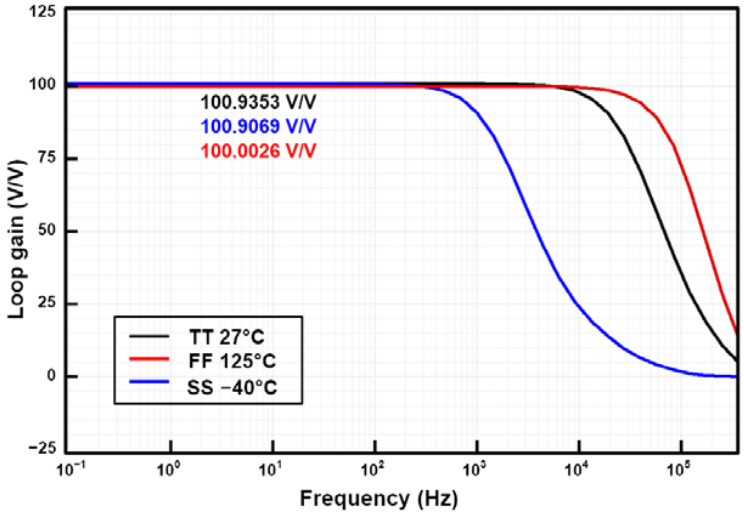


Figure 8. Corner simulation result of the closed-loop gain.

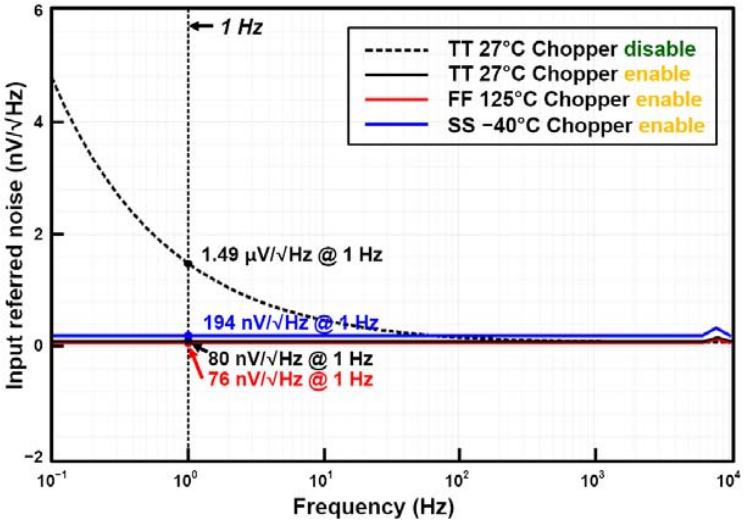
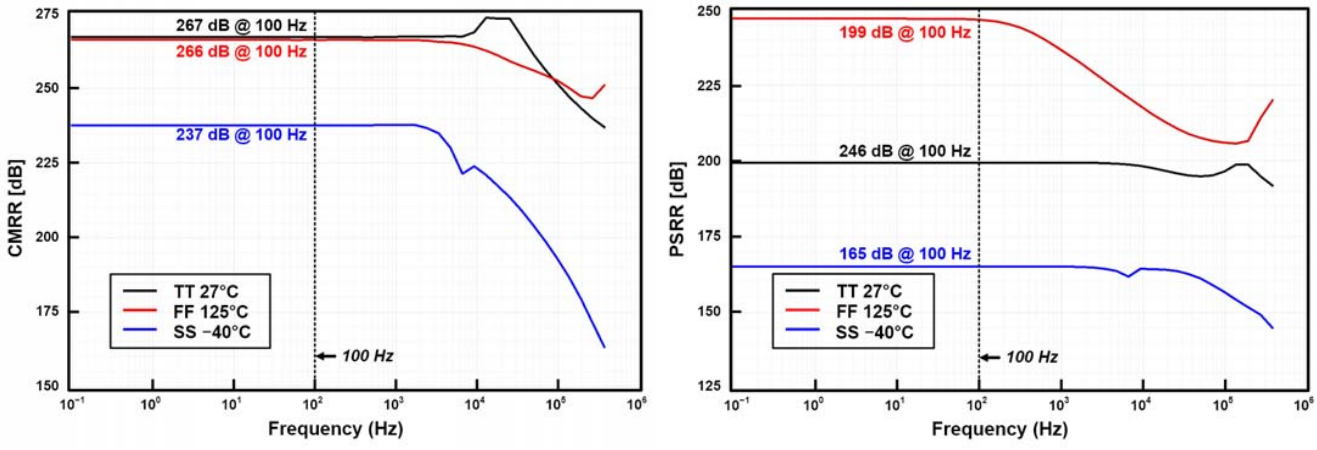
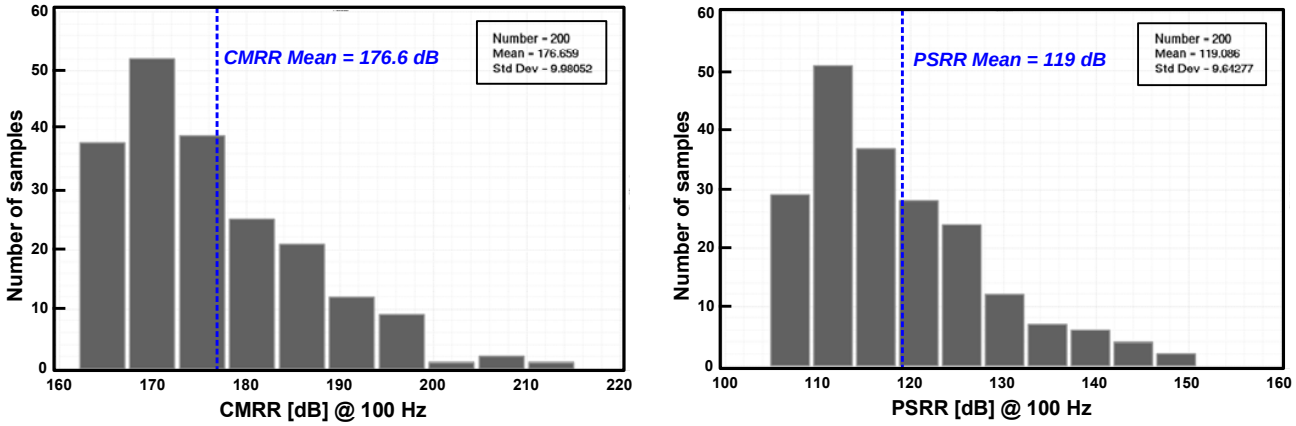


Figure 9. Simulated result of the input-referred noise.



(**a**) (**b**)

Figure 10. Corner simulation results of the (**a**) CMRR and (**b**) PSRR.



(**a**) (**b**)

Figure 11. Monte Carlo simulation results of the (**a**) CMRR and (**b**) PSRR.

2.3. AOCL, LPF, ADC Driving Buffer, and 12-Bit SAR ADC

The proposed CFIA circuit used chopper stabilization techniques for low-noise performance, but the undesired offset of the resistive-bridge sensor also be amplified at the output stage of the CFIA. To solve this problem, we added an automatic offset calibration loop (AOCL) for offset cancellation. The AOCL consists of a comparator, a 12-bit SAR logic block, and a 12-bit R-2R digital-to-analog converter (DAC). When offset is amplified through the CFIA, the output of the CFIA is compared through the comparator input connected to the CFIA output. The output of the comparator passes through the 12-bit SAR logic to generate the corresponding 12-bit digital code and is applied as an input to the 12-bit R-2R DAC, which generates the corresponding compensation voltage to compensate the offset. The low-frequency noise, modulated at the chopper frequency, is shown at the output as a ripple; the 2nd-order 500 Hz LPF was used to remove the chopper ripple. The signal amplified through the IA is converted to the digital signal through the 12-bit SAR ADC, after ADC buffer. The detailed circuit implementations of the 500 Hz 2nd-order LPF, buffers for driving ADC, 12-bit SAR ADC, and AOCL are described in [14–17].

3. Experimental Results

Figure 12 shows the die photograph of the proposed resistive-bridge readout IC. The IC is fabricated using a TSMC 180 nm CMOS process, resulting in the RFC CFIA block size of 293 μm × 183 μm. The printed circuit board (PCB) was designed to evaluate the performance of the proposed IC, the test board and the measurement environment are shown in Figure 13.

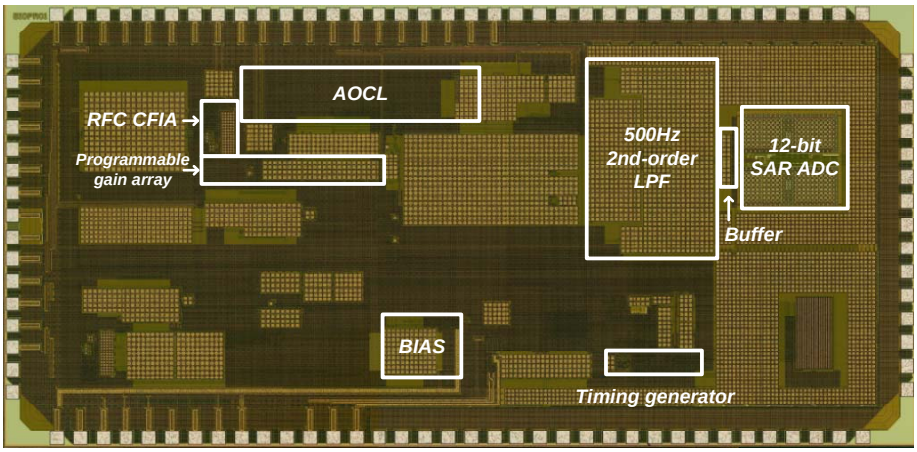


Figure 12. Die photograph of the proposed resistive-bridge readout IC.

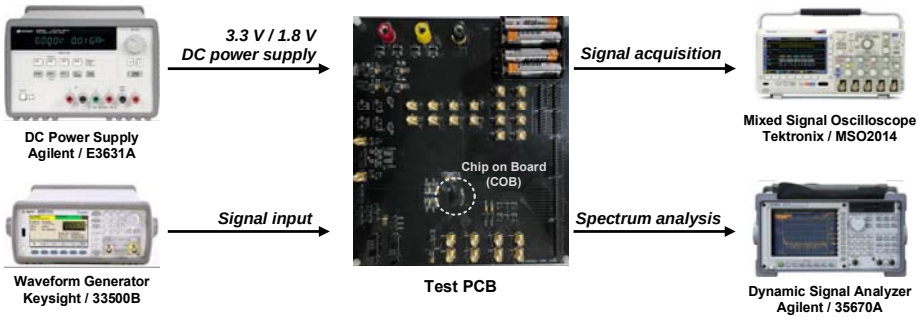


Figure 13. Measurement environment of the proposed IC with test board.

Figure 14 shows the voltage output of the IC, which varies along the pressure applied to the resistive strain gauge force sensor, which has 10 kOhm flat resistance; the resistance varies from 14 kΩ to 26 kΩ [18]. Figure 15a shows the measured transient response when the input source is a 5 mV_{pp} differential sine wave input. Figure 15b shows the measured transfer function of the CFIA when the gain setting is maximum (<*DIN*> = 0000), resulting in 46.12 dB DC gain and 580 kHz unit gain bandwidth (UGBW).

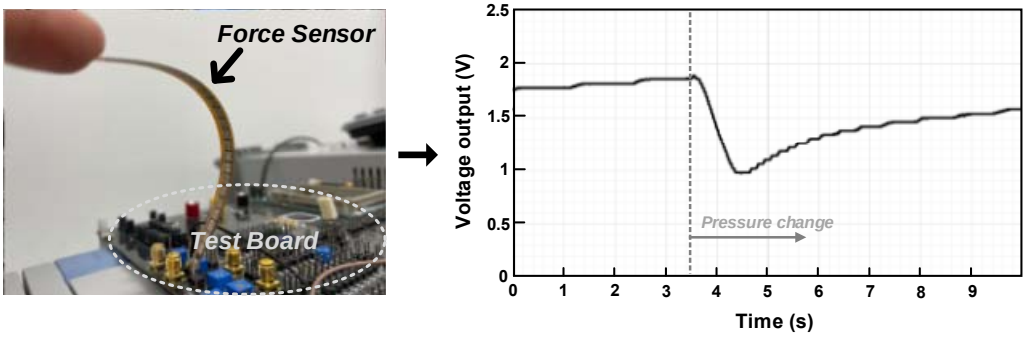


Figure 14. Measured voltage output response, due to pressure changes of the force sensor.

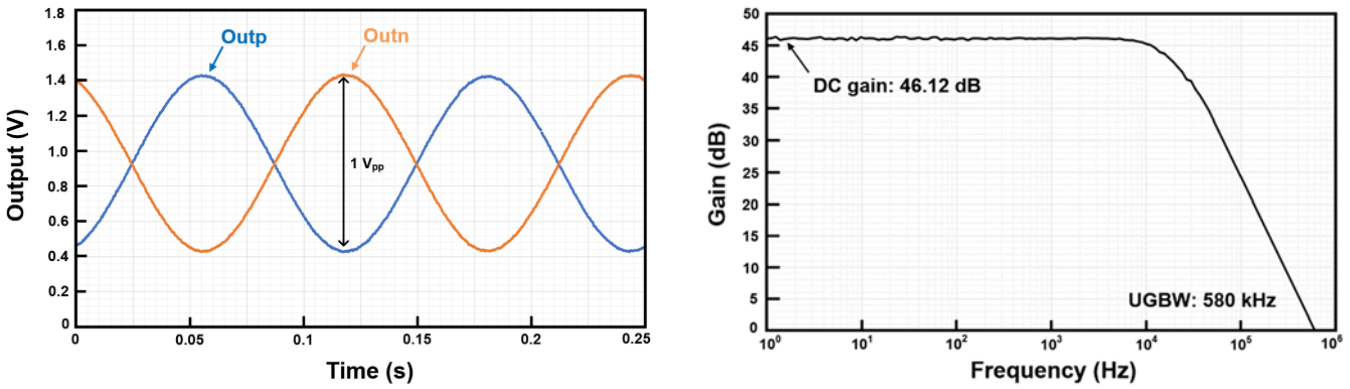


Figure 15. (**a**) Measured transient response (**b**) Transfer function of the proposed CFIA at the maximum gain.

The measured input-referred noise is 86.6 nV/$\sqrt{Hz}$ at 1 Hz and 32.6 nV/$\sqrt{Hz}$ at 200 Hz, as shown in Figure 16. The minimum current consumption of the IC is 3 µA (where only IA and bias block are used and if the LPF, buffer, ADC, and timing generator are fully utilized) the power consumption is 7.954 µA. The noise-efficiency-factor (NEF) is widely used to compare the power–noise trade-offs [19]. The NEF can be calculated by (9).

$$NEF = V_{ni,RMS} \cdot \sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (9)$$

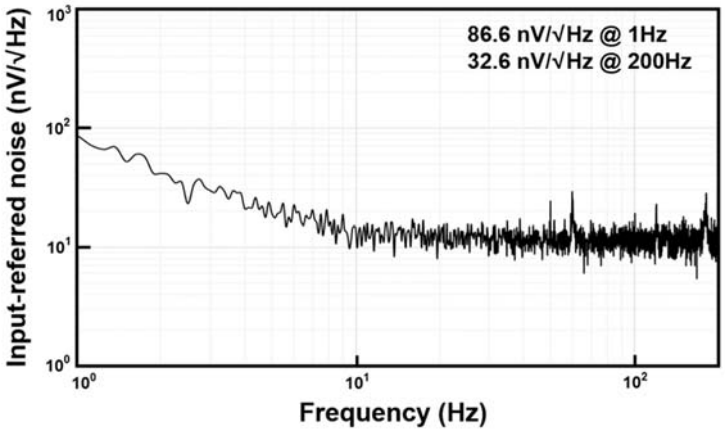


Figure 16. Measured input-referred noise.

The NEF value is proportional to the input reference noise of the IA and the current consumption, which can be used to determine whether IA with low NEF has performance advantages. The NEF of the proposed IA is calculated to be 4.94. The performance comparisons of the proposed circuit, with the previous works regarding resistive-bridge ROIC, are summarized in Table 3.

Table 3. Performance summary of proposed resistive-bridge ROIC and comparison with other studies.

	This Work	[20]	[13]	[21]	[22]
Architecture	CFIA (with RFC) + chopping	CFIA + chopping + RRL	CCIA + chopping	CCIA + chopping + CDS + RRL	RC + chopping
Technology (μm)	0.18	0.18	0.18	0.13	0.35
Supply voltage (V)	1.8	3.3	1.8	3	5
Total current consumption (μA)	7.9	200	1200	326	860
Gain of IA	70–220	100	40	16–32	-
Gain bandwidth (Hz)	580 k	-	-	-	2 k
Current consumption of IA (μA)	2.23	-	-	-	700
Input-referred noise (nV/$\sqrt{}$Hz)	86.6	23	3.7	16	4.2
NEF	4.94	6.1	5.0	11.1	4.7

4. Discussion and Conclusions

In this paper, a low-power, low-noise, resistive-bridge microsensor readout circuit with chopper-stabilized, recycling folded cascode instrumentation amplifier is presented. The readout circuit consists of a chopper-stabilized RFC IA, AOCL, 2nd-order LPF, ADC driving buffer, and 12-bit SAR ADC. The RFC structure was used to achieve low-power consumption. Additionally, low-noise was implemented by applying the chopper stabilization technique, and to realize high-input impedance for accurate signal amplifying, CFIA topology was implemented. The proposed readout circuit was implemented in a standard 0.18 μm CMOS process, with an active area of 12.5 mm^2. The measured input-referred noise at 1 Hz was 86.6 nV/$\sqrt{}$Hz and the noise efficiency factor (NEF) was 4.94, respectively. The total current consumption was 2.23 μA, with a 1.8 V power supply. There were trade-offs between the input-referred noise and power consumption. The input-referred

noise in this paper was higher; however, the power consumptions were lower than the previous research (in Table 3). This chip achieves relatively lower NEF, which shows the power–noise efficiency. The gain of the proposed IA can be adjusted from 70 to 220, via a 4-bit programmable resistor array *DIN<3:0>*, so that it can be expected to be available for various resistive-bridge sensor applications.

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Conflicts of Interest: The authors declare no conflict of interest.

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