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# Prediction of a Two-Transistor Vertical QNOT Gate

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**Abstract:** A new design of quaternary inverter (QNOT gate) is proposed by means of finite-element simulation. Traditionally, increasing the number of data levels in digital logic circuits was achieved by increasing the number of transistors. Our QNOT gate consists of only two transistors, resembling the binary complementary metal-oxide-semiconductor (CMOS) inverter, yet the two additional levels are generated by controlling the charge-injection barrier and electrode overlap. Furthermore, these two transistors are stacked vertically, meaning that the entire footprint only consumes the area of one single transistor. We explore several key geometrical and material parameters in a series of simulations to show how to systematically modulate and optimize the quaternary logic behaviors.

**Keywords:** multi-valued logic; quaternary inverter; QNOT gate; 3-D integration; semiconductor device simulation

## 1. Introduction

The current electronics era was made possible by digital systems that maximize their simplicity in converting, processing, and memorizing a wide range of data into only two available electrical signal levels ("0" and "1"). However, such a standard binary logic architecture seems to hardly meet the increasing requirements for larger information capacities, which laid out the foundation of multi-valued logic (MVL) systems with $n \geq 3$, where $n$ is the number of distinguishable data levels [1–3]. To date, the realization of MVL has no fully established protocols; thus, various strategies are being pursued at the materials, device, and system levels [4–6]. For instance, Kobashi et al., in 2018, proposed a ternary ($n = 3$) inverter based on a lateral heterojunction of organic semiconductors [7,8]. In 2019, Yoo et al. proposed a full-swing ternary circuit using a negative transconductance heterojunction transistor with a modified structure [9]. Such reports suggested that, up to $n = 3$, a two-transistor topology can be effectively maintained (one unipolar and one anti-ambipolar). However, for a higher $n$, previous research mostly adopted circuit-based implementations with the number of transistors roughly corresponding to the number of data levels [10,11], implying the huge technological interest in advanced designs that reduce the transistor count.

In this study, we demonstrate an aggressive projection of quaternary ($n = 4$) digital inverter (or QNOT gate) made of only two field-effect transistors (FETs), by carrying out physically based finite-element simulation. In addition to saving the number of transistors, our proposed logic gate circuit is built by vertical (or three dimensional, 3-D) stacking of its component transistors, also showing the high potential for area-efficient on-chip deployment. In short, this particular geometry combines the two important trending design concepts in current electronics research, namely MVL and 3-D integration, in enabling a greatly simplified QNOT gate with a more efficient use of raw materials, manufacturing resources, and physical support areas. Importantly, the systematical variation of simulation parameters provides an in-depth understanding of how such an operation is obtained and also offers practical engineering guidelines toward targeted performances, which are intended to motivate wide-ranging experimental follow-ups.

## 2. Methods

A finite-element drift-diffusion simulation package (Silvaco ATLAS) was used for this study. Organic semiconductors provide viable routes toward low-cost flexible electronics, by virtue of their secondary bonding nature. However, printed layers can have a feature size that is much larger than those patterned by conventional lithography. In this context, the vertical integration is of particular interest to printed organic electronics [12,13]. We, therefore, employed geometries and parameters relevant to organic materials and devices, yet some of the results will be extendable to other semiconductor platforms. The two-transistor, five-electrode circuit was defined according to the structure depicted in Figure 1a. The single gate electrode embedded in the common dielectric serves as the input node, where the input voltage ($V_{\text{in}}$) is applied. In the base structure, this input electrode is at the middle of the dielectric and is aligned to have no vertical overlap with the source and drain electrodes. The organic semiconductor thickness ($t_{\text{osc}}$) is 50 nm (base structure), and the dielectric thickness ($t_{\text{diel}}$) is 100 nm. The channel length ($L$) and width ($W$) are 50 and 1000 μm, respectively. The dielectric constant of gate dielectric is 3.5. All electrodes are metallic with the work function of 4.5 eV. The p-type FET (PFET) and n-type FET (NFET) are made symmetric both structurally and energetically, with the carrier mobility of 1 $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$, the bandgap of 2 eV, and the effective density of states of $10^{20}\ \text{cm}^{-3}$. The high-occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) energies of the respective semiconductors are systematically varied to generate different charge-injection barriers ($E_b$) [14]. The supply electrode is positioned on top of PFET, and the supply voltage ($V_{\text{DD}}$) is applied to this node, in reference to the ground on the NFET side. The two drain electrodes are declared as the single floating numerical node, where the output voltage ($V_{\text{out}}$) is measured. The terminal characteristics (voltages and currents) along with the internal carrier distributions are self-consistently calculated for the whole circuit, by solving the coupled Poisson's and drift-diffusion equations, under the Boltzmann carrier statistics and based on the Newton method.

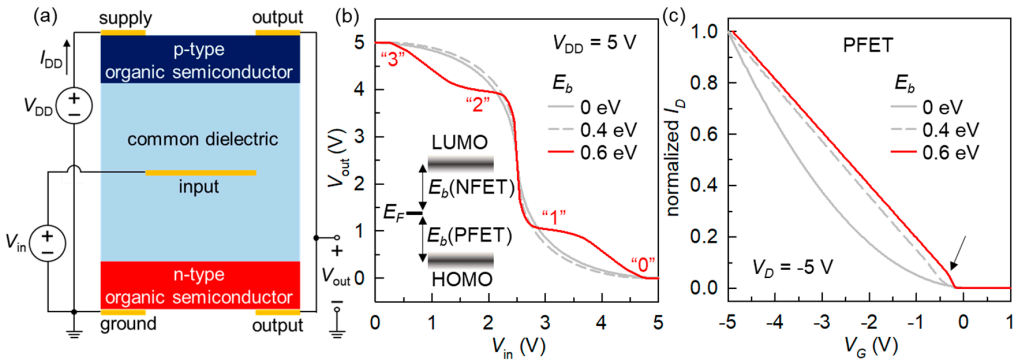


**Figure 1.** (**a**) Cross-sectional illustration and driving configuration of the proposed inverter circuit. (**b**) Simulated voltage-transfer characteristics (VTCs) showing the evolution from binary to quaternary logic. Inset: the energy diagram defining $E_b$ at each field-effect transistor (FET) ($E_F$ is the source/drain metal Fermi level). (**c**) Normalized transfer curve of the p-type FET (PFET) at varying $E_b$.

## 3. Results and Discussion

The proposed layout in Figure 1a is basically analyzed in our previous work on the vertical 3-D organic inverter, which focuses on the voltage-gain improvement by increasing the contact resistance of FETs [13]. Here, we demonstrate for the first time that a substantial increase in $E_b$ at both FETs can dramatically transform the simple 2-level inverter into a fully functional QNOT gate, without any structural modification. Figure 1b shows the simulation results of the voltage-transfer characteristics (VTCs) of the circuit in Figure 1a, at $V_{\text{DD}}$ = 5 V. The parametric variation of $E_b$ was introduced with no change in electrode work function, but by energetically moving the semiconductor HOMO and LUMO levels together keeping the same bandgap (Figure 1b inset). The VTCs reveal that an initial departure

from an ideal ohmic contact ($E_b$ = 0 eV) to a blocking one ($E_b$ = 0.4 eV) actually provides a sharper data transition from high to low $V_{out}$ [13]. Surprisingly, it was found that an $E_b$ of 0.6 eV substantially changes the shape of VTC, where the four data levels ("0", "1", "2", and "3") are clearly identifiable. To gain a first insight into its mechanism, we additionally performed simulations of individual FETs. As shown in Figure 1c, the normalized saturation-regime transfer curve of the PFET at a drain voltage ($V_D$) of −5 V shows a quadratic shape with regard to gate voltage ($V_G$) when $E_b$ = 0 eV, suggesting no contact resistance effects [15,16]. In contrast, increasing $E_b$ resulted in substantial deviation, exhibiting a quasi-linear behavior at $E_b$ = 0.4 eV. At the $E_b$ enabling the quaternary circuit, the drain current ($I_D$) showed an apparent kink (arrow in Figure 1c), which is generally considered as the consequence of a substantial contact resistance [17–19]. Albeit with different biasing, this abrupt slope change on the transfer curve in part rationalizes the QNOT behavior of Figure 1b; this in fact translates into the existence of two distinct regimes with different resistance distribution ratios on a single transistor, during its on-off scan by $V_{in}$.

As the second requirement for QNOT functionality (in addition to $E_b$), the absence of geometrical overlap between the gate (input) and source/drain electrodes is addressed. Figure 2a is the side-by-side comparison of the cases of no overlap (base structure) and the full overlap with an extended gate electrode. Clearly, there is no quaternary effect in the modified circuit with a full electrode overlap. To further our understanding of underlying mechanism, we extracted the charge-carrier distribution at each component device in a full simulated inverter (not from the individual transistor simulation such as that in Figure 1c). Especially, the focus was placed on visualizing the internal distribution at two newly developed data states, one at $V_{in}$ = 2V (level "2") and the other at $V_{in}$ = 3 V (level "1") (in conjunction with Figure 1b). Comparing Figure 2b,c reveals one important difference, which is the apparent carrier pinch-off at the supply node (i.e., source electrode) indicated by the arrow in the no-overlap data of Figure 2b. This actually reminds us of the special property of the source-gated transistor (SGTs), whose operation largely relies on this source pinch-off rather than the drain pinch-off prevailing in traditional FETs [20]. While it was known that such a behavior is fundamentally associated with a high-barrier contact (which is the case here), our data additionally prove that the pinch-off is more accentuated when there is no sufficient gate-source overlap to attract the injected charge carriers toward the channel surface. More importantly, it justifies the presence and absence of the two intermediate voltage levels, since such strong pinching-off at the no-overlap circuit dictates the stable establishment of the constant resistance regime between the complete turning-on and off. Figure 2d,e simply deliver the same message, based on the electron pinch-off at the no-overlap NFET (here the ground is the source) that forms the intermediate state between its full on-off switching.

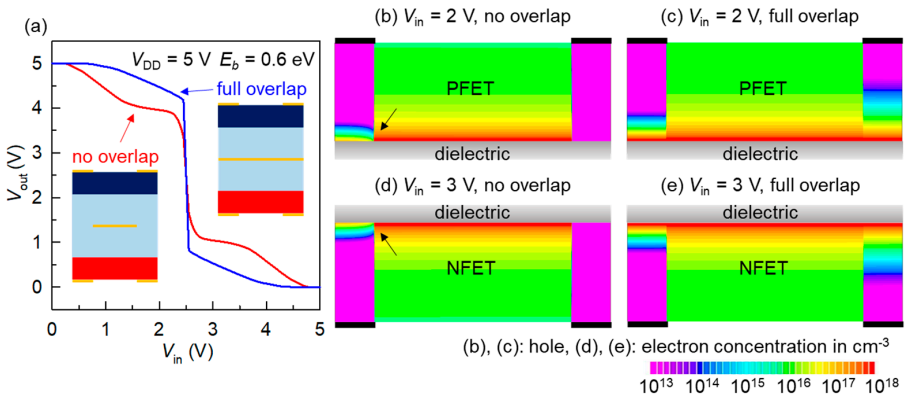


**Figure 2.** (**a**) Simulation results showing the direct impact of the gate-electrode length on VTC. (**b**,**c**) Hole concentration inside the PFET at $V_{in}$ = 2 V (level "2") under no and full overlap conditions. (**d**,**e**) Electron concentration inside the NFET at $V_{in}$ = 3 V (level "1") under no and full overlap conditions.

Now, we return to the base structure ($E_b$ = 0.6 eV, no electrode overlap) and demonstrate the possibilities of VTC engineering. Firstly, the parameter $t_{osc}$ was found to have a significant impact on the level formation, as illustrated in the simulation results of Figure 3a upon changing $t_{osc}$ from 50 to 200 nm. The four output data levels, "3", "2", "1", and "0", were extracted at $V_{in}$ = 0, 2, 3, and 5 V, respectively, from each VTC. As shown in Figure 3b–e, the semiconductor thickness significantly influences the two intermediate data voltages, with a clearly monotonous trend, meaning that a desired value can eventually be obtained through fine tuning of the layer thickness. Meanwhile, little or no impact of $t_{osc}$ was seen on the two extreme levels. This interesting phenomenon can be explained as follows. Since the QNOT behavior in our system originates from the $E_b$ and the contact resistance thereof [13], an enlarged out-of-plane bulk film resistance at a thicker film can significantly modulate the VTC characteristics [14]. More specifically, the FET contact resistance becomes larger with a higher $t_{osc}$ in this staggered electrode architecture [21,22], affecting the establishment of the pinch-off region (see Figure 2b,d), thus pushing the "2" and "1" levels toward $V_{DD}/2$ at the same time.

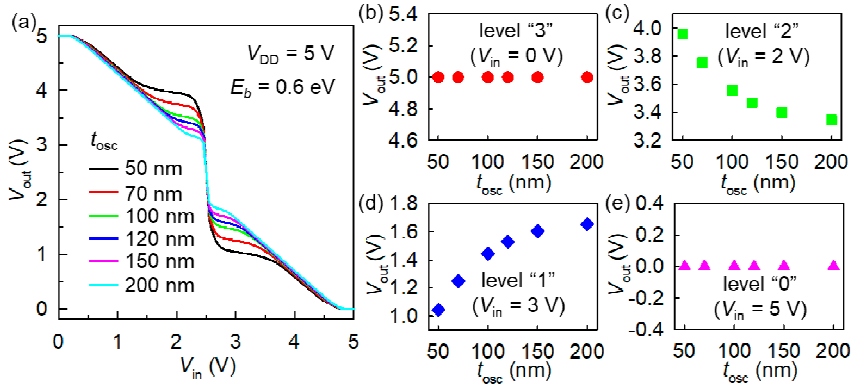


**Figure 3.** (**a**) Change of VTC according to the variation of $t_{osc}$. (**b**–**e**) Extraction of the $V_{out}$ values at four data levels from the results in (**a**).

Secondly, the vertical positioning of the gate electrode was another efficient controlling factor. In fact, separately changing the PFET and NFET gate dielectric thicknesses is a traditional approach in a complementary metal-oxide-semiconductor (CMOS) binary inverter to relatively tune the strength of the transistors [23]. In our simulation, the total thickness of the common dielectric ($t_{diel}$) was fixed as 100 nm, yet the three in-dielectric positions of the gate electrode (center, high, and low) were compared as graphically illustrated in Figure 4a. The high or low position was made by moving the electrode from the center position by 25-nm upwardly or downwardly, respectively. Figure 4b shows that a systematic horizontal movement of the level "2" to "1" transition point was observed by changing the vertical gate position. This is understood as the outcome of the increase in the PFET strength (for the high position) or the NFET strength (for the low position) that redistributes the supplied $V_{DD}$ at different ratios, thus modulating the mid-transition $V_{in}$ point. These results also re-confirm the contact-dominated QNOT mechanism, as evidenced by no practical change in the four data levels and the extreme transitions points, because these properties are mostly determined by the depleted source regions rather than the capacitively modulated channel regions [19].

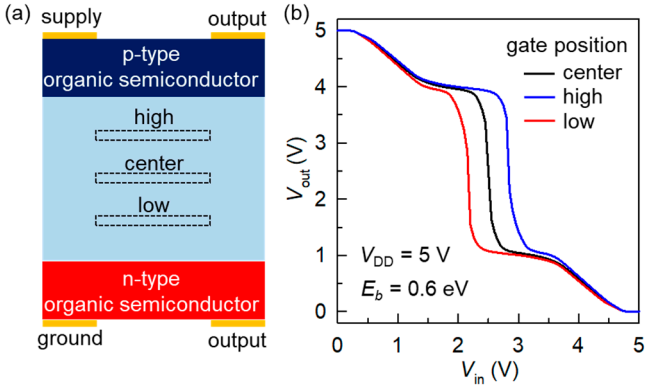


**Figure 4.** (**a**) Illustration showing the structural variation by vertically re-positioning the common gate electrode inside the common dielectric layer. (**b**) VTC comparison for the three gate positions.

Regarding the quaternary inverting behavior in this study, we can make several additional notes. As the $E_b$ increases, the driving current ($I_{DD}$) systematically decreases because of contact resistance. This in turn provides an additional advantage of low power consumption (total power is $V_{DD}$ multiplied by $I_{DD}$) in the QNOT regime (Supplementary Figure S1). Another critical point is that a vertical coupling is essential to QNOT behavior. In our proposed structure, a strong electric field appears between the supply and ground nodes (see Figure 1a), which helps establish an elongated accumulation channel at the source region even without a gate overlap, laying a foundation for the source pinch-off and associated quaternary operation. In stark contrast, comparative simulations showed that both the source and drain contact regions are fully depleted so that less currents flow in the horizontal inverter with no indication of pinch-off and QNOT functionality (Supplementary Figure S2). Also note that a relatively large $t_{diel}$ is used for the relevance to organic electronics. Additional simulations revealed that the operation voltage can be scaled down even in this structure, yet the intermediate levels become indistinct at a $V_{DD}$ below 3 V (Supplementary Figure S3).

## 4. Conclusions

This paper shed light on the technological feasibility of a simple two-transistor vertical QNOT gate. The physical simulation results showed that a substantial $E_b$ and the absence of gate overlap are both required for the appearance of the four data voltage levels. In terms of the VTC engineering, the value of $t_{osc}$ and vertical gate re-positioning were found to be effective in altering the output levels and the mid-transition input voltage, respectively. A systematic correlation between the terminal characteristics, the FET behaviors, and the internal charge distributions established an operation mechanism relying on the source-contact pinch-off and the resulting resistive re-distribution. Our results strategically leveraged the power of material-device-system correlation in developing new structural functionalities, and are expected to serve as a motivation and guideline for next-generation quaternary and higher MVL digital electronics

**Supplementary Materials:** The following are available online at http://www.mdpi.com/2076-3417/10/21/7597/s1, Figure S1: Power consumption; Figure S2: Vertical and horizontal inverter comparison; Figure S3: Scaling property.

**Author Contributions:** Conceptualization, H.H. and C.-H.K.; methodology, H.H.; validation, C.-H.K.; formal analysis, H.H. and C.-H.K.; writing—original draft preparation, H.H.; writing—review and editing, C.-H.K.; supervision, C.-H.K. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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