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Review

Topological Overview of Auxiliary Source Circuits for Grid-Tied Converters †

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Abstract: This paper reviews different types of capacitors and auxiliary source circuit topologies and presents an introduction to control strategies used for circuit applications reducing DC-BUS capacitance. The paper argues in favor of replacing bulky electrolytic capacitors in capacitor-supported power electronic systems with auxiliary source circuits. DC-BUS capacitors are widely used in grid-tied power converters (rectifiers) and utilized for power balance, voltage ripple limitation, and short-term energy storage. The electrolyte capacitor is the Achilles heel of any rectifier and power converter due to its higher rate of failure than other circuitry components. Auxiliary source circuits are key components to qualitatively improve the reliability of the DC links, where they divert the instantaneous pulsating power into extra reliable storage components. Unlike previous work, this review serves to provide a clear picture of an auxiliary source circuit design, in favor of optimal solution selection according to the specific application. Therefore, energy storage components (capacitors), topologies, and control strategies of auxiliary source circuits are comprehensively reviewed in this paper. Additionally, detailed explanations, comparisons, and discussions of auxiliary source circuits are offered.

Keywords: rectifiers; auxiliary source circuit; electronic capacitor

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1. Introduction

Grid-tied power converters produce a predetermined current shape that fulfills standardization requirements for appropriate power quality [1,2]. As a result, the rectified output voltage is forced to contain two different current components: dynamic and static. Moreover, loads that are connected through the interfacing converter can also consume two similar power components: average and pulsating. Because the loads on average consume constant power, while the grid supplies pulsating power, a buffer is required to stabilize the power equation.

In general, a common energy conversion from the grid to the load is performed by two-stage converters: a first-stage interface converter (FSIC) and a second-stage interface converter (SSIC). A bulky capacitor is employed as the buffer to ensure the equality of input/output power balancing. Furthermore, in [3,4], it was shown that capacitive impedance is advantageous in terms of power quality and grid stability. Therefore, adding a bulky electrolytic capacitor to the DC-BUS terminals is the commonly implemented solution [5]. The use of capacitors/passive elements is inevitable in power rectification systems to maintain proper functionality. Figure 1 shows the presently common topology for a generalized two-stage, grid-connected power conversion system, with a bulky electrolyte capacitor (BEC) on the DC-BUS terminals. I' and V' represent the current and voltage of the

SSIC, respectively. The energy flow direction across the SSIC is bidirectional, for example, in cases when a typical load or a solar panel is connected to the power grid.

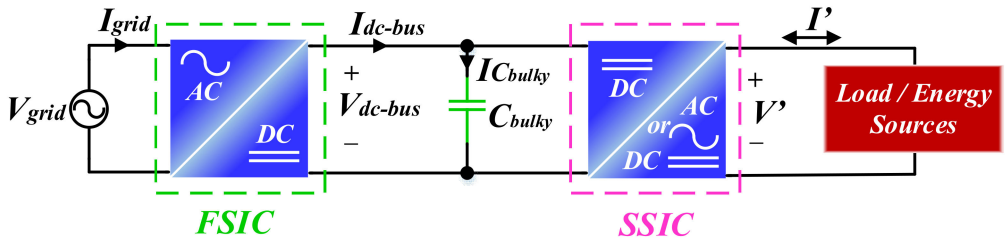

Figure 1. Generalized two-stage, grid-connected power conversion system, electrolyte capacitor-based.

The compulsory power quality requirement from grid-tied rectifiers creates a low-frequency voltage ripple (VR) at the DC-BUS capacitors. The undesirable VR leads to inferior converter performance [6] by increasing voltage fluctuations, reducing the harvesting efficiency of the photovoltaic (PV) panels [7], intensifying LED flicker (lighting applications) [8–10], overheating and reducing the batteries' lifespan [11,12], and, most importantly, by shortening the electrolytic capacitor's lifetime. The major advantage of an electrolytic capacitor over other types, such as film, ceramic, and tantalum, is their higher volumetric energy density. It is often the preferred choice in power electronics applications, where high capacitance and compactness are important [13].

Unfortunately, the BECs usually comprise the system's drawbacks in terms of reliability, lifetime, weight, and size [14]. Therefore, it is imperative to preserve the VR within the predetermined limits to avoid damaging the DC-BUS capacitors or exceeding the SSIC input limits. The VRs are correlated with the power conversion system rating and uncorrelated with the DC-BUS capacitance; by increasing the capacitor value, the VR can be reduced. The multiplicity faults in the BEC occur for two main reasons: (a) voltage fluctuation sensitivity, with emphasis on peak voltage (forced to use 90% of the maximum voltage value) and (b) temperature rise sensitivity (e.g., a drop of 10 degrees doubles the capacitor's lifespan). In addition, due to the capacitor temperature rise, numerous faults are created in other electronic components in its environment, hence the need to implement a suitable replacement for BECs in power converters.

Most of the methods currently used as a suitable replacement for BECs are based on adding an auxiliary source circuit (ASC) that imitates the dynamic capacitor behavior [15]. A virtual capacitor with an infinite capacitance range (as far as possible) can be obtained by replacing the electrolyte capacitor with an ASC unit based on an appropriate control strategy (Section 3). The ASC is based on a bidirectional DC/DC converter [16] and auxiliary capacitor "C_A" (nonelectrolyte technology) with a small capacitance value (smaller by several orders of magnitude than an electrolyte capacitor). The currently common topologies for integrating an ASC unit with a generalized two-stage, grid-tied power conversion system is a series connection with the converter/capacitor side and shunt connection, as presented in Figure 2. The main gap between the topologies is the absence of a DC-BUS capacitor "C" in the shunt connection; this approach allows to replace the DC-BUS capacitor with an ASC (extended explanation in Section 3).

Despite the electrolyte capacitor benefits mentioned above, the equivalent series resistance (ESR) of a film capacitor is invariably lower than the ESR of an electrolytic one across the entire frequency range. In addition, the ESR value of the electrolyte capacitor is significantly decreased as the temperature rises (much more than that of the film capacitor). Moreover, the evaluation confirms that film capacitor utilization yields benefits in terms of improved power density, reduced power losses, low parasitic inductance, and extended lifetime compared to an electrolyte capacitor [17–19]. As a result, the most popular capacitor technology for the auxiliary capacitor implemented in an ASC is a small film capacitor [20]. Therefore, to achieve optimal design (high reliability, reduced temperature sensitivity, longer lifespan, and smaller physical size) for power conversion systems, the electrolyte

capacitor can be replaced with an ASC unit (based on a film capacitor with a much lower capacitance value compared to the electrolyte). Hence, the ASC unit allows limiting the steady-state DC-BUS VRs while reducing the utilized capacitance [21].

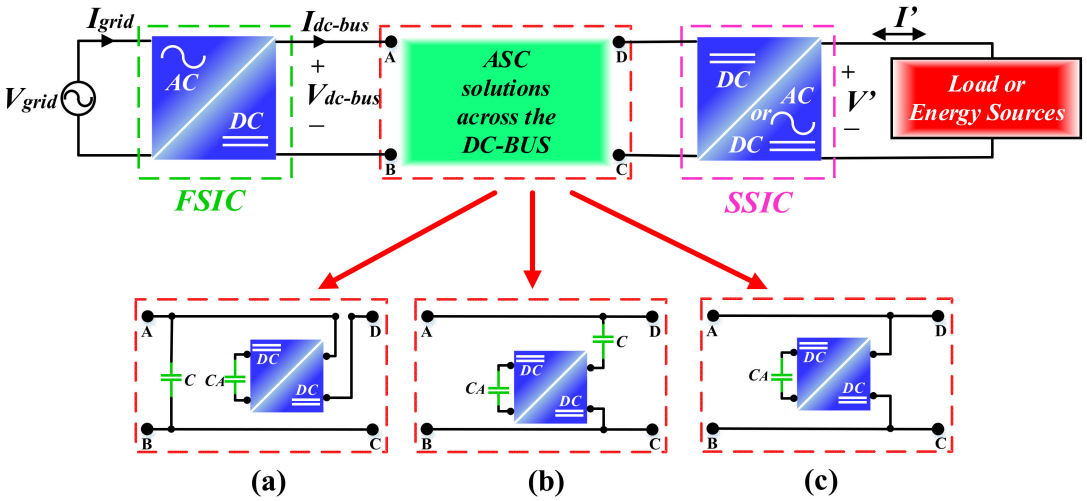

Figure 2. Generalized two-stage, grid-connected ASC-based power conversion system: (**a**) series connection with the converter side; (**b**) series connection with the capacitor side; (**c**) shunt connection.

In this paper, a comprehensive review of ASC-typical capacitors, topologies, and control strategies is presented. The literature presents several solutions to these challenges, and some review reports have been made as mentioned in the introduction. Nonetheless, to achieve a wide range of optimal solutions, it is necessary to introduce a clear picture for all questions in the ASC design process. The ASC design process includes three main considerations: the selection of an energy storage source, topology, and control strategy. The effort to overcome the above challenges is divided into three steps: (a) selecting an optimal DC-BUS capacitor (according to source/load conditions); (b) choosing a suitable topology for implementing an ASC in a power conversion system; and (c) determining an appropriate smart control technique for implementing the strategy according to the system requirements. Therefore, this paper presents a comprehensive overview focused on the following subjects: Section 1 introduces the problems and challenges of a power conversion system based on an electrolytic capacitor. Next, Section 2 presents an extensive overview and discussion on typical capacitors (electrolytic, ceramic, and film) for applications in power conversion systems (with performance comparison). In Section 3, common control strategies for reducing DC-BUS capacitance in circuit applications are classified, presenting control techniques and detailing advantages/disadvantages accordingly. Then, in Section 4, the available ASCs are investigated with a detailed analysis and comparison; in addition, the alternative approaches are further discussed and evaluated to select the most suitable topologies for future capacitor-supported power conversion systems. Some conclusions are drawn in Section 5.

2. DC-BUS Capacitors

2.1. Common Types of DC-BUS Capacitors

A major requirement of the power converter is to employ capacitors on DC-BUS terminals for a variety of reasons, such as input/output power balancing, harmonics absorption, short-term period energy storage, and suppressing the VR [22–25]. Capacitor utilization is most common in power conversion systems, such as off-line converters, lighting drivers, full/hybrid electric propulsion systems [26], and a variety of renewable-energy applications [27]. The BEC is employed in a parallel connection to the DC-BUS terminals, as can be seen in Figure 1. When diagnosing the power converter's reliability, doubtlessly the weakest link in the conversion system is the electrolyte capacitor, due to its short lifespan and high degradation failure rate [28,29]. A detailed analysis of

power converters under DC-BUS capacitor failure and a presentation of their effect on inverter electrical characteristics was previously performed in [30]. Moreover, about 30% of power converter failures are caused by the deterioration of the capacitors [31], as can be seen in the failure distribution chart among major components shown in Figure 3a. However, the capacitor's environmental conditions can also intensify the degradation and increase the failure rate, as presented in the distribution chart of stress sources leading to failures in Figure 3b. Therefore, due to the high failure rate, power converter size limitations, and the surrounding environmental conditions (e.g., high humidity, high ambient temperature, etc.), an optimal DC-BUS capacitor selection should be performed for power conversion systems [32].

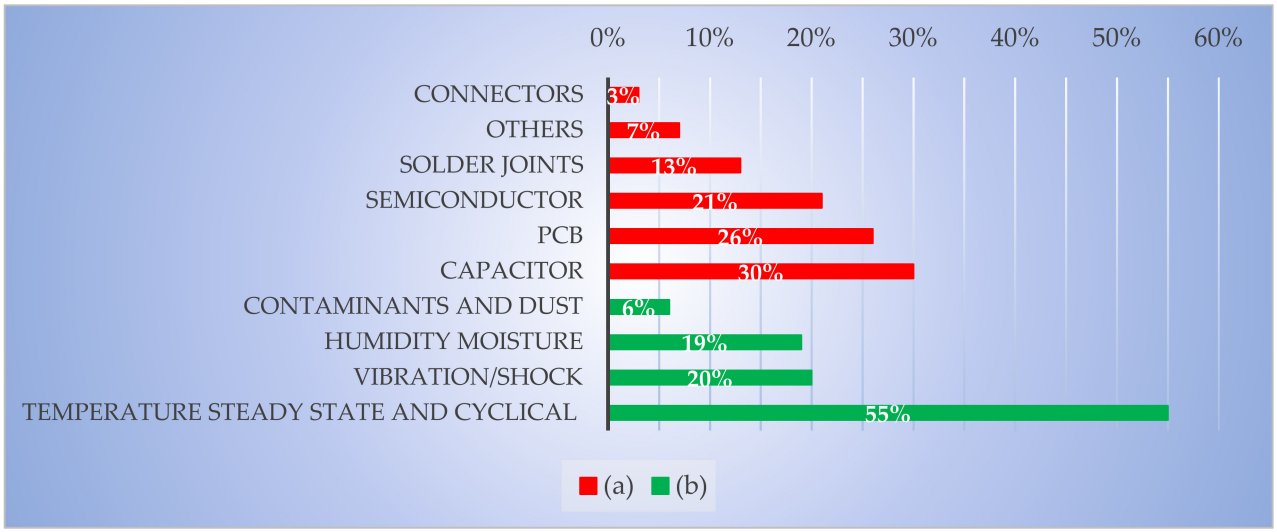

Figure 3. Analyses of failures in power conversion systems. (**a**) Failure distribution among the main components; (**b**) Source of failures.

An optimum DC-BUS capacitor selection means choosing such capacitors for power converters that provide a satisfactory solution to a variety of requirements, such as high reliability, lowest possible volume and/or weight, and minimal cost. Consequently, there is great importance placed on a preliminary analysis of the capacitor characteristics for optimal DC-BUS capacitor selection. The three most common types of capacitors for power converter applications discussed in this article are Aluminum Electrolytic Capacitors (AE-Cs), high-capacitance Multilayer Ceramic Capacitors (MLC-Cs), and Metallized Polypropylene Film Capacitors (MPF-Cs).

2.2. Preliminary Analysis of Capacitor Characteristics by Equivalent Circuit Model and Performance Comparison

A preliminary analysis of capacitor characteristics begins with characterizing a simple tantamount electrical circuit model that describes the equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C) that represent the capacitor's respective physical characteristics [33]. The equivalent circuit model design depends on the type of capacitor, where there is a difference among the cases AE-C, MLC-C, and MPF-C as described in Figure 4. In addition, the equivalent circuit model also represents the insulation resistance R_i (usually large), dielectric loss R_d (significant at high frequencies), and inherent dielectric absorption C_d (only significant in electrolytic capacitors). According to the equivalent circuit model, the capacitor impedance equation can be represented as:

$$|Z_{cap}| = |R + jX| = \sqrt{ESR^2 + \left(2\pi f ESL - \frac{1}{2\pi f C}\right)^2} \quad (1)$$

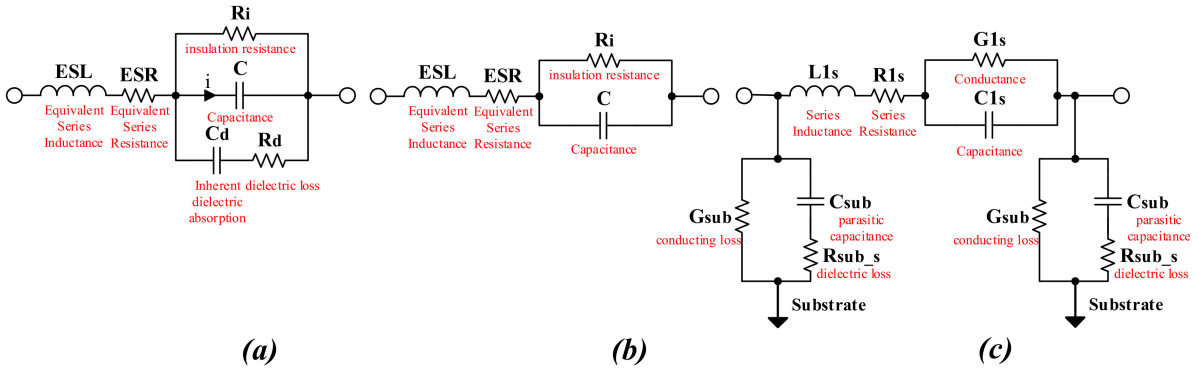

Figure 4. Equivalent circuit model of a capacitor: (**a**) AE-C; (**b**) MPF-C; and (**c**) MLC-C.

A typical structure of an MLC-C comprises vertically stacked internal electrodes that form capacitive layers with dielectric substrate, and therefore the MLC-C-equivalent circuit model is different from the AE-C/MPF-C. The equivalent circuit model can be depicted as a π-model, which includes a total series impedance and two parallel impedances at each port output that have a common reference point as shown in Figure 4c. At the series impedance case (very similar to the case of a single layer), $R1s$, $L1s$, $C1s$, and $G1s$ represent the total series resistance, inductance, capacitance, and conductance, respectively. In the parallel impedance case, the shunt effect between the capacitor and substrate (a major factor for the substrate effect) should be considered when placing the MLC-C on a board [34]. Therefore, the parallel impedance contains the resistance R_{subs} in series, substrate capacitance C_{sub}, and the conductance G_{sub}. Where R_{subs} represents a dielectric loss of bound electrons, the parasitic capacitance of the substrate and a small conducting loss of free electrons are referred to as C_{sub} and G_{sub}, respectively. Note that the paper presents a simple MLC-C first-order model and not a second-order model to avoid very laborious and cumbersome mathematical consequences.

The capacitor's impedance vs frequency is a key parameter when designing a capacitor according to the application conditions. Therefore, based on an equivalent circuit model (Figure 4), a frequency response comparison of a 1 uF capacitor was performed among three cases: AE-C, MPF-C, and MLC-C as shown in Figure 5. The ESL value is generally neglected at lower frequencies (ωL is small), below the self-resonant frequency, which is given by

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

Therefore, at low frequencies, the negative slope of Z is due to the dominance of the capacitive component ($Z \approx \frac{1}{2\pi fC}$), termed as the capacitance component region. At the resistance component region (termed as resonance region), Z is represented by the ohmic resistance ($Z \approx ESR$) only, and at higher frequencies, the inductive reactance begins to dominate ($Z \approx 2\pi fESL$) that is termed as the inductance component region. Admittedly, in some cases, the simple electric capacitor model is not accurate enough (a significant factor in lifespan prediction and capacitor reliability). Therefore, if the goal of the design is to achieve an accurate model of the electrical capacitor as closely as possible, the parameter values of the capacitor model (resistance, capacitance, and inductance) are no longer constant values; these values should vary depending on environmental (humidity, temperature, etc.) and operating (current ripple, voltage stress, etc.) conditions.

When comparing the advantages and disadvantages among different types of capacitors, the first and most important factor to consider is the limit of storable energy (W_V) per volume (in dielectric material). Equation (3) introduces the storable energy limit in a capacitor where E_{max} is the maximum operating field strength, and ε_r is the relative

permittivity. Hence, the values of ε_r and E_{max} (dielectric material properties) are a major factor influencing the limit of storable energy per volume.

$$W_V = \frac{\varepsilon_0 \varepsilon_r E_{max}^2}{2} \tag{3}$$

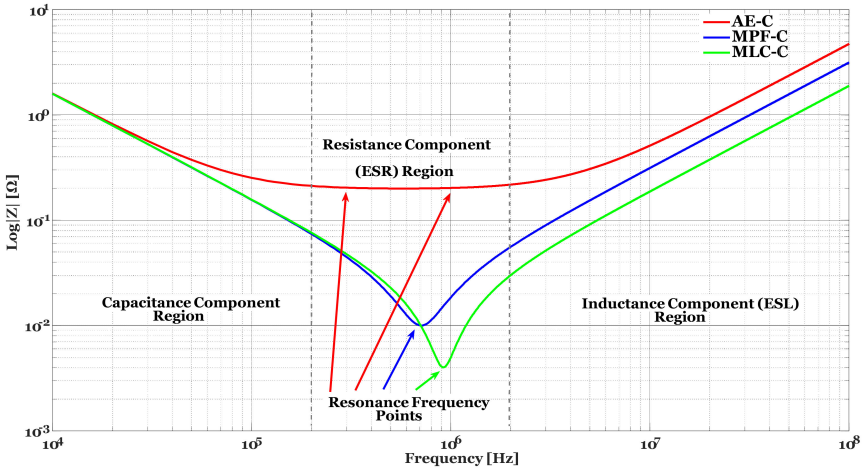

Figure 5. Frequency response of various types of 1µF 450V capacitors.

Figure 6 shows a diagram depicting the energy storage density values for various common dielectrics depending on relative permittivity and operating field strength [35]. From the energy storage density diagram, it can be clearly seen that AI_2O_3 (AE-C material) has the highest energy density, in the range of $10\left[\mathrm{J/cm^3}\right]$ (theoretical limit) to $2\left[\mathrm{J/cm^3}\right]$ (commercially available limit). AE-C has this significant advantage, due to the high relative permittivity (10) and the highest field strength between 200 and $600[\mathrm{V/\mu m}]$. Despite this, polypropylene (MPF-C) contains a high-field strength of 200 $[\mathrm{V/\mu m}]$, but on the other hand, suffers from very low relative permittivity compared to ceramics (1500). Following the advantage (highest relative permittivity) that ceramic (MLC-C) has, it suffers from the lowest field strength, so the energy storage density of the ceramics and the polypropylene is almost equivalent, about $\sim 0.2\left[\mathrm{J/cm^3}\right]$. Note that the biaxial-oriented polypropylene is the favored film material for applications above 250 V.

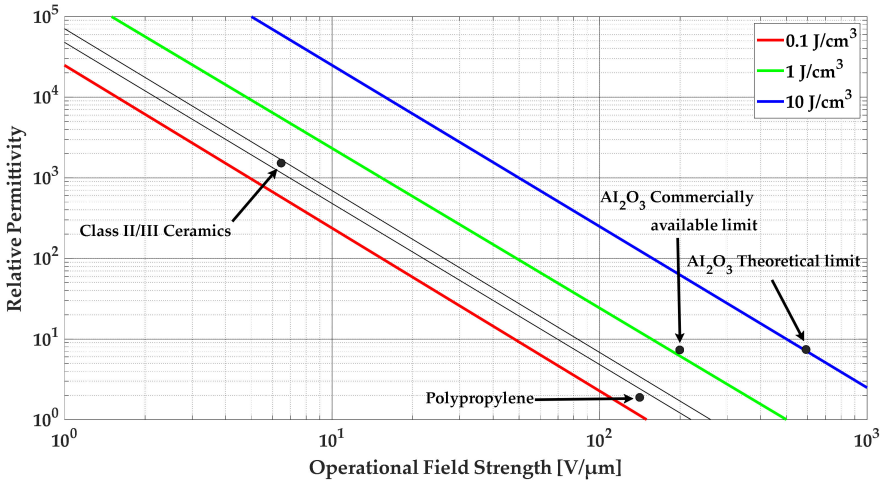

Figure 6. Energy storage density for various dielectrics.

Table 1 shows relative performance comparisons of the three main capacitor types, AE-C, MPF-C, and MLC, for DC-BUS applications [36]. For example, as mentioned above, AI_2O_3 has the highest energy density (up to about 2 $\left[\mathrm{J/cm^3}\right]$); therefore, it has the highest capacitance per volume among the three. In addition, it also has the lowest cost per

joule, but unfortunately, due to electrolyte evaporation, it suffers from low reliability; moreover, due to high-temperature sensitivity, it also suffers from relatively high ESR and low ripple current ratings (typical $20[\mathrm{mA}/\mu\mathrm{F}]$). Another disadvantage of the electrolyte is a low voltage rating (maximum 500–600 V) compared to MPF-C (from a low voltage to 50 kV) as can be seen in Figure 7. The capacitance range vs voltage range plot is an important parameter when choosing a capacitor according to a specific application, while the voltage and capacitance correlate with the physical size and cost. MPF-C presents the optimal parameters of all three types (mentioned above) in terms of the lowest ESR, lowest current ripples (typical 1 $[\mathrm{A}/\mu\mathrm{F}]$), and well-balanced performance for high-voltage applications. Despite a lower financial cost and relatively high capacitance (compared to MLC-C), it is limited to a moderate upper operating temperature, unlike the ceramic capacitor. Other advantages of MPF-C are high reliability and the highest flexibility in device geometry among all capacitor technologies, yet it suffers from a large volume problem due to the lowest energy density (up to about $0.15[\mathrm{J}/\mathrm{cm}^3]$) of the three types. MLC-C offers a high reliability, a wider frequency range (compared to AI_2O_3), and the highest operating temperatures (up to about 200 C°) of all three types. Although MLC-C offers lower ESR and current ripples (compared to AI_2O_3), ceramic capacitors have a much lower energy density than electrolyte capacitators (up to about 0.2 $[\mathrm{J}/\mathrm{cm}^3]$). However, the major disadvantages of the MLC-C are the high financial costs and mechanical sensitivity; these drawbacks are intensified in high-voltage applications.

Table 1. Relative performance comparisons of the three main types of capacitors for DC-BUS applications.

Type	Reliability	Frequency	Ripple Current Capability	ESR	Energy Density	Temperature	Voltage	Cost Effective	Capacitance
AE-C	Poor	Poor	Poor	Poor	Excellent	Intermediate	Intermediate	Excellent	Excellent
MPF-C	Excellent	Excellent	Excellent	Excellent	Poor	Poor	Excellent	Intermediate	Intermediate
MLC-C	Excellent	Excellent	Intermediate	Intermediate	Intermediate	Excellent	Poor	Poor	Poor

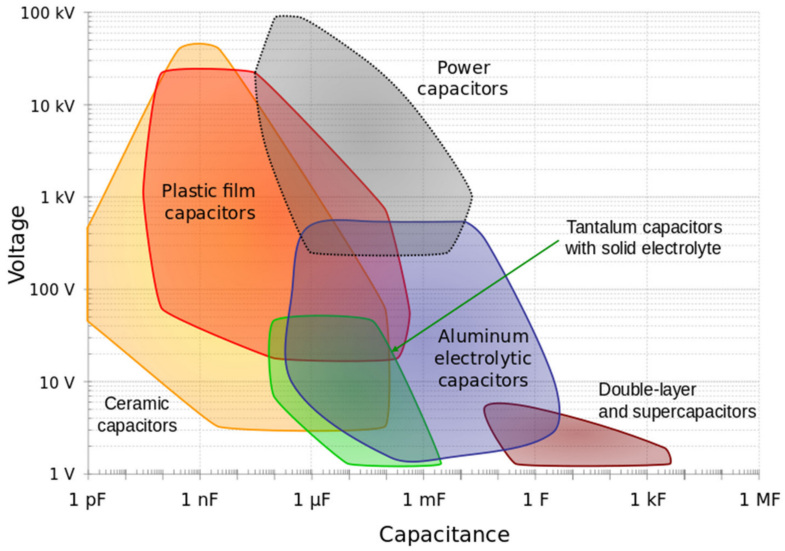

Figure 7. Capacitance ranges vs voltage ranges of different capacitor types [37].

3. Common Techniques for DC-BUS Capacitance Reduction Circuit Applications in Capacitor-Supported Power Conversion Systems

3.1. Introduction to DC-BUS Capacitance Reduction Circuit Applications

After presenting the problem of using electrolytic technology in power conversion systems in Section 1 and then equalizing the performance among the different capacitor technologies in Section 2, this section discusses common topologies and control strategies for DC-BUS capacitance reduction circuit applications and the replacement of electrolytic capacitors with other capacitor technologies. Many attempts to reduce DC-BUS capacitance

and replace electrolytic capacitors are described in the literature. The approaches available in the literature for resolving the electrolyte capacitor issue of power converters and achieving capacitance reduction are shown in Figure 8. The most common solutions are (1) compromise of converter performance, (2) DC-BUS capacitance distribution, (3) ASC addition DC-BUS case, series connection with the converter side, (4) ASC addition DC-BUS case, series connection with the capacitor side, (5) ASC addition DC-BUS case, shunt connection, (6) ASC addition AC case, series connection, and (7) ASC addition AC case, shunt connection. The following is a brief description of the above techniques.

1. Compromise of converter performance: The converter performance is determined by an optimizing process of the DC-BUS capacitor selection shown in [38]. The maximum allowable DC-BUS VRs are then calculated for different types of applications as shown in [39–41], and thus by enhancing VRs over a DC-BUS, capacitance reduction can be achieved. However, this technique is less common due to its suitability for very specific applications that are not sensitive to increased VRs. Applying this technique in systems sensitive to VRs will directly cause a decrease in system performance and may even cause damage; therefore, this technique is not discussed in this paper.
2. DC-BUS capacitance distribution: the DC-BUS capacitance can be divided by an asymmetrical split of the DC-BUS capacitor into two smaller capacitors with a common connection point. The method is based on power flow routing control from the DC-BUS or AC grid to the capacitors by DC–DC converters. This technique is similar to the active capacitor equalization process [42–44].
3. ASC addition DC-BUS case, series connection with the converter side: the topology concept is based on introducing an energy source in series with the DC-BUS to compensate the VR on the DC-BUS capacitor and make the output voltage have a near-zero ripple by directing the pulsating portion of the instantaneous force into the auxiliary capacitor (C_A) [45,46]. Thus, the total required capacity is reduced, and electrolytic capacitors can be substituted by alternatives with an extended lifetime and compatible or reduced volume and cost. The ASC connection is implemented by a bidirectional DC-BUS converter and ends with an auxiliary capacitor with a capacitance value significantly smaller than the required DC-BUS BEC (C_B).
4. ASC addition DC-BUS case, series connection with the capacitor side: The ASC unit is based on the same principle as the previous solution. However, the main difference among the methods is that in this case, the ASC unit is located in series connection with the DC capacitor across the DC-BUS [47,48]. Therefore, unlike the previous solution, the voltage ripple is reduced on both sides of the DC-BUS (AC/DC or DC/AC side). The ASC unit can be applied in full-bridge topology [49] or as a hybrid filter [50,51].
5. ASC addition DC-BUS case, shunt connection: this case is based on the same concept as the above technique, except for the ASC connection topology. The technique offers a shunt connection between the bidirectional DC–DC converter and the DC-BUS. Furthermore, in this case, at the converter output ports, there is an auxiliary capacitor (C_A) with a capacitance value significantly smaller than the required DC-BUS BEC (C_B) [52–58].
6. ASC addition AC case, series connection: In this case, the topology concept is based on introducing an energy source in series with the AC side, as shown in [59]. Similar to the DC-BUS case (converter side), this topology allows control of the VRs of the DC-BUS capacitor (by routing the energy flow across the capacitor) [60]. As a result, the DC-BUS capacitance requirement can be reduced, and a different type of DC-BUS capacitor can even be used, such as film or ceramic. Nevertheless, this solution is less popular and therefore not discussed in this paper.
7. ASC addition AC case, shunt connection: This solution introduces ASC integration in a parallel connection across the AC line [61]. The major benefit of this strategy is the achieved excellent simplicity to performance ratio, because no complex current reference computations are required. However, as in the previous case, this strategy is also unpopular and therefore not discussed in this paper.

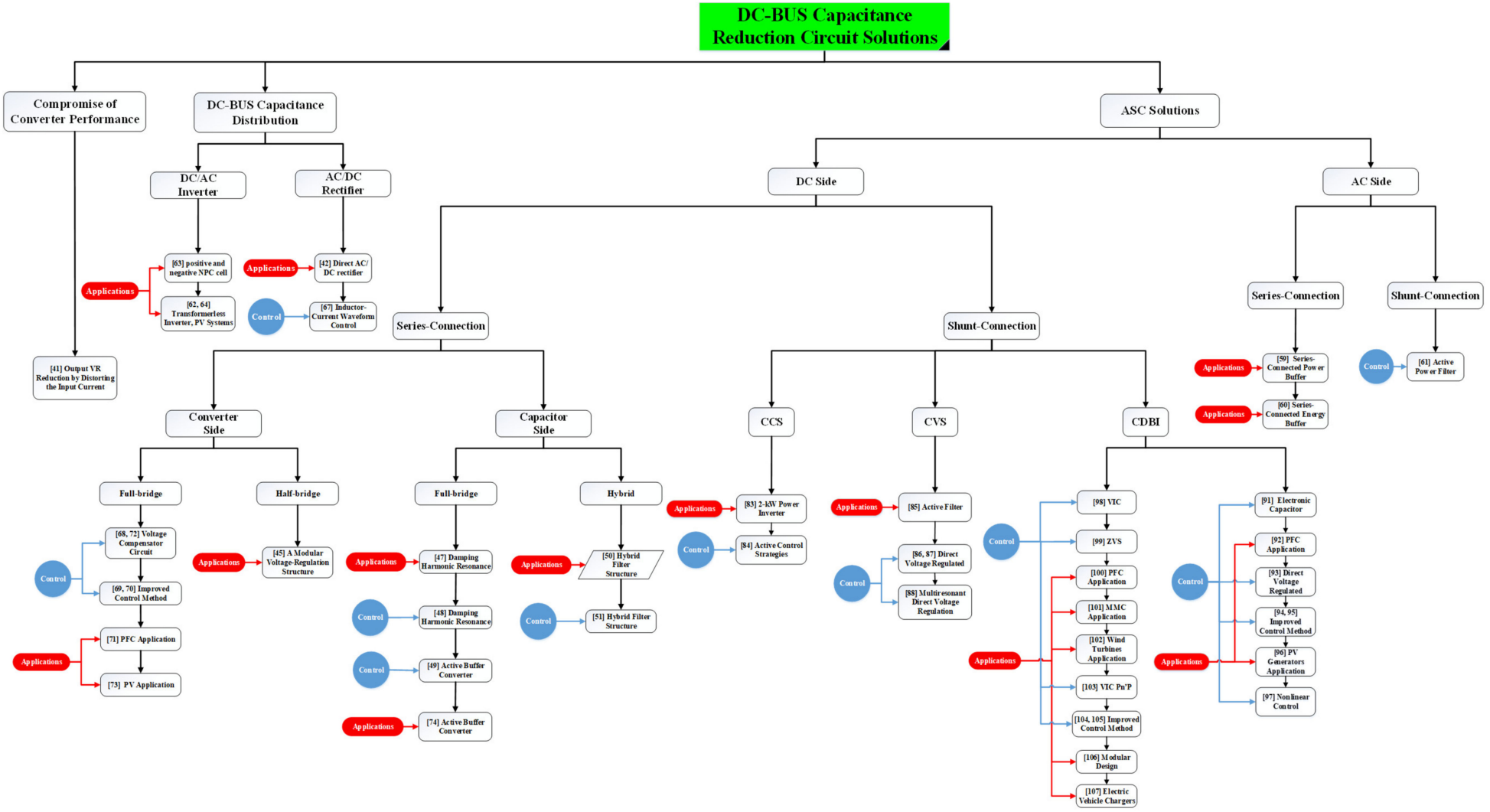

Figure 8. DC-BUS capacitance reduction circuit solution.

The following subsections present an extensive breakdown of each technique separately, including an analysis of the most common control strategies for each topology, each technique's advantages/disadvantages, and a summary.

3.2. DC-BUS Capacitance Distribution

3.2.1. DC-BUS Capacitance Reduction Circuit Applications in a DC–AC Inverter System

One of the methods for significantly reducing the DC-BUS capacitance requirement for DC/AC inverter applications is to split the DC-BUS BEC into two symmetrical capacitors and insert a common-mode (CM) conducting path into the converter's neutral point. The technique is very common among energy conversion system applications between PV panels and the AC grid [62,63]. Efficient use of the CM path opens the possibility of controlling the injection of CM voltages (CM_V) into the output filter capacitors, and thus a power oscillation buffer (pulsed power) can be applied between the converter output and the DC-BUS as shown in Figure 9 [64]. An additional benefit of the CM conducting path method is that the ground leakage current can be sufficiently well eliminated by ground leakage current control (enabled by the PV to ground parasitic capacitance). The topology is based on the introduction of new freewheeling routes into the converter; thus, the source chassis (e.g., PV panel) can be isolated from the output (e.g., AC grid) during freewheeling modes. This could be accomplished by interrupting the CM_i conducting path when zero voltage vectors are employed to the full-bridge inverter either on the DC or AC side. However, the advantage of the ground leakage current control does not contribute to reducing DC-BUS capacitance and therefore is not detailed here.

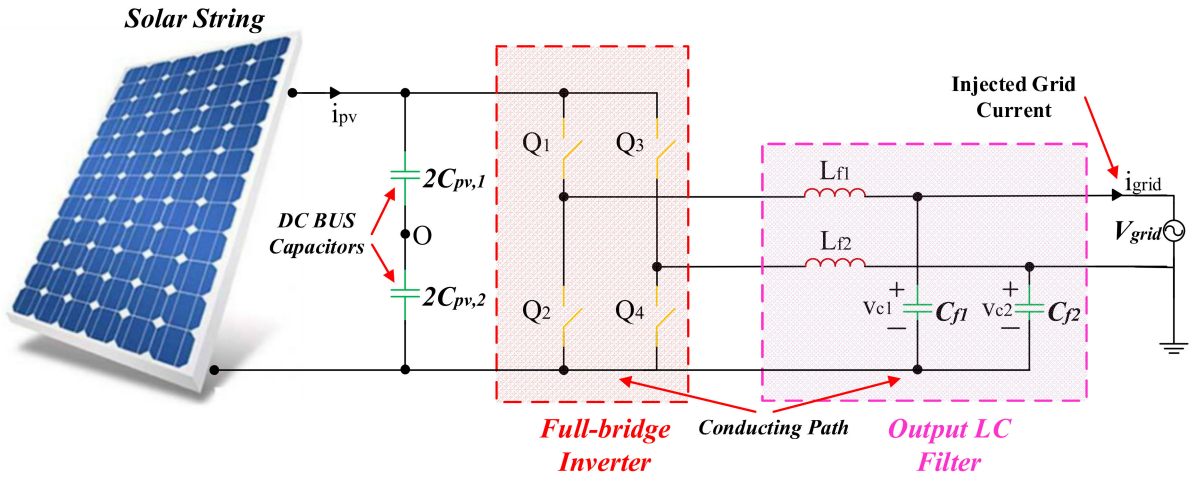

Figure 9. Common-mode path implementation for transformerless inverter for grid-connected PV systems.

The main advantage of this method is the ability to uncouple the well-known double-line-frequency pulsating power (that originated from the AC side) by further injection of CM_V into the output filter capacitors. By this disconnection, the DC-BUS will not sense the second-order pulsating power, and the DC-BUS capacitance requirement will be significantly reduced. In such a case, the requirements for filtering the DC-BUS are increased compared to a standard H-bridge inverter due to the CM_V injection, and this directly affects the filter capacitance value. Descriptively, if the compensation voltage factor (V_{comp}) is satisfied, the second-order pulsating power in the AC network should be well filtered by the filter capacitors C_{f1} and C_{f2}; thus the DC-BUS will not sense these power pulses. However, although the compensation voltage factor can be provided (theoretically), it remains impossible to decouple the entire AC grid-pulsating power, because the fourth-order harmony is added due to the computational interaction between the capacitor voltages and the current's second-order terms. In addition, some other disturbances, such as passive component ESR, variation of the inductance and capacitance, internal filter pulsating

power (due to the inductors), and distortions caused by dead time, are not calculated by this method. Therefore, it could be determined that a residual power ripple appears at the DC-BUS of the PV inverter, and the elimination of fluctuating power is incomplete. Undoubtedly, the advantage of this method is that it requires no auxiliary converter (or any switching components) and has a simple circuit configuration, while the main disadvantage of the method is the necessity for an additional current sensor, which makes plug-and-play operation inapplicable.

3.2.2. DC-BUS Capacitance Reduction Circuit Applications in AC–DC Rectifier System

One of the common methods for direct rectification applications from the mains to DC-BUS is a direct AC/DC differential rectifier that does not use an electrolytic capacitor and has a mitigated low-frequency ripple [65,66]. The presented technique is based on a single-stage direct AC/DC rectifier with no need of an electrolytic capacitor, by using inductor current waveform control methodology [67]. The concept is based on two bidirectional DC/DC converters for AC/DC rectifiers replacing a standard PFC converter. The bidirectional DC/DC converters are series-connected at the input terminal, while the output nodes are in parallel connection to the DC-BUS. In this topology, the electrolytic capacitor was replaced by two capacitors C_1 and C_2, while their voltage drop has an opposing polarity (V_{c1} and V_{c2}, respectively), and the difference is a pure sinusoidal waveform that follows the input AC source shape.

The presented topology utilizes two bidirectional buck–boost power converters connected in the differential configuration as shown in Figure 10; nevertheless, a variety of converters, such as buck–boost, flyback, push–pull, and forward, can also be suitable here. The upper buck–boost is formed by C_1, Q_1, Q_2, and L_1 (upper side), and the lower converter is formed by C_2, Q_3, Q_4, and L_2 (lower side). In a complete AC cycle, the four feasible states ($S_1 - S_4$) of the buck–boost differential are applied to switches $Q_1 - Q_4$. The switch state operation is as follows: S_1: Q_1 OFF; Q_2 ON; Q_3 OFF; and Q_4 ON where S_3 is its reverse state of S_1. In states S_2: Q_1 OFF; Q_2 ON; Q_3 ON; and Q_4 OFF where S_4 is its reverse state of S_2. The operation of the buck differential rectifier is as follows: In the positive half cycle, the possible states are S_1, S_2, and S_3; and in the negative half cycle, the potential conditions are S_1, S_3, and S_4. The presented method is aimed to mitigate the unbalanced instantaneous double-line-frequency input power with the constant output power demand. For example, in the positive half cycle, the upper buck–boost converter delivers more power than required at the dc side. To maintain constant output power, the superfluous energy is accumulated in C_2. Thus, the lower buck–boost converter is only sinking power from the DC-BUS side (Q_1 ON, Q_3 ON, and S_3 modes). This process applies to both half-cycle modes (positive and negative) in the same way and is physically inevitable.

For the presented differential rectifier system, a general control technique for mitigating the double-line-frequency power at the DC side of the circuit for implementing a free electrolytic capacitor system is proposed. Due to the series connection of C_1 and C_2, their differential voltage is equal to the AC line voltage $v_{ac}(t) = v_{c1}(t) - v_{c2}(t) = V_m \sin(\omega t)$. In this case, the output current $i_o(t)$ will contain a double-line-frequency component $i_{o(2\omega)}$. Thus, the input capacitors C_1 and C_2 filter only the high-frequency harmonics. When expending the control bandwidth to cover the double-line-pulsating power, the capacitors can filter it too; hence, the DC line capacitance could be reduced. Consequently, the existing systems without any hardware modification prolong the system's lifetime by a slight change of the control methodology, which is a significant advantage of this method. Nevertheless, the fourth current component $i_{o(4\omega)}$ cannot be eliminated; this component will eventually manifest as output current ripples. However, because these current ripples are typically very low, only a small non-BEC is required for eliminating all ripple current harmonic components at the DC-BUS. The main disadvantage of this method is the multiplicity of the switching components and inductors. For example, a typical boost PFC converter is implemented by a single switch and inductor, instead of four switches and two inductors offered in the above method. This disadvantage can impair the converter's functionality in

a variety of ways, such as high cost, complexity of the power stage, and high probability of future failure due to increased switching components.

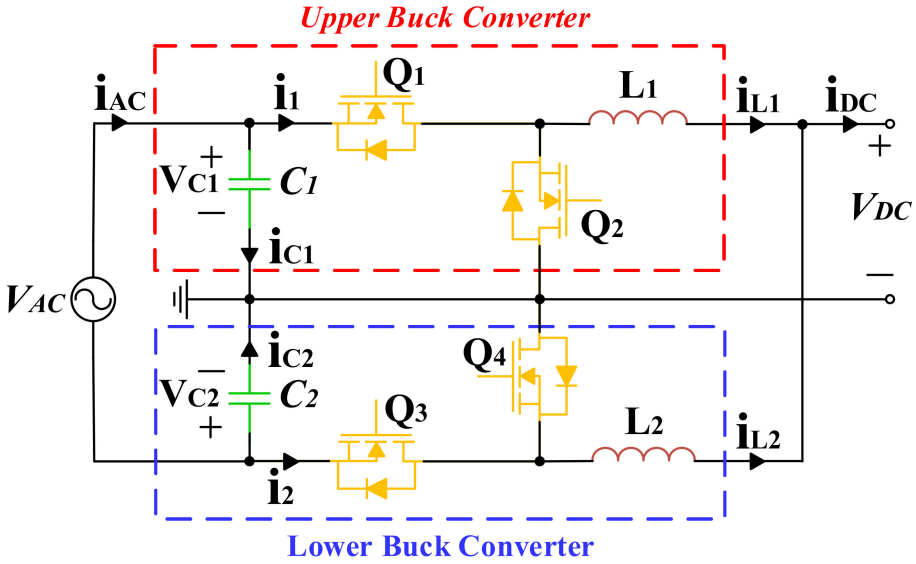

Figure 10. Two bidirectional buck-type differential rectifier configurations used for the inductor current waveform control.

3.3. ASC Addition DC-BUS Case, Series Connection with the Converter Side

An auxiliary voltage source in series connection with the DC-BUS is an applied technique for reducing the required capacitance of the power conversion system [68–70]. This method has been successfully implemented in typical PFC front-end power conversion systems [71]. The concept is based on connecting a serial voltage compensator circuit between the DC-BUS BEC and the load. By utilizing the voltage compensator circuit, the system energy storage is reduced, enabling to utilize lower capacity in a higher performance device. From a power-balancing point of view, the load current flows throughout the auxiliary circuit, where it processes only the reactive power, and the output terminal voltage is AC. Because the voltage compensator circuit processes small VR, the reactive power element has a low power rating. Therefore, the use of a voltage compensator circuit in general capacitor-supported power electronic systems has several major advantages, such as implementation that requires low-voltage devices only, ability to increase the VR in DC-BUS BECs (which is beneficial for power balancing between the line and load), and reduction of the DC-BUS capacitance requirements.

The basic concept of implementing a voltage compensator circuit for a typical energy conversion system [72] is illustrated in Figure 11a. The model consists of a DC-BUS shared by two cascade converters, where C is the capacitor, and V_{ab} represents the auxiliary voltage source as illustrated in the voltage compensator circuit. The capacitor voltage v_C can be separated into two parts: a constant voltage component V_C and a VR component Δv_c, where the capacitor ripple fluctuates at f_{rip}, and the peak to peak ripple is $2|\Delta v_c|$. The auxiliary voltage source (V_{ab}) is connected between the DC-BUS capacitor positive port and the SSIC positive node. The auxiliary voltage source produces a voltage opposite to the VR component of the DC-BUS capacitor where $V_{ab} = \Delta v_c$ (i.e., DV component tends to zero). At the nominal point, v_d has an identical average voltage value as at the DC-BUS capacitor (with zero VR). Therefore, a high VR across the DC-BUS capacitor C is allowed, indicating that the capacitor value can be reduced, but at the expense of increasing the magnitude of v_{ab}. Figure 11b illustrates the voltage compensator circuit, which is based on four low-voltage MOSFETs $Q_1 - Q_4$ and a DC–AC full-bridge inverter with an output filter $L_f - C_f$. The switch gate signals $PWM_1 \sim PWM_4$ in the full-bridge inverter are generated by a PWM. Depending on the type of DC source used, the control signal v_{con} is obtained by sensing different parameters. When utilizing the unidirectional current flow from the line

to the load, a couple of switches could be applied by diode (e.g., Q_2 and Q_3 or Q_1 and Q_4), as in a standard half-bridge circuit.

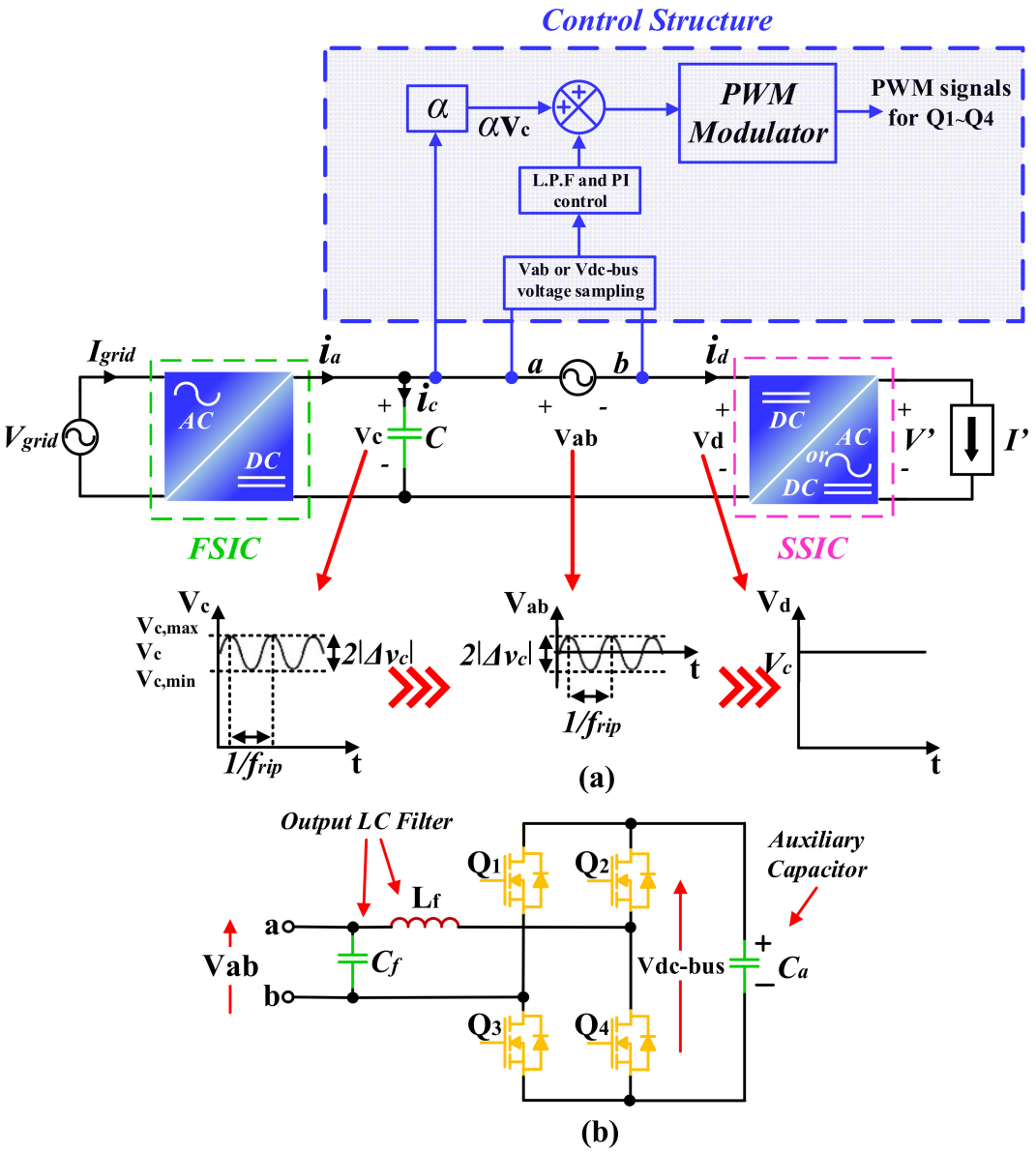

Figure 11. (**a**) Basic concept of implementing a voltage compensator circuit for typical energy conversion system; (**b**) Voltage compensator circuit.

A series auxiliary voltage source circuit can be integrated into a variety of capacitor-supported power electronic systems. A good example of adding an auxiliary source in series with the DC-BUS is the implementation of a voltage compensator circuit in photovoltaic (PV) systems. Figure 12a shows a circuit diagram of a grid-tied solar inverter with a series voltage compensator circuit for reducing the high-voltage DC-BUS capacitance based on a capacitor-supported full-bridge DC–AC converter. The voltage compensator circuit is connected in series to the DC-BUS (power processing side) between the input DC–DC boost converter (PV side) and output DC–AC inverter (grid side) [73]. The voltage compensator circuit, DC–DC boost converter, and the DC–AC inverter, are highlighted on the circuit diagram with red, green, and pink backgrounds, respectively. The compensator circuit generates an AC voltage that counteracts the VR on the output terminals of the boost converter. Therefore, the grid-tied inverter-supplied voltage is equal to the capacitor C_{dc-bus} average voltage. Thus, in this case, the compensator processes an AC power only,

which fluctuates at double the speed of the line frequency. The main controller interface (DSP-based) is presented in Figure 12b, where the subcontrol circuits of the PV boost converter, series voltage compensator circuit, and inverter are highlighted in green, red, and pink, respectively.

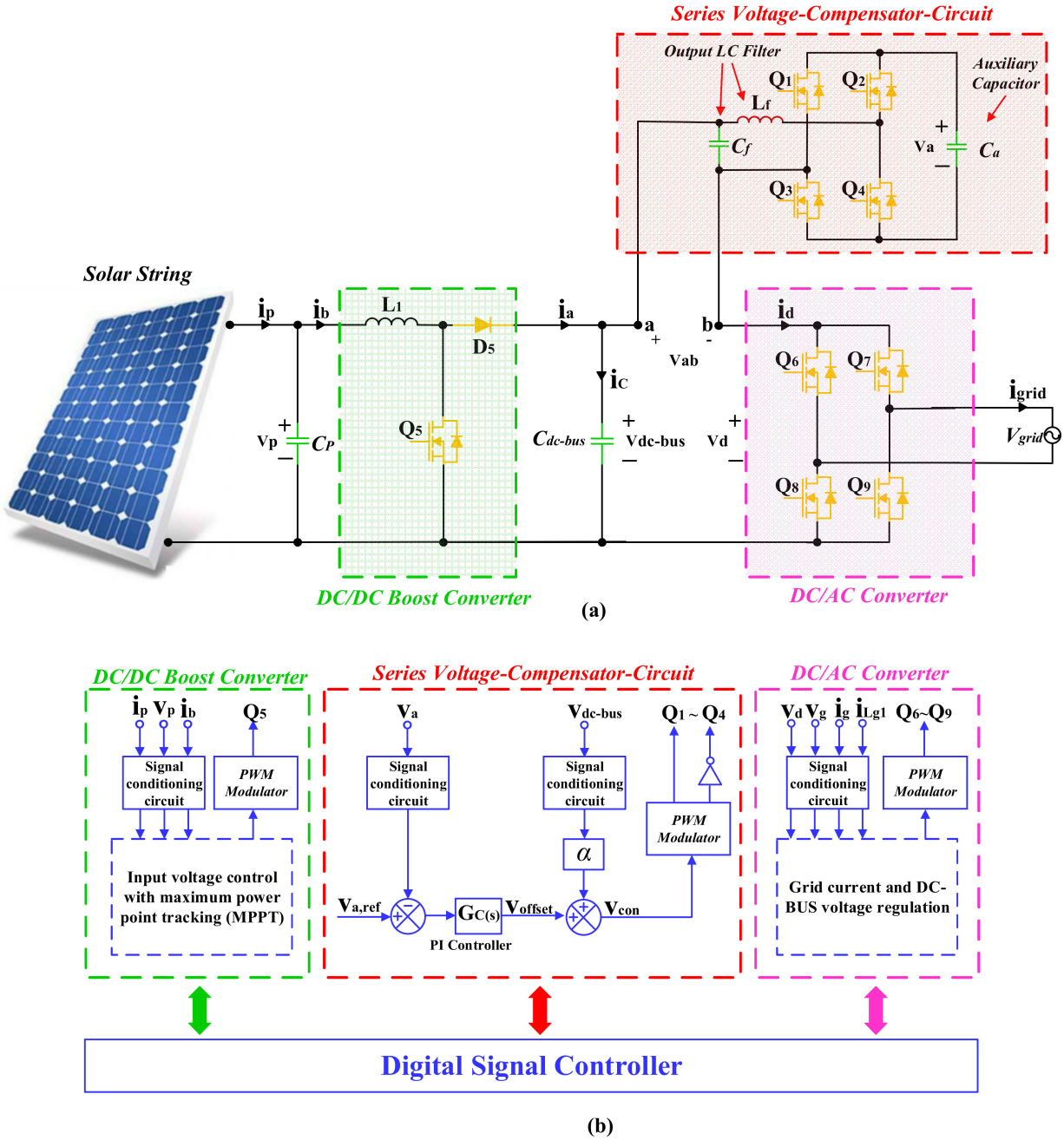

Figure 12. (**a**) Circuit diagram of a grid-tied solar inverter architecture with a series voltage compensator circuit; (**b**) Main controller interface structure (based on DSP).

The series voltage compensator control circuit operation is attached as follows: First, a sample of v_a (auxiliary capacitor voltage) and v_{dc-bus} (DC-BUS voltage) is performed, where α (scaling factor) is the ratio between the triangular carrier signal amplitude in the PWM modulator and $V_{a,ref}$; where $V_{a,ref}$ is the voltage reference for the input voltage compensator circuit V_{ab}. The PI controller (G_s) processes the gap between $V_{a,ref}$ and v_a to give an offset voltage v_{offset}; then, the v_{offset} and α signals undergo a summation operation, and a control signal v_{con} is obtained. At nominal operation, v_{offset} cancels v_{con} and the

αv_{dc-bus} DC component as $V_{offset} = -\alpha v_{dc-bus}$ (where V_{offset} expresses the DC component of v_{offset}, and where V_{dc-bus} expresses the DC component of v_{dc-bus}). The signal v_{con} is diverted to the PWM modulator and generates the voltage v_{ab} that has the same phase and amplitude as Δv_{dc-bus}, and finally the PWM signals are directed to switches $Q_1 \sim Q_4$. Note that for following the cancellation of the αv_{dc-bus} DC component, it is not necessary to use an HPF filter to isolate the AC component from v_{dc-bus}; consequently, by voltage control, a stable DC level of v_a can be achieved. Therefore, this control technique ensures that the voltage compensator circuit only handles the reactive power in the steady state, meaning v_{con} equals the conditioned AC component of αv_{dc-bus} in steady-state operation.

To summarize, the series voltage compensator circuit topology can be realized by a DC–AC converter with a full-bridge circuit; in the case of a unidirectional current flow of i_d, a half-bridge topology is an appropriate solution. In addition, the DC-BUS capacitor selection is no longer set by the VR value (ΔV_d), but instead by the designed allowable voltage stress on the auxiliary capacitor C_a. There are several options for DC-BUS capacitor selection in this configuration due to the DC-BUS capacitor's ability to withstand low-voltage stress. One of the alternatives is to utilize a long-life, high-ripple, low-voltage electrolyte capacitor because they are a very common and cost-effective solution. Another option is to employ a low-voltage film capacitor or ceramic capacitor tank. The main advantage of this technique is the that it allows to implement the auxiliary voltage compensator circuit with very low-voltage switching devices and passive elements, because the compensator processes small VR on the DC-BUS and therefore only the reactive power element. Another advantage of this technique is reducing the capacitance value, which correlates with the input–output power balancing; thus, the DC-BUS VR will increase. In addition, by the possibility of high VRs across C, the capacitance value can be reduced but at the expense of increasing the magnitude of v_{ab}. Despite the advantages mentioned above, this technique has several major drawbacks: (a) A simple fault in the voltage compensator circuit disables the entire system, due to the auxiliary converter's connection in series to the DC-BUS. This disadvantage significantly reduces the energy conversion system's reliability. System reliability is a key factor when designing an energy conversion system, and, as a result, this technique is not common in energy converter applications. (b) This technique is not applicable on existing grid-connected power conversion systems due to the series connection in the voltage compensator circuit, which requires some hardware modifications; thus, the plug-and-play operation cannot be applied. (c) Application complexity: due to the multiplicity of components, a more cumbersome structure and more complicated control circuit are obtained. (d) In the proposed arrangement, the voltage compensator circuit is located between the DC-BUS capacitor and one of the converters (FSIC or SSIC) only. Therefore, always one side is suffering from a lack of stress regulation. (e) Voltage swing limits across the capacitor due the converter (FSIC or SSIC) operating voltage.

3.4. ASC Addition DC-BUS Case, Series Connection with the Capacitor Side

As in the previous solution, the technique here is based on inserting an ASC into the DC-BUS by series connection topology, but the difference is in the ASC location. The above technique offers a series connection between the DC-BUS capacitor and the ASC unit as shown in Figure 13a. The research in [74] presents a high-power-density buffer with high-efficiency performance. This technique offers an appropriate solution to two main requirements when combining an ASC on the DC-BUS system (for pulsating power elimination): the first is energy storage capability and the second is DC voltage regulation. The DC-BUS capacitor energy storage problem arises due to a permissible VR limit on DC-BUS systems, and only a minimal part of the capacitor energy stored is utilized; e.g., for a 3% VR limitation across the DC-BUS, the energy buffering ratio is approximately 6%. Therefore, the first requirement solution is based on adding a DC/DC converter, which is a buffer between the auxiliary capacitor and the DC-BUS; thus, the auxiliary capacitor is no longer subject to the rigid limitations of VRs. Like the preceding case, the series connection benefit over the shunt connection (Section 3.5) is the ability to process only reactive power.

By processing a small VR only, the reactive power element has a low power rating, and the ASC unit can be applied by low-voltage devices. While the previous technique suffers from a reduced VR on just one DC-BUS side and voltage swing limits across the capacitor due to the converter operating voltage (FSIC or SSIC), this research presents an integrated solution to the above problems. By placing the ASC unit in a series connection with the DC capacitor across the DC-BUS, the problem of the reduced VR on only one side is solved, and the voltage swing limit problem is also solved directly due to the series connection topology.

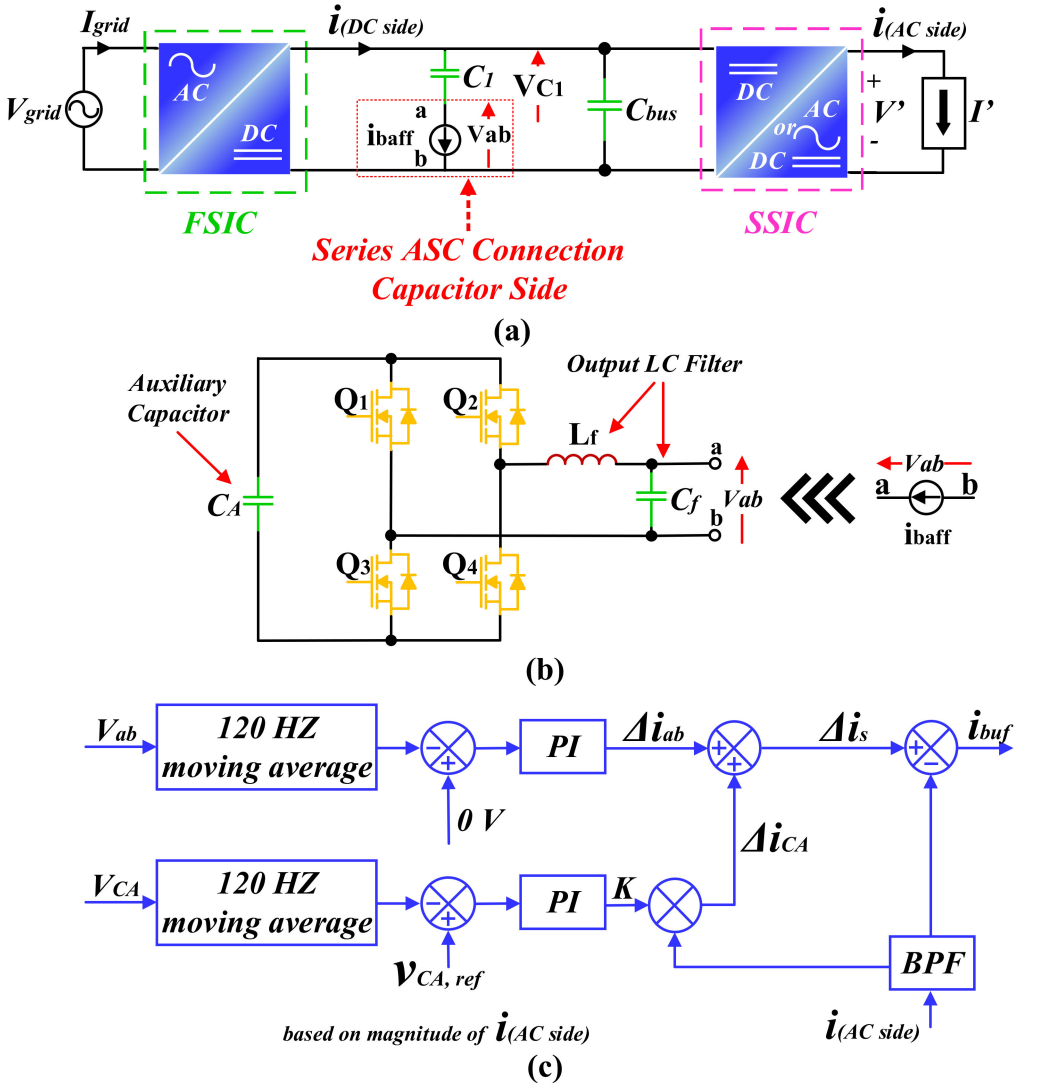

Figure 13. (**a**) Generalized two-stage, grid-connected power conversion system with inserted ASC unit series connection based at the capacitor side; (**b**) series connection ASC circuit; (**c**) controlled current source strategy for series connection topology.

The ASC unit is implemented as a bidirectional current source to balance the instantaneous current gap between the AC and the DC current and consists of a DC–DC -bridge converter ($Q_1 \sim Q_4$), inductor (L_f), capacitor (C_f) for filtration, and auxiliary capacitor (C_A) as shown in Figure 13b. C_{bus} is a small filter capacitor to absorb the switching transients; therefore, its effect is negligible. The bidirectional current source is stacked in series with the major energy storage capacitor C1; thus, it allows a relatively large VR over C1 to increase its energy utilization ratio. For example, instead of a maximum VR of 5~8% (a typical case of $V_{bus} = 400$ V) across C1, the VR can be increased to over 20% of the nominal voltage. For the ASC to behave like a current source, there is a need to design a current control strategy so that the V_{ab} will naturally vary contrarily to the variable voltage of C1

(i.e., $V_{C1} + V_{ab} =$ constant). In fact, because the sum of the instantaneous current gap of each double-line-frequency cycle is zero, automatic energy balancing is performed in each cycle, and the buffer converter does not need a C_A to fulfill its current source function. The control strategy purpose in this research is to force the ASC unit to behave as a controlled current source. Therefore, it is critical to precisely control i_{baff} (instantaneous current gap between the AC and the DC current) in order to keep the V_{DC-BUS} as constant as possible. The required i_{baff} value is equal to the AC component of the AC side, because $i_{DC\ side}$ and $i_{AC\ side}$ have the same average value. First, as shown in Figure 13c, the value of $i_{AC\ side}$ is measured and passes through a BPF (to obtain the double-line-frequency component only) to use as feedback for i_{baff}. The BPF can be divided into two parts: a digital moving average filter and LPF in the analog sensing circuit. To evaluate the DC component only, a microcontroller is used to obtain a moving average filter at 120 Hz (creates an HPF to eliminate the DC component), and the LPF in the analog sensing circuit is for filtering the SSIC switching ripples.

The insertion of an ASC in a series connection with the capacitor side offers a high-efficiency and high-power-density buffer for pulsating power elimination. This technique offers a variety of benefits, such as (a) small DC-BUS VRs, (b) implementation by very low-voltage switching devices and passive elements, and d) reduced VR on both sides of the DC-BUS (FSIC and SSIC). On the other hand, this technique suffers from several drawbacks, such as (a) additional BEC for topology realization is required; (b) similar to the previous solution, the plug-and-play operation cannot be applied on an existing system without hardware modifications; and (c) application complexity: due to the multiplicity of components, a more cumbersome structure and a more complicated control circuit are obtained.

3.5. ASC Addition DC-BUS Case, Shunt Connection

3.5.1. Basic Principle of ASC

The existing literature describes several techniques for reducing the capacitance utilized in a power conversion system and presents comparisons among the different techniques to estimate the minimum capacitance needed for ASC applications [75]. Among them, adding an ASC in shunt connection is probably the most popular one. The principle of operation of these circuits is based on replacing a bulky and low-reliability DC-BUS electrolyte capacitor with a bidirectional DC–DC converter that contains an inductor and two switches and ends in a much smaller auxiliary film capacitor C_A as shown in Figure 14. The offered technique has many uses, and each application has advantages/disadvantages for different system purposes. An example of using an ASC addition in shunt connection is applying the auxiliary source as a DC-BUS-pulsed power load filter, as reported in [76,77]. The principle of the operation of such systems is based on an input/output power balance between the source interface and the load interface. The concept is implemented by adding an energy source (capacitor/supercapacitor) in parallel to the DC-BUS via a bidirectional DC–DC converter. Nevertheless, the target of these systems is to filter the pulsating of the load's power demands (Pulsed Power Supply application) and not to implement DC-BUS capacitance reduction or DC-BUS ripple eliminators. The presented pulsed power filter in [78] shows a DC-BUS capacitance reduction but does not eliminate the DC-BUS ripples and does not support the plug-and-play operation, because the control scheme requires an access to the corresponding load current. In addition, it is designed for special load profiles; therefore, these methods are not discussed in this paper.

This subsection's purpose, rather, is to collect and introduce major methods for applying the above technique, while analyzing results and presenting advantages and disadvantages. This method performs collection by focusing on the main requirements of power conversion systems, such as reduction of DC-BUS capacitance requirements, eliminating DC-BUS ripples, and enabling plug-and-play operation. The DC-BUS ripple eliminators circuit family and DC-BUS capacitance reduction capability have been offered in [6,79]. The ripple eliminator circuit can be divided into three categories based on different control

strategies: controlled current source (active power filter-based), controlled voltage source (direct voltage regulation-based), and capacitor dynamic behavior imitation (infinite capacitor). These control methods are common among ASCs in the shunt connection and therefore should be expanded upon.

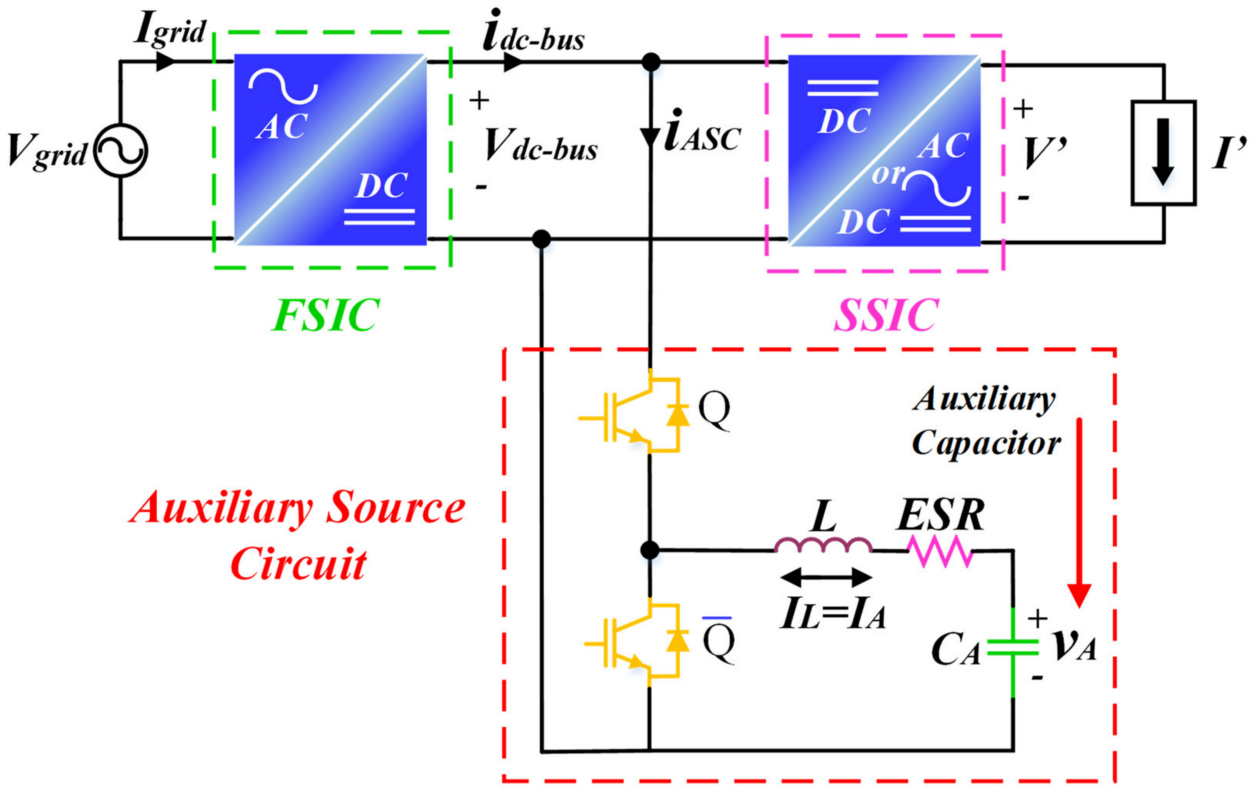

Figure 14. Capacitor-supported power conversion system with additional ASC, shunt connection.

3.5.2. Controlled Current Source Strategy (Active Power Filter-Based)

Extensive use for implementing an active filter-based control technique is found in the literature [80–83]. This control strategy is similar to the active power filter (from DC-BUS point) and operates as the current-controlled current sinks. The basic principle is sampling the total DC-BUS current pulsating component and designating it as control feedback, thus allowing DC-BUS capacitance reduction. In fact, in this technique, the ASC is implemented as a controlled current source toward the DC-BUS. Figure 15 illustrates the control structure and functional diagram of the regulated current source strategy. First, the control technique is based on measuring and summing up the DC-BUS currents ($i_{dc-bus\ 1,\ 2...N}$); then, only the pulsating current component is obtained by the DC eliminator (DCE), and the obtained value ($\sum \Delta i_{dc-bus,\ x}$) is used as the DC-BUS current reference (directly or indirectly). Next, the loss-compensating term $i_{loss}(t)$ (generated by the auxiliary voltage controller) is added to the DC-BUS current reference; it is a necessary operation because the ASC is not ideal. Finally, the ASC switch signals are set by the current controller (CC). Note that between the CC and the ASC switches, there is a PWM modulator unit. As a result, the DC-BUS voltage is indirectly regulated by diverting all the pulsating current components into C_A. Due to the control strategy requirement for measuring the currents, the current sensors are needed as well as access to measurement points outside the ASC. Therefore, this control strategy cannot operate in a plug-and-play approach. This disadvantage is even more noticeable if there are N converters connected to the DC-BUS. In this case, it is necessary to install N current sensors and corresponding measurement points. Another disadvantage of this control strategy is the additional delay that enters the system due to the DCE.

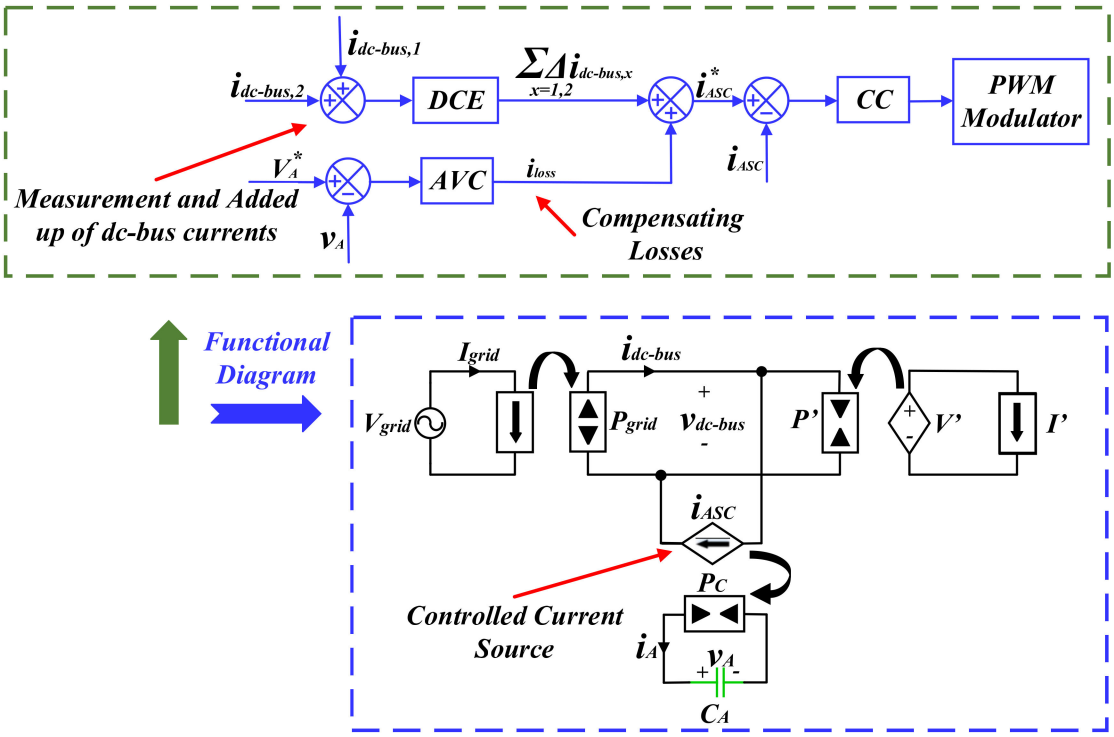

Figure 15. Controlled current source strategy, control structure, and functional diagram.

3.5.3. Controlled Current Source Strategy (Active Power Filter-Based)

Many ASC control strategies based on direct voltage regulation have been investigated as described in [84–86], and in this case, the control strategy operates as voltage-controlled current sinks. In fact, in this technique, the ASC is implemented as a regulated voltage source toward the DC-BUS, Figure 16 (V^*_{dc-bus}) voltage controller (VC)–CC. In this strategy (unlike the previous one), the pulsating current component is displaced into the ASC only by using information regarding the DC-BUS voltage and without external current measuring. This is a great advantage over the other methods, due to dispensing with DC-BUS current measurements; thus, adding current sensors is not required, and only DC-BUS voltage sensing is required.

Unfortunately, the system's active power balance indicator does not function when the DC-BUS voltage is under tight regulation. Thus, when the auxiliary capacitor absorbs the pulsating power component, v_A and v_{dc-bus} no longer reflect the system's power balance. In such a case, the FSIC voltage control loop should utilize v_A as the controlled variable instead of v_{dc-bus}. This means that v_A must be the state variable of FSIC VC after appropriate filtering, shifting, and scaling (FSS). The consequence is that implementation of this control strategy also does not allow operation in the plug and play mode. When the VRs are eliminated, the ASC is an infinite capacitor as reported in [87]. However, in this case, system power balancing is no longer indicated at the capacitor terminals, additional feedback of v_A is required, and operation in the plug-and-play mode is impossible.

The ASC control strategy of direct voltage regulation was proposed in [88,89]. These techniques enable a plug and play operation because the capacitor ripple voltage is regulated to zero by extracting the ripple component from the capacitor voltage. Figure 17 illustrates the control structure of the controlled voltage source strategy based on plug-and-play operation. First, only the v_{dc-bus} is measured, and after that the pulsating component is solely obtained by DCE. By utilizing multiresonant VC, the residual pulsating elements are regulated to zero. At the same time, in this arrangement as well (as with a controlled current source) the loss-compensating term $i_{loss}(t)$ is added (an additional voltage loop closed across v_A). Finally, the ASC switch signals are set by the current controller. In this case (unlike the previous technique), the average bus voltage preserves its value, yet it

could be utilized as an indicator for system power balance by FSIC VC; i.e., no extra FSIC voltage control loop is required, so the plug and play operation can be implemented by this technique. However, this technique is, likewise, based on DCE; thus, this system will also suffer from additional delays that enter the system. Another drawback of the proposed technique is the requirement for additional data related to the pulsating element frequencies or the base frequency that are necessary for designing a multiresonant controller.

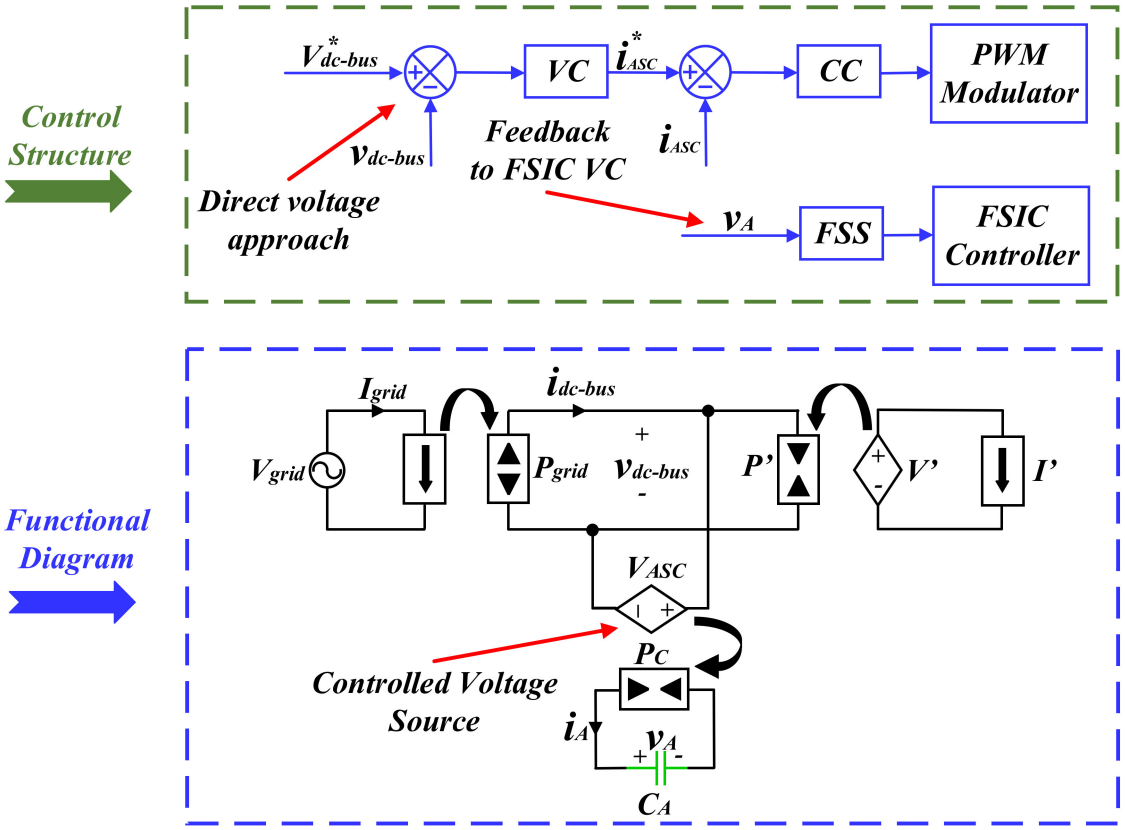

Figure 16. Controlled voltage source strategy, control structure, and functional diagram.

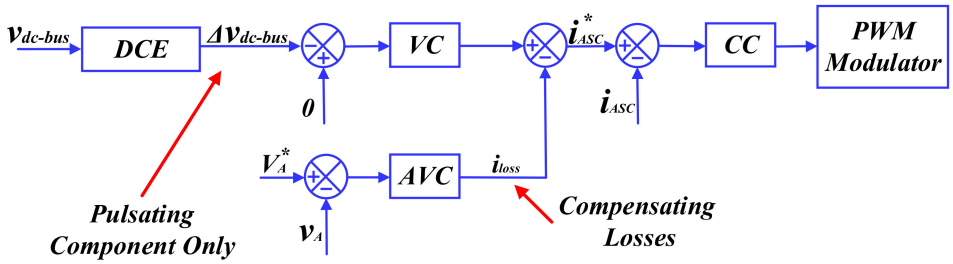

Figure 17. Control structure of controlled voltage source strategy based on plug-and-play operation.

3.5.4. Capacitor Dynamic Behavior Imitation Strategy (Infinite Capacitor)

Like the previous one, this strategy is also based on direct voltage regulation, but the difference of the Capacitor Dynamic Behavior Imitation (CDBI) approach from its predecessors (active power filter and direct voltage regulation) is that the ASC model is forced to imitate the dynamic capacitor's behavior toward the DC-BUS as shown in Figure 18. Much research is reported in the literature on ASC applications based on the capacitor dynamic behavior imitation; for example, [90–94] discuss the functional operation of an electronic capacitor based on an ASC that imitates the capacitor behavior. In this case, there is no requirement to decrease the voltage ripple below a specific value (for example, below the ripple existing in a system based on electrolytic capacitance). While reducing

the DC-BUS capacity requirement, one of the benefits allows plug-and-play operation; in such a case, it is essential to mimic the dynamic behavior of the replaced bulky capacitor. The VC of the converters (FSIC/SSIC) that are responsible for system power balancing are tuned according to the value of the originally utilized capacitor. Hence, it is important to regulate the ASC to function as a capacitor (from the DC-BUS point of view) to conserve the system's low-frequency dynamics while utilizing the initial capacitor. This would inevitably allow the plug-and-play process. The ASC control strategy approach is based on a voltage regulation technique to overcome its main drawbacks. The first one is additional system delay (created by using DCE) and the second is information that is required for designing the multiresonant controller, such as data about the frequency bases or the pulsating frequency components. The main difference between these approaches is that as an alternative for regulating the DC-BUS voltage to a constant value V^*_{dc-bus}, the reference signal is time-varying, calculated from the DC-BUS side ASC input current according to Equation (4).

$$v^*_{dc-bus}(t) = \frac{1}{C^*_{ASC}} \int (i_{ASC}(\tau) - i_{loss}(\tau))d\tau \tag{4}$$

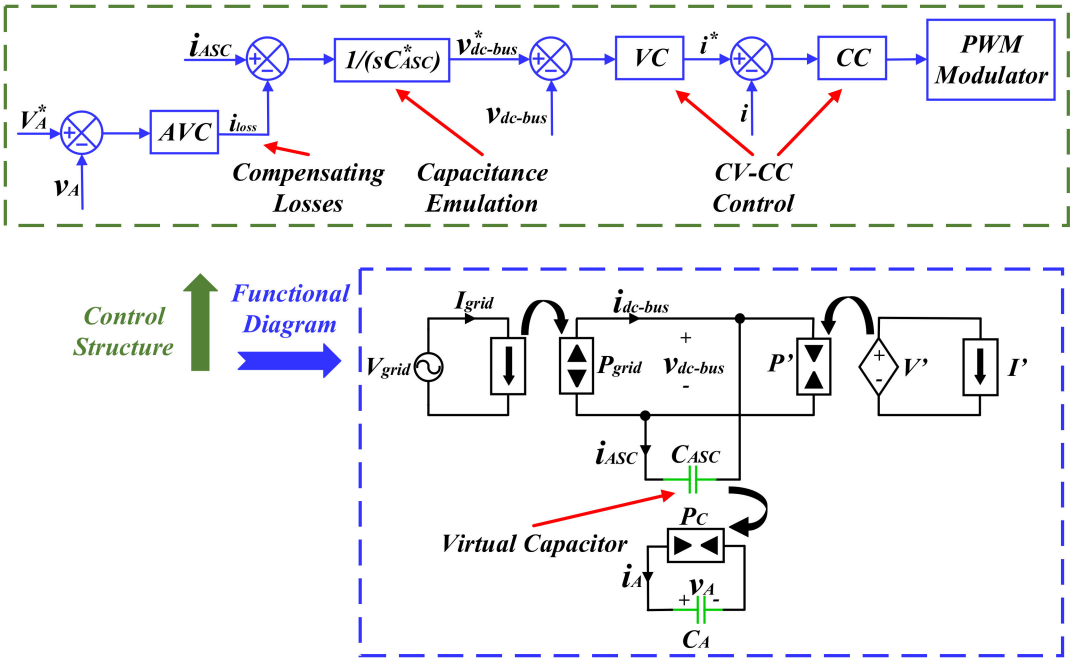

Figure 18. Capacitor dynamic behavior imitation strategy, control structure, and functional diagram.

The dynamic capacitor imitation control structure can be divided into three subsystems as shown in Figure 18. The first subsystem is loss compensation. Loss-compensating term $i_{loss}(t)$ (generated by the auxiliary voltage controller) is added to the DC-BUS current reference. When considering a loss-free system operating at a steady state, the calculated $i_{loss}(\tau)$ is equal to zero; therefore, as long as $v_{dc-bus} = {v_{dc-bus}}^*(t)$, the ASC performs as a capacitor ${C_{ASC}}^*$. Furthermore, the AVC is added to maintain the system's power balance (via $i_{loss}(t)$) because C_{ASC} is a virtual capacitor, and pulsating power components are still displaced into C_A. In fact, this is the main contribution of this research compared to its predecessors. The second subsystem is capacitance emulation; it implements Equation (4) to create the desired ${v_{dc-bus}}^*$, acting as converter output voltage reference signal, while the emulated capacitance could be time-varying. The third subsystem is CV/CC control and forces the bus instantaneous voltage V to tightly follow the reference ${v_{dc-bus}}^*$ by processing the tracking error through standard CV/CC controllers and running the converter switches accordingly. This research has been developed and extended to many applications based on ASC circuits in a shunt connection, such as a two-stage power conversion system based

on the DC-BUS for interfacing photovoltaic generators with AC mains [95] and improving the control structure of the electronic capacitor [96].

Other comprehensive research papers dealing with ASC applications based on the capacitor dynamic behavior imitation are presented in virtual infinite capacitor (VIC) research [97]. The VIC approach is defined as a nonlinear capacitor in which for an interval of the charge Q (the operating range), the voltage V (V_{ref}) remains steady. The dynamic capacitance C at a given point Q could be defined by $\frac{1}{C} = \frac{dV}{dQ}$; thus, the energy accumulated by the capacitor during an infinitesimal change of charge ($dQ = idt$) as: $dE = VdQ$. Therefore, a nonlinear capacitor at any voltage $V(Q)$ has a flat region, namely $\frac{dV}{dQ} = 0$ for $Q \in [Q_{min}, Q_{max}]$, named VIC. The Q–V curve shown in Figure 19 illustrates the operation area of Q as V_{ref} remains constant. While capacitor voltage dependence V (in a typical case) on Its stored charge Q is linear, as shown in Equation (5), the VIC offers an ASC that performs an imitation of nonlinear capacitor behavior.

$$Q_{(t)} = \int_0^t i_{(\tau)} d\tau \tag{5}$$

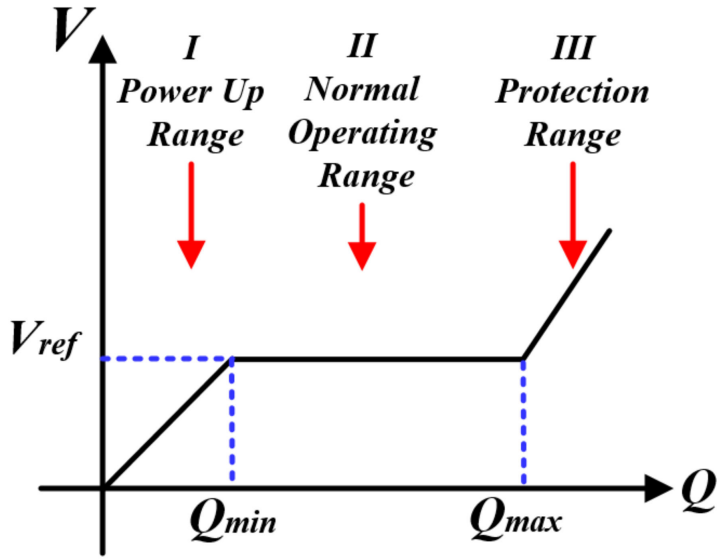

Figure 19. VIC Q–V characteristics. The effective operating range is where $Q \in [Q_{min}, Q_{max}]$.

The principle of the VIC control operation is based on two controllers, a voltage controller (acts fast to maintain the desired terminal voltage) and charging controller (acts more slowly and may regulate the incoming current in the low-frequency range; thus Q remains in the desired range). Figure 20 presents the VIC control structure; a detailed control process explanation is found in [97]. Note that the VIC has become more efficient in [98] with lossless zero-voltage switching realization, and a variety of VIC-based ASC applications can be found on the capacitor-supported power conversion system, such as MMCs, wind turbine systems, and PFCs in [99–101].

However, because Q cannot be evaluated from V in the useful operating range, having an infinite capacitor feature at the ASC requires additional measurement for the Q revaluation (meaning an additional output). In the above area, the dynamic capacitance is infinite, but the quantity of stored energy (the left region of the Q–V curve) is restricted and not very large. Therefore, this method is recommended for use as a voltage regulator or filter capacitor (DC-BUS voltage ripple elimination) but is not intended for energy storage. The major drawback of this control method is that the reference voltage is fixed (V_{ref} is a constant value). To ensure that the DC-BUS voltage reaches an equilibrium exactly at this value, the charge controller of the VIC must be integrated with the FSIC. Therefore, even in this case (as in direct voltage regulation), the system power balance is no longer indicated by the bulky capacitance, and additional feedback of auxiliary capacitance voltage is necessary.

As a result, this disadvantage prevents the plug-and-play operation benefit. Following the above method, the research was expanded, and the VIC control has been improved in [102]; the new algorithm regulates the VIC reference voltage instead of forcing the bus voltage to follow the reference signal. The proposed control algorithm allows to connect the VIC directly to the DC-BUS in the same way as a passive capacitor; therefore, in this case, plug-and-play operation is applicable. Note that this work is a breakthrough for much of the VIC-based research that allows plug-and-play operation, including a significant reduction of DC-BUS ripples to a very low level by an improved control method [103,104], modular realization of the active capacitor [105], and electric vehicle (EV) charger applications [106].

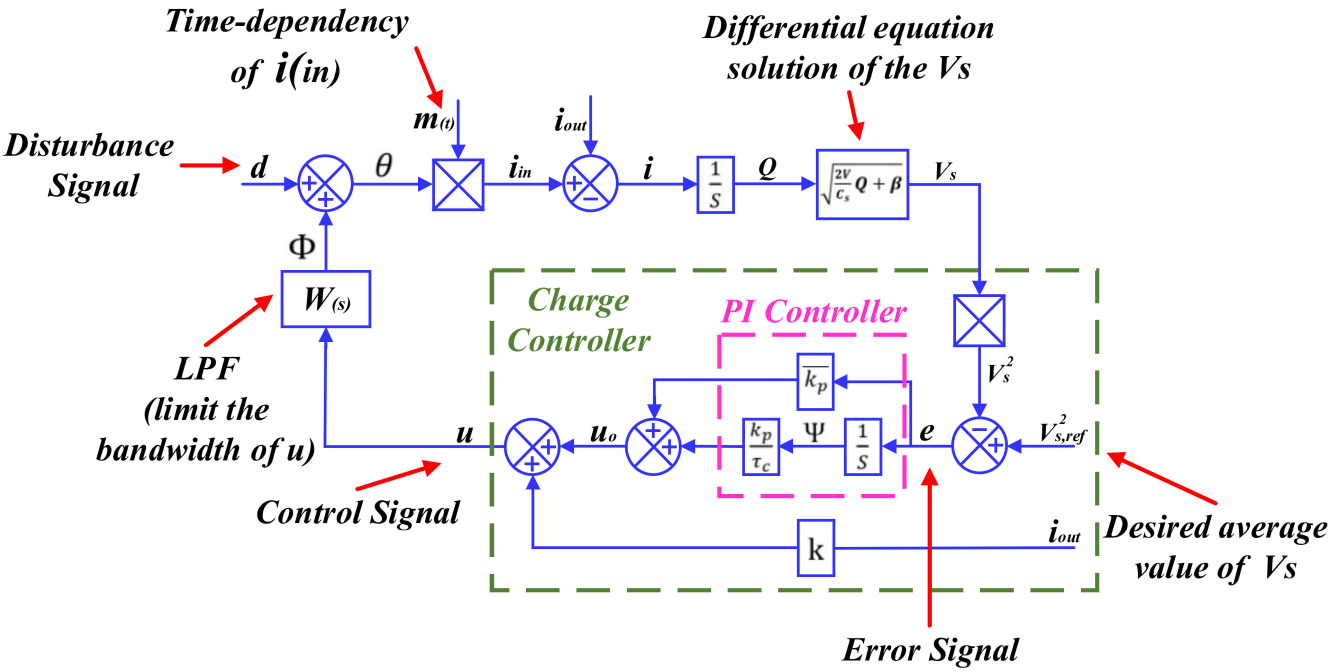

Figure 20. Control structure of a VIC charge controller, using a PI controller.

4. A Detailed Analysis and Comparison of the Available ASCs

Recently, the integration of ASCs in capacitor-supported power conversion systems has attracted the attention of researchers due to its high reliability and appropriate power quality. Moreover, the integrated ASC provides benefits, such as a reduction of cost, weight, and size of the conversion stage. The use of a compact ASC abolishes the use a bulky electrolytic capacitor and can even be implemented as a source of energy bursts supply for pulsating loads. Many topologies of ASCs already exist (as presented in Section 3) for the benefits mentioned above, but researchers are still developing a new version of ASC topology for a variety of advantages in different applications. The presented topologies throughout the paper can be classified into five solutions: DC-BUS capacitance distribution (passive), DC-BUS capacitance distribution (active), ASC series connection with the converter side, ASC series connection with the capacitor side, and shunt connection. The differences among the topologies can be diagnosed by five criteria as shown in Table 2: Converter Rating, Current, Voltage Stress, Simplicity of Topology/Component Count, and Control Effort. The converter rating at DC-BUS capacitance distribution solutions is in a cascade connection; thus, the rating is with full energy, and the ASC solutions process only the pulsating power; therefore, they demonstrate top performance over other solutions. In terms of current, the shunt connection and series connection (capacitor side) topologies process the smallest current value due to the DC-BUS parallel topology. In the series connection case, the ASC handles only the ripple voltage across the DC-BUS; therefore, it has the lowest voltage stress. Undoubtedly, the shunt connection has the simplest topology

due to the low component count and plug-and-play capability. On the other hand, due to the CDBI requirement, the control effort in the shunt connection solutions is the highest.

Table 2. Design considerations for ASC solutions according to the different topologies.

Authors, Year, and Ref.	Topology	Converter Rating	Current	Voltage Stress	Simplicity of Topology/Component Count	Control Effort
Tang Y et al., 2016. [64]	DC-BUS Capacitance Distribution	High	High	High	Low	Moderate
Li S et al., 2015. [67]	DC-BUS Capacitance Distribution	High	High	High	High	Moderate
Wang H et al., 2014. [72]	ASC, Series Connection with the Converter Side	Low	High	Low	High	Low
Qin S et al., 2017. [74]	ASC, Series Connection with the Capacitor Side	Low	Moderate	Low	High	Low
Strajnikov P et al., 2020. [94]	ASC, Shunt Connection	Low	Moderate	Moderate	Low	High

Nowadays, the main contribution of the ASC is a reduction of the DC-BUS capacitance requirement, eliminating the DC-BUS ripples, filtering the powering pulsed power loads, and finally, allowing plug-and-play operation (major benefit). The selection of the appropriate topology for a specific application is challenging because every topology has its own pros and cons depending on the implemented control strategy. Therefore, the selection of the topology for a particular application is based on the control strategy and topology structure as a detailed comparison in Table 3. In addition, the DC-BUS capacitance reduction circuit topologies are reviewed based on the three different categories: DC-BUS capacitance distribution, addition of a supplementary source, and series/shunt connection configurations. In the case of the DC-BUS capacitance distribution topology, there is no need to add an auxiliary storage. This advantage confers greater circuit simplicity compared to other topologies, by slightly changing the control strategy. Series connection topology provides an option to implement the ASCs with very low-voltage switching devices and passive elements, due to the small ripple voltage on the DC-BUS and reactive power only. However, shunt connection configurations have the highest reliability and efficiency compared to the rest, and therefore, it is also the most dominant configuration. Furthermore, this structure (not all control strategies support this option as shown in Table 3) allows plug-and-play operation compared to the series connection. This section's purpose is to summarize all the main techniques for optimizing capacitor-supported power conversion systems and to present the advantages and disadvantages of each topology relating to the selected control strategy.

Table 3. Comparison of different topologies and control strategies.

Authors, Year, and Ref.	Topology	Control Strategy	Brief Description of the Work	Plug-and-Play Operation	Remarks
Tang Y et al., 2016. [64]	DC-BUS capacitance distribution		Single-phase transformerless inverter topology, solving leakage current and pulsating power issues in grid-connected photovoltaic (PV) systems.	X	• No need for adding an ASC. • Simplicity of the circuit configuration. • Always a residual ripple power in the DC-BUS of the PV inverter, and the elimination of fluctuating power is not complete (due to fourth-order harmony and other disturbances that are not calculated by this method).
Li S et al., 2015. [67]	DC-BUS capacitance distribution		Differential AC/DC rectifier based on the use of an inductor current waveform control methodology.	X	• No need for adding an ASC. • Elimination of fluctuating power is not complete. • Low reliability and high cost due to the multiplicity of switching components and inductors.
Wang H et al., 2014. [72]	ASC, Series Connection with the Converter Side		A new technique of reducing the DC-BUS capacitance in a capacitor-supported system by ASC series connection across the DC-BUS, to compensate the VR.	X	• The ability to implement the ASC with very low-voltage switching devices and passive elements. • The VRs in the DC-BUS capacitors can be increased, which is beneficial for balancing the power between the line and load. • Low reliability: a simple fault with the ASC disables the entire system, due to the ASC series connection across the DC-BUS. • Always one side of the FSIC/SSIC that is connected to the DC-BUS capacitor suffers from a lack of stress regulation.
Liu W et al., 2015. [73]	ASC, Series Connection with the Converter Side		A grid-tied solar inverter with a series ASC for reducing the high-voltage DC-BUS capacitance.	X	• The ability to implement the ASC with very low-voltage switching devices and passive elements. • The VRs in the DC-BUS capacitors can be increased, which is beneficial for balancing the power between the line and load. • Low reliability: a simple fault with the ASC disables the entire system, due to the ASC series connection across the DC-BUS.
Qin S et al., 2017. [74]	ASC, Series Connection with the Capacitor Side	CCS	A high-power-density buffer for pulsating power decoupling inherent in single-phase AC systems, by placing the ASC unit in a series connection with the DC-capacitor.	X	• A high-efficiency and high-power-density buffer for pulsating power decoupling. • The ability to implement the ASC with very low-voltage switching devices and passive elements. • Additional DC-BUS capacitor is needed. • Consumed BEC for topology realization.

Table 3. *Cont.*

Authors, Year, and Ref.	Topology	Control Strategy	Brief Description of the Work	Plug-and-Play Operation	Remarks
Zhong QC et al., 2016. [83]	ASC, Shunt Connection	CCS	Developing a ripple eliminator circuit, based on an advanced control strategy so that the ripple current can be instantaneously compensated.	X	• Allowing elimination of the DC-BUS VR. • Allowing reduction of the DC-BUS capacitance requirement. • Multiple components. If there are N converters, it is necessary to install N invasive current sensors. • DCE circuit constitutes an additional delay to the system.
Mellincovsky M et al., 2018. [85]	ASC, Shunt Connection	CVS	Control analysis and operational issues of a direct voltage-regulated active capacitance reduction circuit, consisting of an ASC interfaced to DC-BUS.	X	• Allowing elimination of the DC-BUS VR. • Allowing reduction of the DC-BUS capacitance requirement. • No need to add invasive current sensors. • Once the DC-BUS voltage is tightly regulated, v_A and the v_{dc-bus} do not reflect the system's power balance; i.e., FSIC voltage control loop should utilize v_A as the controlled variable instead of v_{dc-bus}. (v_A must be feedback to FSIC VC after appropriate FSS).
Li S et al., 2018. [89]	ASC, Shunt Connection	CVS	A plug-and-play ripple mitigation technique development for stabilizing the DC-BUS voltage (direct voltage regulation control)	√	• Allowing elimination of the DC-BUS VR. • Additional FSIC voltage control loop is not required. • DCE circuit constitutes additional delay to the system. • Information about the base frequency or frequency of pulsating components required for multiresonant controller design is required.
Mutovkin A et al., 2019. [92]	ASC, Shunt Connection	CDBI	Development of a control algorithm allowing reduction of the bulky DC-BUS capacitance in a plug-and-play mode for grid-connected energy conversion systems (direct voltage regulation control).	√	• No need for DCE (additional delay to the system). • No information is required regarding the base frequency, or the frequencies of pulsating components required for multiresonant controller design. • Low-frequency DC-BUS ripple feasibility (once the ASC emulates a finite-valued capacitance, it automatically reproduces VR across the DC-BUS).

Table 3. *Cont.*

Authors, Year, and Ref.	Topology	Control Strategy	Brief Description of the Work	Plug-and-Play Operation	Remarks
Strajnikov P et al., 2020. [94]	ASC, Shunt Connection	CDBI	A modification of ASC control structure, allowing to achieve near-zero DC-BUS ripple while maintaining accurate transient dynamics of a specific finite-valued capacitance.	√	• No need for DCE (additional delay to the system). • No information is required regarding the base frequency or frequencies of the pulsating components required for multiresonant controller design. • Elimination (near-zero) of the low-frequency steady-state DC-BUS ripple (by adding a notch filter to the control subsystem).
Yona G et al., 2017. [97]	ASC, Shunt Connection	CDBI	Introducing a virtual infinite capacitor (VIC), an electronic circuit that replaces a large filter capacitor and VIC realization using a bidirectional DC/DC converter with sliding mode control.	X	• Allowing elimination of the DC-BUS VR. • Is not meant to store energy. • The reference voltage V_{ref} is fixed, i.e., to ensure that the dc bus voltage reaches an equilibrium exactly at this voltage, the charge controller of the VIC must be integrated with the FSIC. • The algorithm requires megahertz switching frequency to stabilize the system.
Lin J and Weiss G. 2019. [103]	ASC, Shunt Connection	CDBI	A plug-and-play (PnP) realization of the VIC, which enables the VIC to be connected directly to the DC-BUS like a passive capacitor by adaptive control of the PnP VIC.	√	• Ripple elimination is available on a wide range of voltages and frequencies. • The proposed control method reduces DC-BUS VR to a very low level (much smaller than [76]). • Allowing to absorb arbitrary harmonics on a DC-BUS.

CDBI: Capacitor Dynamic Behavior Imitation. CVS: Controlled Voltage Source. CCS: Controlled Current Source.

5. Conclusions

The capacitor-supported power conversion systems with ASCs are used extensively in distributed generation systems to eliminate the need for BECs. Optimal ASC design and the use of a proper control strategy in these converters have paramount importance to increase efficiency, improve performance, and achieve high reliability in the power conversion process. Therefore, this review paper has largely focused on the reduction of DC-BUS capacitance by utilizing circuit topologies under four different common solutions, such as DC-BUS capacitance distribution, ASC series connection with the converter/capacitor sides, and shunt connection. In each solution, several control strategies that have been developed are identified in the literature and presented with highlighted information. In addition, a separate comparison is made for each technique as shown in Table 3 with an emphasis on its parameters and remarks. ASC solutions with the features of high reliability, appropriate power quality, plug-and-play operation, low price/weight, and reduced conversion stage size are always expected. Nevertheless, there is no such thing as a free meal. Each energy storage source, topology, and control strategy has its pros and cons, and therefore, a performance comparison among the different uses is necessary. Reviewing the available techniques for a DC-BUS capacitance reduction circuit reveals that shunt connection ASCs based on CDBI control are the most common solution due to their highest energy density, lowest converter rating, and plug-and-play operation. Still, the literature is poor in discussing the integration of ASCs with power converters feeding dynamic loads (e.g., pulsating load) that support plug-and-play operation. Future research within this subject will greatly contribute toward the integration of ASCs in various dynamic applications. It is expected that this review will be a helpful reference on ASCs for researchers, design engineers, and manufacturers who are seeking reliable power converters.

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Abbreviations

The following abbreviations and nomenclatures are used in this manuscript:

BEC	Bulky Electrolytic Capacitor
ASC	Auxiliary Source Circuit
FSIC	First-Stage Interface Converter
SSIC	Second-Stage Interface Converter
VR	Voltage Ripple
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
AE-C	Aluminum Electrolytic Capacitor
MLC-C	Multilayer Ceramic Capacitor
MPF-C	Metallized Polypropylene Film Capacitor
BOPP	Biaxial-Oriented Polypropylene

C_B	Bulky Capacitor
C_A	Auxiliary Capacitor
CM	Common Mode
CM_V	CM Voltage
CM_i	CM Current
R_p	Insulation Resistance
R_d	Dielectric Loss
C_d	Inherent Dielectric Absorption
W_V	Limit Storable Energy
PFC	Power Factor Correction
PWM	Pulse Width Modulation
DSP	Digital Signal Processing
HPF	High-Pass Filter
LPF	Low-Pass Filter
CCS	Controlled Current Source
CVS	Controlled Voltage Source
CDBI	Capacitor Dynamic Behavior Imitation
DCE	DC Eliminator
CC	Current Controller
CV	Voltage Controller
FSS	Filtering, Shifting, and Scaling
AVC	Auxiliary Voltage Controller
VIC	Virtual Infinite Capacitor
PI	Proportional Integral
EV	Electric Vehicle
V_{comp}	Compensation Voltage Factor
f_{rip}	Ripple Frequency
$i_{loss}(t)$	Loss-Compensating Term
MMC	Modular Multilevel Converter

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