

## Article

# Breakdown Characteristics of Ga<sub>2</sub>O<sub>3</sub>-on-SiC Metal-Oxide-Semiconductor Field-Effect Transistors

Maolin Zhang <sup>1,2</sup>, Lei Wang <sup>1,2</sup>, Kemeng Yang <sup>1,2</sup>, Jiafei Yao <sup>1,2</sup>, Weihua Tang <sup>1,2,\*</sup> and Yufeng Guo <sup>1,2,\*</sup>

<sup>1</sup> College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China

<sup>2</sup> National and Local Joint Engineering Laboratory for RF Integration and Micro-Assembly Technologies, Innovation Center for Gallium Oxide Semiconductor (IC-GAO), Nanjing 210023, China

\* Correspondence: whtang@njupt.edu.cn (W.T.); yfguo@njupt.edu.cn (Y.G.)

**Abstract:** Ultra-wide bandgap semiconductor gallium oxide (Ga<sub>2</sub>O<sub>3</sub>) features a breakdown strength of 8 MV/cm and bulk mobility of up to 300 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>, which is considered a promising candidate for next-generation power devices. However, its low thermal conductivity is reckoned to be a severe issue in the thermal management of high-power devices. The epitaxial integration of gallium oxide thin films on silicon carbide (SiC) substrates is a possible solution for tackling the cooling problems, yet premature breakdown at the Ga<sub>2</sub>O<sub>3</sub>/SiC interface would be introduced due to the relatively low breakdown strength of SiC (3.2 MV/cm). In this paper, the on-state properties as well as the breakdown characteristics of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC metal-oxide-semiconductor field-effect transistor (MOSFET) were investigated by using the technology computer-aided design (TCAD) approach. Compared with the full-Ga<sub>2</sub>O<sub>3</sub> MOSFET, the lattice temperature of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET was decreased by nearly 100 °C thanks to the high thermal conductivity of SiC. However, a breakdown voltage degradation of >40% was found in an unoptimized Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET. Furthermore, by optimizing the device structure, the breakdown voltage degradation of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET is significantly relieved. As a result, this work demonstrates the existence of premature breakdown in the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET and provides feasible approaches to further enhance the performance of hetero-integrated Ga<sub>2</sub>O<sub>3</sub> power devices.



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**Keywords:** gallium oxide; metal-oxide-semiconductor field-effect transistor; silicon carbide; thermal management; breakdown voltage

## 1. Introduction

Due to the wide bandgap (~4.8 eV) [1], high Baliga's figure-of-merit (BFOM) [2], and outstanding breakdown strength (~8 MV/cm) [3], gallium oxide (Ga<sub>2</sub>O<sub>3</sub>) has shown great potential in power devices including metal-oxide-semiconductor field effect transistors (MOSFETs) and Schottky barrier diodes (SBDs) [4–6]. For high-power devices, thermal cooling efficiency is vital for operation robustness and lifetime, which requires dedicated thermal management [7–9]. A major disadvantage of gallium oxide is its low thermal conductivity [10], which, if not well considered, will reduce the performance of Ga<sub>2</sub>O<sub>3</sub>-based devices. Device robustness is critical for electronic systems, especially for high-power systems, and thermal management is the key to improving device robustness. System failure may occur due to the harsh radiation, which is more likely to occur when the device is at a high working temperature [11–16]. One solution to this problem is packaging Ga<sub>2</sub>O<sub>3</sub>-based devices with materials or structures with high thermal conductivity [8]. Another method is fabricating devices on a high-thermal conductivity substrate. Al<sub>2</sub>O<sub>3</sub> (thermal conductivity = 0.3 W·cm<sup>-1</sup>K<sup>-1</sup>) is a suitable substrate material for Ga<sub>2</sub>O<sub>3</sub>-based power devices and shares a better thermal conductivity than Ga<sub>2</sub>O<sub>3</sub> (thermal conductivity = 0.13 W·cm<sup>-1</sup>K<sup>-1</sup>). However, compared with Al<sub>2</sub>O<sub>3</sub>, silicon carbide (SiC) is

an ideal substrate that features a superior thermal conductivity of  $4.9 \text{ W}\cdot\text{cm}^{-1}\text{K}^{-1}$  and is a material with which  $\text{Ga}_2\text{O}_3$  hetero-epitaxy can be realized [17].

It has been revealed that hetero-epitaxial  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFETs have more advantages in thermal performance than homo-epitaxy [18,19]. However, SiC has a relatively low critical electric field compared with  $\text{Ga}_2\text{O}_3$ , which could impair the breakdown voltage (BV) due to premature breakdown [20]. Meanwhile, crystal dislocations could be introduced at the interface of two materials, which results in harmful interface states [21]. However, thanks to the progress in epitaxial technology, such a non-ideal factor would be relieved [22,23]. Previous studies mainly focused on the on-state performance of the  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFET by considering the lattice self-heating effects but with little concentration on breakdown characteristics [18,19,24,25].

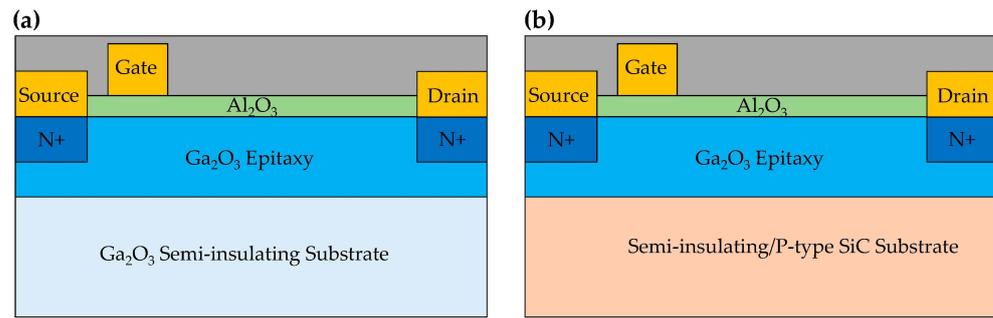
The low-cost method of numerical computation has been widely used for the research of material properties, device design, circuit, and system analysis [26–32]. For SiC-based devices, the convergence of numerical computation has been solved by advances in computing technology [33]. However, for  $\text{Ga}_2\text{O}_3$  devices, the poor convergence of numerical computation is currently an issue due to the ultra-wide bandgap of  $\text{Ga}_2\text{O}_3$  [34] and the low intrinsic carrier concentration.

In this study, the  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFET was designed, and its on-state as well as breakdown characteristics were simulated. Performance, including the transfer, output, and electric field distribution, is presented using Synopses Sentaurus TCAD. On-state, lattice self-heating effects were taken into consideration, lattice temperatures were calculated, and their effects on carriers' mobility were discussed. By comparing the differences between MOSFETs on SiC substrates and  $\text{Ga}_2\text{O}_3$  substrates in temperature distribution and on-state performance, the thermal effects of the SiC substrate are verified. Off-state, electric field distribution was adopted to indicate the breakdown voltage in this study [26]. The effect of SiC concentration, SiC thickness,  $\text{Ga}_2\text{O}_3$  epitaxial doping concentration, and  $\text{Ga}_2\text{O}_3$  epitaxial thickness on the breakdown voltage was evaluated. SiC premature breakdown was discussed, and basic improvements to minimize this nonideal effect are also provided.

## 2. Device Structure and Simulation Setup

The structures of MOSFETs in this study are shown in Figure 1. In Figure 1a, the conventional  $\text{Ga}_2\text{O}_3$  MOSFET consists of a semi-insulating  $\text{Ga}_2\text{O}_3$  substrate (thickness =  $200 \mu\text{m}$ ) and a  $\text{Ga}_2\text{O}_3$  epitaxy layer. In Figure 1b, the  $\text{Ga}_2\text{O}_3$  substrate was replaced by a p-type/semi-insulating SiC layer. Below the p-type/semi-insulating SiC layer, the conductive n-type substrate (thickness =  $200 \mu\text{m}$ ) and substrate electrode were set for thermal simulation, which are not shown in the figure. For both device structures, thermal contacts were deployed, and the contact temperature was set to 300 K. The source and drain electrodes were treated as ohmic contacts, and the work function of the gate electrode was set at 5.3 eV. The distance between the drain and gate, also known as the drift length in power devices, was set to  $7.5 \mu\text{m}$ , and the distance between the source and gate was  $0.5 \mu\text{m}$ . A thickness of 20 nm of  $\text{Al}_2\text{O}_3$  was used as the gate dielectric, and a passivation layer of  $\text{Si}_3\text{N}_4$  was also introduced. All parameters are selected based on experimental results, and the simulation has been calibrated [35]. Detailed structural parameters can be found in Table 1.

In this study, carrier mobility was obtained by solving several physical equations in conjunction with each other. The carrier's mobility is mainly governed by three effects, namely: doping concentration dependence, high-field saturation, and surface effect [36]. In this study, the carriers, i.e., electrons, were distributed in the channel region of the MOSFET. Thereby, the surface effect can be considered to have a relatively minor impact on the carrier's mobility and thus was ignored. The high electric field saturation effect and the carrier doping concentration effect were considered. Many theoretical approaches were used to calculate mobility. The experimental results were summarized by the Arora model to represent the effect of carrier doping effects on carrier mobility. The corresponding model representation is as follows [37]:



**Figure 1.** Schematic diagrams of the (a) conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET and (b) Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET.

**Table 1.** Device structural parameters.

Structural Parameters	Unit	Value
Substrate thickness $t_{\text{sub}}$	$\mu\text{m}$	200
Drain to gate distance $L_{\text{gd}}$	$\mu\text{m}$	7.5
Al <sub>2</sub> O <sub>3</sub> thickness $t_{\text{ox}}$	nm	20
Gate work function $W_{\text{F}}$	eV	5.3
Substrate temperature $T_{\text{sub}}$	K	300
Ga <sub>2</sub> O <sub>3</sub> channel thickness $t_{\text{ch}}$	$\mu\text{m}$	0.235 for on-state, 0.1–0.5 for off-state
Ga <sub>2</sub> O <sub>3</sub> channel doping $D_{\text{ch}}$	$\text{cm}^{-3}$	$1 \times 10^{17}$ for on-state, $1 \times 10^{16}$ – $5 \times 10^{17}$ for off-state
SiC layer thickness $t_{\text{SiC}}$	$\mu\text{m}$	30 for on-state, 5–30 for off-state
SiC layer doping $D_{\text{SiC}}$	$\text{cm}^{-3}$	$1 \times 10^{12}$ for on-state, $1 \times 10^{15}$ – $1 \times 10^{16}$ for off-state

$$\mu_{\text{doping}} = \mu_{\text{min}} + \frac{\mu_{\text{d}}}{1 + \left(\frac{N_{\text{A},0} + N_{\text{D},0}}{N_0}\right)} \quad (1)$$

$$\mu_{\text{min}} = A_{\text{min}} \left(\frac{T}{T_0}\right)^{\alpha_{\text{m}}} \quad (2)$$

$$\mu_{\text{d}} = A_{\text{d}} \left(\frac{T}{T_0}\right)^{\alpha_{\text{d}}} \quad (3)$$

$$N_0 = A_{\text{N}} \left(\frac{T}{T_0}\right)^{\alpha_{\text{N}}} \quad (4)$$

$$A^* = A_{\text{a}} \left(\frac{T}{T_0}\right)^{\alpha_{\text{a}}} \quad (5)$$

where  $A_{\text{min}}$ ,  $A_{\text{d}}$ ,  $A_{\text{N}}$ , and  $A_{\text{a}}$  are the model parameters depending on materials,  $T$  is the ambient temperature, and  $T_0$  is the room temperature, which was taken as 300 K in this study.  $N_{\text{D},0}$  and  $N_{\text{A},0}$  in Equation (1) are the donor and acceptor concentrations, respectively.  $\mu_{\text{min}}$  is the minimum mobility for materials with a high doping concentration.  $\mu_{\text{d}}$  is the differential value between minimum mobility and mobility under low doping conditions. Equation (1) interprets the relationship between doping concentration and carrier mobility. In Equations (1)–(5), when the temperature is fixed,  $N_0$ ,  $\mu_{\text{d}}$ , and  $\mu_{\text{min}}$  are all fixed values. With a higher  $N_{\text{D},0}$  or  $N_{\text{A},0}$ , the  $\mu_{\text{doping}}$  decreases. This model successfully shows the trend of doping concentration as a function of carrier mobility. The parameters of the Ga<sub>2</sub>O<sub>3</sub> Arora model in this work were extracted from experimental results in references [36,38]. The calibration results were shown in Figure 2, and the extracted parameters were listed in Table 2.

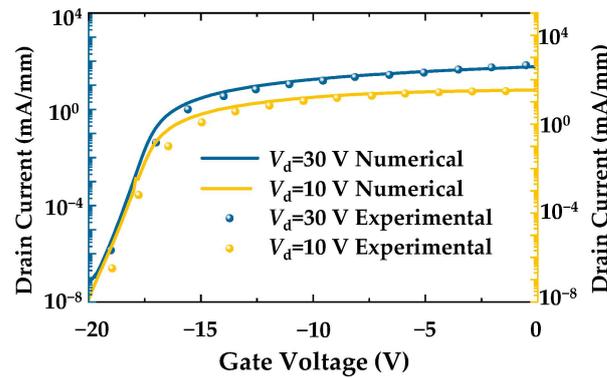


Figure 2. Calibration of simulated transfer curves with experimental results from [38].

Table 2. Arora model variables in Ga<sub>2</sub>O<sub>3</sub>.

Variables	Electron	Hole	Unit
$A_{\min}$	13	0.016	cm <sup>2</sup> /V·s
$\alpha_m$	−0.57	−0.57	1
$A_d$	235	0.2	cm <sup>2</sup> /V·s
$\alpha_d$	0.78	0.78	1
$A_N$	$1.1 \times 10^{18}$	$1.25 \times 10^{17}$	cm <sup>−3</sup>
$\alpha_N$	2.4	2.4	1
$A_a$	0.78	0.78	1
$\alpha_a$	−0.146	−0.146	1

As for the carriers' high electric field saturation effects, the Canali model was used in this study, which was derived from the Caughey-Thomas model. The mobility can be expressed by Equations (6) and (7), where  $\mu_{\text{low}}$  is the carrier mobility at a low electric field,  $\mu_{\text{low}}$  is determined by the mobility previously obtained at a low electric field condition, and  $v_{\text{sat}}$  is the carrier saturation velocity. In semiconductors subject to scattering, there is an upper limit to the carrier velocity, and it varies for different materials. The coefficient  $\beta$  is a temperature-dependent quantity that satisfies the following relationship. The Canali model parameters used in this study for Ga<sub>2</sub>O<sub>3</sub> are shown in Table 3 [36,39,40].

$$\mu(E) = \mu_{\min} + \frac{(\alpha + 1)\mu_{\text{low}}}{\alpha + [1 + (\frac{(\alpha+1)\mu_{\text{low}}E}{v_{\text{sat}}})^\beta]^{1/\beta}} \quad (6)$$

$$\beta = \beta_0 \left(\frac{T}{T_0}\right)^{\beta_{\text{exp}}} \quad (7)$$

Table 3. Ga<sub>2</sub>O<sub>3</sub> Canali model variables.

Variables	Value	Unit
$\alpha$	0	1
$\beta_0$	1	1
$\beta_{\text{exp}}$	0	1

Meanwhile, in this study, carrier mobility was found to be closely related to lattice temperature. It has been shown that the mobility of the carrier has a negative exponential relationship with the lattice temperature, as expressed in Equation (8), where  $\mu_0$  represents the electron mobility at 300 K,  $T$  represents the lattice temperature,  $T_0$  is 300 K,  $\alpha_1$  represents

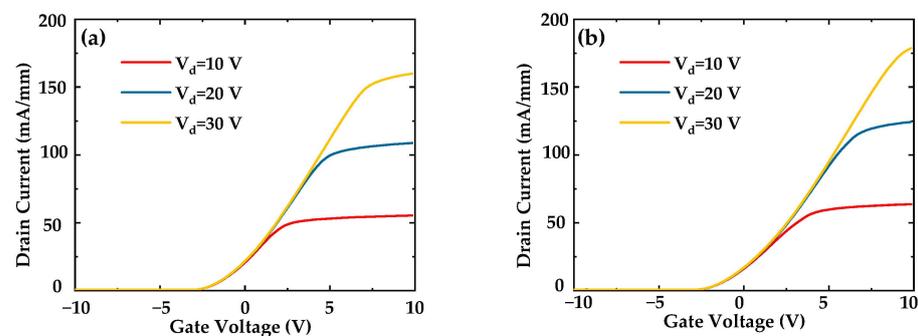
the corresponding exponential coefficient, and a value of 2 is typically used for  $\alpha_1$  in Ga<sub>2</sub>O<sub>3</sub> [41].

$$\mu = \mu_0 \left( \frac{T}{T_0} \right)^{-\alpha_1} \quad (8)$$

For breakdown characteristics, avalanche breakdown is the key point. In this process, electron-hole pairs were generated by impact ionization. However, due to the ultra-wide bandgap and low carrier concentration of Ga<sub>2</sub>O<sub>3</sub> ( $10^{-22}$  cm<sup>-3</sup>), it was difficult to directly calculate the reverse current by numerical calculation and often encountered non-convergence. To address this issue, the internal electric field distribution was calculated at different voltages. According to the related literature, the critical breakdown field strengths of Ga<sub>2</sub>O<sub>3</sub> and SiC are 8 and 3.2 MV/cm [1,33], respectively. In this study, the drain voltage was continuously increased to analyze the internal electric field distribution, and the device was considered to break down when either Ga<sub>2</sub>O<sub>3</sub> or SiC reached its breakdown field strength, which is a common method adopted for determining the breakdown voltage of Ga<sub>2</sub>O<sub>3</sub>-based devices [26].

### 3. On-State Characteristics

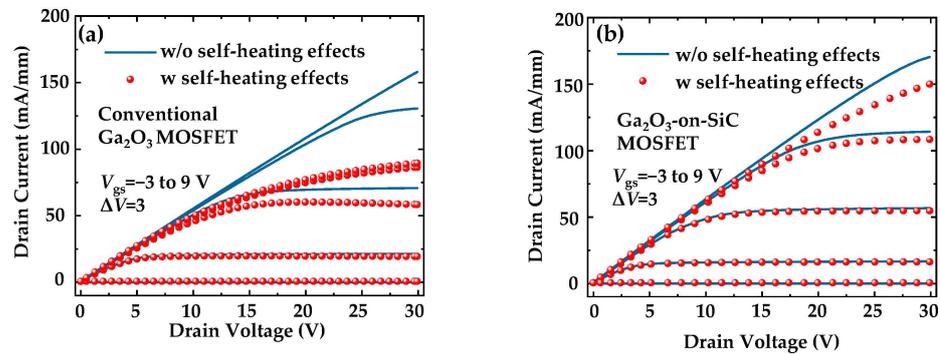
The transfer characteristics of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET and the conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET were first investigated. As shown in Figure 3, the transfer characteristics are displayed, where Figure 3a presents the transfer characteristics of a conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET with a semi-insulating Ga<sub>2</sub>O<sub>3</sub> substrate and Figure 3b shows those of a Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET. No significant difference in the threshold voltage between the two MOSFETs can be found, indicating that the transfer characteristics of the device were not affected by the change in substrate material. Although there are differences in the work function between Ga<sub>2</sub>O<sub>3</sub> and SiC, the transfer characteristics of MOSFETs are mainly dependent on the gate dielectric and the work function difference between the gate metal and the channel layer.



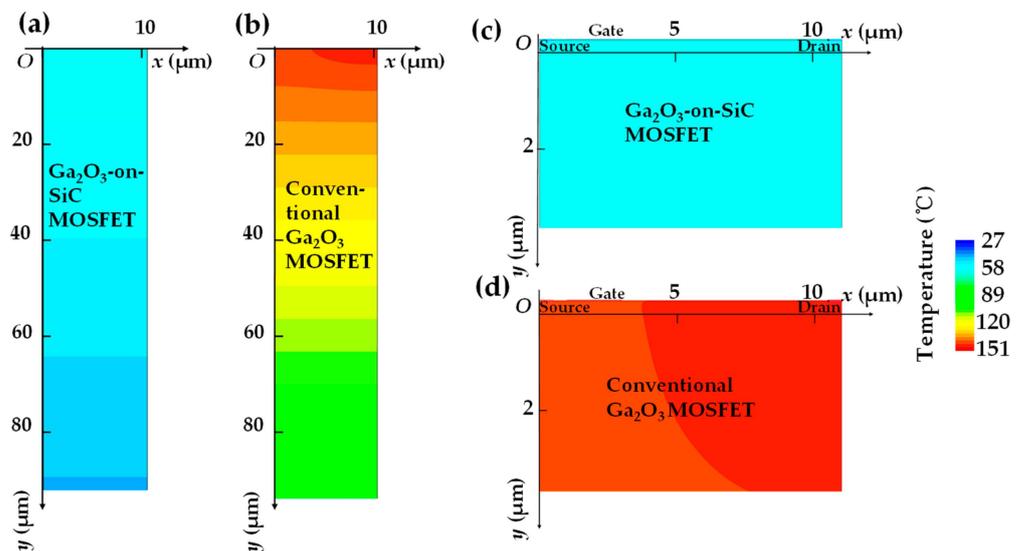
**Figure 3.** Transfer characteristics of (a) conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET and (b) Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET.

Furthermore, the output characteristics of the MOSFETs were discussed. The output characteristics of the two devices before and after considering the thermal effects are shown in Figure 4. The output characteristic of the conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET is shown in Figure 4a, where it is seen that with the increase in gate voltage, the drain current decreases significantly after considering the self-heating effects. The output characteristics of a Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET are shown in Figure 4b. It can be observed that the drain current nearly remains identical before and after adding the thermal model. To explore the physical mechanisms, the lattice temperature distribution is calculated and shown in Figure 5. The lattice temperature in the channel region of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET is only 58 °C, while the temperature in the channel region of the conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET increases to 151 °C. The poor thermal conductivity of Ga<sub>2</sub>O<sub>3</sub> results in a higher lattice temperature, and thus drain current is reduced. The mobility of carriers decreases exponentially with increasing temperature, and according to Equation (8), the conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET has a 39% reduction in carrier mobility compared to the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET. Similar

results were reported in previous work, suggesting SiC hetero-substrate is a feasible method for reducing the self-heating effect [18,19,24,25].



**Figure 4.** Output characteristics of (a) conventional  $\text{Ga}_2\text{O}_3$  MOSFET and (b)  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFET. The self-heating effect is considered and compared.



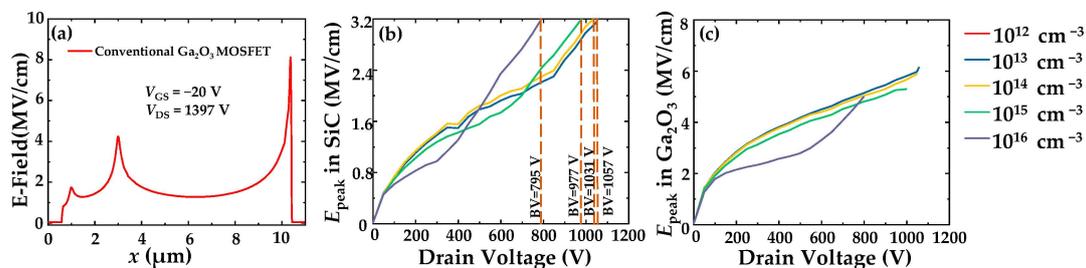
**Figure 5.** Lattice temperature distribution of (a) the  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFET and (b) the conventional  $\text{Ga}_2\text{O}_3$  MOSFET. (c,d) are enlarged channel regions of  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFET and conventional  $\text{Ga}_2\text{O}_3$  MOSFET with temperature distribution displayed, respectively.

## 4. Breakdown Characteristics

### 4.1. SiC Thickness and Doping Concentration

Unlike devices consisting of a single semiconductor material, not only the breakdown in the  $\text{Ga}_2\text{O}_3$  layer but also the breakdown in the SiC layer shall be considered in  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFETs. Although the doping concentration of the SiC layer is lower than that of the  $\text{Ga}_2\text{O}_3$  layer in the design, the coupling effect can result in an electric field peak at the interface of the two materials. As mentioned previously, the critical breakdown field of SiC is much smaller than that of  $\text{Ga}_2\text{O}_3$ , so breakdown may happen in SiC rather than  $\text{Ga}_2\text{O}_3$ . To verify that, the relationship between the breakdown voltage and the doping concentration of the SiC layer was first studied. After that, the impact of the SiC thickness on breakdown voltage was investigated. Since the  $\text{Ga}_2\text{O}_3$  channel has n-type doping, only p-type or semi-insulating SiC substrates can be selected to prevent leakage current. For an n-type drift region, a p-type layer is expected to form the reduced surface electric field (RESURF) effect, which has been applied in Si-based and GaN-based MOSFETs and exhibits a satisfying effect on improving the breakdown voltage [42–44]. The basic principle is to reduce the peak electric field in the drift region and increase the depletion region width, thereby improving the breakdown voltage of the device.

The relationship between the breakdown voltage and the SiC doping concentration is shown in Figure 6. For comparison, the electric field profile of the conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET at breakdown is illustrated in Figure 6a. A breakdown voltage of 1397 V was achieved. The peak electric field in SiC as a function of the drain voltage was shown in Figure 6b, and the corresponding peak electric field in Ga<sub>2</sub>O<sub>3</sub> was shown in Figure 6c. Note that the breakdown voltage is assumed to correspond to the drain voltage at which the electric field peak in Ga<sub>2</sub>O<sub>3</sub> or SiC reaches a critical field strength. As shown in Figure 6b, the peak electric field in SiC increased as the drain voltage increased, and finally, 3.2 MV/cm was achieved. In Figure 6c, the peak electric field in Ga<sub>2</sub>O<sub>3</sub> was far lower than the critical breakdown strength of Ga<sub>2</sub>O<sub>3</sub> (8 MV/cm), indicating a premature SiC breakdown was formed. From Figure 6b, a breakdown voltage of 795 V was obtained with a doping concentration of 10<sup>16</sup> cm<sup>-3</sup>, and a breakdown voltage of 1057 V was achieved with a doping concentration of 10<sup>12</sup> cm<sup>-3</sup>. As the SiC concentration decreases, the breakdown voltage of the MOSFET increases. With a lower doping concentration, the depletion region width in SiC was increased, thereby allowing a greater drain voltage to be withstood. The peak electric field in the SiC substrate can be effectively suppressed at a low doping concentration, leading to premature breakdown.

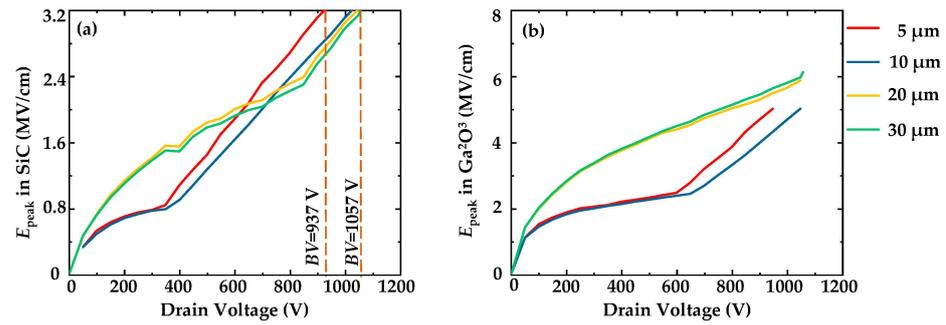


**Figure 6.** (a) Electric field distribution of the conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET at the breakdown. A breakdown voltage of 1397 V is obtained. Peak electric fields in (b) SiC and (c) Ga<sub>2</sub>O<sub>3</sub> as a function of drain voltage with various SiC doping concentrations.

As shown in Figure 6c, a wider depletion region in Ga<sub>2</sub>O<sub>3</sub> was formed with the help of the p-type SiC substrate, and charges in the depletion region were redistributed. As a result, the average electric field intensity in Ga<sub>2</sub>O<sub>3</sub> is lowered, and the peak electric field intensity is reduced. Although the peak electric field in Ga<sub>2</sub>O<sub>3</sub> decreases with the increase in p-type doping concentration in SiC, this is at the expense of a higher peak electric field in SiC. By increasing the doping concentration of SiC, its depletion region is reduced, resulting in an earlier breakdown. As can be seen from Figure 6c, the peak electric field in Ga<sub>2</sub>O<sub>3</sub> is always far below its critical breakdown field. Therefore, the breakdown occurs at the interface of SiC/Ga<sub>2</sub>O<sub>3</sub>. In other words, a lower doping concentration of SiC is favorable.

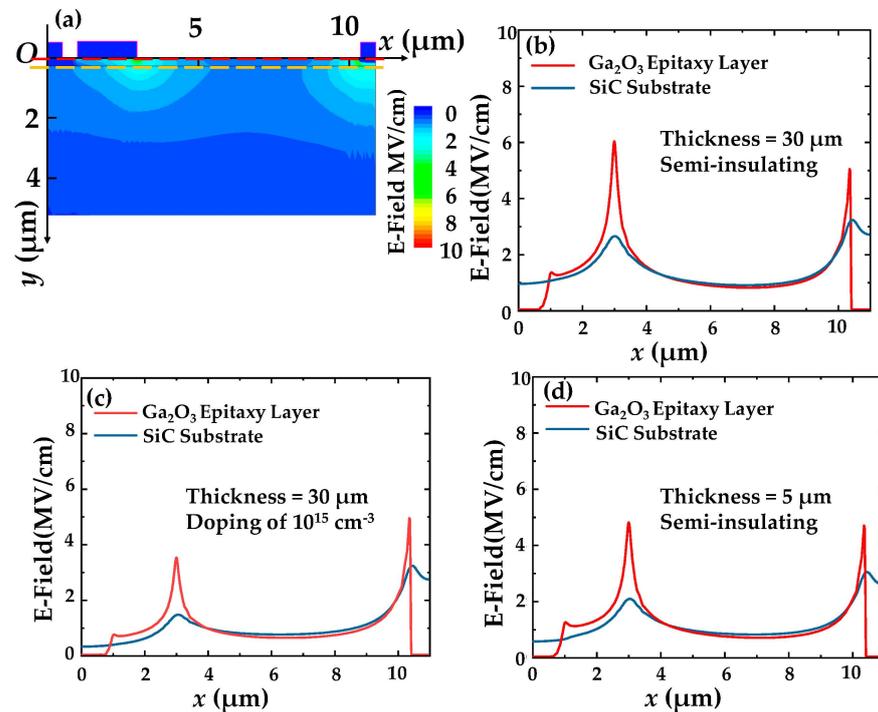
According to theoretical calculations, when the doping concentration in SiC is less than 10<sup>12</sup> cm<sup>-3</sup>, the SiC substrate has already achieved semi-insulation. Therefore, for the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET, the semi-insulating SiC substrate can achieve the maximum breakdown voltage. Although the p-type SiC substrate has a RESURF effect on the Ga<sub>2</sub>O<sub>3</sub> layer, it will cause premature breakdown in the substrate, and will not improve the breakdown performance of the device.

In addition to the substrate doping concentration, according to the RESURF theory [45], the thickness of the SiC also has a great impact on the breakdown voltage. Figure 7 shows the peak electric field in SiC and Ga<sub>2</sub>O<sub>3</sub> as a function of SiC layer thickness. As shown in Figure 7a, with the increase in substrate thickness, the breakdown voltage also increases. However, with a further increase in thickness, i.e., thickness ≥ 20 μm, the breakdown voltage of the device tends to saturate. Figure 7b shows the peak electric field in Ga<sub>2</sub>O<sub>3</sub> at various drain voltages. The electric field in Ga<sub>2</sub>O<sub>3</sub> is higher than that in SiC, yet it is still far below its breakdown limit. As a result, the breakdown voltage of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET is determined to be 1057 V with a thick semi-insulating SiC layer.



**Figure 7.** Peak electric field in (a) SiC and (b) Ga<sub>2</sub>O<sub>3</sub> as a function of drain voltage with different SiC thicknesses.

To further understand the breakdown mechanisms of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET, the electric field distribution at the breakdown is shown in Figure 8. The two-dimensional electric field distribution of the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET is shown in Figure 8a, where the thickness and the doping concentration of SiC are 30 μm and 10<sup>12</sup> cm<sup>-3</sup>, respectively. It is seen that two electric field peaks at the gate edge and the drain edge are formed due to the full depletion. In addition, electric field peaks can be found both in the Ga<sub>2</sub>O<sub>3</sub> layer and the SiC layer, which result from the coupling effect [46]. Specifically, the electric field profiles in the Ga<sub>2</sub>O<sub>3</sub> and in the SiC extracted from Figure 8a are shown in Figure 8b. In this case, the intensity of two electric field peaks in the SiC is similar.



**Figure 8.** The electric field distribution in a Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET. (a) Two-dimensional distribution of the device with a 30 μm semi-insulating SiC. The electric field profiles in (b,c) for Ga<sub>2</sub>O<sub>3</sub> and SiC are extracted from the red cutline and the yellow cutline, respectively. Electric field profiles in Ga<sub>2</sub>O<sub>3</sub> and SiC with (b) 30 μm semi-insulating SiC, (c) 30 μm SiC with a doping concentration of 10<sup>15</sup> cm<sup>-3</sup> and (d) 5 μm semi-insulating SiC.

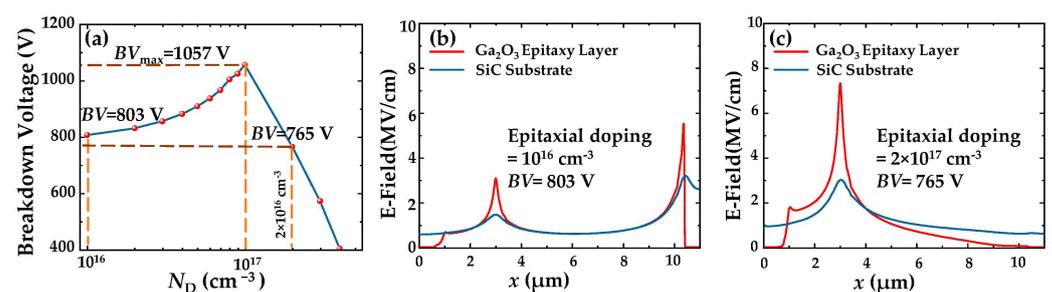
Yet for non-ideal conditions, i.e., higher doping concentration and lower thickness of SiC, a visible difference between the electric field peaks can be observed, indicating a lower average electric field in SiC and a reduced breakdown voltage. The electric field profiles

in SiC and Ga<sub>2</sub>O<sub>3</sub> with a SiC doping concentration of  $10^{15} \text{ cm}^{-3}$  and a SiC thickness of  $30 \text{ }\mu\text{m}$  were shown in Figure 8c. Compared with the electric field profile in Figure 8b, the electric field intensity in SiC is lower. As discussed previously, with a higher SiC doping concentration, depletion is more advanced, and the peak electric field is thus reduced. Similarly, we presented the electric field distribution with a  $5 \text{ }\mu\text{m}$ -thick semi-insulating SiC, as shown in Figure 8d. The profiles of the surface electric fields of SiC and Ga<sub>2</sub>O<sub>3</sub> are shown in Figure 8d. Identical electric field peaks can be found in Ga<sub>2</sub>O<sub>3</sub>, yet the electric field in SiC is lower in comparison with the optimal case in Figure 8b. It is well known that the breakdown voltage can be obtained by integrating an electric field profile. Therefore, the dissimilar electric field peaks in SiC are the main reason for the lower breakdown voltage.

#### 4.2. Epitaxy Thickness and Doping

The thickness and doping concentration of the Ga<sub>2</sub>O<sub>3</sub> epitaxial layer also have a significant impact on the breakdown voltage of the device. Therefore, we used the aforementioned method to further investigate the optimal parameters of the Ga<sub>2</sub>O<sub>3</sub> epitaxial layer in this section. A semi-insulating SiC layer was adopted according to the optimization results. In addition, the doping concentration in Ga<sub>2</sub>O<sub>3</sub> varied from  $1 \times 10^{16}$  to  $5 \times 10^{17} \text{ cm}^{-3}$ , and different thicknesses of Ga<sub>2</sub>O<sub>3</sub> were used in the range from  $0.1 \text{ }\mu\text{m}$  to  $0.5 \text{ }\mu\text{m}$ .

In Figure 9a, we exhibit the breakdown voltage as a function of the Ga<sub>2</sub>O<sub>3</sub> doping concentration. The device achieved the highest breakdown voltage of  $1057 \text{ V}$  at a concentration of  $1 \times 10^{17} \text{ cm}^{-3}$ . When the doping concentration is less than  $1 \times 10^{17} \text{ cm}^{-3}$ , the breakdown voltage slowly increases with a higher doping concentration. However, when the doping concentration is greater than  $1 \times 10^{17} \text{ cm}^{-3}$ , the breakdown voltage of the device decreases sharply. Figure 9b,c shows the electric field distribution profile of the device at a Ga<sub>2</sub>O<sub>3</sub> doping concentration of  $1 \times 10^{16} \text{ cm}^{-3}$  and  $2 \times 10^{17} \text{ cm}^{-3}$ , respectively. At a lower concentration, i.e.,  $1 \times 10^{16} \text{ cm}^{-3}$ , there are two peak electric fields, located below the gate and the drain. Due to the low doping concentration, the Ga<sub>2</sub>O<sub>3</sub> layer was fully depleted, and the electric field intensity close to the drain region was increased. In a conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET, such a low doping concentration is desired since the electric field peak under the gate electrode is reduced, and thus breakdown voltage can be improved. However, for the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET, the electric field distribution in SiC is more vital. It is worth noting that a significant premature breakdown is presented for a lower Ga<sub>2</sub>O<sub>3</sub> doping concentration, and two electric field peaks in SiC were not identical.

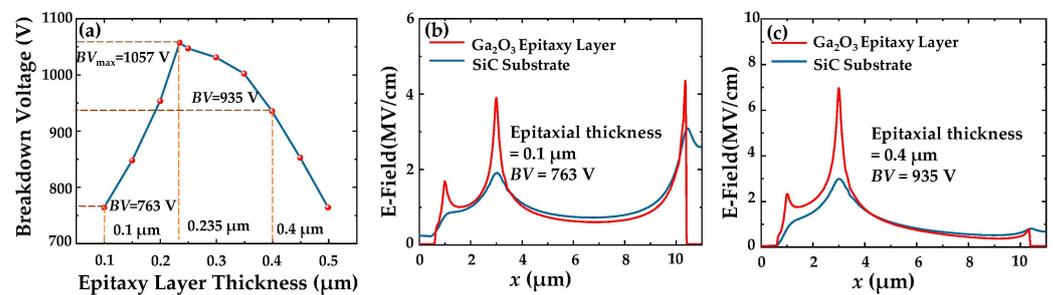


**Figure 9.** (a) The relationship between breakdown voltage and doping concentration of the Ga<sub>2</sub>O<sub>3</sub> epitaxial layer. The electric field profiles at the breakdown with a doping concentration of (b)  $1 \times 10^{16} \text{ cm}^{-3}$  and (c)  $2 \times 10^{17} \text{ cm}^{-3}$ .

As mentioned, the electric field in SiC is coupled with that in Ga<sub>2</sub>O<sub>3</sub>. Therefore, a peak electric field in SiC under the drain can be observed, and it has reached the critical breakdown field. When the concentration is high, i.e.,  $2 \times 10^{17} \text{ cm}^{-3}$ , a partial depletion is introduced in Ga<sub>2</sub>O<sub>3</sub>, leading to the single electric field peak in the SiC layer. It is well known that partial depletion is harmful to the breakdown voltage, which is the main cause of the rapidly decreased breakdown voltage with a high doping concentration of Ga<sub>2</sub>O<sub>3</sub>.

Finally, the relationship between the thickness of the Ga<sub>2</sub>O<sub>3</sub> epitaxial layer and the breakdown voltage was investigated. As shown in Figure 10a, the device achieved a

maximum breakdown voltage of 1057 V at an epitaxial thickness of 0.235  $\mu\text{m}$ , and the breakdown voltage increased as the thickness of the epitaxial layer rose until it exceeded 0.235  $\mu\text{m}$ , after which the breakdown voltage began to decrease. Figure 10b,c shows the electric field profiles of the  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFET with epitaxial thicknesses of 0.1  $\mu\text{m}$  and 0.4  $\mu\text{m}$ , respectively. With a thin epitaxy layer, there are two electric field peaks located under the gate and drain. In  $\text{Ga}_2\text{O}_3$ , a full depletion region was formed. Less carriers are expected in a thin epitaxy layer, and thus it can be fully depleted by the applied drain voltage. Similarly, the two-peaks property is also validated in the SiC layer, which is the main reason for the higher electric peak near the drain side. Consequently, a lower breakdown voltage is obtained. With an optimal thickness, two similar electric field peaks should be introduced. For a thicker  $\text{Ga}_2\text{O}_3$  epitaxial layer, full depletion is hard to perform, and thus the single electric field at the gate edge is observed in Figure 10c. Therefore, we can conclude that the best combination for the  $\text{Ga}_2\text{O}_3$  layer is a doping concentration of  $1 \times 10^{17} \text{ cm}^{-3}$  and a thickness of 0.235  $\mu\text{m}$ .



**Figure 10.** (a) The relationship between breakdown voltage and thickness of the  $\text{Ga}_2\text{O}_3$  epitaxial layer. Electric field distributions at the breakdown with an epitaxial thickness of (b) 0.1  $\mu\text{m}$  and (c) 0.4  $\mu\text{m}$ .

One can learn from the above results that the thermal benefit obtained from the  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFET is verified. However, an early breakdown could be a major hindrance to power devices with a high breakdown voltage. We must admit that the optimal parameters could be varied with different device architectures, such as trench MOSFETs or field-plate MOSFETs. More importantly, to enhance the breakdown voltage of  $\text{Ga}_2\text{O}_3$ -on-SiC MOSFETs, structural engineering can be considered, including the incorporation of field plate techniques, passivation optimization, variation of lateral doping (VLD), and improvement of epitaxial layer quality. These approaches collectively contribute to improving the breakdown characteristics and overall performance of the MOSFETs [47]. However, the major contribution of this work is to identify the existence of premature breakdown arising from the hetero-material with a lower breakdown strength. Our results suggest that a dedicated device design is required to alleviate premature breakdown.

In addition to the device's structural optimization, an alternative approach is to introduce a substrate with high breakdown strength as well as high thermal conductivity, such as AlN. Previous reports have indicated the possibility of heteroepitaxy for AlN/ $\text{Ga}_2\text{O}_3$  [48]. It is also worth noting that the near junction method [8] by using high thermal conductivity passivation, including amorphous diamond, could be effective for lateral power devices.

It should be noted that except for the above discussion regarding the premature breakdown of SiC, the non-ideal interface is another issue that may lead to premature breakdown. When hetero-epitaxy is conducted, lattice mismatch can lead to a non-ideal interface, resulting in the presence of interface traps or dislocations. Under high electric field conditions, interface traps may undermine carrier mobility [49,50]. Furthermore, dislocations introduce structural distortions, leading to localized strain and an electric field peak, thereby affecting the device's performance and reliability. It is essential to assess these interface issues to comprehend material properties, electrical characteristics, and breakdown behavior under high electric field conditions [51,52]. Thereby, further

investigation is much needed to provide the technical basis for product applications of Ga<sub>2</sub>O<sub>3</sub>-based power MOSFETs.

## 5. Conclusions

In this study, the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET was designed and simulated, including its transfer, output, and breakdown characteristics. For on-state performance, a Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET was found to reduce the lattice temperature by nearly 100 °C and increase the drain current by 95%. More importantly, the premature breakdown caused by SiC was studied in this work. By optimizing the structure parameters, including doping concentration and epitaxy thickness, the early breakdown can be well relieved. Compared with p-type SiC, semi-insulating SiC can effectively alleviate SiC premature breakdown, obtaining a higher breakdown voltage. Additionally, a thick (>20 μm) semi-insulating SiC substrate is beneficial to obtain a higher breakdown voltage. As for the Ga<sub>2</sub>O<sub>3</sub> epitaxial layer, under the conditions of a concentration of  $1 \times 10^{17} \text{ cm}^{-3}$  and a thickness of 0.235 μm, a breakdown voltage of 1057 V is achieved, which is 75% of the breakdown voltage for the conventional Ga<sub>2</sub>O<sub>3</sub> MOSFET. In summary, by optimizing the device structure, the Ga<sub>2</sub>O<sub>3</sub>-on-SiC MOSFET can realize superior thermal management performance without sacrificing a significant breakdown voltage.

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