



Article On-State Voltage Drop Analytical Model for 4H-SiC Trench IGBTs

Yanjuan Liu¹, Dezhen Jia¹ and Junpeng Fang^{2,*}

- ¹ The College of Electronic and Information Engineering, Shenyang Aerospace University, Shenyang 110136, China; liuyanjuan@hrbeu.edu.cn (Y.L.); jdz@sau.edu.cn (D.J.)
- ² School of Integrated Circuits, Tsinghua University, Beijing 100084, China
- * Correspondence: fjp18@mails.tsinghua.edu.cn

Abstract: In this paper, a model for the forward voltage drop in a 4H-SiC trench IGBT is developed. The analytical model is based on the 4H-SiC trench MOSFET voltage model and the hole-carrier concentration profile in the N-drift region for a conventional 4H-SiC trench IGBT. Moreover, an on-state voltage drop analytical model is validated using a 2D numerical simulation, and the simulation results demonstrate that there is good agreement between the ATLAS simulation data and analytic solutions.

Keywords: 4H-SiC IGBT; forward voltage drop; analytical model

1. Introduction

In recent years, power semiconductor devices based on 4H-SiC have attracted more attention due to the material's high power and high temperature applications arising from its superior material properties [1–4]. Compared with SiC MOSFETs, SiC IGBTs can achieve a lower forward voltage drop when the blocking voltage is equal to or higher than 10 kV. Although the conductivity modulation effect makes the forward voltage drop lower, the turn-off loss is higher. Therefore, for IGBTs, there is conflict between the on-state voltage drop and turn-off loss. Many researchers have placed much emphasis on how to improve the trade-off relationship between the on-state voltage drop and the turn-off loss of 4H-SiC IGBTs [5–13], such as the adoption of the current storage layer (CSL) [10,11] and the proposed Cluster IGBT (CIGBT) [12,13].

While much research has been undertaken on how to improve the trade-off relationship [5–13], less work has been conducted on the analytical model and theoretical analysis of the static-state (forward voltage drop) and the dynamic-state (turn-off loss) [14–16]. In this paper, based on our previous findings [17–19], an on-state voltage drop analytical model for an n-channel 4H-SiC trench IGBT is developed. Additionally, a 2D numerical simulation using the ATLAS module of Silvaco TCAD [20] is utilized to validate the correctness of the proposed analytical model.

2. Forward Voltage Drop Analytical Model

The forward voltage drop (V_{on}) of a 4H-SiC IGBT is composed of the upper MOS voltage part (V_{MOS}), the N-type voltage blocking layer voltage (V_{drift}), and the built-in potential at junction J_1 (V_{P+N}), which are shown on the left of Figure 1.



Citation: Liu, Y.; Jia, D.; Fang, J. On-State Voltage Drop Analytical Model for 4H-SiC Trench IGBTs. *Crystals* **2022**, *12*, 582. https:// doi.org/10.3390/cryst12050582

Academic Editors: Zeng Liu, Shan Li and Dmitri Donetski

Received: 11 March 2022 Accepted: 18 April 2022 Published: 22 April 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/).

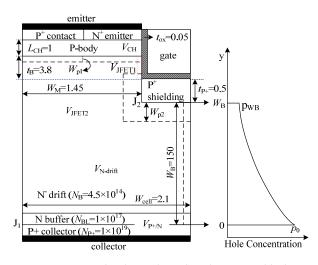


Figure 1. Forward voltage drop distribution and hole concentration profile.

Firstly, the upper MOS voltage part includes three parts: the channel voltage (V_{CH}), the parasitic JFET1 (composed of a P– body and P+ shielding) voltage (V_{JFET1}), and the parasitic JFET2 (composed of P+ shielding in two close cells) voltage (V_{JFET2}). Based on the existing 4H-SiC trench MOSFET voltage model, V_{CH} , V_{IFET1} , and V_{IFET2} can be calculated as:

$$V_{\rm CH} = J_{\rm C} R_{\rm CH,sp} = \frac{J_{\rm C} L_{\rm CH} W_{\rm cell}}{\mu_{\rm inv} C_{\rm ox} (V_{\rm GE} - V_{\rm th(on)})}$$
(1)

$$V_{\rm JFET1} = J_{\rm C} R_{\rm JFET1, sp} = J_{\rm C} \rho_{\rm JFET1} W_{\rm cell} \left(\frac{t_{\rm P+} + W_{\rm p1}}{t_{\rm B} - 2W_{\rm p1}} \right)$$
(2)

$$V_{\rm JFET2} = J_{\rm C} R_{\rm JFET2} = J_{\rm C} \rho_{\rm JFET2} W_{\rm cell} \left(\frac{t_{\rm P+} + W_{\rm p2}}{W_{\rm M} - W_{\rm p2}/2} \right)$$
(3)

So, V_{MOS} can be expressed [21] as:

$$V_{\rm MOS} = V_{\rm CH} + V_{\rm JFET1} + V_{\rm JFET2} \tag{4}$$

where C_{ox} is the specific capacitance of the gate oxide; μ_{inv} is the inversed electron mobility in channel region; ρ is the resistivity; V_{GE} is the applied gate bias; $V_{th(on)}$ is the threshold voltage; and W_{p1} and W_{p2} are the depletion length in the p-body/current storage layer (CSL) and P+ shielding/N-drift junction @ $V_{ce} = 0$ V, respectively. Additionally, the C_{ox} [21], ρ , and $W_{p1/2}$ can be written as:

$$C_{\rm ox} = \frac{\varepsilon_{\rm oxide}\varepsilon_0}{t_{\rm ox}} \tag{5}$$

$$\rho_{\text{JFET1/2}} = \frac{1}{qn\mu_{\text{n}}} = \frac{1}{qN_{\text{CSL/B}}\mu_{\text{n}}} \tag{6}$$

$$W_{\rm p1/2} = \sqrt{\frac{2\varepsilon_{\rm SiC}\varepsilon_0 V_{\rm PN}}{qN_{\rm CSL/B}}} \tag{7}$$

where $\varepsilon_{\text{oxide}}$ and ε_{SiC} are the relative permittivity for the gate oxide and 4H-SiC; ε_0 is the permittivity of free space; μ_n is the electron mobility; $N_{\text{CSL/B}}$ is the doping of CSL (or drift) region; *q* is the amount of electric charge of an electron; and V_{PN} is the built-in potential of the PN junction (about 2.7 V).

Moreover, according to the formula of the PN junction built-in potential, V_{P+N} can be calculated [22] as:

$$V_{\rm P+N} = \frac{kT}{q} \ln\left(\frac{p_0 N_{\rm BL}}{n_{\rm i}^2}\right) \tag{8}$$

In Formula (8), *k* is the Boltzmann constant; *T* is the ambient temperature; n_i is the intrinsic carrier concentration; N_{BL} is the doping of the N buffer region; and p_0 is the hole concentration at junction J_1 .

In order to simplify the analytical model of the voltage dropped on the N-type drift layer, the hole-carrier concentration, which is shown on the right of Figure 1, can be depicted as:

$$p(y) = Ae^{-\frac{y}{L_a}} + B \tag{9}$$

In (9), L_a is the ambipolar diffusion length; and p_0 and p_{WB} , which are the hole concentrations at P+ collector/N-buffer and P+ shielding/N-drift junctions, can be obtained using:

$$p_0 = p(y)|_{y=0} = p(0) = \frac{p_{0,\text{BL}}L_{p,\text{BL}}L_{n,\text{P}+}}{q(D_{p,\text{BL}}p_{0,\text{BL}}L_{n,\text{P}+} + D_{n,\text{P}+}n_{0,\text{P}+}L_{p,\text{BL}})}$$
(10)

$$p_{W_{\rm B}} = p(y)|_{y=W_{\rm B}} = p(W_{\rm B}) = \frac{J_{\rm C}}{qv_{\rm sat}}$$
 (11)

in which $p_{0,BL}$ and $n_{0,P+}$ are the hole and electron concentrations at a state of equilibrium; $D_{p,BL}$ and $D_{n,P+}$ are the diffusion coefficients in the buffer layer and P+ collector region; $L_{p,BL}$ and $L_{n,P+}$ are the diffusion lengths in the buffer layer and P+ collector region; J_C is the total current density; and v_{sat} is the drift velocity of the carriers.

If we replace Equations (10) and (11) into Equation (9), p(y) can be obtained.

By integrating an electric field across the N-type drift region, the N-drift region voltage can be calculated as:

$$V_{\rm drift} = \int_0^{W_{\rm B}} E(y) dy = \int_0^{W_{\rm B}} \frac{J_{\rm p-drift}}{q\mu_{\rm p} p(y)} dy \tag{12}$$

In (12), μ_p is the hole mobility, and $J_{p-drift}$ is the hole current density flowing in the drift region, which is depicted as:

$$J_{\text{p-drift}} = \frac{\mu_{\text{p}}}{\mu_{\text{p}} + \mu_{\text{n}}} \left[J_{\text{C}} - q \left(\frac{\mu_{\text{n}}}{\mu_{\text{p}}} - 1 \right) D_{\text{p}} \frac{dp(y)}{dy} \right]$$
(13)

1...(..)

In (13), D_p is the hole diffusion coefficient.

If we replace Equation (13) into (12), V_{drift} is changed as follows:

$$V_{\text{drift}} = \int_{0}^{W_{\text{B}}} \frac{J_{\text{C}}}{q(\mu_{\text{p}}+\mu_{\text{n}})p(y)} + \frac{(\mu_{\text{n}}-\mu_{\text{p}})D_{\text{p}}\frac{dp(y)}{dy}}{\mu_{\text{p}}(\mu_{\text{p}}+\mu_{\text{n}})p(y)}dy = \frac{J_{\text{C}}}{q(\mu_{\text{p}}+\mu_{\text{n}})\text{B}} \left(W_{\text{B}} + L_{\text{a}}\ln\frac{p(W_{\text{B}})}{p(0)}\right) + \frac{(\mu_{\text{n}}-\mu_{\text{p}})D_{\text{p}}}{\mu_{\text{p}}(\mu_{\text{p}}+\mu_{\text{n}})}\ln\frac{p(W_{\text{B}})}{p(0)}$$
(14)

Then, the forward voltage can be calculated.

3. Simulation Results and Verification

This section describes the simulations carried out to investigate I-V characteristics and verify the forward voltage drop analytical model. The physical parameters of the investigated structure are given in Figure 1. In the simulation, the models utilized were as follows: the bandgap narrowing model (BGN); the AUGER and Shockley–Read–Hall (SRH) models for recombination and carrier lifetime; and doping and temperature-dependent field mobility models (ANALYTIC). Moreover, all the simulations were performed using Fermi–Dirac statistics. Selberherr's impact ionization model was also utilized. In addition, it is worth noting that the simulator was calibrated to the experimental data of ref. [23]. Thus, in this paper, we adopted the same physical parameters as ref. [23]. Moreover, $\tau_{n-buffer}$ was set at 0.1 µs. The effect of τ_{drift} is also discussed.

Figure 2 shows the transfer curve (at $V_{ce} = 4$ V) and the I-V curve (at $V_{GE} = 20$ V). From these graphs, it can be determined that $V_{th(on)}$ is 5.8 V, and V_{on} at $J_C = 100$ A/cm² is 8.68 V. The concentration distribution of the hole carriers at the buffer and drift regions is presented in Figure 3 and compared with analytic solutions obtained by the analytical model (Equation (9)). The analytical model can accurately describe the carrier's concentration distribution, except for region A. The main reason may be explained as follows: Although the hole-carrier concentration is decaying in an exponential manner in both regions, $L_{p,BL}$ is larger than that in the N-drift region. So, in the buffer layer, the minor carrier concentration decreases faster. However, in this paper, we assume that the hole-carrier concentration undergoes an exponential decay from junction J_1 to J_2 , and L_a is the exponential decay index.

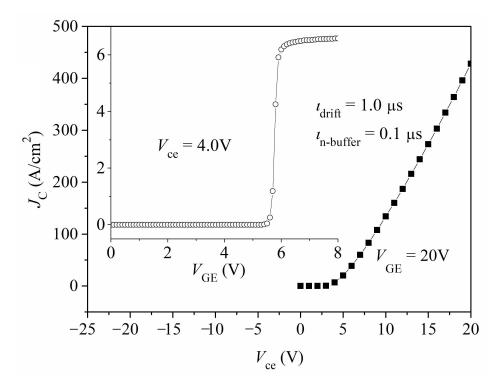


Figure 2. Transfer and I–V characteristics.

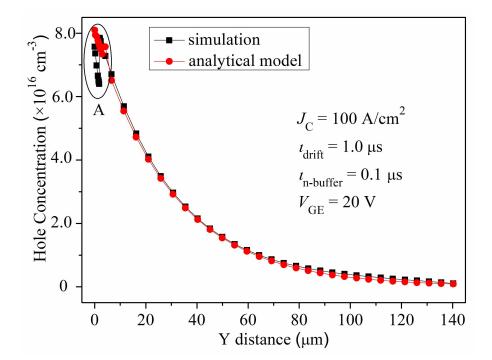


Figure 3. Hole-carrier concentration profile in buffer and drift regions.

The influence of τ_{drift} on V_{on} is given in Figure 4, and is also compared with analytical values. From this figure, it can be seen that the simulation value coincides well with the analytical values at the higher carrier lifetime. The difference between the simulation and analytical values is larger at the lower carrier lifetime, because the built analytical model neglects the influence of carrier recombination occurring in the N-drift region. However, a recombination effect cannot be omitted when the carrier lifetime is lower, causing the appearance of the above-mentioned deviation.

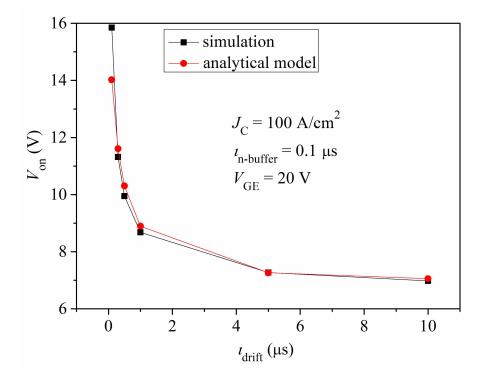


Figure 4. Influence of carrier lifetime in the drift region on forward voltage drop.

4. Conclusions

A forward voltage drop analytical model was developed and investigated. The analytical model considered the hole-carrier concentration profile as a simple exponential form, in order to calculate the N-drift voltage more simply. A 2D numerical simulation was used to verify the correctness of the analytical model. The investigation results demonstrate that the developed model can exactly describe the distribution of the minor carrier concentration, and the analytical values agree well with the simulation results in quantity.

Author Contributions: Conceptualization, Y.L. and J.F.; methodology, Y.L.; software, Y.L., J.F. and D.J.; validation, Y.L. and D.J.; investigation, Y.L. and J.F.; writing—original draft preparation, Y.L.; writing—review and editing, Y.L., D.J. and J.F. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Natural Science Foundation of Liaoning Province, grant number 2021-BS-192 and, in part, by the PhD research startup foundation of Shenyang Aerospace University, grant number 19YB47.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

- 1. Roccaforte, F.; Fiorenza, P.; Greco, G.; Nigro, R.L.; Giannazzoa, F.; Iucolanob, F.; Saggiob, M. Emerging Trends in Wide Band Gap Semiconductors (SiC and GaN) Technology for Power Devices. *Microelectron. Eng.* **2018**, *187–188*, 66–77. [CrossRef]
- Nawaz, M. Predicting Potential of 4H-SiC Power Devices Over 10 kV. In Proceedings of the 2013 IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS), Kitakyushu, Japan, 22–25 April 2013; pp. 1291–1296.
- 3. Kumar, V.; Verma, J.; Maan, A.S.; Akhtar, J. Epitaxial 4H-SiC based Schottky diode temperature sensors in ultra-low current range. *Vacuum* 2020, *182*, 109590. [CrossRef]
- 4. Kumar, V.; Maan, A.S.; Akhtar, J. Barrier height inhomogeneities induced anomaly in thermal sensitivity of Ni/4H-SiC Schottky diode temperature sensor. *J. Vac. Sci. Technol. B* 2014, *32*, 041203. [CrossRef]
- Tang, G.; Tang, X.; Song, Q.; Yang, S.; Zhang, Y.; Zhang, Y.; Zhang, Y. Frequency-Improved 4H-SiC IGBT with Multizone Collector Design. *IEEE Trans. Electron Devices* 2020, 67, 198–203. [CrossRef]
- 6. Wei, J.; Zhang, M.; Jiang, H.P.; Li, B.K.; Chen, K.J. Gate Structure Design of SiC Trench IGBTs for Injection-Enhancement Effect. *IEEE Trans. Electron Devices* 2019, *66*, 3034–3039. [CrossRef]
- Wang, Y.; Yu, C.; Mao, H.; Wu, X.; Su, F.; Li, X.; Yang, J. Low Turn-Off Loss 4H-SiC Insulated Gate Bipolar Transistor with a Trench Heterojunction Collector. *IEEE J. Electron Devices Soc.* 2020, *8*, 1010–1015. [CrossRef]
- Yang, T.; Wang, Y.; Yue, R. SiC Trench MOSFET with Reduced Switching Loss and Increased Short-Circuit Capability. *IEEE Trans. Electron Devices* 2020, 67, 3685–3690. [CrossRef]
- Wen, Z.-X.; Zhang, F.; Shen, Z.-W.; Chen, J.; He, Y.-W.; Yan, G.-G.; Liu, X.-F.; Zhao, W.-S.; Wang, L.; Sun, G.-S.; et al. Design and Fabrication of 10-kV Silicon-Carbide p-channel IGBTs with Hexagonal Cells and Step Space Modulated Junction Termination Extension. *Chin. Phys. B* 2019, 28, 068504. [CrossRef]
- 10. Chowdhury, S.; Hitchcock, C.; Stum, Z. 4H-SiC n-Channel Insulated Gate Bipolar Transistors on (0001) and (000-1) Oriented Free-Standing n– Substrates. *IEEE Electron Device Lett.* **2016**, *37*, 317–320. [CrossRef]
- Ryu, S.; Capell, C.; Van Brunt, E. Ultra High Voltage MOS Controlled 4H-SiC Power Switching Devices. Semicond. Sci. Technol. 2015, 30, 084001. [CrossRef]
- Menon, K.G.; Nakajima, A.; Ngwendson, L. Performance Evaluation of 10-kV SiC Trench Clustered IGBT. *IEEE Electron Device* Lett. 2011, 32, 1272–1274.
- 13. Menon, K.G.; Narayanan, E.M.S. Numerical Evaluation of 10-kV Clustered Insulated Gate Bipolar Transistor in 4H-SiC. *IEEE Trans. Electron Devices* **2013**, *60*, 366–373. [CrossRef]
- Lee, M.C.; Huang, A.Q. An Injection Efficiency Model to Characterize the Injection Capability and Turn-off Speed for >10 kV 4H-SiC IGBTs. *Solid-State Electron.* 2014, 93, 27–39. [CrossRef]
- 15. Wang, H.Y.; Su, M.; Sheng, K. Theoretical Performance Limit of the IGBT. IEEE Trans. Electron Devices 2017, 64, 4148–4192.
- 16. Hohannesson, D.; Nawaz, M.; Norrga, S.; Anders, H.; Nee, H.-P. Static and Dynamic Performance Prediction of Ultrahigh-Voltage Silicon Carbide Insulated-Gate Bipolar Transistors. *IEEE Trans. Power Electron.* **2021**, *36*, 5874–5891. [CrossRef]
- 17. Liu, Y.; Wang, Y.; Yu, C.; Fei, C. 4H-SiC Trench IGBT with Lower On-State Voltage Drop. *Superlattices Microstruct.* 2017, 103, 53–63. [CrossRef]
- Liu, Y.-J.; Wang, Y.; Hao, Y.; Yu, C.-H.; Cao, F. 4H-SiC Trench IGBT with Back-Side n-p-n Collector for Low Turn-Off Loss. *IEEE Trans. Electron Devices* 2017, 64, 488–493. [CrossRef]
- 19. Liu, Y.-J.; Wang, Y.; Hao, Y.; Fang, J.P.; Shan, C.; Cao, F. A Low Turn-Off Loss 4H-SiC Trench IGBT with Schottky Contact in the Collector Side. *IEEE Trans. Electron Devices* **2017**, *64*, 4575–4580. [CrossRef]
- 20. Silvaco Int. Two Dimensional Device Simulation Program; Silvaco Int.: Santa Clara, CA, USA, 2012.
- Jayant Baliga, B. Silicon Carbide Power Devices, 3rd ed.; 5 Toh Tuck Link; World Scientific Publishing Co., Pte. Ltd.: Singapore, 2006; pp. 343–345.
- Jayant Baliga, B. Fundamentals of Power Semiconductor Devices, 3rd ed.; 5 Toh Tuck Link; World Scientific Publishing Co., Pte. Ltd.: Singapore, 2008; pp. 208–215.
- Usman, M.; Nawaz, M. Device design assessment of 4H–SiC n-IGBT—A simulation study. Solid-State Electron. 2014, 92, 5–11. [CrossRef]