



Article Seeding-Layer-Free Deposition of High-k Dielectric on CVD Graphene for Enhanced Gate Control Ability

Yunpeng Yan ^{1,2}, Songang Peng ^{1,3,*}, Zhi Jin ^{1,*}, Dayong Zhang ^{1,3} and Jingyuan Shi ¹

- ¹ High-Frequency High-Voltage Device and Integrated Circuits R&D Center, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China; yanyunpeng@ime.ac.cn (Y.Y.); zhangdayong1@ime.ac.cn (D.Z.); shijingyuan@ime.ac.cn (J.S.)
- ² University of Chinese Academy of Sciences, Beijing 100049, China
- ³ Key Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
- * Correspondence: pengsongang@ime.ac.cn (S.P.); jinzhi@ime.ac.cn (Z.J.)

Abstract: The gate insulator is one of the most crucial factors determining the performance of a graphene field effect transistor (GFET). Good electrostatic control of the conduction channel by gate voltage requires thin gate oxides. Due to the lack of the dangling bond, a seed layer is usually needed for the gate dielectric film grown by the atomic layer deposition (ALD) process. The seed layer leads to the high-quality deposition of dielectric films, but it may lead to a great increase in the thickness of the final dielectric film. To address this problem, this paper proposes an improved process, where the self-oxidized Al_2O_3 seed layer was removed by etching solutions before atomic layer deposition, and the Al_2O_3 residue would provide nucleation sites on the graphene surface. Benefiting from the decreased thickness of the dielectric film, the transconductance of the GFET using this method as a top-gate dielectric film deposition process shows an average 44.7% increase compared with the GFETs using the standard Al evaporation seed layer methods.

Keywords: graphene; seedinglayer; Al₂O₃; carrier mobility; transistor

1. Introduction

Graphene, a two-dimensional material composed of a single atomic layer of carbon, was discovered in 2004 and has attracted much attention [1]. Benefiting from its atomic thin film layer and extremely high carrier mobility, graphene is considered to be one of the most promising candidates for extending Moore's law in future nanoelectronics. For example, a graphene field effect transistor (GFET) with high cut-off frequency (407 GHz) and maximum oscillation frequency (200 GHz) has been fabricated [2,3]. In addition, a graphene frequency multiplier and a monolithic integrated receiver on eight-inch wafers have also been reported [4,5]. In GFET, the conductance between source and drain is modulated by a gate. Hence, the gate insulator is quite crucial in determining the performance of the GFET. In order to improve the performance and integrated density of the integrated circuits based on graphene, the channel length should be scaled down. To maintain strong gate control on conduction channel during the dimension scaling down, an increasingly thinner gate oxide is required for improving the drain-current response of the transistor to the applied gate voltage, and to avoid the short channel effect [6]. As a result, the deposition of an ultrathin, high-k gate dielectric layer with nanoscale thickness, and few pin holes on the graphene is necessary [7].

In conventional silicon processes, the dielectric layer of transistors with top-gate structures is often deposited by evaporation, sputtering, and chemical vapor deposition. Unfortunately, the above methods may not be suitable for the gate dielectric deposition of GFET. This can be attributed to two reasons. One is that the regular deposition processes discussed above usually cause difficulty in obtaining a dielectric layer with the required



Citation: Yan, Y.; Peng, S.; Jin, Z.; Zhang, D.; Shi, J. Seeding-Layer-Free Deposition of High-k Dielectric on CVD Graphene for Enhanced Gate Control Ability. *Crystals* **2022**, *12*, 513. https://doi.org/10.3390/ cryst12040513

Academic Editor: Dmitri Donetski

Received: 8 February 2022 Accepted: 1 April 2022 Published: 7 April 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). precision and thickness. The other reason is that the deposition process may introduce great damage to the graphene film. Therefore, it is an urgent requirement to deposit high-quality gate dielectric films on the graphene surface without significantly damaging the graphene structure or deteriorating the graphene properties.

Atomic layer deposition (ALD) is an important technique for depositing ultrathin dielectric films. The sample was exposed to a mixed gas reaction atmosphere. The kind of reaction gases, grown temperature, and grown cycles can be precisely controlled. Due to the self-limiting reaction of the chemical source on the material surface, the ALD process enables precise thickness control and excellent uniformity of the dielectric film over large areas [8]. Compared with other processes, the ALD process usually works at lower temperatures and therefore does not tend to introduce additional defects on the graphene. Due to these advantages, ALD is the best choice for depositing dielectric layers on graphene surfaces.

However, there are still some challenges for the atomic layer deposition of high-k film on a graphene surface. For example, the surface of graphene is chemically inert and hydrophobic. Therefore, the graphene lacks dangling bonds, which are necessary for the atomic layer deposition process. The high-k dielectric film is difficult to nucleate on graphene through the direct ALD deposition process. Previous reports have illustrated that the quality of the deposited film strongly depends on the synthesis method of graphene. In the case of the exfoliated graphene, the direct ALD deposition process will lead to a nonuniform coverage of the film on the graphene. The region at the step edge is usually preferentially covered [9]. The coverage of the ALD dielectric film on graphene grown by chemical vapor deposition (CVD) shows a significant increase due to some dangling bonds induced by defects and wrinkles during transfer. However, the dielectric film is still discontinuous [10]. To overcome this issue, various surface preparation techniques have been proposed. Lin et al. [11] used NO₂ to functionalize graphene. The functional layer introduces a large number of dangling bonds on the graphene surface and leads to a uniform ALD dielectric film. However, the breakage of C-C bonds during the NO₂ function process will result in a significant degeneration of carrier mobility for graphene [12]. Zhang et al. [13] also obtained uniform Al_2O_3 films on the graphene surface through controlling the growth temperature and choosing a suitable purging time in the ALD process. However, the overdependence on the experimental conditions could significantly affect the reproducibility of the experiments due to the extreme sensitivity of 2D materials to environmental changes. Cao et al. [14] and Zheng et al. [15] achieved uniform ALD dielectric films on the graphene surface by utilizing the pre-water treatment. In this method, four cycles of pre-water treatment provided uniform nucleation sites for ALD, resulting in uniform Al₂O₃ films with a dielectric constant of 7.2 and a breakdown critical electrical field of 9 MV/cm. However, the bonding of the CVD graphene and substrate was poor, and the pre-water treatment can lead to graphene detachment from the substrate. Meanwhile, there are few related studies, and the stability of the conditions needs to be further explored [16]. In addition, various kinds of polymers have been used as ALD seed layers, such as NFC [7], PTCDA [17], and BCB [18]. However, the polymer layers tend to be thicker and have lower dielectric constants, which can significantly reduce the gate capacitance and control capability. Moreover, the polymer layers may introduce unintentional doping in graphene. Recently, the metal oxide seed layer has been introduced into the fabricating process of top-gated GFETs for ALD dielectric deposition [19]. The thin nucleation layer of oxidized Al was deposited on the graphene before the ALD process. Using this method, the dielectric grown by the ALD process can have few pinholes. However, due to the high surface mobility of aluminum atoms on graphene, the Al metal deposited by e-beam evaporation tends to aggregate and form clusters. In order to cover the entire graphene surface, high critical thickness of the aluminum seed layer is needed [20]. Due to the oxidation ratio of the Al metal greater than 1, the actual thickness of an Al_2O_3 film formed by the Al natural oxidation process will be expanded [21]. In addition, the incompletely oxidized

seed layer may introduce some charged impurities, which enhance the electron scattering at the graphene surface. These factors lead to the degeneration of the device performance.

In this paper, the high-k dielectric deposition method in GFET using alumina residual as a seed layer was proposed. Firstly, the Al metal film was deposited on the surface of the graphene. After the Al was naturally oxidized, it was removed by ammonia. Subsequently, the ultrathin Al_2O_3 film was deposited by ALD and the continuous ultrathin dielectric film was thus formed. The surface morphology of graphene samples before and after the atomic layer deposition was observed by scanning electron microscopy (SEM) and atomic force microscopy (AFM). Raman analysis showed that the treatment process would not introduce additional defects in the graphene. Finally, top-gate graphene transistors using the regular process and the improved process were fabricated. The electrical properties of the devices were measured at room temperature using the Keithley 4200 semiconductor parameter analyzer. The gate transconductance (g_m)of our GFET was increased by 44.7% compared with that using the regular dielectric deposition method, in which a metal oxide film was used as a seed layer. The increasing g_m indicates improved gate control capability of our GFET.

2. Experiment

The monolayer graphene used in our study was synthesized by chemical vapor deposition (CVD). The graphene film was transferred onto Si substrates with a 300 nm-thick SiO₂ layer via the PMMA-assisted transfer method. Aluminum films with 2 nm, 5 nm, and 10 nm thickness were deposited on the surface of graphene by e-beam evaporation and exposed in air to form self-oxidized Al_2O_3 . Then, the surface morphology of graphene before and after atomic layer deposition was analyzed by SEM and AFM.

In the former reports, the Al metal oxide layer on graphene was naturally oxidized as the seed layer for the ALD process. However, the self-oxidized Al_2O_3 seed layer may lead to the unwanted increase in dielectric film thickness and introduce some extra charged scatters. In this study, the self-oxidized Al_2O_3 layer was removed and its residue on the graphene surface acted as the seed layer for the ALD process. The self-oxidized Al_2O_3 film was etched with different solutions, solution A (1 partH₃PO₄:10 part DI water) and solution B (1 part 36% NH₄OH:10part DI water), at room temperature. The residues provided nucleation sites on the graphene surface for the following ALD process. The self-oxidized Al_2O_3 layers with the different thickness of 2 nm, 5 nm, and 10 nm were chosen to investigate the suitable dielectric growing condition. The self-oxidized Al_2O_3 films were removed by solution B. Subsequently, all samples were carried into a commercial ALD reactor (BENEQ TFS 200) and 10 nm-thick Al_2O_3 was deposited at 200 °C using Trimethylaluminum (TMA) and water as precursors.

The quality of the final dielectric film after atomic layer deposition was analyzed by SEM. Meanwhile, Raman spectroscopy (LabRAM HR Raman system with a laser wavelength of 473 nm) was used to estimate the defects of graphene during the whole process.

In order to study the effect of the modified process in the device, top-gated graphene transistors were fabricated using our modified process and the standard Al seed layer process, respectively. The electrical measurements of GFETs were measured at room temperature using the Keithley 4200 semiconductor parameter analyzer.

3. Results and Discussion

Figure 1 presents the SEM image of the surface of Al_2O_3 deposited on the graphene without a seed layer. The Al_2O_3 film is patchy and discontinuous on the chemically inert graphene, which can be contributed to the lack of dangling bonds in the completed lattice area. For the CVD graphene, wrinkles and defects were introduced by the growing and transfer process. The dangling bonds, originating from the wrinkles and defects, provided the nucleation for the ALD deposition. The Al_2O_3 film with large pinholes is not suitable for subsequent top-gate GFET fabrication.



Figure 1. SEM image of the direct Al₂O₃ ALD on CVD graphene.

In this paper, the alumina residual layer, originating from the removed naturally oxidized Al film, was the seed layer for the ALD process. The Al films with different thicknesses of 2 nm, 5 nm, and 10 nm were first grown on the graphene surface, and then exposed in air to form self-oxidized Al₂O₃. The surface morphologies were analyzed by SEM and AFM, respectively (seen in Figure 2a-c). Owing to the high mobility, the aluminum atoms on the graphene surface tend to form island clusters. Hence, a large number of pinholes and cracks were observed in the seed layer, which was formed by a 2 nm Al film on graphene. However, the coverage of the seed layer can be improved as the thickness of the Al film increases. Such improvement is even more notable on the 10 nm seed layer, as shown in Figure 2c. The root mean square (RMS) roughness values of the 2 nm, 5 nm, and 10 nm seed layer surfaces were measured by AFM, which were 1.192 nm, 1.108 nm, and 1.61 nm, respectively. The lowest roughness was found on the 5 nm seed layer surface, which can be attributed to the effect of increased alumina coverage being greater than the effect of the increased crack depth. As the thickness of the seed layer increased, the size of the alumina clusters also gradually increased, which meant that the surface of the seed layer presented the highest roughness at 10 nm. The 10 nm Al_2O_3 film was further deposited on each seed layer by the ALD process. The surface morphologies of the final dielectric films are shown in Figure 2d-f. It can be found in Figure 2d that, for the 2 nm seed layer, the obtained dielectric is inhomogeneous, and a large number of pinholes can be observed on the film surface. However, it can be seen from Figure 2e,f that closed dielectric films can be obtained on the seed layers of 5 nm and 10 nm, which is mainly attributed to the increased coverage of the seed layer. Therefore, the fabrication of graphene transistors requires aluminum films at least 5 nm thick as seed layers for the standard Al evaporation methods.

Figure 3 shows the Raman spectra of pristine graphene (black line) as well as the graphene after deposition of 2 nm (red line), 5 nm (green line), and 10 nm (blue line) Al films bye-beam evaporation and natural oxidation to Al_2O_3 seed layers in air, respectively. The baselines of the pristine graphene and the graphene with a 2 nm alumina seed layer are relatively flat over the entire range of measurements. In contrast, the graphene with 5 nm and 10 nm alumina seed layers show significant background signals, indicating the presence of incompletely oxidized aluminum metal in the 5 nm and 10 nm seed layers. The incompletely oxidized aluminum particles could generally introduce strong electron scattering in graphene and lead to the deterioration of carrier mobility.



Figure 2. SEM images of different thicknesses Al films deposited by e-beam evaporation on the CVD graphene surface and naturally oxidized to Al_2O_3 in air: (a) 2 nm; (b) 5 nm; (c) 10 nm. SEM images of corresponding samples after further ALD of 10 nm Al_2O_3 : (d) 2 nm; (e) 5 nm; (f) 10 nm.



Figure 3. Raman spectra of pristine graphene (black line) as well as the graphene after deposition of 2 nm (red line), 5 nm (green line), and 10 nm (blue line) Al films by e-beam evaporation and natural oxidation to Al₂O₃ seed layers in air, respectively.

As mentioned previously, the Al₂O₃ seed layer limits the minimal possible thickness of dielectrics and may also introduce extra scattering centers. In order to avoid this adverse effect, we attempt to remove the Al_2O_3 seed layer from the graphene surface using an etching solution. The alumina residual provides the nucleation sites for the following ALD process. Solution A (1 partH₃PO₄:10 part DI water) and solution B (1 part 36%NH₄OH:10 part DI water) were used as etching solutions, respectively. Generally, alumina does not react with ammonia, but the ultrathin Al₂O₃ films can be etched by ammonia solution. Figure 4a shows the graphene surface of 2 nm self-oxidized Al_2O_3 seed layer etched by solution A at room temperature for 5 min. Figure 4b–d show the 2 nm, 5 nm, and 10 nm self-oxidized Al₂O₃ seed layers, etched by solution B at the same conditions. It can be clearly seen that the Al_2O_3 film can be removed by both solution A and solution B. The residues of which would be retained on the graphene surface previously covered by Al₂O₃. The residues of the self-oxidized Al₂O₃ films can provide the necessary nucleation sites for subsequent ALD process. The surface morphologies of the residue-seeded Al₂O₃, treated by solution A and solution B, are shown in Figure 4e,f. It can be seen that the Al_2O_3 film, deposited on the seed layer, treated by solution B, exhibited higher quality with fewer

pinholes compared with that treated by solution A. This may be attributed to the following reason. Because of the more active reaction between alumina and H_3PO_4 compared with that between ammonia and H_3PO_4 , less residue will be left on the surface of the graphene after the etching process with solution A than solution B. The inadequate enucleation sites meant that the ALD Al_2O_3 film deposition was of poor quality. The effect of the removed seed layer thickness on the Al_2O_3 dielectric layer was further investigated. The graphene samples covered with 5 nm and 10 nm Al_2O_3 seed layers were etched by solution B. Then, the 10 nm ALD Al_2O_3 layer was deposited on the graphene. Figure 4f–h show the SEM images of the surface morphology of the Al_2O_3 dielectric layers for different thickness seed layers etched by solution B. The number of pinholes decreases as the thickness of the removed seed layer can provide enough nucleation sites for the subsequent ALD process and lead to a good uniformity of Al_2O_3 film. However, the number of particles that are not completely removed also increases with the thickness of the seed layer, which may lead to an increased roughness of the dielectric film.



Figure 4. SEM images of samples etched with different conditions for 5 min at room temperature: (a) the etching of 2 nm self-oxidized Al_2O_3 with solution A; (b) the etching of 2 nm self-oxidized Al_2O_3 with solution B; (c) the etching of 5 nm self-oxidized Al_2O_3 with solution B; (d) the etching of 10 nm self-oxidized Al_2O_3 with solution B. SEM images of corresponding samples after further ALD of 10 nm Al_2O_3 : (e) condition a; (f) condition b; (g) condition c; (h) condition d.

Raman spectra further confirmed that no extra defects were generated in the graphene with the seed layer etching process. Figure 5 shows the Raman spectra of graphene for different process steps during the deposition of the dielectric film. For the pristine graphene transferred to the SiO_2/Si substrate, the G and 2D peaks in the Raman spectra are located at 1587 cm⁻¹ and 2708 cm⁻¹, respectively. Usually, the G and 2D peaks of graphene are at 1580 cm⁻¹ and 2700 cm⁻¹, respectively. However, the blueshifts of the G peak and the 2D peak of graphene were observed in our sample. The blue shift of the Raman peak indicates increased phonon energy in graphene, which can be attributed to the doping effect originating from the absorption of water in the air during the transfer process [22–26]. In addition, the intensity ratio of the 2D peak to the G peak (I_{2D}/I_G) in the Raman spectra is estimated to be 2.13, which indicates that the graphene in the experiment is a single layer. It can be seen from the figure that a D peak also appears near the position of 1370 cm⁻¹, indicating the presence of point defects or structural disorders in the graphene. The disorders may originate from the wrinkles generated during the transfer process [27]. After the graphene surface was covered by the 2 nm Al_2O_3 film, deposited by electron beam evaporation, the intensity of all peaks in the Raman spectra became weaker. The 2D peak shifted left, to the position of 2705 cm⁻¹. The redshift of the 2D peak may be due to the electron doping of graphene caused by Al₂O₃ film. The extra electrons mainly originate from the negative charge induced in graphene by Al³⁺ in alumina. After the etching of 2 nm Al_2O_3 by solution B, the position of the 2D peak in the corresponding Raman spectra

shifted right to 2706 cm⁻¹, but it was still lower than 2708 cm⁻¹ in the original graphene. The result suggests that some residues of Al_2O_3 still existed on the graphene surface. It should be noted that the intensity ratio of the D-peak to the G-peak (I_D/I_G) in the Raman spectra of graphene did not change significantly before and after the etching process, which indicates that the graphene was not damaged and reserved its original properties. The subsequent ALD deposition made the position of the 2D peak shift slightly left again, to 2705 cm⁻¹.



Figure 5. Raman spectra of graphene measured for different processes steps during the deposition of the dielectric film: pristine graphene (black line); 2 nm Al film deposited by e-beam evaporation on the graphene surface and naturally oxidized to alumina in air (red line); the etching of 2 nm Al_2O_3 with solution B for 5 min at room temperature (green line); the ALD of 10 nm Al_2O_3 (blue line).

The top-gated graphene field effect transistor was further fabricated using our improved high-k dielectric deposition method. First, the active region of graphene was etched by oxygen plasma to isolate the device. Then, the source and drain electrodes were defined using regular lithography followed by e-beam evaporation of Ti/Au (20/200 nm) metal contacts, and the lift-off process. Subsequently, a 10 nm Al film was deposited on the graphene surface by electron-beam evaporation and naturally oxidized in air to form Al₂O₃, which was then removed by solution B. An additional Al₂O₃ film (10 nm) was grown as the top-gate dielectric by ALD. Finally, the Ti/Au (20/200 nm) top-gate electrode was fabricated. We also prepared the graphene transistor using the regular process with the seed layer of 5 nm and an additional Al₂O₃ film of 10 nm. Figure 6a,b show optical images of top-gate graphene transistors fabricated using the improved process and the regular process, respectively. The gate length and gate width of GFET were 2.5 μ m and 40 μ m, respectively.

The electrical characteristics of both graphene transistors were measured by the Keithley 4200 semiconductor parameter analyzer at room temperature. Figure 6c shows the output characteristics of top-gate graphene transistors fabricated by the improved (blue line) and regular (red line) processes, respectively. The drain voltage (V_{DS}) scanned from 0 V to 1 V. The top-gate voltage (V_G) swept from -2 V to 2 V. It can be observed that the drain currents of both devices showed almost linear correlation with the drain voltages, and no current saturation occurred in the measured ranges. The linear relationship between I_{DS} and V_{DS} was attributed to the zero-gap band structure of the graphene. However, in some cases, due to the presence of both carriers in the graphene channel, the drain current will first enter saturation, and then enter the secondary linear region, which is known as the "kink" effect [28]. When the drain voltage is kept constant, the drain current of both devices decreases as the gate voltage increases. This is because when the gate voltage is in the range of -2V to 2V, the graphene transistor works in the branch of the hole conducting, and the number of hole carriers decreases gradually with the increase gate voltage. Under the same conditions, the drain current of the improved device was significantly larger than that of the regular device. The increasing drain current of the GFET fabricated by improved dielectric deposition method can be attributed to the enhanced gate control capability induced by the thinner dielectric film. Benefiting from the enhanced gate control capability, the number of carriers in the graphene channel increased. Figure 6d shows the transfer characteristics of top-gate graphene transistors prepared using the improved (blue line) and regular (red line) processes at different drain biases of 1.5 V, 1.75 V, and 2 V. Generally, the transfer characteristic curve of a standard GFET presents a "V" shape. The conductance of GFET in the positive direction of the curve is controlled by electrons, while that in the negative direction of the curve is controlled by holes [29]. However, our GFET only showed the hole branch in the measurement range. This indicates that our GFET was p-type doped, which can be attributed to the photoresist residue and water adsorption on graphene.



Figure 6. Optical images of top-gate graphene transistors: (**a**) the improved device; (**b**) the regular device. (**c**) The output characteristics of top-gate graphene transistors fabricated by the improved (blue line) and regular (red line) processes, respectively. The drain voltage (V_{DS}) scans from 0 V to 1 V and the top-gate voltage (V_G) sweeps from -2 V to 2 V. (**d**) The comparison of transfer characteristic curves of improved device (blue line) and regular device (red line) at different V_{DS} of 1.5 V, 1.75 V, and 2 V. Inset: the corresponding transconductance (g_m) as a function of gate voltage (V_{TG}). (**e**) The top-gate leakage current (I_{GS}) as a function of V_{TG} for the improved device and the regular device at different V_{DS} of 1.5 V, 1.75 V, and 2 V.

The transconductance (g_m) specifies the current response of the transistor to a small modulation of the gate voltage. It is a key parameter for the radio frequency performance of GFETs. The g_m can be calculated as the derivative of I_{DS} with respect to V_G ($g_m = dI_{DS}/dV_G$). The inset of Figure 6d shows the variation of the transconductance as a function of gate voltage for the improved GFET (blue line) and regular GFET (red line) at different drain biases of 1.5 V, 1.75 V, and 2 V. Respectively, the peak values of g_m in the regular GFET were 1.57 mS, 1.68 mS, and 1.77 mS, while that of improved device were 2.18 mS, 2.43 mS, and 2.68 mS, with an average enhancement of 44.7%, showing the apparent improvement by adopting this new dielectric deposition method. In addition, the field effect carrier

mobility of a GFET(μ) can be estimated through $\mu = g_m L/V_{DS} W C_{OX}$ [29–31]. The L is the gate length, W is the total gate width, and C_{OX} is the capacitance per unit area of the oxide layer. The dielectric constant of alumina is determined as 7.9 (seen in the Supplementary Materials [19,32]). Considering the dielectric layer thicknesses of 10 nm and 15 nm for the improved and regular devices, respectively, their capacitances per unit area of oxide layer can be obtained as 7×10^{-3} F/m² and 4.67×10^{-3} F/m², respectively. The hole mobility of both devices can be calculated as 119.6 cm²/Vs and 118.4 cm²/Vs at V_{DS} = 2 V, which are approximately equal. This suggests that the improved process of growing ALD dielectric layer using Al₂O₃ residues proposed in this paper does not lead to the degradation of graphene carrier mobility. Top-gate leakage currents were also measured in both devices. Figure 6e shows the top-gate leakage current (I_{GS}) as a function of V_{TG} for the improved device and the regular device at different V_{DS} of 1.5 V, 1.75 V, and 2 V. It can be seen that the I_{GS} of both devices was only several nA in the measurement range from -1.5 V to 1.5 V, and even though the gate dielectric thickness of the improved device was 5 nm less than that of the regular device, its insulation did not deteriorate significantly within the range of error. These indicate a good quality of the top-gate dielectric Al₂O₃ film fabricated by our new dielectric deposition method.

4. Conclusions

In summary, we developed a new method for metal oxide ALD deposition on graphene and grew high-quality dielectric films on the graphene surface using the residues left after the self-oxidized Al₂O₃ was removed. Moreover, we confirmed the effect of different etching solutions for treating the Al₂O₃ and analyzed the effect of the thickness of the removed seed layer on the subsequent ALD growth. The results of Raman spectra confirmed that the proposed process introduced no additional defects into the graphene. We further fabricated the top-gate graphene transistors using the improved process and the regular process and measured the electrical properties of both devices with the Keithley 4200 semiconductor parameter analyzer, demonstrating that the carrier mobility of graphene does not deteriorate significantly during the process. Most importantly, the improved process is simple to use and compatible with existing processes. Benefiting from the thinner dielectric film, the transconductance of the GFET using this method as top-gate dielectric film deposition process showed a 51% increase compared with the GFETs using standard Al evaporation seed layer methods. Our study paves the way for novel high-performance graphene transistor technology.

Supplementary Materials: The following supporting information can be downloaded at: https: //www.mdpi.com/article/10.3390/cryst12040513/s1. Figure S1: (a) The top-gated transfer characteristics at several back gate voltages (V_{BG}) varying from -20 V to 20 V with a drain bias of 0.1 V. (b) The Dirac voltage varies linearly with the top and back gate voltages. References [19,32] are cited in the Supplementary Materials.

Author Contributions: Conceptualization, Y.Y., S.P., and Z.J.; software, D.Z.; validation, J.S.; formal analysis, S.P.; investigation, Y.Y.; resources, S.P.; data curation, Y.Y.; writing—original draft preparation, Y.Y.; writing—review and editing, S.P.; visualization, Z.J.; supervision, D.Z.; project administration, S.P.; funding acquisition, S.P. All authors have read and agreed to the published version of the manuscript.

Funding: Youth Innovation Promotion Association of Chinese Academy of Sciences.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: This work was financially supported by Youth Innovation Promotion Association of Chinese Academy of Sciences.

Conflicts of Interest: The authors declare no conflict of interest.

References

- Novoselov, K.S.; Geim, A.K.; Morozov, S.V.; Jiang, D.; Zhang, Y.; Dubonos, S.V.; Grigorieva, I.V.; Firsov, A.A. Electric field effect in atomically thin carbon films. *Science* 2004, 306, 666–669. [CrossRef] [PubMed]
- 2. Yu, C.; He, Z.Z.; Li, J.; Song, X.B.; Liu, Q.B.; Cai, S.J.; Feng, Z.H. Quasi-free-standing bilayer epitaxial graphene field-effect transistors on 4H-SiC (0001) substrates. *Appl. Phys. Lett.* **2016**, *108*, 013102. [CrossRef]
- 3. Wu, Y.; Zou, X.; Sun, M.; Cao, Z.; Wang, X.; Huo, S.; Zhou, J.; Yang, Y.; Yu, X.; Kong, Y.; et al. 200 GHz Maximum Oscillation Frequency in CVD Graphene Radio Frequency Transistors. *ACS Appl. Mater. Interfaces* **2016**, *8*, 25645–25649. [CrossRef] [PubMed]
- Han, S.J.; Valdes-Garcia, A.; Bol, A.A.; Franklin, A.D.; Farmer, D.; Kratschmer, E.; Jenkins, K.A.; Haensch, W. Graphene Technology with Inverted-T Gate and RF Passives on 200 mm Platform. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 5–7 December 2011; p. 4.
- Han, S.-J.; Garcia, A.V.; Oida, S.; Jenkins, K.A.; Haensch, W. Graphene radio frequency receiver integrated circuit. *Nat. Commun.* 2014, 5, 3086. [CrossRef]
- Peng, S.; Jin, Z.; Zhang, D.; Shi, J.; Niu, J.; Zhu, C.; Zhang, Y.; Yu, G. The Effect of Metal Contact Doping on the Scaled Graphene Field Effect Transistor. *Adv. Eng. Mater.* 2021, 2100935, 1–7. [CrossRef]
- Farmer, D.B.; Chiu, H.-Y.; Lin, Y.-M.; Jenkins, K.A.; Xia, F.; Avouris, P. Utilization of a Buffered Dielectricto Achieve High Field-Effect Carrier Mobility in Graphene Transistors. *Nano Lett.* 2009, *9*, 4474–4478. [CrossRef] [PubMed]
- 8. George, S.M. Atomic Layer Deposition: An Overview. Chem. Rev. 2010, 110, 111–131. [CrossRef] [PubMed]
- 9. Wang, X.; Tabakman, S.M.; Dai, H. Atomic Layer Deposition of Metal Oxideson Pristine and Functionalized Graphene. J. Am. Chem. Soc. 2008, 130, 8152–8153. [CrossRef] [PubMed]
- 10. Vervuurt, R.H.J.; Karasulu, B.; Verheijen, M.A.; Kessels, W.E.M.M.; Bol, A.A. Uniform Atomic Layer Deposition of Al₂O₃ on Graphene by Reversible Hydrogen Plasma Functionalization. *Chem. Mater.* **2017**, *29*, 2090–2100. [CrossRef] [PubMed]
- Lin, Y.M.; Jenkins, K.A.; Valdes-Garcia, A.; Small, J.P.; Farmer, D.B.; Avouris, P. Operation of Graphene Transistors at Gigahertz Frequencies. *Nano Lett.* 2009, *9*, 422–426. [CrossRef] [PubMed]
- Pirkle, A.; Wallace, R.M.; Colombo, L. Insitustudies of Al₂O₃ and HfO₂ dielectrics ongraphite. *Appl. Phys. Lett.* 2009, 95, 133106. [CrossRef]
- 13. Zhang, Y.; Qiu, Z.; Cheng, X.; Xie, H.; Wang, H.; Xie, X.; Yu, Y.; Liu, R. Direct growth of high-quality Al₂O₃ dielectric on graphene layers by low-temperature H₂O-based ALD. *J. Phys. D-Appl. Phys.* **2014**, *47*, 055106. [CrossRef]
- 14. Cao, Y.Q.; Cao, Z.Y.; Li, X.; Wu, D.; Li, A.D. A facile way to deposit conformal Al₂O₃ thin film on pristine graphene by atomic layer deposition. *Appl. Surf. Sci.* 2014, 291, 78–82. [CrossRef]
- Zheng, L.; Cheng, X.H.; Cao, D.; Wang, G.; Wang, Z.J.; Xu, D.W.; Xia, C.; Shen, L.Y.; Yu, Y.H.; Shen, D.S. Improvement of Al₂O₃ Films on Graphene Grown by Atomic Layer Deposition with Pre-H₂O Treatment. ACS Appl. Mater. Interfaces 2014, 6, 7014–7019. [CrossRef]
- Vervuurt, R.H.J.; Kessels, W.M.M.; Bol, A.A. Atomic Layer Deposition for Graphene Device Integration. *Adv. Mater. Interfaces* 2017, 4, 1700232. [CrossRef]
- Alaboson, J.M.P.; Wang, Q.H.; Emery, J.D.; Lipson, A.L.; Bedzyk, M.J.; Elam, J.W.; Pellin, M.J.; Hersam, M.C. Seeding Atomic Layer Deposition of High-k Dielectrics on Epitaxial Graphene with Organic Self-Assembled Monolayers. ACS Nano 2011, 5, 5223–5232. [CrossRef] [PubMed]
- Jin, Z.; Ma, P.; Wang, S.; Peng, S.; Zhang, D.; Shi, J.; Niu, J.; Yu, G.; Wang, X.; Li, M. Hydroxyl-free buffered dielectric for graphene field-effect transistors. *Carbon* 2015, *86*, 264–271. [CrossRef]
- 19. Kim, S.; Nah, J.; Jo, I.; Shahrjerdi, D.; Colombo, L.; Yao, Z.; Tutuc, E.; Banerjee, S.K. Realization of a high mobility dual-gated graphene field-effect transistor with Al₂O₃ dielectric. *Appl. Phys. Lett.* **2009**, *94*, 062107. [CrossRef]
- 20. Canto, B.; Gouvea, C.P.; Archanjo, B.S.; Schmidt, J.E.; Baptista, D.L. On the Structural and Chemical Characteristics of Co/Al₂O₃/graphene Interfaces for Graphene Spintronic Devices. *Sci. Rep.* **2015**, *5*, 14332. [CrossRef]
- 21. Xu, C.; Gao, W. Pilling-Bedworth ratio for oxidation of alloys. Mater. Res. Innov. 2000, 3, 231–235. [CrossRef]
- 22. Wu, G.F.; Tang, X.; Meyyappan, M.; Lai, K.W.C. Doping effects of surface functionalization on graphene with aromatic molecule and organic solvents. *Appl. Surf. Sci.* 2017, 425, 713–721. [CrossRef]
- Yan, H.G.; Xia, F.N.; Zhu, W.J.; Freitag, M.; Dimitrakopoulos, C.; Bol, A.A.; Tulevski, G.; Avouris, P. Infrared Spectroscopy of Wafer-Scale Graphene. Acs Nano 2011, 5, 9854–9860. [CrossRef] [PubMed]
- 24. Yan, J.; Zhang, Y.B.; Kim, P.; Pinczuk, A. Electric field effect tuning of electron-phonon coupling in graphene. *Phys. Rev. Lett.* 2007, 98, 166802. [CrossRef] [PubMed]
- Peng, S.; Zhang, J.; Jin, Z.; Zhang, D.; Shi, J.; Wei, S. Electric-Field Induced Doping Polarity Conversion in Top-Gated Transistor Based on Chemical Vapor Deposition of Graphene. *Crystals* 2022, *12*, 184. [CrossRef]
- 26. Peng, S.; Jin, Z.; Yao, Y.; Huang, X.; Zhang, D.; Niu, J.; Shi, J.; Zhang, Y.; Yu, G. Controllable p-to-n Type Conductance Transition in Top-Gated Graphene Field Effect Transistor by Interface Trap Engineering. *Adv. Electron. Mater.* **2020**, *6*, 2000496. [CrossRef]
- Zheng, L.; Cheng, X.; Yu, Y.; Xie, Y.; Li, X.; Wang, Z. Controlled direct growth of Al₂O₃-doped HfO₂ films on graphene by H₂O-based atomic layer deposition. *Phys. Chem. Chem. Phys.* 2015, 17, 3179–3185. [CrossRef]
- Meric, I.; Han, M.Y.; Young, A.F.; Ozyilmaz, B.; Kim, P.; Shepard, K.L. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nat. Nanotechnol.* 2008, *3*, 654–659. [CrossRef]

- 29. Peng, S.A.; Jin, Z.; Zhang, D.Y.; Shi, J.Y.; Niu, J.B.; Huang, X.N.; Yao, Y.; Zhang, Y.H.; Yu, G.H. How Do Contact and Channel Contribute to the Dirac Points in Graphene Field-Effect Transistors? *Adv. Electron. Mater.* **2018**, *4*, 7. [CrossRef]
- Peng, S.-A.; Jin, Z.; Ma, P.; Yu, G.-H.; Shi, J.-Y.; Zhang, D.-Y.; Chen, J.; Liu, X.-Y.; Ye, T.-C. Heavily p-type doped chemical vapor deposition graphene field-effect transistor with current saturation. *Appl. Phys. Lett.* 2013, 103, 223505. [CrossRef]
- Peng, S.; Jin, Z.; Yao, Y.; Li, L.; Zhang, D.; Shi, J.; Huang, X.; Niu, J.; Zhang, Y.; Yu, G. Metal-Contact-Induced Transition of Electrical Transport in Monolayer MoS₂: From Thermally Activated to Variable-Range Hopping. *Adv. Electron. Mater.* 2019, 5, 1900042. [CrossRef]
- 32. Lee, B.; Mordi, G.; Kim, M.J.; Chabal, Y.J.; Vogel, E.M.; Wallace, R.M.; Cho, K.J.; Colombo, L.; Kim, J. Characteristics of high-k Al₂O₃ dielectric using ozone-based atomic layer deposition for dual-gated graphene devices. *Appl. Phys. Lett.* **2010**, *97*. [CrossRef]