



# Article Crystalline Silicon Spalling as a Direct Application of Temperature Effect on Semiconductors' Indentation

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**Abstract**: Kerf-less removal of surface layers of photovoltaic materials including silicon is an emerging technology by controlled spalling technology. The method is extremely simple, versatile, and applicable to a wide range of substrates. Controlled spalling technology requires a stressor layer, such as Ni, to be deposited on the surface of a brittle material; then, the controlled removal of a continuous surface layer can be performed at a predetermined depth by manipulating the thickness and stress of the Ni layer, introducing a crack near the edge of the substrate, and mechanically guiding the crack as a single fracture front across the surface. However, spalling Si(100) at 300 K (room temperature RT) introduced many cracks and rough regions within the spalled layer. These mechanical issues make it difficult to process these layers of Si(100) for PV, and in other advanced applications, Si does not undergo phase transformations at 77 K (Liquid Nitrogen Temperature, LNT); based on this fact, spalling of Si(100) has been carried out. Spalling of Si(100) at LNT improved material quality for further designed applications. Mechanical flexibility is achieved by employing controlled spalling technology, enabling the large-area transfer of ultrathin body silicon devices to a plastic substrate at room temperature.

**Keywords:** indentation; room temperature; liquid nitrogen temperature; spalling; Si-NWs; nanoscale chemical templating (NCT); PV

## 1. Introduction

The mechanical deformation of crystalline silicon induced by micro-indentation has been studied [1-4]; when crystalline silicon Si(100) is hydrostatically compressed at room temperature, to pressures in the range of 11-15 GPa, it transforms from face-centered cubic (diamond structure) phase silicon to a body-centered tetragonal phase (Si-II), which is metallic [1,2]. This transformation is not reversible, as when the hydrostatic pressure is released, the Si-II phase transforms into the body-centered cubic phase (Si-III), which is also metastable [3–6]. On the one hand, it has been well established that when Si single crystals undergo indentation at 300 K [6–9], their crystalline structure transforms mainly to Si-III at lower pressures, as indentation includes an element of shear stresses in addition to hydrostatic pressures [1,4]. On the other hand, it has been proven experimentally that Si(100) does not transform at 77 K using Raman spectroscopy [4], along with electrical characterizations [6–8]. The current work is based on a detailed study undertaken in 2007 by Khayyat et al. [6] at sample temperatures higher than 77 K but lower than 300 K, where the temperature range could be determined below which Vickers indentation-induced phase transitions in single crystals of silicon would not occur. Both in situ electrical resistance measurements and ex situ Raman spectroscopy of indentations were employed for these investigations, and it has been found that the sample temperature indeed has a very significant influence on the occurrence, or otherwise, of the indentation-induced phase transition from Si-I (face-centered cubic structure) to Si-II (body-centered tetragonal structure) [10,11].

Thin-film electronic materials have been extensively studied for the realization of a wide range of mechanically flexible electronic devices such as light-emitting diodes, thin-

film transistors, photovoltaic solar cells, and sensors. So far, mainstream flexible electronics have been based on thin-film organic and amorphous semiconductors that allow direct device fabrication on a flexible substrate at relatively low temperatures ( $\leq$ 300 °C). The salient feature of this processing scheme is the ability to achieve very-large-area flexible electronics at a relatively low processing cost. However, the inherently defective and highly disordered crystalline structure in such materials severely limits overall device performance and reliability when the device dimensions are scaled down.

The aim of this study is to introduce additional control into the material spalling process, thus improving both crack initiation and propagation, and increasing the range of selectable spalling depths that are provided. The method includes providing a stressor layer on the surface of a base substrate at an initial temperature, which is room temperature. Next, the base substrate, including the stressor layer, is brought to a second temperature, which is lower than room temperature. The base substrate is spalled at the second temperature to form a spalled material layer. Thereafter, the spalled material layer is returned to room temperature, i.e., the first temperature. This investigation describes in some detail how indentations at 77 K have led to an important application in producing thin, flexible Si films for advanced applications [12,13].

## 2. Materials and Methods

The indentation experiments were conducted on the following sample: silicon single crystals Si(100). The single crystal specimens were of the dimensions 10 mm, 10 mm, 0.38 mm, all of which had been cut from a 50 mm diameter Si(100) wafer supplied by Wacker-Chemitronic GMBH (Munich, Germany). The wafer was n-type and the dopant was phosphorous; its resistivity was 50  $\Omega$  cm and carrier concentration was ~10<sup>14</sup> cm<sup>-3</sup>. The temperature of the sample was measured with a thermocouple junction placed on the ceramic header package. In these investigations, the sample temperature could be varied in a controlled manner to an accuracy of  $\pm 5$  K, as the experimental set-up allows N<sub>2</sub> (g), at temperatures as close as possible to 77 K, to follow above the sample to prevent air vapor condensation and temperature fluctuations in the range of 150 to 300 K (see Figure 1). A silica tube containing nitrogen gas, which was supplied from a metallic cylinder, was passed through a dewar cooler to bring it as close as possible to liquid nitrogen temperature. The cooled nitrogen gas passed through a cooling apparatus. Consequently, the sample was cooled by being mounted on the cooling apparatus. A thermocouple (type T) was attached to the sample and then, the temperature was measured using a FLUKE 54 II thermometer. The cooling apparatus consisted of a box of brass; a tube of brass was built inside the box with two openings to inlet and outlet nitrogen gas. The sample was mounted on the surface of the brass box. The sample was equilibrated at the temperature of interest for around 10 min, with fluctuations in temperature of  $\pm 5$  °C or below for most of the time. This was achieved by controlling the nitrogen gas flow through the cooling apparatus.



Figure 1. Set-up for indentation in an Instron machine at different temperatures.

In order to make relatively high load indentations in the silicon samples that were cooled to down temperatures in the range of 150–300 K and in a moisture-free atmosphere, which was suitable for Raman studies, we carried out another series of experiments. In this series, a single crystal Si(100) sample of the dimensions 10 mm, 10 mm, 0.38 mm

was mounted onto the copper block (described above), and a thermocouple junction was stuck onto the sample with a piece of adhesive tape [11]. This assembly was then placed inside a 500 mL Pyrex glass beaker. The cooling of the copper block was carried out in the same manner, as described above. However, the cold, dry nitrogen gas exiting from the copper block was allowed to fill the Pyrex glass beaker. A Vickers diamond was used as the indenter, which was mounted on a 20 N load cell, that, in turn, was screwed onto the cross beam of an Instron Model 1122 mechanical testing machine. To make an indentation on the test sample, the indenter was loaded at a speed of  $0.05 \text{ mm/min}^{-1}$ . After reaching the desired indenter load, it was held constant for 15 s, and then, the indenter was unloaded at the same speed. Another site on the sample was then brought under the indenter, the sample cooled down to another desired temperature, and an indentation was made at another preselected load. In this manner, several indentations were made at various temperatures and under different indenter loads. After having made all the necessary indentations, the sample was allowed to gradually warm up to room temperature, making sure that, at no stage, did any water condensation occur on the sample. The indented samples were then stored in a desiccator. Some of the residual Vickers indentations made at 300 and 77 K were examined with an FEI Co., environmental scanning electron microscope (Eindhoven, The Netherlands, model XL 30). These samples were not coated, as surface charging did not take place inside the experimental chamber of this microscope.

## 3. Results and Discussion

#### 3.1. Indentations at 300 K and 77 K

Environmental scanning electron micrographs of residual indentations made at 300 and 77 K are shown in Figure 2, respectively. It can be seen from Figure 2a that there is clear evidence for material extrusion from the indentation. This extrusion has generally been accepted as evidence for Si-I to Si-II phase transition. On the other hand, it can be seen from the micrograph of the residual indentation made at 77 K (see Figure 2b) that there is no extrusion of material, and instead, shear lines within the indentation are quite clearly visible. These observations also suggest that in indentations made at 77 K, there is no Si-I to Si-II phase transition.



**Figure 2.** (**a**) 300 K Vickers indentation in Si(100) under a load of 2.63 N; the arrow highlights the extrusion. (**b**) 77 K Vickers indentation in Si(100) under a load of 5.21 N; the arrow points at a shear line.

Using two complementary techniques, namely, in situ four-terminal dc electrical resistance measurements of the bare silicon when indented with a Vickers diamond indenter [10,11], and Raman spectroscopy [10] of the residual indentations, combined with environmental scanning electron microscopy of residual indentations made at different temperatures [11], it has been shown that indentation-induced phase transformation of a silicon crystal is significantly affected by its temperature. Whereas indentations at room temperature caused Si-I to transform to Si-II within the plastically deformed zone around

the indentation, no such phase transition occurred when the sample had been cooled down to 200 K or lower.

During compression to ~11 GPa, Si-I (f.c.c) transforms into Si-II (body-centered tetragonal, also known as beta-tin structure); Si-II has low resistivity, which is similar to that of copper. In contrast, at decompression at 300 K and in the pressure range of 8 to 2 GPa, Si-II transforms to Si-XII, which is rhombohedral. From 2 GPa down to one atmosphere, Si-III forms, which is body-centered cubic or bc8; at these pressures, Si-XII is only a tiny fraction of the recovered silicon [2–5].

It has been assumed that there are temperature rises during indentation which assist phase transformation [11]. Figure 3 shows a schematic representation of the indentation-induced phase transition model, where the phase-transformed zone is just underneath the indenter and embedded within the plastic zone. It has been assumed that there is heat elevation in the indented zone of the material. An estimated local adiabatic temperature rises is generated during the indentation process, as explained in Equation (1) [12].

$$\Delta T = \frac{\gamma \varepsilon}{\rho c} = 460 \text{ K} \tag{1}$$

where  $\Delta T$  is the maximum temperature rise, Y is the uniaxial yield stress,  $\varepsilon$  is the maximum plastic strain around a Vickers indentation,  $\rho$  is the density, and c is the heat capacity. The shear yield stress  $\tau$  of silicon at room temperature has been given as 1 GPa, which gives  $Y = 2\tau = 2$  GPa using the Tresca criterion [13]. The density  $\rho$  is  $2.33 \times 10^3$  kg m<sup>-3</sup> and heat capacity c of silicon is  $0.67 \times 10^3$  J kg<sup>-1</sup> K<sup>-1</sup> [14]. Therefore, the estimated maximum temperature rise T during a Vickers indentation in silicon would be ~460 K. This temperature rise provides the required energy to rebuild the crystal structure-producing phase transitions. Cooling the sample down to 77 K will suppress this rebuilding of the crystal structure-producing structural phase-transformed zone within the plastically deformed area.



**Figure 3.** Schematic representation of the indentation-induced phase transition model; the phase-transformed zone is embedded within the plastic zone.

#### 3.2. Si Crystals Spalling at 300 K and 77 K

Kerf-less removal of surface layers of materials, including silicon, is demonstrated by controlled spalling technology. The method is extremely simple, versatile, and applicable to a wide range of substrates. Controlled spalling technology, as has been described schematically in Figure 3, requires a stressor layer (Figure 4a) to be deposited on the surface of a brittle material, and the controlled removal and placement of a tape such as Kapton tape on the top of the stressor layer (Figure 4b); then, spalling of the surface layer is undertaken at a predetermined depth (Figure 4c). The stress layer (Ni) thickness affects the depth of the spalling, as strain distribution due to lattice-mismatch between these two layers increases with the increase in the thickness of the tensile layer, and consequently, increases the spalled layer thickness [15].



Figure 4. Schematic representation describes the main steps (a-c) of spalling [12,13].

Silicon (Si(100)) spalling at 77 K (liquid nitrogen temperature) is described schematically in Figure 4. Moreover, Figure 5 shows successful spalling of Si(111) wafer from the ingot.



Figure 5. Spalling of Si(111), wafer <111> from the ingot of a diameter of 100 mm.

By manipulating the thickness and stress of the Ni layer, a crack is introduced near the edge of the substrate and mechanically guided as a single fracture front across the surface at room temperature (300 K). Spalling from an ingot Si(111) is presented in Figure 5. However, there are many issues with spalling Si(100) at room temperature, such as cracks or irregularities in thickness. Based on previous knowledge of indentations at 77 K [11], where phase transformations and cracks disappear in comparison to indentation at 300 K, it has been suggested that spalling be undertaken at 77 K (Figure 6).

Figure 7 shows in detail the difference in appearance (optical microscope and SEM images) between Si(100) spalled at 300 K, and that spalled at 77 K, where the spalling at room temperature is performed first mechanically by introducing a crack as explained earlier, then by exposing the same sample to liquid nitrogen vapor at a fresh region, where it is spalled spontaneously. The resulted spalled layer at room temperature looks different to that spalled at liquid nitrogen temperature, as the outer surface looks rough (see Figure 7a, where this observation has been confirmed by SEM micrographs (Figure 7b,c)).



**Figure 6.** Liquid nitrogen temperature Si(100) spalling can be carried out as follows: pieces of 100 semiconductor materials (nominally 1.5, 3 inch pieces) are HF-dipped until hydrophobic (optional),  $N_2$ -dried, immediately placed into a sputter system for metal layer deposition, and then, Kapton tape is placed onto the Ni surface and cooled using liquid nitrogen.



Figure 7. (a) Optical image of Si(100) spalled at 300 K and at 77 K in different areas of the same piece

of wafer. (b) SEM micrograph of the side view of Si(100) spalled at 300 K. The variation in spalled layer thickness, as shown by green lines, is between 3.91 to 5.43  $\mu$ m. (c) Side view SEM micrograph of Si(100) spalled at 77 K, where the thickness of the spalled film is almost constant at around 22.38  $\mu$ m.

When we spall Si(100) at room temperature, the spalled layer, as shown on the micrograph (Figure 7), has many cracks and rough regions, which makes it difficult to process for PV applications. As it has been shown previously that Si does not undergo phase transformations at 77 K, we cooled down the Si(100) (which has a stressor layer of Ni on its surface) as close as possible to 77 K. Then, when we carried out further examinations on the spalled samples, such as SEM micrographs, the spalled Si(100) samples at low temperatures showed less rough areas, and could be processed further for PV applications. Clearly, it is advantageous to carry out spalling, particularly for Si(100), at 300 K. Figure 8 shows a free standing chip of Si(100) spalled at 77 K (Figure 8a), along with side views of the spalled layers (Figure 8b–d).





**Figure 8.** Cross-Section or side views of Si(100) spalled at 77 K. (a) Rough regions can be found. (b) Significant surface area is very smooth. (c) Spall material has thickness of 40–85  $\mu$ m. (d) A broad area of the spalled layer of a length more than 1 mm shows the even spalled surface.

A detailed study of spalled Si(100) is presented in Figure 9. The thickness of the spalled Si(100) decreases from above 60  $\mu$ m to below 50  $\mu$ m, with the temperature increasing from 77 K to less than 200 K.



**Figure 9.** Temperature-dependence of spalling for Si(100). Spalled at various low temperature points. Data points represent thickness in smooth areas. Si error bars denote thickness variation in rough areas (see SEM images on Figure 8).

### 3.3. Applications on Spalling Technique

A stressor layer is formed atop a base substrate at a first temperature, which induces an initial tensile stress in the base substrate that is below its fracture toughness. The base substrate and stressor layer are then brought to a second temperature, which is lower than the first temperature. The second temperature induces a second tensile stress in the stressor layer which is greater than the first tensile stress, and which is sufficient to allow for spalling mode fracturing to occur within the base substrate. The base substrate is spalled at the second temperature to form a spalled material layer. Spalling occurs at a fracture depth, which is dependent upon the fracture toughness and stress level of the base substrate, and the second tensile stress of the stressor layer induced at the second temperature.

Spalling includes depositing a stressor layer on a substrate, placing an optional handle substrate on the stressor layer, and inducing a crack and its propagation below the substrate/stressor interface. This process, which is performed at room temperature, removes a thin layer of the base substrate below the stressor layer. By thin, it is meant that the layer thickness is typically less than 100 microns, with a layer thickness of less than 50 microns being more typical.

The ultimate goal of spalling is to produce thin films for advanced application of electronic device fabrications; Figure 10 describes the main steps involved in this process [14]. Si nanowires are an emerging PV technology [15,16]; nanoscale chemical templating (NCT) for the controlled growth of Si nanowires catalyzed by Al has shown good progress with regard to PV technology (see Figure 11), proving the principle of the NCT technique.

The fact that controlled spalling is able to remove layers of arbitrary size and shape allows one to design circuits and subsystems at the wafer scale and selectively remove them by selected deposition of the stressor layer on these regions [17,18]. The side view of previously grown nanowires [17,19], using controlled growth of Si nanowires, demonstrated a novel nanoscale chemical templating method, achieving controlled spatial placement of Si NWs by using patterned SiO<sub>2</sub> as a mask and Al as the seed material. The main advantage of this method lies in its suitability for the oxygen-reactive seed materials, which are of great interest for electronic applications. The NCT method can also have fewer steps compared

to conventional patterning approaches, not requiring lift-off of a metal layer or removal of the mask. The method is also flexible, as it is amenable to both standard lithography techniques and self-assembled patterning techniques such as microsphere lithography. Patterning and growth parameters can be chosen to achieve high selectivity, growth yield, and fidelity; where no NWs grow between openings, most openings are occupied by one or more NWs and the majority are occupied by a single vertical NW. NCT will have several applications in nanotechnology research such as solar cells.



**Figure 10.** Handling and processing of spalled films for further applications such as solar cells (PV applications).



(b)

**Figure 11.** SEM Side views. (a) Nanoscale chemical templating (NCT), showing controlled growth of a group of Si nanowires. (b) Controlled growth of single Si nanowires at each opening; arrow 1 shows the thin oxidized layer of Al (Al<sub>2</sub>O<sub>3</sub>), and arrow 2 points to the planer growth of Si; the average nanowire length is 5  $\mu$ m.

A promising field for future low-cost, medium-efficiency solar cell devices is the use of vapor–liquid–solid (VLS)-grown nanowires (NWs) as the active region of large scale (greater than 1 mm<sup>2</sup> area) photovoltaic devices. There are several advantages of using NWs. NWs can be doped as they are grown, helping with the formation of PV structures. NW-based PV structures require shorter carrier diffusion distances than are

needed for a similarly thick planar absorber layer. At the same time, due to scattering and other optical phenomena, the NW structure is able to trap more light and improve overall light absorption. This, combined with the ability to grow nanowires on cheap substrates or reuse the growth substrate multiple times using spalling, makes NWs promising for future-generation PV devices.

## 4. Conclusions

Indeed, spalled single crystals are of immense technological importance. However, spalling Si(100) at room temperature exhibits several mechanical issues and corresponding technical limitations. It has been shown that when Si(100) single crystals are indented at liquid nitrogen temperature (77 K), there is no phase transformation. Owing to the presence of high shear stresses during indenter loading, most of the original Si remains unaltered in structure. It has been suggested that the difference in phase transition at the two temperatures can be explained by the following hypothesis: a temperature rise, which alongside high hydrostatic and shear stresses assists phase transition, occurs during indentation at room temperature.

Based on the fact that spalling of Si(100) at temperatures close to 77 K produces undeformed layers of relatively controlled thickness for further applications such as PV technologies, devices of flexible Si—if the spalled layer is thin enough—have many advantages over their bulk counterparts. By virtue of less material being used, thin-film devices ameliorate the material cost associated with device production and lower device weight, both of which are important in the semiconductor industries for a wide range of efficient thin materials applications—particularly, if this technology of bulk Si spalling is combined with controlled growth of Si-NWs, as has been proposed for PV devices. Furthermore, if a device layer is removed from a substrate that can be reused, additional fabrication cost reduction can be achieved.

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**Data Availability Statement:** The data used to support the findings of this study are included within the article.

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