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Implementation of a Programmable Electronic Load for Equipment Testing

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Abstract: This paper presents the implementation of an AC three-phase programmable electronic load (PEL) that emulates load profiles and can be used for testing equipment in microgrids (MGs). The implemented PEL topology is built with a voltage source inverter (VSI) which works as a current controlled source and a Buck converter which permits the dissipation of active power excess. The PEL operation modes according to the interchange of active and reactive power and its operation in four quadrants were determined. The power and current limits which establish the control limitations were also obtained. Three control loops were implemented to independently regulate active and reactive power and ensure energy balance in the system. The main contribution of this paper is the presentation a detailed analysis regarding hardware limitations and the operation of the VSI and Buck converter working together. The PEL was implemented for a power of 1.8 kVA. Several experimental results were carried out with inductive, capacitive, and resistive scenarios to validate the proper operation of the PEL. Experimental tests showed the correct behavior of the AC three-phase currents, VSI input voltage, and Buck converter output voltage of the PEL for profile changes, including transient response.

Keywords: programmable electronic load; power electronics; control; equipment testing; renewable energy

Citation: Serna-Motoya, L.F.; Ortiz-Castrillón, J.R.; Gil-Vargas, P.A.; Muñoz-Galeano, N.; Cano-Quintero, J.B.; López-Lezama, J.M. Implementation of a Programmable Electronic Load for Equipment Testing. *Computers* **2022**, *11*, 106. https://doi.org/10.3390/computers11070106

Academic Editors: Pedro Pereira and Mostafa Rahimi Azghadi

Received: 18 May 2022
Accepted: 21 June 2022
Published: 28 June 2022

1. Introduction

Non-conventional renewable energy sources (NCRESs) and their installation in MGs are part of a global trend toward clean and sustainable electricity generation. This brings challenges in terms of stability, generation, interconnection and control to allow these systems to connect and operate properly together with conventional electricity generation systems. NCRES such as solar and wind depend on several factors such as temperature, irradiance, and wind speed; in consequence, NCRESs are volatile and depend on the time, day, and season of the year (weather conditions). Therefore, the correct design of an MG implies a detailed sizing, considering safety and continuity of service as a priority [1]. For this reason, it is important to verify the correct operation of all devices that compose the MG before its connection, in order to guarantee a correct synchronization, operation, and communication.

A PEL is a power electronics device that allows for the testing of equipment and NCRESs in MGs [2]. It emulates several load or source profiles such as transient and steady-state operation for equipment under test (EUT) [3–5]. This is done to assess the performance of a single or several devices working jointly within an MG. A PEL can be seen as a regulated current source, the control system of which regulates the current to emulate the desired load or NCRES profiles. There are two PEL types: unidirectional and bidirectional. Unidirectional PELs can be further classified in two categories: the first one

only consumes energy from the power grid and can be related with residential, commercial, or industrial end users that may have linear loads (such as household appliances and motors) and non-linear loads (such as computers and illumination). This PEL type is able to modify the power factor and waveform of the current for emulating loads that introduce harmonics to the grid. The second unidirectional PEL emulates distributed generators (DGs) that only inject power to the electrical grid, such as solar and eolic generators [6–12]. Bidirectional PELs are able to emulate load or power sources. This type of PEL features functions for energy consumption and injection depending on its operation mode, which includes storage energy systems (batteries), chargers for batteries from electric vehicles, inverters, converters, and solar panels.

Several topologies of PELs can be found in the scientific literature (single-phase, three-phase, and DC) [3–5,13–21] from conventional topologies based on variable resistances [7] up to topologies based on joint operation of converters and inverters (such as boost, Buck-boost, back to back, and multilevel) [3,7,21]. The most common PEL applications in MG for testing equipment are storage systems, uninterruptible power supplies, measurement, converters, and inverters (voltage source inverter, VSI) [6,19,22]. PELs have limited functions and different control strategies according to the EUT. For example, a PEL based on a DC/DC Buck-boost converter allows for emulating loads as battery storage systems. This topology is able to consume or inject energy into DC systems. In the same way, back-to-back topology has two emulation modes (consumer and generator) for equipment in AC [3,6,13,22–28].

In the technical literature, PEL topologies with VSI integrated with Buck converters are reported in [19,29,30]. In [29], a PEL is simulated in PSIM with its model and control scheme. In [19], single-phase and three-phase PEL topologies are simulated, developing several control schemes to emulate different load profiles. In these studies, the real implementation of the power electronics equipment was not performed; the authors only present simulation results and the performance of the PEL was only evaluated in a steady state. In [30], the implementation of a PEL is reported; in this paper, equations for the sizing of the system components and filters were presented. However, the model is not addressed in depth, and neither is the exploration of the operational limits of the PEL. It is worth mentioning that the operational quadrants of the PEL were not taken into account in the aforementioned publications.

This paper presents the implementation of a PEL that can be used for testing equipment in MGs, the maximum active power of which is 1.8 kW. The PEL was developed by the integration of two topologies. The first of these is an inverter (three legs, four wires) to emulate three-phase load profiles, and the second of these is a DC/DC Buck converter to control the DC bus and dissipate the excess of power energy into a resistive element. The main advantage of this implementation lies in its reduced cost with respect to commercially available alternatives. The deduction of the four operating modes is detailed according to the interchange of active and reactive power with the grid. Power and current limits are obtained according to hardware limitations, so it is possible to avoid the malfunctioning of the PEL in its operation. Three control loops are proposed for regulating active and reactive powers, which at the same time ensures the energy balance of the system.

PELs are necessary devices for the performance of tests in MGs in order to verify the adequate behavior of all equipment before their connection with the electrical power grid. For this reason, this paper presents the implementation of a PEL for testing equipment in MGs. This document is organized as follows. In Section 1, the state of the art regarding PEL types and main applications in MGs is presented, showing the PELs' importance for MGs. In Section 2, the operation principle of a PEL is detailed according to its operation quadrants. Section 3 presents the PEL topology built in this paper. Section 4 presents the control scheme for the developed PEL. In Section 5, the developed PEL is detailed together with its experimental tests. Finally, the most relevant conclusions are presented in Section 6.

2. PEL Operation Modes and Limits

This section presents the operational principle of a PEL connected to the electrical grid based on the energy interchange between two sources (see Figure 1). The PEL is modeled as a voltage source (V_{PEL}) in series with an inductor (L), whereas the electrical grid (V_G) (EUT for this case) operates as another energy source. The magnitude and phase of the current (I) that flows in the circuit directly depends on the voltage difference between V_{PEL}, V_G, and the grid impedance ($Z = j\omega L$). This allows us to make a first current approach that is represented by using Equation (1). If the electrical grid is used as an angle reference, it is possible to obtain a desired current, modifying the magnitude and phase of V_{PEL}:

$$I = \frac{V_G - V_{PEL}}{Z}. \tag{1}$$

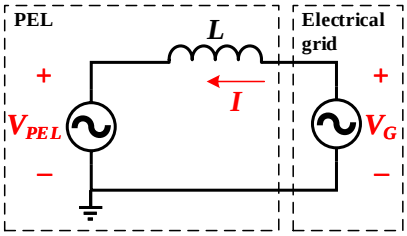

Figure 1. PEL operation principle.

PELs are current source devices that permit the emulation of load profiles. In this case, the reference current $I = |I|\angle\theta_I$ corresponds to the desired current that permits the emulation of different load profiles. Equation (2) relates the AC voltage and the current in the PEL AC terminals ($V_{PEL} = |V_{PEL}|\angle\theta_{PEL}$), which are obtained from Equation (1), where θ_{PEL} is the PEL phase voltage angle respective to the angle of V_G. Grid voltage is defined as $V_G = |V_G|\angle\theta_G$ with $\theta_G = 0°$, because the electrical grid is the system reference

$$V_{PEL} = V_G - ZI. \tag{2}$$

Figure 2 illustrates the phasor diagrams of I and V_{PEL}. These are depicted as keeping the magnitude of I constant and varying θ_I between 0° and 360°. The circumferences represent the paths for each phasor where the coordinate origin is the tail for each phasor. The left circumference (the smallest one) represents the set of phasors for I. Its center is the origin of the complex plane with a real axis (abscissa) and an imaginary axis (ordinate). The right circumference represents the set of phasors for V_{PEL}, where its center corresponds to the value of (V_G). Both circumferences are related by Equation (2). Each circumference has its four quadrants (I, II, III, IV) with dotted and colored lines; this representation allows us to see the relationship between the set of phasors I and V_{PEL}. Each group of current phasors (colored and numbered) is related to the corresponding group of voltage phasors having the same numbering and the same color. This relationship is established by Equation (2). This relationship is due to V_Z, which is the coupling impedance voltage required to complete Kirchhoff's voltage law.

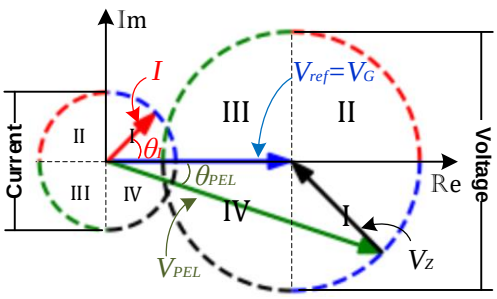

Figure 2. Phasor diagram of the PEL current and voltages path.

Figure 3 presents the operational modes of the PEL developed in this paper. Note that the amplitude of I is constant, varying its phase in the four quadrants ($0° \leq \theta_I < 360°$) with steps of 45°. Figure 3a illustrates the beginning of the phasor path ($\theta_I = 0°$) and Figure 3i illustrates its end ($\theta_I = 360°$). The blue phasor corresponds to the reference of the grid voltage or angular reference ($V_{ref} = V_G = |V_G|\angle 0°$). The black phasor corresponds to the impedance voltage Z ($V_Z = |V_Z|\angle\theta_Z$). The green phasor is the PEL voltage ($V_{PEL} = |V_{PEL}|\angle\theta_{PEL}$). Finally, the red phasor is the current ($I = |I|\angle\theta_I$). In this case, Z is an inductive reactance; hence, the current I has a phase of 90° in lagging with respect to V_Z ($\theta_Z - \theta_I = 90°$). The purpose of this figure is to show how V_{PEL} must behave (in magnitude and angle) in order to obtain a desired current and analyzes when the PEL acts as a load or source, and as inductive or capacitive. The paths of the current and voltages allow us to conclude the following. (1) If the current moves in quadrants I and IV, the PEL behaves as a load. On the contrary, for the current in quadrants II and III, the PEL behaves as a source. (2) The current in quadrants I and II is lagging, whereas the current in quadrants III and IV is leading. Therefore, there are eight operation modes for the PEL:

- Figure 3a,i, PEL as pure resistive load. PEL only consumes active power and its current has the same phase and direction as the electrical grid ($\theta_I = 0°$).
- Figure 3b, PEL as load resistive–capacitive (RC). If desired, a current in the first quadrant ($0° < \theta_I < 90°$), then V_{PEL} should move for the first quadrant of voltage circumference (both are shown with blue dotted lines).
- Figure 3c, PEL as capacitive load. PEL only consumes reactive power and the current is $\theta_I = 90°$ leading wih respect to the electrical grid.
- Figure 3d, PEL as leading source. If a current in the second quadrant is desired ($90° < \theta_I < 180°$), then V_{PEL} should move for the second quadrant of voltage circumference (both are shown with red dotted lines).
- Figure 3e, PEL as pure active source. PEL only injects active power and its current has a phase and direction in opposition to the electrical grid ($\theta_I = 180°$).
- Figure 3f, PEL as lagging source. If a current in the third quadrant is desired ($180° < \theta_I < 270°$), then V_{PEL} should move for the third quadrant of voltage circumference (both are shown with green dotted lines).
- Figure 3g, PEL as pure lagging source. PEL only injects reactive power and the current is $\theta_I = -90°$ lagging with respect to the electrical grid.
- Figure 3h, PEL as resistive–inductive load (RL). If desired, a current in the fourth quadrant ($270° < \theta_I < 360°$), then V_{PEL} should move for the four quadrant of voltage circumference (both are shown with black dotted lines).

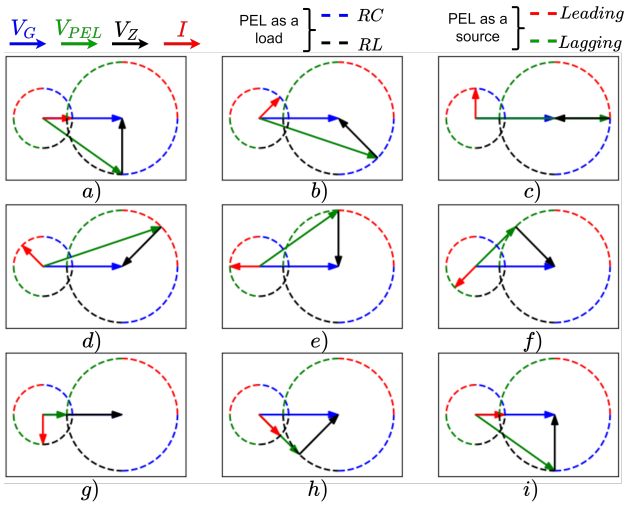

Figure 3. Operation modes of the PEL: $|I| = |I_{max}|$ with $0° \leq \theta_I < 360°$. (**a**) pure resistive load, (**b**) resistive-capacitive load, (**c**) capacitive load, (**d**) leading source, (**e**) pure active source, (**f**) lagging source, (**g**) pure lagging source, (**h**) resistive-inductive load, (**i**) pure resistive load.

Figure 4 also illustrates the PEL operation mode in its four quadrants. However, the PEL voltage amplitude is constant and greater than the grid voltage amplitude. The purpose of this figure is to show how the current behaves when the PEL voltage is constant and its angle varies ($0° \leq \theta_{PEL} < 360°$). Figure 4a illustrates $\theta_{PEL} = 0°$ whereas Figure 4i illustrates $\theta_{PEL} = 360°$. In this operation, point $\theta_{PEL} = \theta_G = 0°$; hence, the current amplitude is at minimum due to the lowest difference of the potential in Z. By varying the angle of the PEL ($0° < \theta_{PEL} < 180°$) (Figure 4a–d), the current increases its magnitude, obtaining its maximum value in $\theta_{PEL} = 180°$ (Figure 4e) when V_{PEL} has the opposite direction of V_G and the potential difference is at maximum in Z. On the other hand, when the PEL voltage varies between $180° < \theta_{PEL} < 360°$, the amplitude of the current decreases (Figure 4f–h), obtaining its minimum value in $\theta_{PEL} = 360° = 0°$ (Figure 4i).

PELs in AC are power electronics devices built with inverters (single-phase or three-phase); then, the amplitude of the PEL voltage ($|V_{PEL}| = MV_{DC}$) can be controlled as a linear function of the DC bus voltage (V_{DC}) and the inverter modulation index (M). Additionally, θ_{PEL} can be modified (controlled) by means of the sinusoidal signal (reference) that forms the SPWM signal to actuate the inverter switches.

We can conclude the following. (1) The capacitive profiles depend on the DC bus voltage which are higher than the grid voltage; on the other hand, if the magnitude of the AC and DC voltages is the same, then only currents in quadrants III and IV are possible. (2) The magnitude of the leading currents are smaller than the lagging currents, considering the same DC bus voltage. In other words, with the same DC bus voltage, it is possible to emulate inductive profiles of greater magnitude than those of the capacitive profiles.

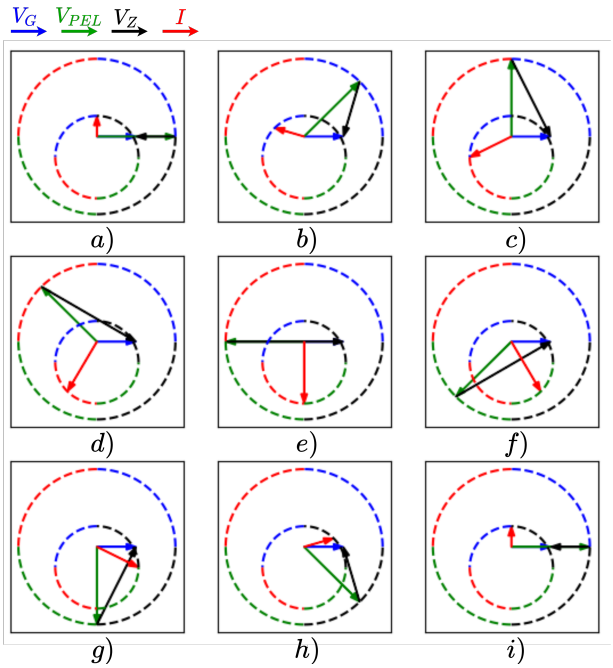

Figure 4. Operation modes of the PEL: $|V_{PEL}| = |V_G|$ with $0^o \leq \theta_{PEL} < 360°$. (**a**) pure resistive load, (**b**) resistive-capacitive load, (**c**) capacitive load, (**d**) leading source, (**e**) pure active source, (**f**) lagging source, (**g**) pure lagging source, (**h**) resistive-inductive load, (**i**) pure resistive load.

Both magnitude and angle of V_{PEL} determine the power interchange of the PEL. Figure 5 shows the power interchange that permits explaining the PEL behavior. The modulation index is in the vertical axis, and θ_{PEL} is in the horizontal axis. In this case, there are four operative zones:

- Yellow zone, in which θ_I is between 0° and 90°; then, the PEL behaves as a resistive–capacitive load.

- Green zone, in which θ_I is between 90° and 180°; then, the PEL behaves as a leading source.
- Blue zone, in which θ_I is between 180° and 270°; then, the PEL behaves as a lagging source.
- Pink zone, in which θ_I is between 270° and 360°; then, the PEL behaves as a resistive–inductive load.

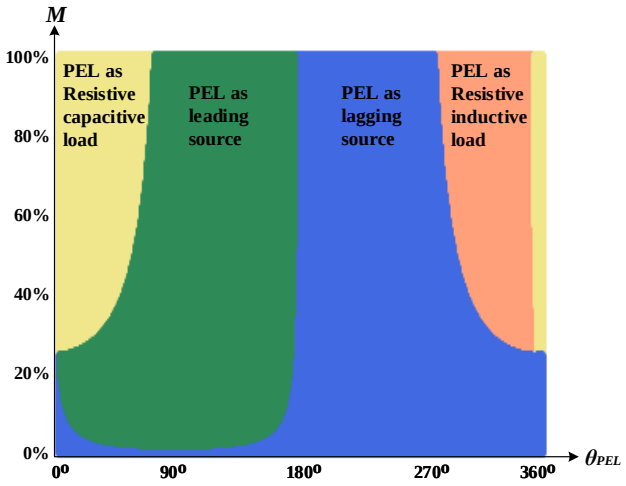

Figure 5. Operation modes of the PEL.

Figure 6 shows a 3D representation of the apparent power S (Figure 6a), active power (Figure 6b), the magnitude of I (Figure 6c), and reactive power (Figure 6d); each one is a function of the modulation index and phase of the PEL. The purpose of Figure 6 is to determine the maximum values of power and current to find the PEL operative limits. In the experimental process, it is necessary to know these limits to avoid exposure to values higher than the PEL can withstand. In ideal operational conditions, the PEL has its maximum capacity when the modulation index is close to 100%. In this case, the magnitude of S has its maximum value when the phase is 180° and its minimum value at 0° and 360°; then, the most relevant variable to regulate the amplitude of S is the modulation index. For the active power, a phase of 180° marks the limit when the PEL consumes power ($P > 0$) or it operates as a source of active power ($P < 0$). The magnitude of I presents a similar behavior to the magnitude of S. The apparent power is directly proportional to the PEL current. The reactive power has its maximum value at 180° as a load and its minimum values (as a source) at 0° and 360°. Equations (3) and (4) generalize the PEL behavior for the three-phase systems depicted in Figure 6:

$$P_{3\phi} = \frac{3V_G V_{PEL} sin(\theta_{PEL})}{\omega L} \tag{3}$$

$$Q_{3\phi} = \frac{3V_G V_{PEL} cos(\theta_{PEL}) - 3V_G^2}{\omega L}. \tag{4}$$

The most relevant information from what has been exposed in this section are the operating limits of the PEL hardware and control. This information includes that the main operational limits of the hardware are the currents and voltages that the PEL components must withstand. Moreover, with regard to voltage magnitude, the insulation of the reactors, the operating voltage of the capacitors and the voltage of the VSI, among others. Furthermore, in terms of current, this information includes protections, thermal capacity of conductors, reactors and VSI, among others. The minimum active power coincides with 90°, and the maximum active power coincides with 270°. On the other hand, the minimum reactive power coincides with 0° and the maximum reactive power coincides with 180° (observe the maximum points in Figure 6 and Equations (3) and (4)). The most important

variable in the operating limits is the DC bus voltage, because the power transfer and load profiles depend on the voltage magnitude and angle as concluded by plotting the operating phasor system in Figure 3. It should be noted that power electronics equipment are static equipment, and unlike synchronous machines can operate at high angles without the risk of losing synchronism. Some scenarios of design and control are presented which can be solved with the exposed in this section:

- If the hardware does not have the capacity to support the maximum current, then the modulation index of the PEL control must be limited.
- If it is desired to emulate a particular load profile and the grid voltage V_G is known, then it is possible to determine the current with Equation (1). Therefore, it is possible to determine the phasor diagram of the system (see Figure 2) and obtain the magnitude of the DC bus voltage required to emulate that profile.
- If the DC bus voltage is known and the maximum current is supported by the PEL hardware, then Figure 5 can be obtained, each region representing the power quadrant to be emulated as a function of the amplitude and angle emulated by the PEL. However, in case the PEL is unidirectional, it can only operate in two quadrants (yellow and pink), and Figure 5 can be used to constrain the control values based on the relationship of the regions and the axes representing the control variables.

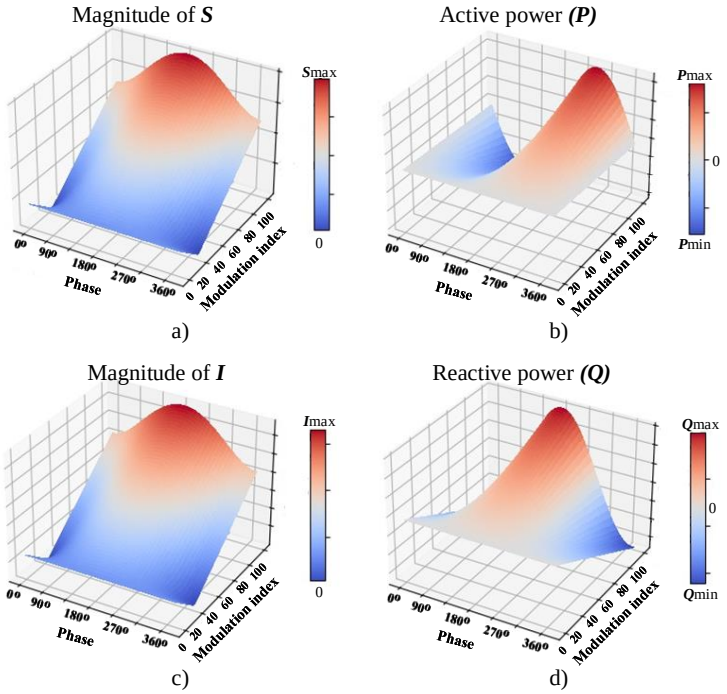

Figure 6. Operation modes of the PEL: A 3D representation. (**a**) magnitude of S, (**b**) active power, (**c**) magnitude of I, (**d**) reactive power

3. Programmable Electronic Load: Implemented Topology

This section presents the implemented topology of the PEL (see Figure 7). This topology has five stages from right to left according to power flow direction: (1) The sources v_R, v_S, and v_T represent the connection with the electrical grid with a neutral line. The auto-transformer composed of L_4, L_5, and L_6 allow a reduction of the voltage level and a balancing of the three-phase grid voltages. (2) Inductors L_1, L_2, and L_3 are the filters to coupling the grid with a voltage source inverter (VSI). (3) The VSI corresponds to a three-phase, four-wire inverter. (4) The DC bus (split with a neutral line) is responsible for storing energy and allows us to stabilize the DC voltage. Resistances R_{C1} and R_{C2} are responsible for balancing the voltage in capacitors C_1 and C_2. (5) The Buck converter dissipates the active power when the PEL absorbs energy from the AC power grid by

means of R_{load}. More information concerning Buck converters and their applications in MGs can be consulted in [31].

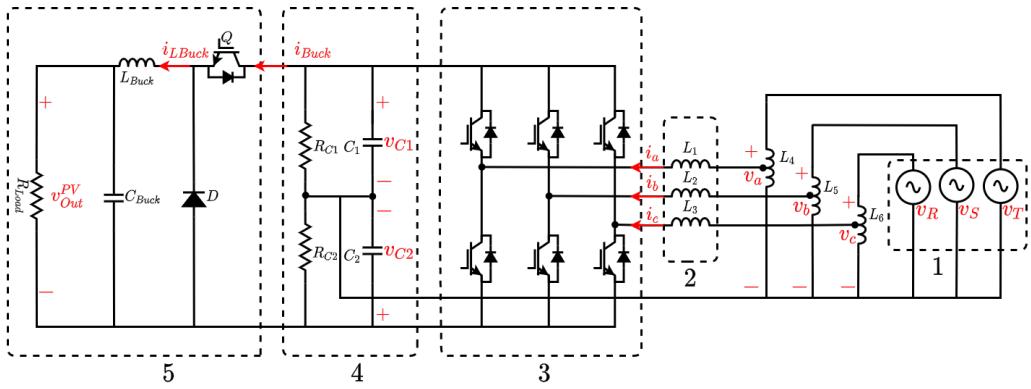

Figure 7. PEL hardware topology.

3.1. VSI Mathematical Model

The mathematical modeling of the VSI is presented in Equation (5), and the procedure to obtain the equations can be consulted in [32]. In this case, $v_{DC} = v_{C_1} - v_{C_2}$ is the total DC bus voltage with $C_1 = C_2 = C$ and resistances $R_{C_1} = R_{C_2} = R_o$. Current i^{abc} and voltage v^{abc} are the vectors which represent the current of PEL and the grid voltage for each phase (a, b, c) respectively:

$$\begin{array}{rcl} L\dfrac{di^{abc}}{dt} & = & -\dfrac{v_{DC}}{2}u^{abc} + v^{abc} \\ C\dfrac{dv_{DC}}{dt} & = & i^{abc}u^{abc^T} - \dfrac{v_{DC}}{R_o} \end{array}. \tag{5}$$

The logic of control is given by Equation (6), and the control function (F) is defined as $u^{abc} = 2F_{1,3,5} - 1$ for the switches of the inverter upper level ($F_{1,3,5}$) whereas $u^{abc} = 1 - 2F_{2,4,6}$ for the switches of the inverter low level ($F_{2,4,6}$):

$$u^{abc} = \begin{cases} 1 & \text{if} \quad F_{1,3,5} = on \quad \text{and} \quad F_{2,4,6} = off \\ -1 & \text{if} \quad F_{1,3,5} = off \quad \text{and} \quad F_{2,4,6} = on \end{cases}. \tag{6}$$

The representation of Equation (5) in the dq reference system is given by Equation (7), where v^{pcc} is the voltage in the connection point:

$$\begin{array}{l} L\dfrac{di_d}{dt} = -\dfrac{v_{DC}}{2}u_d - L\omega i_d + v_d^{pcc} \\ L\dfrac{di_q}{dt} = -\dfrac{v_{DC}}{2}u_q + L\omega i_d + v_d^{pcc} \\ C\dfrac{dv_{DC}}{dt} = i_d u_d + i_q u_q - \dfrac{v_{DC}}{R_o} \end{array}. \tag{7}$$

3.2. Mathematical Model of the DC/DC Buck Converter

The Buck converter controls the DC bus voltage by means of energy dissipation through R_{Load}. Its mathematical model is given by Equation (8) [31] for the input current i_{Buck} and the converter output voltage v_{out}^{PV}, where u_{Buck} is the variable that represents the control signal of the Buck converter switch:

$$\begin{array}{rcl} L_{Buck}\dfrac{di_{Buck}}{dt} & = & v_{DC}u_{Buck} - v_{out}^{PV} \\ C_{Buck}\dfrac{dv_{out}^{PV}}{dt} & = & i_{LBuck} - \dfrac{v_{out}^{PV}}{R_{Load}}. \end{array} \tag{8}$$

3.3. Transfer Functions

The procedure to obtain the transfer functions consists of applying the dq transformation and state-space representation to the mathematical model [32]. Starting from the large-signal model shown in (7), the PEL small-signal model can be obtained by using the following state-space formulation:

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ \mathbf{y} &= \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \end{aligned} \tag{9}$$

with

$$\begin{aligned} \mathbf{A} &= \left(\frac{\partial f(\mathbf{x},\mathbf{u})}{\partial x_i}\right)_{\mathbf{x}_e,\mathbf{u}_e} & \mathbf{B} &= \left(\frac{\partial f(\mathbf{x},\mathbf{u})}{\partial u_i}\right)_{\mathbf{x}_e,\mathbf{u}_e} \\ \mathbf{C} &= \left(\frac{\partial h(\mathbf{x},\mathbf{u})}{\partial x_i}\right)_{\mathbf{x}_e,\mathbf{u}_e} & \mathbf{D} &= \left(\frac{\partial h(\mathbf{x},\mathbf{u})}{\partial u_i}\right)_{\mathbf{x}_e,\mathbf{u}_e}, \end{aligned} \tag{10}$$

where x_i corresponds to the ith state variable, $f(x,u)$ corresponds to each equation of Model (7), and $h(x,u)$ are the equations that relate state and output variables. It is considered that $h(x,u) = x$. The subscripts e in (10) are state variables (x_e) and input variables (u_e) in their rated values; they are represented by using capital letters.

A, B, C, and D matrices are obtained by using the following definitions: state variables $\mathbf{x} = \left[i_S^d, i_S^q, v_{DC}\right]^T$; input variables $\mathbf{u} = \left[u^d, u^q, v_{pcc}^d, v_{pcc}^q\right]^T$; and output variables that are equal to state variables as $\mathbf{y} = \mathbf{x} = \left[i_S^d, i_S^q, v_{DC}\right]^T$.

The PEL state model is obtained after applying (9) and (10) over the model (7). This representation linearizes the system around an operation point. The representation of matrices A and B is as follows:

$$\mathbf{A} = \begin{bmatrix} -\frac{R_L}{L} & \omega & -\frac{U^d}{2L} \\ -\omega & -\frac{R_L}{L} & -\frac{U^q}{2L} \\ \frac{U^d}{C} & \frac{U^q}{C} & -\frac{1}{R_o C} \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} -\frac{V_{DC}}{2L} & 0 & \frac{1}{L} & 0 \\ 0 & -\frac{V_{DC}}{L} & 0 & \frac{1}{L} \\ \frac{I_S^d}{C} & \frac{I_S^q}{C} & 0 & 0 \end{bmatrix}. \tag{11}$$

Matrix $\mathbf{C}$ corresponds to a 3×3 identity matrix whereas matrix $\mathbf{D}$ is a 4×3 matrix of zeros. The state-space representation is in the time domain. Equation (12) yields the frequency domain representation as follows:

$$G(s) = \frac{1}{det(s\mathbf{I} - \mathbf{A})}\mathbf{C}[adj(s\mathbf{I} - \mathbf{A})]^T\mathbf{B} + \mathbf{D}. \tag{12}$$

The transfer functions to design the control system of the PEL are given by Equations (13) and (14). Equation (13) presents the transfer function ($G_{i_d}(s)$) for the current associated with the active power (i_d) with respect to its modulation variable (u_d). Equation (14) presents the transfer function ($G_{i_q}(s)$) for the current associated with reactive power (i_q) with respect to its modulation variable (u_q):

$$\frac{G_{i_d}(s)}{u_d} = \frac{\begin{bmatrix} -2CLR_oV_{DC}s^2 + (-2I_dLR_oU_d - 2LV_{DC})s \\ -2I_dLR_oU_q\omega - R_o(U_q)^2V_{DC} \end{bmatrix}}{\begin{bmatrix} 4CL^2R_os^3 + (4L^2)s^2 + (4CL^2R_o\omega^2 + 2LR_o(U_d)^2 \\ +2LR_o(U_q)^2)s + 4\omega^2L^2 \end{bmatrix}} \tag{13}$$

$$\frac{G_{i_q}(s)}{u_q} = \frac{\begin{bmatrix} -2CLR_oV_{DC}s^2 + (-2I_qLR_oU_q - 2LV_{DC})s \\ +2I_qLR_oU_d\omega - R_o(U_d)^2V_{DC} \end{bmatrix}}{\begin{bmatrix} 4CL^2R_os^3 + (4L^2)s^2 + (4CL^2R_o\omega^2 + 2LR_o(U_d)^2 \\ +2LR_o(U_q)^2)s + 4\omega^2L^2 \end{bmatrix}}. \quad (14)$$

For the external loop control, it is necessary to deduce a transfer function for the voltage in the DC bus ($G_{v_{DC}}(s)$) with respect to its input variable (i_d) (please see Equation (15)). This Equation was deduced by considering that i_d and i_q are modeled as sources of controlled current in (7) and applying again the procedure of Equations (9) and (12):

$$\frac{G_{v_{DC}}(s)}{i_d} = \frac{R_oU_d}{R_oCs + 1}. \quad (15)$$

The procedure for obtaining the transfer function that permits regulating the output voltage in the Buck converter is obtained after applying the procedure of Equations (9) and (12) over Model (8). In this case, the transfer function is given by Equation (16):

$$\frac{V_{out}^{PV}}{U_{Buck}} = \frac{V_{DC}R_{Load}}{R_{Load}L_{Buck}C_{Buck}s^2 + L_{Buck}s + R_{Load}}. \quad (16)$$

4. Programmable Electronic Load: Control System

This section presents the implemented PEL control system. The control has as its main function the emulation of different load profiles, and at the same time, keeping the DC bus voltage stable. Figure 8 shows the implemented control system that is described as follows.

Currents i_a, i_b, and i_c correspond to the measured PEL line currents, whereas signal ωt is obtained from a phase lock loop (PLL) for synchronizing AC voltages with the control system. i_a, i_b, i_c, and ωt are processed by using an abc to dq transformation block. The outputs of this block are the current on the d axis (I_d^{PV}), and the current on q axis (I_q^{PV}). The measured voltage at the DC bus of the VSI is v_{DCbus}^{PV}.

The load profiles implemented in this paper are made of active and reactive currents; the VSI and Buck converter are coupled for this purpose. The VSI is controlled by using two controllers (d-loop and q-loop). The reactive power of the PEL is controlled by using the q-loop controller with the setpoint I_q^{SP}. The d-loop corresponds to a cascade control responsible for controlling the active power of the PEL. The Buck converter is controlled by using the p-loop controller for dissipating the excess of power in the R_{load} when the PEL is absorbing energy. The control logic of the p-loop and d-loop are not related; nevertheless, both physically interact on the DC bus. The p-loop takes energy from the DC bus and the d-loop gives energy to the DC bus from the electrical grid.

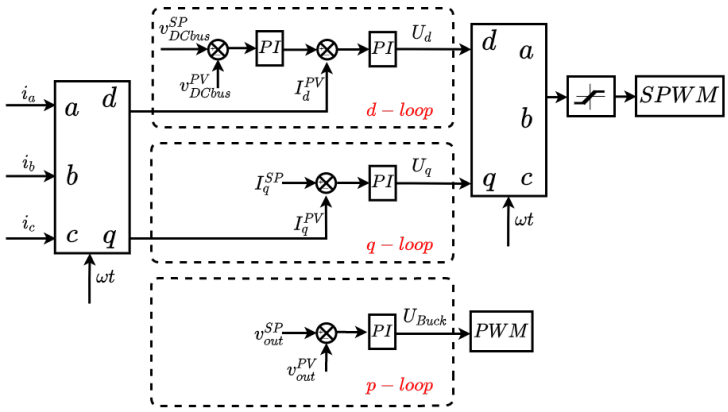

Figure 8. PEL control system.

The inputs and outputs of the three control loops are described as follows:

- The d-loop is a cascade control. Its external loop regulates the voltage in the DC bus whereas its inner loop controls the current of the d-axis. v_{DCbus}^{SP} is the set point of the DC bus voltage whereas the measured DC voltage is v_{DCbus}^{PV}. The PI controller of the external loop gives reference to the inner loop, compared with the measured current in the d-axis I_d^{PV}. The control signal of this cascade system (U_d) is one of the two inputs of dq to abc transformation. The parameters for this control are presented in Table 1.
- The q-loop is a PI control loop where I_q^{SP} is the set point, and I_q^{PV} is the measured current in the q-axis. The control signal of this system (U_q) is the other input of the dq to abc transformation block. The output of the dq to abc transformation block passes by a limiter in order to avoid over-modulation in the SPWM block.
- The p-loop is in charge of determining the dissipated active power in R_{load}, adjusting the output voltage v_{out}^{PV} with the Buck converter. The set point is v_{out}^{SP} and the measurement is v_{out}^{PV}. The control signal of this system (U_{Buck}) is the input of the PWM block. The control parameters for the Buck converter are given in Table 2.

Table 1. PEL control parameters.

	Parameters	Value
External d-loop	Kc_{vdc}	0.026
	Ti_{vdc}	0.015
Inner d-loop	Kc_{id}	0.1
	Ti_{id}	0.0008
q-loop	Kc_{iq}	0.108069
	Ti_{iq}	0.0008

Table 2. Buck control parameters.

Parameters	Value
Kc_{Buck}	0.074532
Ti_{Buck}	0.32

5. Experimental Results

This section presents the experimental results for the implemented PEL. Experimental tests were carried out for several load profiles and for several changes in their operation points. The results show that the PEL behaves adequately, emulating the programmed load profiles and stabilizing the DC bus.

5.1. Experimental Setup

Figure 9 presents the implemented PEL and its main components which are described as follows. (1) The main protection and line contactor that are in charge of protecting and connecting the PEL to the electrical grid. (2) Auxiliary protections that are in charge of protecting each PCB and control circuits. (3) Voltage source of $5V$ for polarizing the control system. (4) Voltage source of $15V$ for polarizing the trigger drivers of the VSI. (5) PCB for voltage measurement; this PCB measures v_a, v_b, v_c, and v_{DCbus}^{PV} with differential connection. This PCB is based on AMC1200 integrated circuits. (6) PCB of the digital signal processor (DSP) TMS3202F of Texas Instrument. (7) PCB for current measurement; this PCB measures i_a, i_b, and i_c and is based on ACS714 sensors. (8) Pre-charge bypass contactor. (9) Pre-charge resistors for the DC bus. (10) Control relays which are the interface between the control signals from the DSP and the contactors. (11) Capacitors (C_1, C_2) and resistors (R_1, R_2) of the DC bus. (12) Inductors L_1, L_2, and L_3 used for grid coupling. (13) IGBT bridge (VSI) coupled with the trigger drivers IRAM136-3063B. The values of parameters of the implemented PEL are summarized in Table 3.

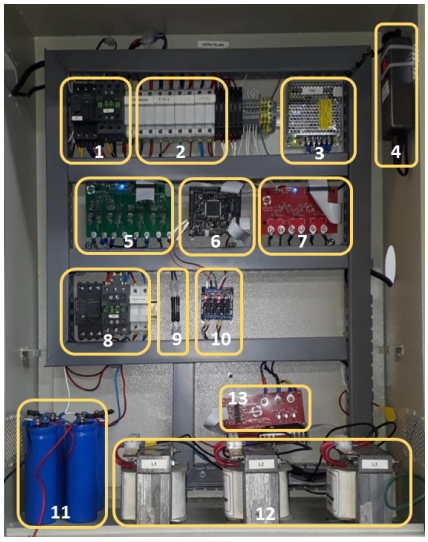

Figure 9. PEL hardware implementation.

Table 3. Implemented PEL parameters.

Parameters	Symbol	Value
Inductances	L_1 L_2 L_3 L_{Buck}	23.7 mH 23.7 mH 23.7 mH 23.7 mH
Capacitances	C_1, C_2 C_{Buck}	4400 uF 2700 uF
Resistances	R_1, R_2 R_{load}	30 k Ω 114 Ω
V_{in} PEL	v_a	208 V
PEL apparent power	S_{PEL}	1.8 kVA
DC bus voltage	v_{DCbus}^{SP}	60 V
Oscilloscope		$R\&S^{®}RTH1004$

5.2. Emulation of Three-Phase Load Profiles

This section has the purpose of validating the three-phase currents of the PEL when inductive, resistive, and capacitive load profiles are emulated. Figure 10 corresponds to an inductive load profile. This profile was obtained by using $i_q^{SP} = -4A$ as a setpoint, whereas the Buck converter output voltage was set to $v_{out}^{SP} = 0V$. The oscillogram depicted in Figure 10 plots the voltage and current signals at the AC coupling point versus time. Signal C4 (blue) is the measured voltage in phase a (v_a) with respect to the neutral point, scaling to 10V per division. Signals C1, C2, and C3 are the line currents i_a, i_b, and i_c (yellow, green, and orange, respectively) with a scale of 2 A per division, whereas the timescale is 5 ms per division. In Figure 10, it can be observed that the measurement cursors located at the maximum values of voltage v_a and current i_a, both have a time difference of approximately 4 ms; this represents $-86.4°$ which emulates an inductive load profile. The difference between measured and theoretical phase angle is due to the PEL active power losses. PEL must have satisfied internal power losses of semiconductors and wires. It can be stated that the implemented controller satisfactorily follows the current reference.

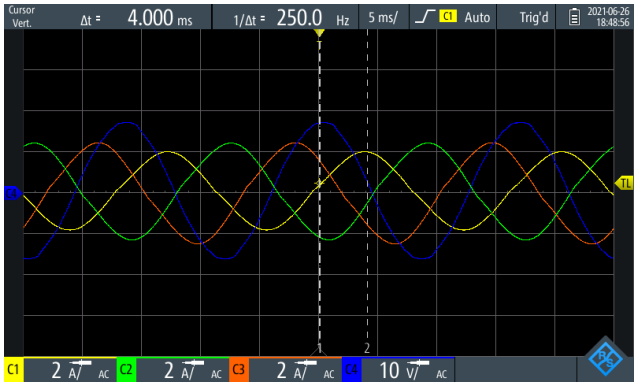

Figure 10. Three-phase inductive load profile.

Figure 11 corresponds to a resistive load profile. This profile was obtained by using $i_q^{SP} = 0$ as a setpoint, whereas the Buck converter output voltage was set to $v_{out}^{SP} = 45VDC$. Taking into account that the R_{load} is 114Ω and the output voltage v_{out}^{SP} is known, the dissipated power in the Buck converter is $17.7W$. It can be seen that v_a (blue) and i_a (yellow) are in phase.

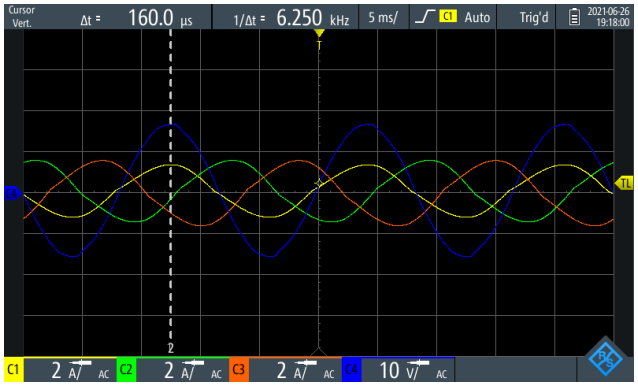

Figure 11. Three-phase resistive load profile.

Figure 12 corresponds to a capacitive load profile. The current setpoint is $i_q^{SP} = 1.5A$. Because it is not necessary an active power dissipation, the Buck output voltage was set to $v_{out}^{SP} = 0$. Note that the magnitude of i_q^{SP} for the capacitive profile ($1.5A$) is lower than the one for the inductive profile ($-4A$). This is because capacitive profiles require higher DC bus voltages. This phenomenon is consistent with the theory that was previously explained in Section 2.

Figure 12. Three-phase capacitive load profile.

5.3. DC Bus Stability with Different Load Profiles

This section has the purpose of validating the AC and DC voltages of the PEL when inductive, resistive and capacitive load profiles are emulated.

Figure 13 presents the measurements of currents and voltages of the PEL operation when a resistive–capacitive load profile is emulated. Signal C4 (blue) is v_a, signal C1 (yellow) is i_a, signal C2 (green) is the output voltage of the Buck converter (v_{out}^{PV}), and signal C3 (orange) is the DC bus voltage (v_{DCbus}^{PV}). The setpoint p-load Buck control loop (v_{out}^{SP}) was set with a value of $29V$. In this case, the PEL only consumes $7.4W$ of active power. The set point I_q^{SP} was set to $2A$ in the q-load loop.

PEL consumes active and reactive powers with a leading power factor. However, the voltage on the DC bus is not a constant default value and depends on the operating point. Therefore, the cascade controller described in Section 4 is responsible for keeping the DC voltage stable, and at the same time, regulating the direct current consumed from the grid (i_d^{PV}). The DC output voltage of the Buck converter (v_{out}^{PV}) allows for the determination of the active power consumed in the load resistor (R_{load}). The active power is reflected in the AC network consumption because it is dissipated by the Joule effect in the resistor R_{load}. Generally speaking, the active power dissipated by the Buck converter comes from the energy stored in the DC bus capacitors (C); which, in turn, also comes from the energy supplied by the power grid.

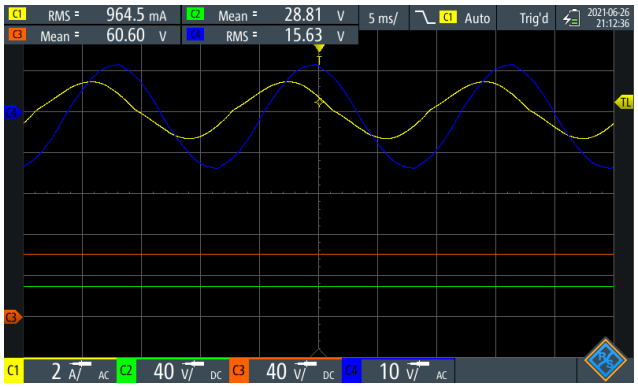

Figure 13. Resistive-capacitive load profile and DC voltages.

Figure 14 describes an inductive profile. This profile was obtained by using $i_q^{SP} = -4A$ as a setpoint whereas the Buck converter output voltage was set to $v_{out}^{SP} = 0V$. Figure 15 corresponds to a resistive load profile. This profile was obtained by using $i_q^{SP} = -4A$ as a setpoint whereas the Buck converter output voltage was set to $v_{out}^{SP} = 0V$. For both cases, the PEL follows the references operating appropriately. The DC bus voltage (v_{DCbus}^{PV}) remains stable under the different PEL operating conditions, evidencing the robustness of the d-loop control loop.

Figure 14. Inductive load profile and DC voltages.

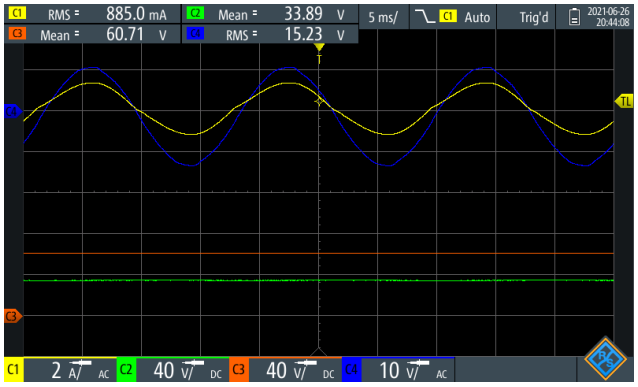

Figure 15. Resistive load profile and DC voltages.

5.4. Transient Behavior of the PEL with Changes in Load Profile

Figure 16 describes the transient behavior of the PEL. Note that the time scale (1 s/divison) is larger than the ones illustrated in previous subsections. The PEL was parameterized to emulate a leading and lagging reactive profile with setpoint steps (i_q^{SP}) of 0A, −1A, −2A, −2A, −2A, −1A, 0A, 0.25A, 0.5A, 0.5A, 1A, 0.5A, 0.25A, and 0A, changing its magnitude every 750 ms. The sign of the setpoint implies either leading or lagging. One of the conclusions of the principle of operation is that for the same voltage on the DC bus, it is possible to emulate lagging currents of greater magnitude with respect to the magnitudes in leading, which explains the asymmetry of Figure 16. The d-loop cascade control loop is in charge of keeping the DC bus voltage stable; note that C3 signal has over- and under-voltages, accounting for the disturbance and the d-loop control action. In conclusion, the PEL emulates different profiles with variations in time, remaining with stable control.

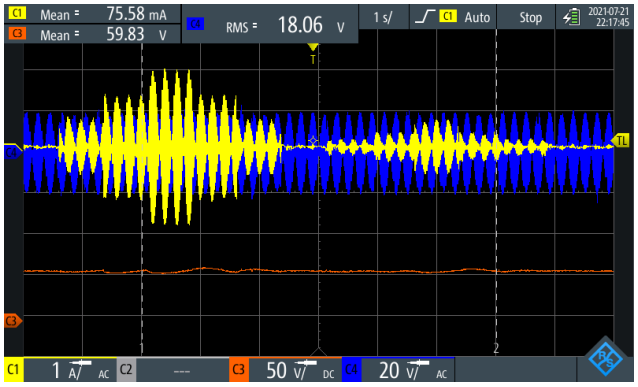

Figure 16. v_{DCbus}^{PV} and variable reactive loads profiles.

6. Conclusions

This paper presented the development of an AC three-phase PEL which allows the emulation of load profiles that are useful for testing MGs equipment. The four zones or quadrants obtained determine the PEL operation modes allowing us to establish the conditions that are necessary for programming the load profiles. There were also obtained the power and current limits which establish the control limitations. Three control loops were implemented in the PEL. Two controllers (d-loop and q-loop) were used for the VSI, a d-loop to control the active power and a q-loop to control the reactive power. The control of the Buck converter consists of a p-loop controller which permits the dissipation of excess of active power.

The load profiles shown in the results section allow us to validate the proper operation of the PEL. The emulation of three-phase currents was carried out in pure reactive power and active power scenarios. The DC voltages of the device remained stable, due to the

robust parameterization of the control loops. Finally, the transient behavior was evaluated, and the DC bus disturbances were stabilized by the control system.

Author Contributions: Conceptualization, L.F.S.-M., N.M.-G. and J.B.C.-Q.; data curation, L.F.S.-M. and P.A.G.-V.; formal analysis, L.F.S.-M., N.M.-G. and J.B.C.-Q.; funding acquisition, J.B.C.-Q., J.M.L.-L. and N.M.-G.; investigation, L.F.S.-M., N.M.-G. and J.B.C.-Q.; methodology, L.F.S.-M., N.M.-G. and J.B.C.-Q.; project administration, N.M.-G. and J.M.L.-L.; resources, L.F.S.-M., N.M.-G. and J.B.C.-Q.; supervision, N.M.-G., J.M.L.-L. and J.B.C.-Q.; visualization, L.F.S.-M., N.M.-G. and J.B.C.-Q.; writing—original draft, J.R.O.-C., L.F.S.-M. and P.A.G.-V.; writing—review and editing, J.M.L.-L., L.F.S.-M., J.R.O.-C., P.A.G.-V. and N.M.-G. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Colombia Scientific Program within the framework of the so-called Ecosistema Científico (Contract No. FP44842- 218-2018).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors gratefully acknowledge the support from the Colombia Scientific Program within the framework of the call Ecosistema Científico (Contract No. FP44842- 218-2018). The authors also want to acknowledge Universidad de Antioquia for its support through the project "estrategia de sostenibilidad".

Conflicts of Interest: The authors declare that they have no conflict of interest.

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