micromachines

Article

Numerical Investigation of Transient Breakdown Voltage Enhancement in SOI LDMOS by Using a Step P-Type Doping Buried Layer

Xiaoming Yang [1], Taiqiang Cao [1,*], Xiaohua Zhang [2], Tianqian Li [1] and Hang Luo [3]

[1] School of Electrical Engineering and Electronic Information, Xihua University, Chengdu 610039, China
[2] Department of Intelligent Systems, Hiroshima Institute of Technology, Hiroshima 7315193, Japan
[3] School of Mechanical Engineering, Sichuan University, Chengdu 610065, China
* Correspondence: tqcaoxhu@126.com

Abstract: In this paper, the transient breakdown voltage (*TrBV*) of a silicon-on-insulator (SOI) laterally diffused metal-oxide-semiconductor (LDMOS) device was increased by introducing a step P-type doping buried layer (SPBL) below the buried oxide (BOX). Device simulation software MEDICI 0.13.2 was used to investigate the electrical characteristics of the new devices. When the device was turned off, the SPBL could enhance the reduced surface field (RESURF) effect and modulate the lateral electric field in the drift region to ensure that the surface electric field was evenly distributed, thus increasing the lateral breakdown voltage (BV_{lat}). The enhancement of the RESURF effect while maintaining a high doping concentration in the drift region (N_d) in the SPBL SOI LDMOS resulted in a reduction in the substrate doping concentration (P_{sub}) and an expansion of the substrate depletion layer. Therefore, the SPBL both improved the vertical breakdown voltage (BV_{ver}) and suppressed an increase in the specific on-resistance ($R_{on,sp}$). The results of simulations showed a 14.46% higher *TrBV* and a 46.25% lower $R_{on,sp}$ for the SPBL SOI LDMOS compared to those of the SOI LDMOS. As the SPBL optimized the vertical electric field at the drain, the turn-off non-breakdown time (T_{nonbv}) of the SPBL SOI LDMOS was 65.64% longer than that of the SOI LDMOS. The SPBL SOI LDMOS also demonstrated that *TrBV* was 10% higher, $R_{on,sp}$ was 37.74% lower, and T_{nonbv} was 10% longer than those of the double RESURF SOI LDMOS.

Keywords: silicon-on-insulator; MOS devices; deep depletion; breakdown voltage; transient breakdown voltage; step P-type doping buried layer

Citation: Yang, X.; Cao, T.; Zhang, X.; Li, T.; Luo, H. Numerical Investigation of Transient Breakdown Voltage Enhancement in SOI LDMOS by Using a Step P-Type Doping Buried Layer. *Micromachines* **2023**, *14*, 887. https://doi.org/10.3390/mi14040887

Academic Editors: Nam-Trung Nguyen and Ha Duong Ngo

Received: 28 February 2023
Revised: 15 April 2023
Accepted: 17 April 2023
Published: 20 April 2023

1. Introduction

In the passing years, as the number of electric vehicles, charging piles, and intelligent electronic equipment is on the rise, there is a sustained and strong demand for power MOSFET. Despite those wide bandgap semiconductor power devices such as SiC and GaN developing in leaps and bounds, silicon devices still occupy the largest market share due to their low cost and mature technology. A silicon-on-insulator (SOI) laterally diffused metal-oxide-semiconductor (LDMOS) devices offer the advantages of high speed, low loss, and easy integration and are widely used in power integrated circuits [1–5]. Breakdown voltage (*BV*) is an important performance indicator of the SOI LDMOS and comprises the static *BV* (*StBV*) and the transient *BV* (*TrBV*). An electron inversion layer is formed under the buried oxide (BOX) of the SOI LDMOS in static conditions, such that there is no deep depletion (DD) effect in the substrate, which sustains very little *StBV* [6,7]. Thus, the device has low *StBV*. Scholars have obtained many results after long-term research on *StBV*. Some of these results have been obtained using an analytical model of *StBV* [8–14], and others are related to new structures [15–27], in some of which *StBV* can reach more than 1000 V [25–27]. However, when a device is turned off rapidly, there is insufficient time for an electron inversion layer to form under the BOX, which can induce a DD effect in the

substrate. The depletion layer in the substrate can sustain a portion of *TrBV* [6]. E. Napoli proposed a one-dimensional *TrBV* analytical model [7] and performed simulations and experiments [6,28,29] that verified that an appropriate reduction in the substrate doping concentration (P_{sub}) of the SOI LDMOS can increase *TrBV*. In [30], a new device structure is proposed that achieves a good trade-off between *TrBV* and specific on-resistance ($R_{on,sp}$). Like *StBV*, *TrBV* is determined by the smaller of the lateral breakdown voltage (BV_{lat}) and the vertical breakdown voltage (BV_{ver}). Studies have shown that although reducing the P_{sub} can promote expansion of the depletion layer and increase BV_{ver}, the surface field (RESURF) effect is reduced [31]. An extremely low P_{sub} can lead to an increase in the surface electric field at the source and premature breakdown, thus reducing BV_{lat} and resulting in a substantial decrease in *TrBV* [31]. Therefore, the doping concentration in the drift region (N_d) needs to be reduced simultaneously to obtain high *TrBV* [31], whereby $R_{on,sp}$ is also considerably increased. Double RESURF, step doping in the drift region, and linear variable doping in the drift region techniques are commonly applied to improve BV_{lat} of SOI LDMOS devices [32–35]. If BV_{lat} limits *TrBV*, these three techniques can also enhance *TrBV*. SOI LDMOS with a P-top layer is called a double RESURF SOI LDMOS (D-RESURF SOI LDMOS), whose P-top layer can improve BV_{lat} and lower $R_{on,sp}$ [33,34]. The lateral electric field distribution in the drift region of devices with step doping and a linear variable doping profile is more uniform than that of conventional devices. Therefore, they can achieve higher *TrBV* at the same drift region length. However, they have high $R_{on,sp}$ due to the too-low doping concentration in the drift region near the source optimizing for *TrBV*, and these two techniques are often suitable for ultra-thin SOI devices.

TrBV is an important performance indicator for high-speed SOI LDMOS switching devices. To improve *TrBV* and suppress the increase in $R_{on,sp}$, a SPBL was introduced below the BOX of the SOI LDMOS. The SPBL could optimize the lateral and vertical electric fields of the device and improve the *TrBV* of the device without increasing the $R_{on,sp}$. The simulation results showed that the *TrBV* of SPBL SOI LDMOS was higher than that of SOI LDMOS and D-RESURF SOI LDMOS, and the $R_{on,sp}$ was lower. As the vertical electric field was optimized, the turn-off non-breakdown time (T_{nonbv}) of the SPBL SOI LDMOS was longer than that of the SOI LDMOS and D-RESURF SOI LDMOS.

2. Device Structure and Simulation Settings

Figure 1a shows the SPBL SOI LDMOS device structure and simulation circuit, which differ from those of the conventional SOI LDMOS device shown in Figure 1c in that there was an SPBL below the BOX. The SPBL was divided into five-step P-type doping regions, and the doping concentration decreased from P_1 to P_5 by the same difference. x and y represent lateral distance from the left edge of the device and vertical distance from the top silicon surface, respectively. When the device is turned off, the high-concentration doping region of the SPBL near the source can enhance the RESURF effect and reduce the surface electric field at the source, whereas the low-concentration doping region near the drain promotes the downward expansion of the substrate depletion layer. After the SPBL is depleted, the negative charges in the SPBL exhibit a stepped distribution. This charge distribution has a significant modulation effect on the lateral electric field in the drift region, which causes the surface electric field in the middle to rise. The enhancement of the RESURF effect by the SPBL can decrease P_{sub}. Therefore, the SPBL enables the device to maintain a small $R_{on,sp}$ and increases BV_{lat} and BV_{ver}. Figure 1b shows the D-RESURF SOI LDMOS. A P-type doping layer, namely the P-top layer, is on the top of the drift region. P_{top} and t_{top} are the doping concentration and depth of the P-top layer, respectively. At high N_d, the source surface electric field of SOI LDMOS increases rapidly with the increase of drain voltage. However, the P-top layer in D-RESURF SOI LDMOS can effectively reduce the increasing speed of the surface electric field at the source and obtain higher *StBV*. If optimized for *StBV*, the N_d of the D-RESURF SOI LDMOS is twice that of SOI LDMOS. In other words, the $R_{on,sp}$ of the D-RESURF SOI LDMOS is smaller than that of SOI LDMOS at the same *StBV*. For *TrBV*, the P-top layer can also enhance the RESURF

effect, maintain high BV, and obtain lower $R_{on,sp}$. As mentioned in the introduction, most step doping SOI LDMOS and linear variable doping SOI LDMOS are usually ultra-thin SOI devices, and their $R_{on,sp}$ is high. Therefore, they were not added to the paper as a reference.

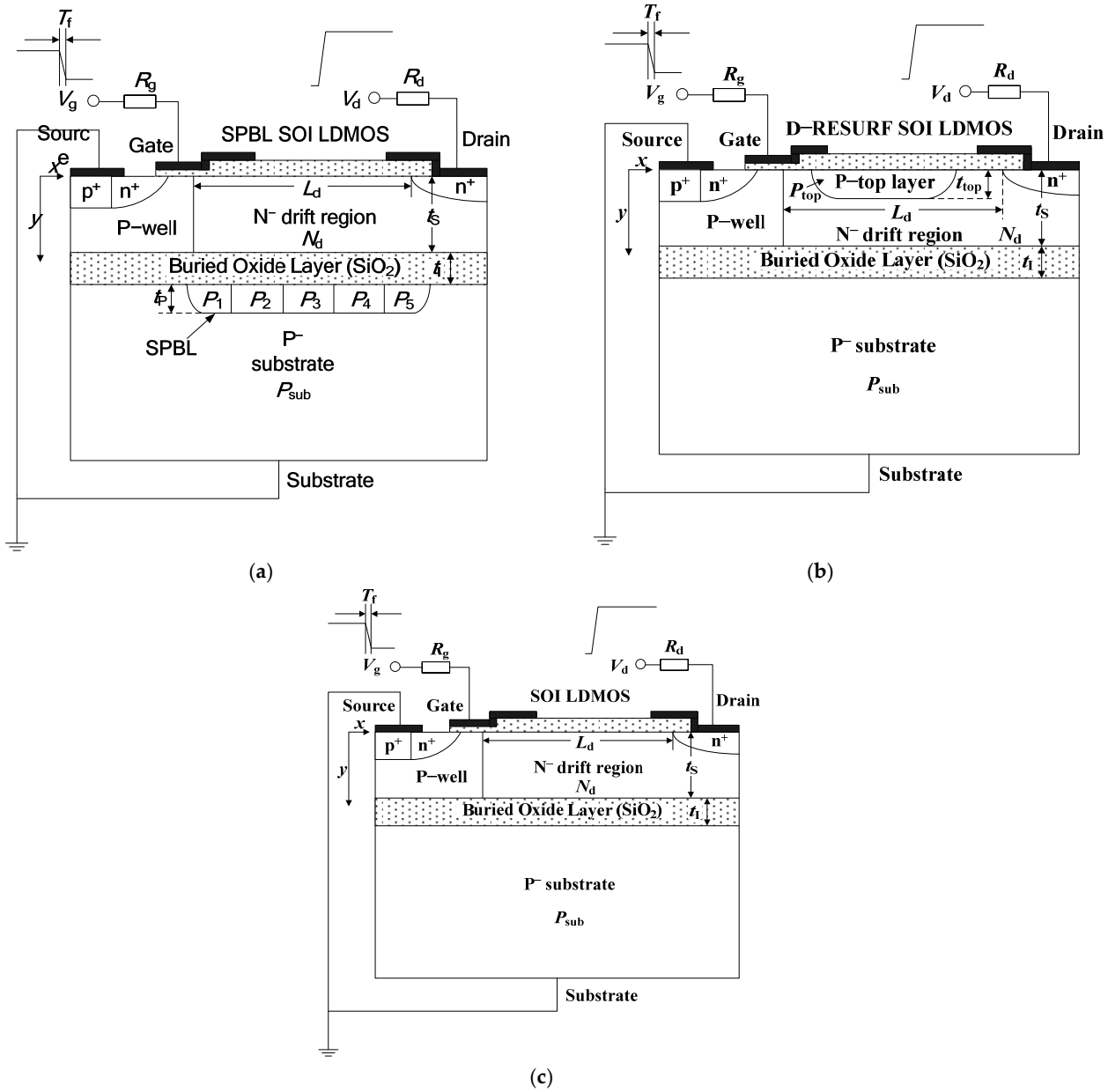


Figure 1. Device structure and simulation circuit of (**a**) SPBL SOI LDMOS, (**b**) D−RESURF SOI LDMOS, and (**c**) SOI LDMOS.

Step doping profile can be achieved by adjusting the implantation window width and multiple ion implantations [34]. The main manufacturing process of the SPBL SOI LDMOS is shown in Figure 2. First, a P-type substrate was lithographically aligned, followed by boron-ion implantation from the window to form the first doping region. Next, the window width was doubled to the right, and another boron-ion implantation was performed to form the second doped region. After five consecutive ion implantations, a SPBL was formed, as in Figure 2c. Then, SiO_2 was deposited on the P-type substrate to form a BOX; the BOX and substrate were treated with double-sided lithography for alignment marks, and the SiO_2 was planarized. Finally, the n-type SOI layer was bonded to the BOX, the SOI layer was thinned, and the lithography was aligned with the marks. The rest of the SPBL SOI LDMOS

manufacturing steps are compatible with the standard manufacturing process of the SOI LDMOS. Device fabrication steps and costs increase with the number of doping regions. Therefore, the number was two or three, and the cost could be effectively controlled.

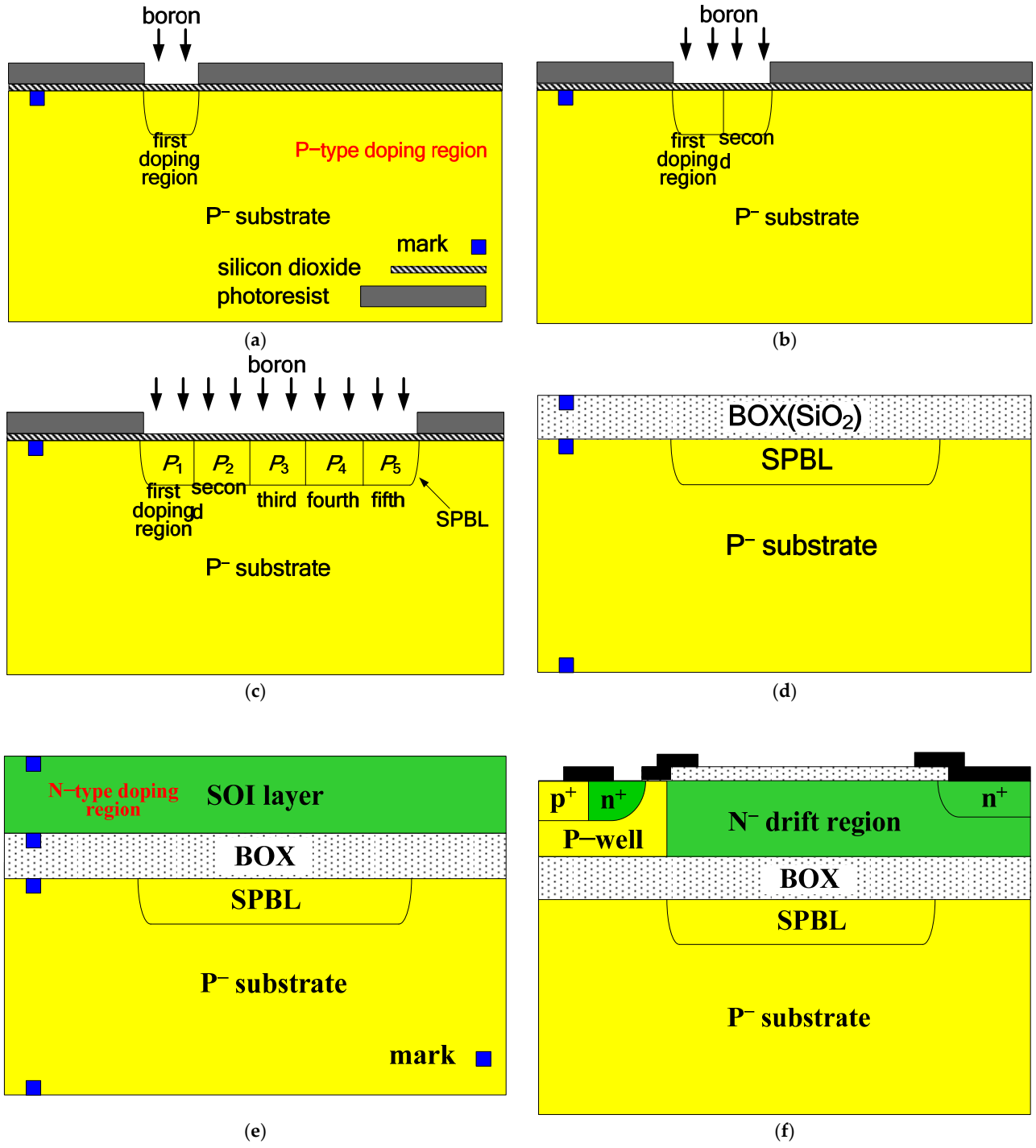


Figure 2. The main manufacturing process of an SPBL SOI LDMOS: (**a**) lithography alignment with marks, boron−ion implantation from the window to form the first doping region; (**b**) double the width of the window to the right, another boron−ion implantation to form the second doping region; (**c**) after five consecutive ion implantations, the formation of a SPBL; (**d**) deposition and planarization of SiO_2 and creation of alignment marks for double−sided lithography; and (**e**) bonding of SiO_2 and Si, thinning of the SOI layer and lithography alignment with marks. (**f**) The other manufacturing steps for the device are compatible with the standard manufacturing process for an SOI LDMOS.

The device parameters of the SOI LDMOS and the D-RESURF SOI LDMOS are listed in Table 1, while those of the D-RESURF SOI LDMOS are described later. To make a fair comparison of the *TrBV*s of the three devices, their P_{sub} was set to 2×10^{14} cm^{-3}, and the N_d of the SOI LDMOS was optimized to 2.4×10^{15} cm^{-3} based on the *TrBV*. To obtain a small $R_{on,sp}$ in the SPBL SOI LDMOS and the D-RESURF SOI LDMOS, N_d was set to 5×10^{15} cm^{-3}. Optimized for *TrBV* and $R_{on,sp}$, P_{top} and t_{top} in the D-RESURF SOI LDMOS were 1.1×10^{16} cm^{-3} and 1 µm, respectively. The other parameters of this device were the same as in SOI LDMOS. Figure 1 shows the circuit used to simulate the *TrBV* of the device [31]. The source and substrate electrodes of the test device were grounded, gate voltage V_g was applied to the gate through the gate resistor R_g, and a fixed drain voltage V_d was applied to the drain through the drain resistor R_d. R_g was set to a small value to ensure that the test device could be quickly turned off. The function of R_d was to limit the drain current to prevent damage to the device from an excessive current. MEDICI 0.13.2 software of Synopsys was used to perform a two-dimensional simulation of *TrBV* in the device. Several models, such as recombination, impact ionization, band-gap narrowing, mobility, and lifetime, were used in the simulation [30] The temperature (T) of the simulated device was 300 K by default. The breakdown condition of the device was that the drain current I_d exceeded 1×10^{-7} A/µm in the off-state. To simulate *TrBV*, V_d was a low positive voltage at which the test device did not break down, and V_g was decreased from 15 V to 0 V within 0.1 µs to turn the test device off. As a device is quickly turned off, there is insufficient time for an electron inversion layer to form under the BOX, the DD effect is induced in the substrate, which sustains a portion of V_d [6,7,28,29]. Then, V_d is increased until the test device breaks down. The V_d at breakdown is the *TrBV* of the test device. Every time V_d was changed, a simulation was carried out. This work was done by executing a batch file. If V_d was greater than or equal to *StBV*, the device could be broken down after being in the off-state for a period of time. The time between turning the device off and breakdown is T_{nonbv}. To simulate the T_{nonbv}, V_d was a voltage greater than *StBV*, and V_g was decreased from 15 V to 0 V within 0.1 µs to turn the test device off. After a period of time, I_d increased rapidly and exceeded 1×10^{-7} A/µm in the off-state. Data of I_d with time was stored in a log file by MEDICI. T_{nonbv} could be obtained by subtracting the turn-off time from the breakdown time.

Table 1. Device parameters.

Symbol	Device Parameters	SPBL SOI LDMOS	SOI LDMOS
L_d	Length of drift region	50 µm	50 µm
L_{chan}	Channel length	5 µm	5 µm
t_g	Gate oxide thickness	50 nm	50 nm
t_S	Drift region thickness	4 µm	4 µm
t_I	Buried oxide thickness	0.5 µm	0.5 µm
t_P	SPBL thickness	1 µm	-
P_{well}	Doping concentration in P-well	2×10^{17} cm^{-3}	2×10^{17} cm^{-3}
N_d	Doping concentration in N^- drift region	5×10^{15} cm^{-3}	2.4×10^{15} cm^{-3}
P_{sub}	Doping concentration of P^- substrate	2×10^{14} cm^{-3}	2×10^{14} cm^{-3}
P_1	Doping concentration in first region	1.1×10^{16} cm^{-3} $\rightarrow$ 1.8×10^{16} cm^{-3}	-
P_5	Doping concentration in fifth region	1×10^{15} cm^{-3} $\rightarrow$ 7×10^{15} cm^{-3}	-

3. Results and Discussion

Figure 3 shows the distribution of the charge under the BOX and lateral electric field and the potential of the three devices. The doping concentration of SPBL was reduced from $P_1 = 1.5 \times 10^{16}$ cm^{-3} to $P_5 = 1 \times 10^{15}$ cm^{-3} in five steps of 3.5×10^{15} cm^{-3} each. *TrBV* of the SPBL SOI LDMOS was 768 V, which corresponded to a 14.46% increase from that of the SOI LDMOS (671 V) and a 10% increase from that of the D-RESURF SOI LDMOS (698 V). Note that using an N_d of 5×10^{15} cm^{-3} for the SOI LDMOS and optimizing P_{sub} to

1.7×10^{15} cm^{-3} with respect to *TrBV* resulted in a *TrBV* of only 337 V. Figure 3a shows that compared to those of the SOI LDMOS and the D-RESURF SOI LDMOS, the distribution of equipotential lines in the drift region was more uniform and the substrate depletion layer was deeper in the SPBL SOI LDMOS, that is, the lateral electric field in the drift region was more uniform and both BV_{lat} and BV_{ver} were larger. The surface potential of SPBL SOI LDMOS in the drift region decreased from 768 V to 0 V with a relatively constant value, and the potential distribution line was relatively straight, as in Figure 3a. The decrease rate of the surface potential of the other two devices varied greatly, and the two potential distribution lines fluctuated obviously. Figure 3b shows the distribution of the charge concentration under the BOX for the three devices. There were five steps in the charge distribution below the BOX of the SPBL SOI LDMOS. The charge concentration iwas 1.5×10^{16} cm^{-3} in the first region near the source and decreased to 1×10^{15} cm^{-3} in the fifth region near the drain in fixed step sizes. These four sudden changes in the charge concentration in the SPBL could introduce spikes into the lateral electric field. The charge concentration of 2×10^{14} cm^{-3} under the conventional SOI LDMOS and the D-RESURF SOI LDMOS was evenly distributed, and it did not contribute to the improvement of the electric field in the middle of the drift region. Figure 3c shows the lateral electric field distribution of the three devices. Unlike with the SOI LDMOS, there were four clear electric field spikes in the lateral electric field inside the BOX (y = 4.49 μm) and the bottom of the drift region (y = 3.99 μm) of the SPBL SOI LDMOS, where the lateral electric field in the middle was higher. The surface electric field (y = 0.001 μm) of the new device was far from the SPBL and was weakly modulated. Although there was no electric field spike on the surface of the drift region of the SPBL SOI LDMOS, the electric field in the middle was uniform and higher than that of the conventional SOI LDMOS and the D-RESURF SOI LDMOS, indicating that the depleted SPBL modulated the lateral electric field in the drift region, which increased the BV_{lat} of the new device. The P-top layer of the D-RESURF SOI LDMOS could also modulate the surface electric field, but the surface electric field of the D-RESURF SOI LDMOS was not as uniform as that of the SPBL SOI LDMOS. Figure 4 shows the current distribution in the drift region of the three devices at V_g = 15 V and V_d = 0.1 V. The N_d and the current distribution area determine the drain current in the drift region. The N_d of the SPBL SOI LDMOS was 5×10^{15} cm^{-3}, and the current distributed throughout the drift region, as in Figure 4a. Therefore, its I_d was the largest among those of the three devices. The N_d of the D-RESURF SOI LDMOS was the same as that of the SPBL SOI LDMOS, and there was no current in the P-top layer, as seen in Figure 4b. Its I_d was the second largest among those of the three devices. Although the current of the SOI LDMOS distributed throughout the drift region, the N_d was less than half that of the other two devices. Its current was the smallest among those of the three devices. According to the I_d of these three devices, their $R_{on,sp}$ could be calculated. The $R_{on,sp}$ was 7.82 Ω·mm^2 for the SPBL SOI LDMOS, which was 46.25% lower than that of the SOI LDMOS (14.55 Ω·mm^2) and 37.74% lower than that of the D-RESURF SOI LDMOS (12.56 Ω·mm^2).

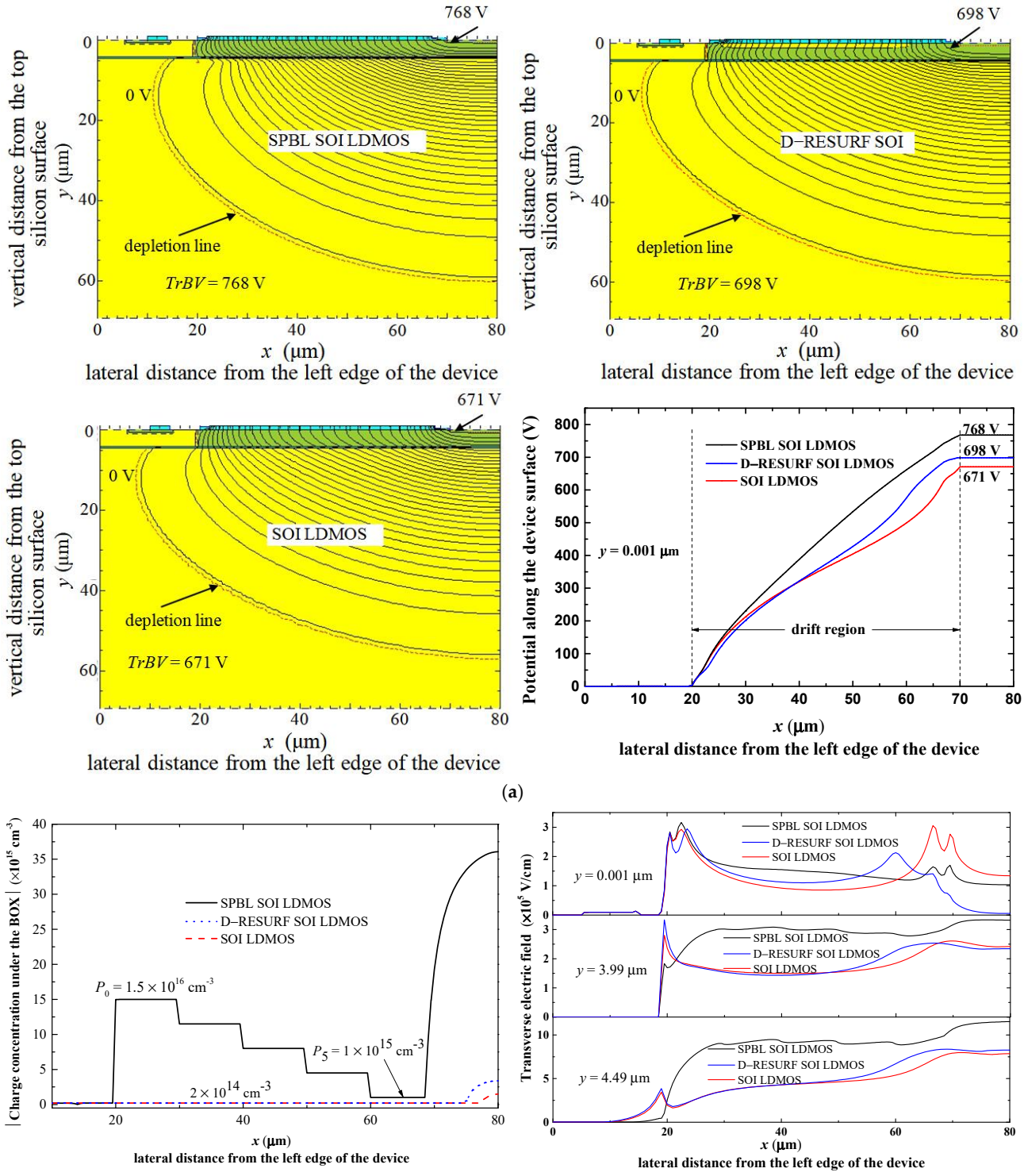


Figure 3. Distributions of SPBL SOI LDMOS, D−RESURF SOI LDMOS, and SOI LDMOS devices' (**a**) potential (20 V/contour), (**b**) charge under the BOX, and (**c**) lateral electric field.

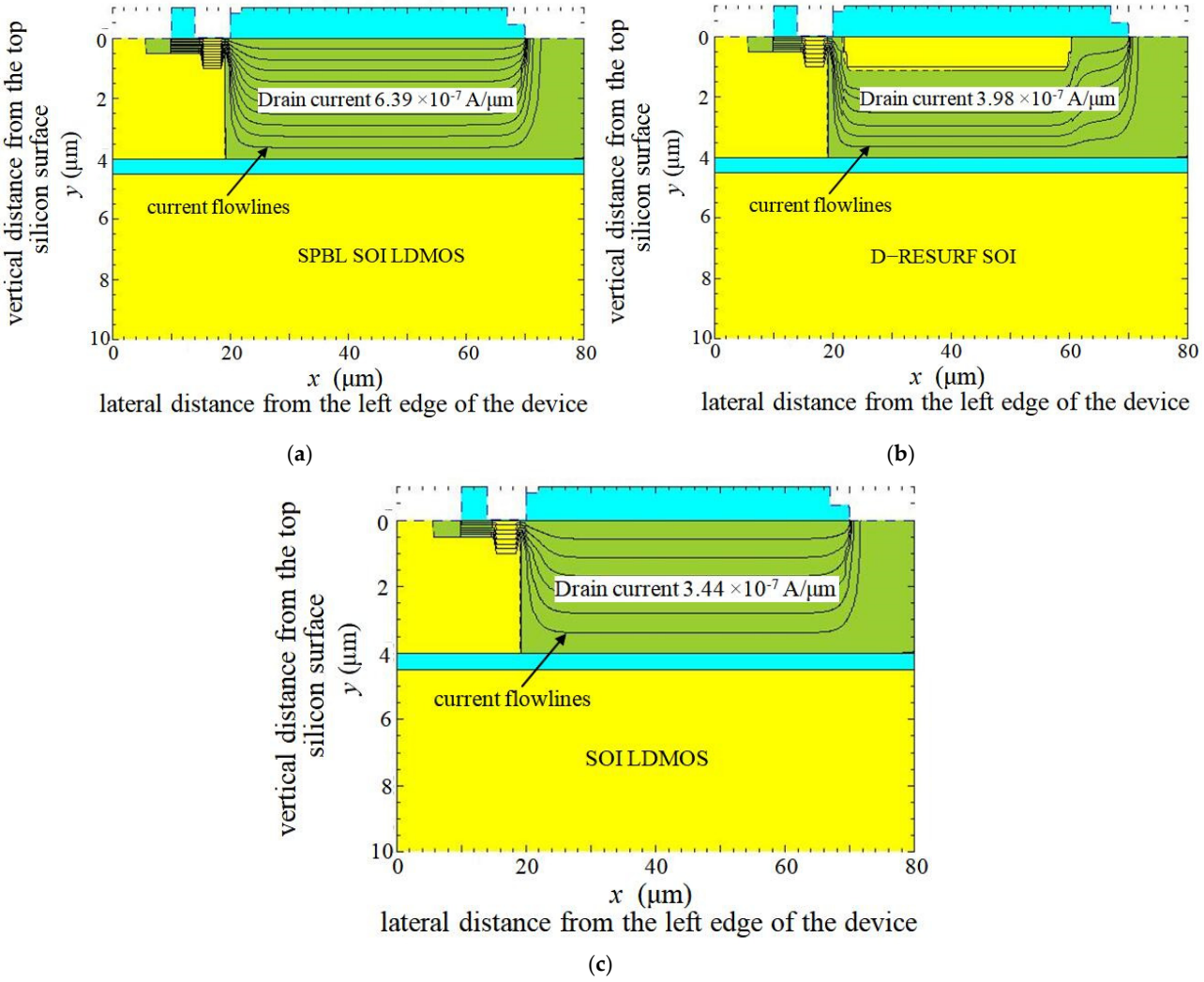


Figure 4. Current distributions in the drift region of (**a**) SPBL SOI LDMOS, (**b**) D−RESURF SOI LDMOS, and (**c**) SOI LDMOS at V_g = 15 V and V_d = 0.1 V.

Figure 5 shows the effect of the SPBL doping concentration on *TrBV*. The *TrBV* of the SOI LDMOS device depended on the smaller of BV_{lat} and BV_{ver}, both of which were affected by the SPBL doping concentration. Increasing the SPBL doping concentration weakened the surface electric field at the source, which was conducive to increasing BV_{lat} and hindered the downward expansion of the substrate depletion layer to reduce BV_{ver}. To obtain the maximum *TrBV*, P_1 and P_5 needed to be optimized. At a fixed P_5 and a low P_1, the SPBL did not sufficiently weaken the surface electric field at the source, resulting in premature breakdown of the device at the source surface, and BV_{lat} was lower than BV_{ver}. The *TrBV* was limited by BV_{lat}. Therefore, increasing P_1 could reduce the surface electric field at the source and increase BV_{lat}, thereby increasing the *TrBV* of the device. At a P_5 of 1×10^{15} cm^{-3}, *TrBV* initially increased with P_1 to a maximum value of 768 V at $P_1 = 1.5 \times 10^{16}$ cm^{-3}. BV_{lat} was equal to BV_{ver}. As P_1 increased, the doping concentration of the other regions (except for the fifth region) also increased accordingly, which enhanced the blocking effect of the SPBL on the downward expansion of the substrate depletion layer, resulting in BV_{ver} being lower than BV_{lat}. The *TrBV* was limited by BV_{ver}. Therefore, as P_1 increased from 1.5×10^{16} cm^{-3} to 1.8×10^{16} cm^{-3}, *TrBV* was affected by the decrease in BV_{ver} and continued to decrease. In short, when P_5 was constant, P_1 increased from low to high, BV_{lat} increased from low to high, and BV_{ver} decreased from high to low. When BV_{lat} was lower than BV_{ver}, *TrBV* was determined by BV_{lat}, and *TrBV* increased with P_1. When

BV_{lat} equaled BV_{ver}, *TrBV* reached the maximum. When BV_{ver} was less than BV_{lat}, *TrBV* was determined by BV_{ver}, and *TrBV* decreased with the increase of P_1. Similarly, increasing P_5 promoted the weakening of the surface electric field at the source and increased BV_{lat} but hindered the downward expansion of the depletion layer and reduced BV_{ver}. It can be seen from Figure 5 that for different P_5 values, the trend of *TrBV* with increasing P_1 was consistent. The larger P_5, the earlier *TrBV* reached a maximum in P_1. However, the increase in P_5 reduced BV_{ver} and thereby the maximum *TrBV*.

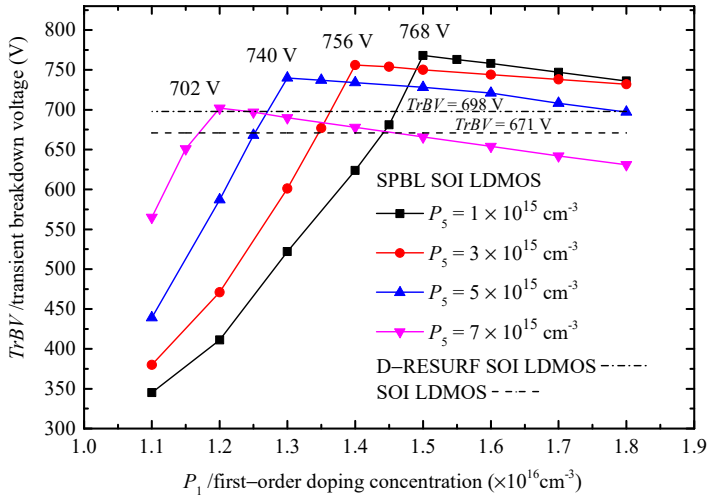
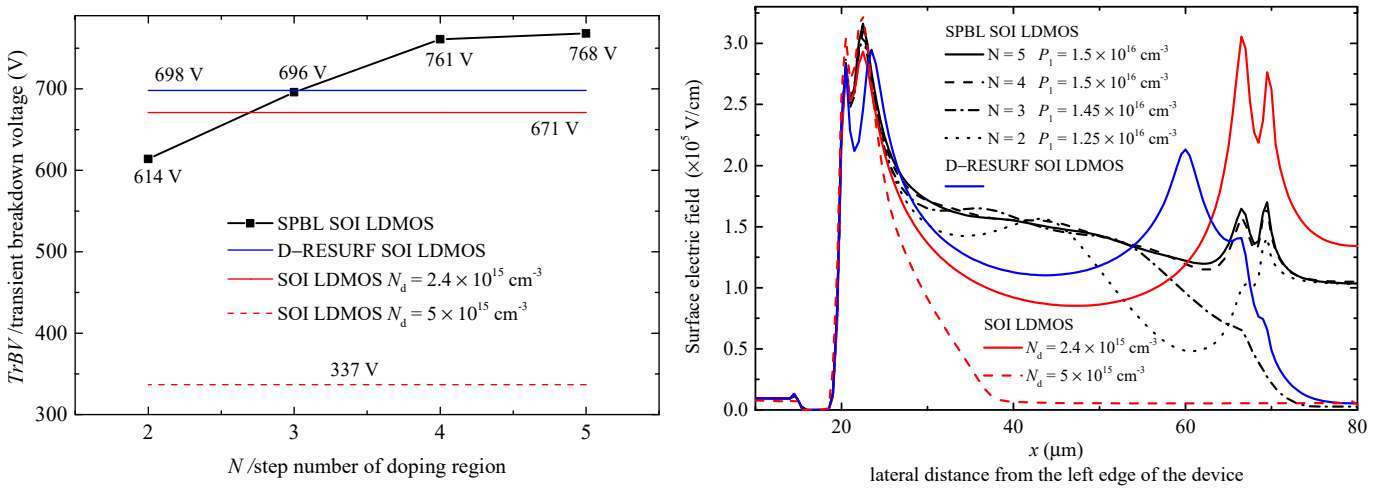


Figure 5. Effect of the SPBL doping concentration on the *TrBV* of the SPBL SOI LDMOS.

Figure 6 shows the influence of the number of doping regions (*N*) of SPBL on *TrBV* and surface electric field. The *TrBV* of the SPBL SOI LDMOS listed in Figure 6a was the maximum value that could be gained by optimizing the doping concentration of SPBL at different *N*. The *TrBV* of the device increased with the *N* and then tended to be saturated. In Figure 6b, the surface electric fields of the SPBL SOI LDMOS were compared at different *N*. When $N = 2$, there was a comparatively high peak in the middle of the surface electric field, but the electric field near the drain was too low. *TrBV* was 614 V. When $N = 3$, there were two peaks in the middle of the surface electric field, which made the surface electric field more uniform and the electric field near the drain higher. *TrBV* increased to 696 V. When $N = 4$, the surface electric field in the middle of the drift region and near the drain was more uniform, and *TrBV* was further increased to 761 V. When $N = 5$, the surface electric field distribution was almost the same as that of $N = 4$, and *TrBV* was 768 V and only increases by 7 V. Therefore, with an increase of *N*, the SPBL modulated the surface electric field more uniformly, and a higher *TrBV* could be obtained. For the SOI LDMOS, the surface electric field at the source was too high at $N_d = 5 \times 10^{15}$ cm^{-3}. The device was prematurely broken down, and its *TrBV* was 337 V. When $N_d = 2.4 \times 10^{15}$ cm^{-3}, the surface electric field peaks were at the source and drain, and the electric field at the middle of the drift region was low. *TrBV* was increased to 671 V. Compared to that of the SOI LDMOS, the surface electric field of the D-RESURF SOI LDMOS in the drift region was more uniform and higher, and its *TrBV* was also 27 V higher. The $R_{on,sp}$ of the SPBL SOI LDMOS was the lowest among those of the three devices. At $N = 3$, the *TrBV* of the SPBL SOI LDMOS was as high as that of the D-RESURF SOI LDMOS and higher than that of the SOI LDMOS. At $N > 3$, the *TrBV* of the SPBL SOI LDMOS was higher than that of the other two devices.



(**a**) (**b**)

Figure 6. Influence of N on $TrBV$ and surface electric field of SPBL SOI LDMOS: (**a**) the influence of N on $TrBV$, (**b**) influence of N on surface electric field distribution ($P_N = 1 \times 10^{15}$ cm^{-3}).

Turning the device off generates electron-positron pairs in the substrate depletion layer. Under an electric field, the electrons move into and continuously accumulate at the bottom of the BOX, and the holes move to the edge of the depletion layer and recombine with the electrons, thereby continuously thinning the depletion layer [30]. Therefore, with increasing time, the voltage sustained by the device substrate continuously decreases, and the voltage sustained by the drift region and the BOX continuously increases. The maximum voltage that the drift region and BOX can sustain is approximately equal to $StBV$. If V_d is greater than or equal to $StBV$, the device can be broken down after being in the off-state for a period of time. T_{nonbv} serves as a reference for the lowest operating frequency of the device [31]. Figure 7 shows the effect of different Ts and V_ds on T_{nonbv}. The higher the V_d, the more rapid the rate of increase in the voltage sustained by the drift region and BOX, and the smaller the T_{nonbv}. The effect of T on T_{nonbv} was more significant. The generation rate of electrons and holes in the substrate depletion layer increased rapidly with T, resulting in a rapid thinning of the depletion layer and a significant decrease in T_{nonbv}. Figure 7 shows that for a constant T, the T_{nonbv} of the three devices decreased rapidly with increasing V_d. The T_{nonbv} of the three devices decreased sharply with increasing T. However, for fixed T and V_d, the SPBL SOI LDMOS always had a larger T_{nonbv} than the SOI LDMOS and the D-RESURF SOI LDMOS did. For a T of 400 K and V_d above 500 V, the substrate depletion layer of the SOI LDMOS thinned sufficiently rapidly that the device could no longer be turned off. The D-RESURF SOI LDMOS also could not be turned off when V_d was higher than 550 V. Figure 8 shows the distribution of the vertical electric field and potential at the drain of the three devices at different times for T = 373 K and V_d = 500 V. They were turned off at t = 3.7 μs: the SOI LDMOS device was broken down first at t = 9.55 μs, the D-RESURF SOI LDMOS device was broken down at t = 12.51 μs, and the SPBL SOI LDMOS was broken down at t = 13.39 μs. The T_{nonbv} of the SPBL SOI LDMOS of 9.69 μs was 65.64% longer than that of the SOI LDMOS (5.85 μs), indicating that the operating frequency had a lower minimum and a wider range for the SPBL SOI LDMOS than the SOI LDMOS. The T_{nonbv} of the D-RESURF SOI LDMOS was 8.81 μs, and it was slightly shorter than that of the SPBL SOI LDMOS. The vertical electric field in and the voltage sustained by the drift region and the BOX of the three devices were set to E_1 and V_1, respectively, and the voltage sustained by the substrate depletion layer was set to V_2. Figure 8a shows that for a fixed time, the electric field at the vertical n+/n- junction at the drain of the SPBL SOI LDMOS was much lower than that of the SOI LDMOS because the N_d of the SPBL SOI LDMOS was more than twice that of the SOI LDMOS. Solving the Poisson equation with boundary conditions shows that E_1 was lower for the SPBL SOI LDMOS than the SOI LDMOS. Therefore, for

the same time and V_d, the SPBL SOI LDMOS had a smaller V_1, a larger V_2, and a deeper substrate depletion layer than those of the SOI LDMOS. During device breakdown of the SPBL SOI LDMOS and SOI LDMOS, the maximum voltage sustained by the depletion layer and BOX and the substrate depletion layer depth were almost the same. Thus, the depletion layer of the SPBL SOI LDMOS was deeper than that of the SOI LDMOS during turn-off, and the depletion layer depth of both devices was equal during breakdown, such that the T_{nonbv} of the SPBL SOI LDMOS was longer than that of the SOI LDMOS. Figure 8b shows that at t = 3.7 µs and V_d = 500 V, the depth of the substrate depletion layer and V_1 were 52 µm and 74 V, respectively, for the SPBL SOI LDMOS. The depth of the substrate depletion layer and V_1 were 50 µm and 109 V, respectively, for the SOI LDMOS. At t = 9.55 µs, the depth of the substrate depletion layer of the SPBL SOI LDMOS decreased to 49.5 µm, V_1 increased to 128 V, and the device was not broken down, whereas for the SOI LDMOS, the depth of the substrate depletion layer was 47.5 µm and V_1 increased to 170 V, which exceeded *StBV*, resulting in device breakdown. Note that the *StBV* of the device was higher at T = 373 K than that at T = 300 K. At t = 13.39 µs, the depth of the substrate depletion layer of the SPBL SOI LDMOS decreased further to 48 µm, V_1 increased to 162 V, and the device was broken down. Because the N_d of the D-RESURF SOI LDMOS was the same as that of the SPBL SOI LDMOS, their electric field and potential distribution were almost the same during turn-off and breakdown. The P-top layer in the D-RESURF SOI LDMOS not only weakened the electric field of the source but also enhanced the electric field of the drain. When the substrate depletion layer decreased, the E_1 of the D-RESURF SOI LDMOS increased faster than that of the SPBL SOI LDMOS. The D-RESURF SOI LDMOS was broken down earlier than the SPBL SOI LDMOS. The T_{nonbv} of the D-RESURF SOI LDMOS was slightly shorter than that of the SPBL SOI LDMOS but longer than that of SOI LDMOS.

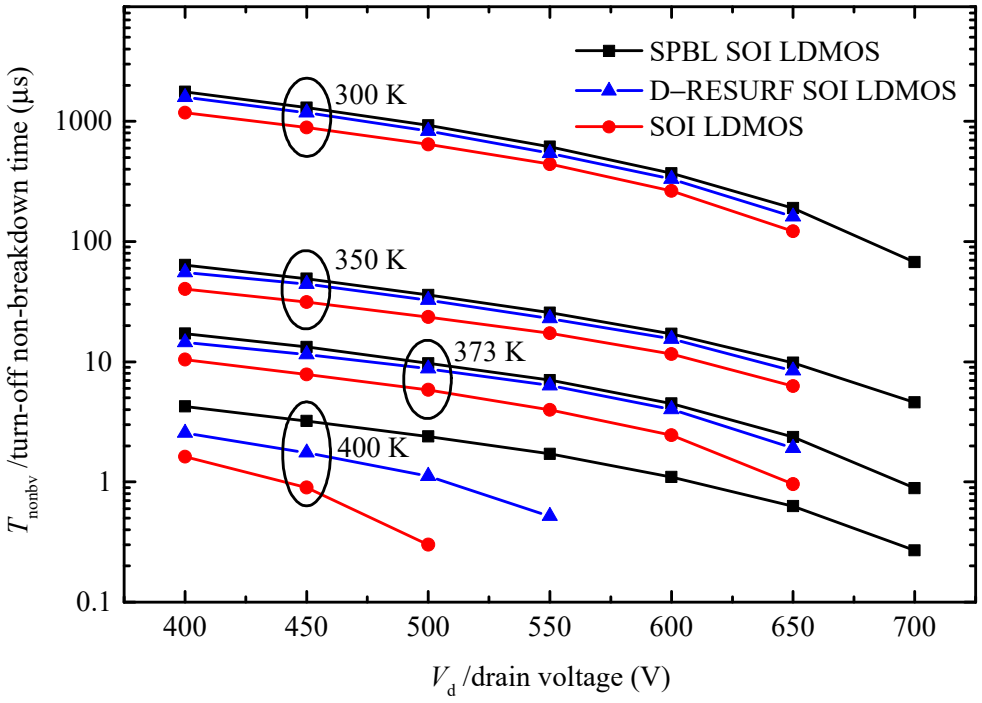


Figure 7. Relationship between T_{nonbv} and V_d at different device temperatures.

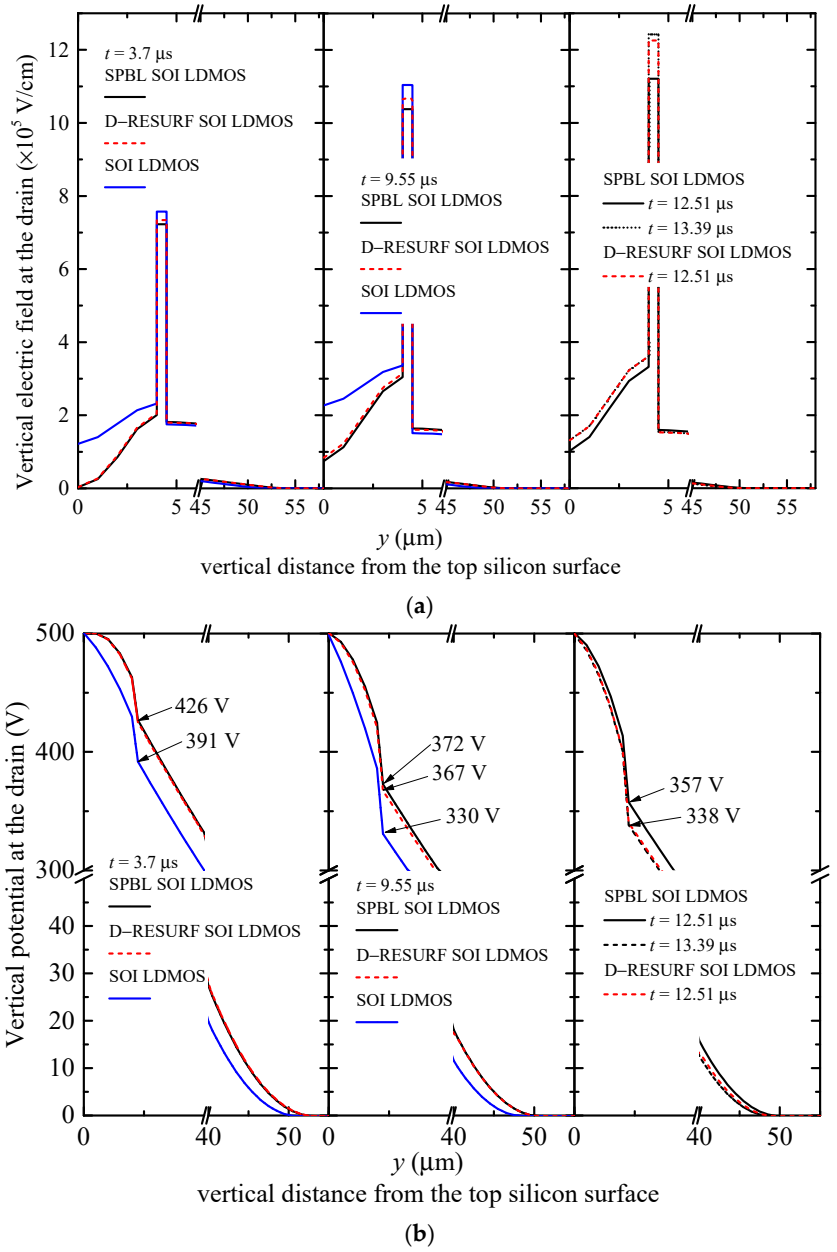


Figure 8. Distribution of vertical electric field and potential at the drain of the SPBL SOI LDMOS, D−RESURF SOI LDMOS and SOI LDMOS at different time points (T = 373 K, V_d = 500 V): (**a**) vertical electric field distribution and (**b**) vertical potential distribution.

4. Conclusions

The introduction of an SPBL into an SOI LDMOS improved the *TrBV* and suppressed the increase in $R_{on,sp}$ by optimizing the lateral and vertical electric fields of the device. At t_S = 4 μm, t_I = 0.5 μm, L_d = 50 μm, and N_d = 5 × 10^{15} cm^{-3}, the *TrBV* of the SPBL SOI LDMOS was 768 V, which was 127.89% higher than that of the SOI LDMOS for the same N_d. For a fixed P_{sub} = 2 × 10^{14} cm^{-3}, the *TrBV* and $R_{on,sp}$ were 14.46% higher and 46.25% lower, respectively, in the SPBL SOI LDMOS than in the SOI LDMOS. At T = 373 K and V_d = 500 V, the T_{nonbv} of the SPBL SOI LDMOS was 65.64% longer than that of the SOI LDMOS. The SPBL SOI LDMOS also demonstrated that *TrBV* was 10% higher, $R_{on,sp}$ was 37.74% lower, and T_{nonbv} was 10% longer than in the D-RESURF SOI LDMOS.

Subsequent research will focus on the manufacturing process of the new device and its application in the switching power supply circuit. The process of forming a SPBL with

only one ion implantation to reduce the cost will be studied. If V_g is constant at 0 V and V_d is higher than *StBV* due to a circuit fault, the device will be broken down. A protection circuit needs to be designed to avoid device breakdown.

Author Contributions: Conceptualization, X.Y., T.C., X.Z. and T.L.; methodology, software, and validation, X.Y., H.L. and T.L.; formal analysis, investigation, data curation, and writing—original draft preparation, X.Y.; writing—review and editing, X.Y., T.C. and X.Z. All authors have read and agreed to the published version of the manuscript.

Funding: The work is supported in part by the Ministry of Education "Chunhui Plan" Foundation of China under Grant Z2016147 and Z2017073, the Science and Technology Foundation of Chengdu, China, under Grant 2021-JB00-00025-GX, the Sichuan Science and Technology Program under Grant 2023YFG0350 and the Xihua University Key Fundation under Grant Z1320926.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Cristoloveanu, S. Far-future trends in SOI technology: A guess. *Int. J. High Speed Electron. Syst.* **2002**, *12*, 343–351. [CrossRef]
2. Cristoloveanu, S. Silicon on insulator technologies and devices: From present to future. *Solid State Electron.* **2001**, *45*, 1403–1411. [CrossRef]
3. Nakagawa, A. Impact of dielectric isolation technology on power ICs. In Proceedings of the 3rd International Symposium on Power Semiconductor Devices and ICs, Baltimore, MD, USA, 22–24 April 1991. [CrossRef]
4. Shimamoto, S.; Yanagida, Y.; Shirakawa, S.; Miyakoshi, K.; Oshima, T.; Sakano, J.; Wada, S.; Noguchi, J. High-Performance p-Channel LDMOS Transistors and Wide-Range Voltage Platform Technology Using Novel p-Channel Structure. *IEEE Trans. Electron. Devices* **2013**, *60*, 360–365. [CrossRef]
5. Zhang, W.; Qiao, M.; Wu, L.; Ye, K.; Wang, Z.; Wang, Z.; Luo, X.; Zhang, S.; Su, W.; Zhang, B.; et al. Ultra-low specific on-resistance SOI high voltage trench LDMOS with dielectric field enhancement based on ENBULF concept. In Proceedings of the 25th International Symposium on Power Semiconductor Devices, Kanazawa, Japan, 26–30 May 2013. [CrossRef]
6. Napoli, E.; Udrea, F. Substrate deep depletion: An innovative design concept to improve the voltage rating of SOI power devices. In Proceedings of the 2006 IEEE International Symposium on Power Semiconductor Devices and IC's, Naples, Italy, 4–8 June 2006. [CrossRef]
7. Napoli, E. One Dimensional Model for the Duration of the High Breakdown Phase in Deep Depletion Power Devices. In Proceedings of the 2007 International Semiconductor Conference, Sinaia, Romania, 15 October–17 September 2007. [CrossRef]
8. Kim, I.; Matsumoto, S.; Sakai, T.; Yachi, T. Analytical approach to breakdown voltages in thin-film SOI power MOSFETs. *Solid State Electron.* **1996**, *39*, 95–100. [CrossRef]
9. Chung, S.; Han, S.; Shin, J.; Choi, Y.; Kim, S. An analytical model for minimum drift region length of SOI RESURF diodes. *IEEE Electron. Device Lett.* **1996**, *17*, 22–24. [CrossRef]
10. Chung, S.; Han, S. Analytical model for the surface field distribution of SOI RESURF devices. *IEEE Trans. Electron. Devices* **1998**, *45*, 1374–1376. [CrossRef]
11. Popescu, A.; Ng, R.; Milne, W.I.; Udrea, F. Analytical modelling for the RESURF effect in JI and SOI power devices. *IEE Proc. Circuits Devices Syst.* **2002**, *149*, 273–284. [CrossRef]
12. Hu, X.; Wang, W.; Ji, Y.; Hua, Q. The influence of the N+ floating layer on the drift doping of RESURF LDMOS and its analytical model. *IEICE Electron. Express* **2016**, *13*, 20160852. [CrossRef]
13. Xing, J.; Duan, B.; Dong, Z.; Wang, X.; Yang, Y. Analytical model of buried air partial SOI LDMOS. *Superlattices Microstruct.* **2019**, *132*, 106162. [CrossRef]
14. Yang, K.; Guo, Y.; Zhang, J.; Yao, J.; Li, M.; Du, L.; Huang, X. An Analytical Breakdown Model for the SOI LDMOS With Arbitrary Drift Doping Profile by Using Effective Substrate Voltage Method. *IEEE J. Electron. Devices Soc.* **2020**, *8*, 49–56. [CrossRef]
15. Cheng, J.; Lin, J.; Chen, W.; Wu, S.; Huang, H.; Yi, B. Lateral Power Fin MOSFET With a High-k Passivation for Ultra-Low On-Resistance. *IEEE Access* **2020**, *8*, 48991–48999. [CrossRef]
16. Zhang, W.; Li, L.; Qiao, M.; Zhan, Z.; Cheng, S.; Zhang, S.; He, B.; Luo, X.; Li, Z.; Zhang, B. A Novel High Voltage Ultra-Thin SOI-LDMOS With Sectional Linearly Doped Drift Region. *IEEE Electron. Device Lett.* **2019**, *40*, 1151–1154. [CrossRef]
17. Guo, J.; Hu, S.; Huang, Y.; Yuan, Q.; Yang, D.; Yang, L.; You, L.; Yu, J. Improved SOI LDMOS performance by using a partial stepped polysilicon layer as the buried layer. *Mate. Sci. Semicond. Process.* **2019**, *90*, 7–12. [CrossRef]
18. Wang, B.; Wang, Z.; Kuo, J.B. A Substrate-Dissipating (SD) Mechanism for a Ruggedness-Improved SOI LDMOS Device. *IEEE J. Electron. Devices Soc.* **2018**, *6*, 739–746. [CrossRef]
19. Lei, J.; Hu, S.; Yang, D.; Huang, Y.; Chen, L.; Guo, J.; Liu, C.; Liu, T.; Wang, Y. Performance analysis of a novel trench SOI LDMOS with centrosymmetric double vertical field plates. *Results Phys.* **2019**, *12*, 810–815. [CrossRef]

20. Wu, L.; Wu, Y.; Zhang, Y.; Lei, B.; Zhu, L.; Huang, Y. High-Voltage Lateral Double-Diffused Metal-Oxide Semiconductor with Double Superjunction. *J. Electron. Mater.* **2019**, *48*, 2456–2462. [CrossRef]
21. Wu, L.; Huang, Y.; Wu, Y.; Zhu, L.; Lei, B. Investigation of the stepped split protection gate L-Trench SOI LDMOS with ultra-low specific on-resistance by simulation. *Mater. Sci. Semicond. Process.* **2019**, *101*, 272–278. [CrossRef]
22. Luo, X.; Udrea, F.; Wang, Y.; Yao, G.; Liu, Y. Partial SOI Power LDMOS With a Variable Low-k Dielectric Buried Layer and a Buried P Layer. *IEEE Electron. Device Lett.* **2010**, *31*, 594–596. [CrossRef]
23. Wang, Z.; Zhang, B.; Fu, Q.; Xie, G.; Li, Z. An L-Shaped Trench SOI-LDMOS With Vertical and Lateral Dielectric Field Enhancement. *IEEE Electron. Dev. Lett.* **2012**, *33*, 703–705. [CrossRef]
24. Wang, Y.; Wang, Z.; Bai, T.; Kuo, J.B. Modeling of Breakdown Voltage for SOI Trench LDMOS Device Based on Conformal Mapping. *IEEE Trans. Electron. Devices* **2018**, *65*, 1056–1062. [CrossRef]
25. Luo, X.; Zhang, B.; Li, Z. New High-Voltage (>1200 V) MOSFET With the Charge Trenches on Partial SOI. *IEEE Trans. Electron. Devices* **2008**, *55*, 1756–1761. [CrossRef]
26. Yang, X.; Li, T.; Cai, Y.; Wang, J.; Chen, C. High voltage (>1100 V) SOI LDMOS with an accumulated charges layer for double enhanced dielectric electric field. *IEICE Electron. Express* **2013**, *10*, 20130057. [CrossRef]
27. Qiao, M.; Wang, Y.; Li, Y.; Zhang, B.; Li, Z. Design of a 1200-V ultra-thin partial SOI LDMOS with n-type buried layer. *Superlattices Microstruct.* **2014**, *75*, 796–805. [CrossRef]
28. Napoli, E. Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. *IEEE Electron. Device Lett.* **2007**, *28*, 753–775. [CrossRef]
29. Napoli, E. Deep Depletion SOI Power Devices. In Proceedings of the 2006 International Semiconductor Conference, Sinaia, Romania, 27–29 September 2006. [CrossRef]
30. Napoli, E.; Udrea, F. Substrate engineering for improved transient breakdown voltage in SOI lateral power MOS. *IEEE Electron. Device Lett.* **2006**, *27*, 678–680. [CrossRef]
31. Yang, X.; Li, T.; Cao, T.; Li, J. Analysis of the Influence of Silicon-on-Insulator Lateral Double-Diffused MOS Device Substrate Deep Depletion on the Transient Breakdown Voltage. *IEEE Access* **2020**, *8*, 151383–151391. [CrossRef]
32. Zingg, R.; Weijland, I.; Zwol, H.; Boos, P.; Lavrijsen, T.; Schoenmakers, T. 850V DMOS-switch in silicon-on insulator with specific Ron 13 $\Omega \cdot mm^2$. In Proceedings of the 2000 IEEE International SOI Conference, Wakefield, MA, USA, 2–5 October 2000. [CrossRef]
33. Sunkavalli, R.; Tamba, A.; Baliga, B. Step drift doping profile for high voltage DI lateral power devices. In Proceedings of the 1995 IEEE International SOI Conference, Tucson, AZ, USA, 3–5 October 1995. [CrossRef]
34. Luo, J.; Cao, G.; Ekkanath Madathil, S.; De Souza, M. A high performance RF LDMOSFET in thin film SOI technology with step drift profile. *Solid State Electron.* **2003**, *47*, 1937–1941. [CrossRef]
35. Zhang, S.; Sin, J.K.; Lai, T.M.; Ko, P.K. Numerical model of linear doping profiles for high-voltage thin-film SOI devices. *IEEE Trans. Electron. Devices* **1999**, *46*, 1036–1041. [CrossRef]