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Simplified Model Predictive Current Control of Four-Level Nested Neutral Point Clamped Converter

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Abstract: Model predictive control (MPC) is an efficient and growing approach to power converter control. This paper proposes an improved and simplified model predictive current control (MPCC) technique for a four-level nested neutral point clamped (4L-NNPC) converter. Conventional MPCC exhibits better performances as compared to the conventional linear control system such as fast dynamic response, consideration of the system constraints, and nonlinearities. However, the application of the conventional model predictive current control (MPCC) approach on complex systems provokes a significant number of calculations, which is the main hurdle to its practical implementation. To fix this flaw, this paper proposes an effective algorithm to shorten the execution time of the conventional MPCC. In this proposed technique, 216 current predictions of the conventional MPCC are skipped and converted into one required voltage vector (RVV) prediction. With this equivalent reference voltage transformation, the calculation burden of MPCC is significantly reduced, while the output performance is not influenced. The results of the simplified MPCC for the 4L-NNPC converter are analyzed and compared with the conventional MPCC. The computational time is reduced by 19.56% using the simplified MPCC, while keeping an approximately similar error of output currents. The switching frequency and total harmonic distortion (THD) of the proposed method are reduced by 8.16% and 0.07%, respectively, as compared to the conventional technique. These results demonstrate the fact that that the performance of a conventional MPCC is enhanced with the proposed MPCC. The proposed algorithm can be applied to several inverter topologies.

Keywords: nested neutral point clamped converter; model predictive current control; total harmonic distortion

Citation: Atif, R.; Hassan, M.; Shahid, M.B.; Munir, H.M.; Saeed, M.S.R.; Shahzad, M.; Isik, S.; Alharbi, M. Simplified Model Predictive Current Control of Four-Level Nested Neutral Point Clamped Converter. *Sustainability* **2023**, *15*, 955. https://doi.org/10.3390/su15020955

Academic Editors: Hassan M. Hussein Farh, Saad Mekhilef, Ahmed Fathy and Abdullrahman Abdullah Al-Shamma'a

Received: 15 November 2022
Revised: 19 December 2022
Accepted: 29 December 2022
Published: 4 January 2023

1. Introduction

Multilevel converters are preferred candidates in high-power conversion applications such as distributed generation systems, microgrids, and motor drives, used to gain the desired voltage and performance in the medium-voltage range [1]. Multilevel converter topologies are the favored choice to achieve the required high levels of power and voltages. In comparison with a two-level voltage source converter (VSC), the primary characteristics of these arrangements are their effectiveness in decreasing the THD of the ac-side signals, switching the stresses of the rate of change of voltage, switching losses, and diminishing or even removing the interface transformer [2–6].

Optimal control carries out good quality and efficiency in power conversion with the high fidelity of power converters. For instance, to handle common-mode voltages, vibration suppression is used in the power converter to reduce power losses as well as current harmonics and enhance the protection of the system [7–11]. Numerous control techniques are used to control the variables of power converters as presented. Of all of these controls, hysteresis and linear controls with PWM are very familiar and easy to implement [12–14]. However, the implantation of modern and more intelligent control methods is feasible with the growth of new fast digital signal processors and microcontrollers. Some modern control techniques are fuzzy logic, sliding mode control, and model predictive control (MPC).

1.1. Motivation and Incitement

Optimal control can be easily employed with the help of MPC for numerous objectives. It has a good attraction in the control system because of its characteristics such as essential decoupling, rapid dynamic response, reactive power compensation, and the easy addition of constraints [15–30]. The finite control-set model predictive control (FCS-MPC) has grown quickly in the last decade, covering many fields, such as UPS, renewable energy systems, electric grids, multi-level converters, electric drives, etc. [31–35].

1.2. Literature Review and Research Gaps

Nevertheless, there exists a hurdle in the actual implementation of MPC: a smaller interval of control loop time to attain the same performance as conventional control methods [36,37]. Consequently, the permitted time to accomplish the calculations is reduced in such a way that it is impossible to implement conventional MPC on low-speed processors. Furthermore, the volume of calculations will rise with the complexity of the technique, the inclusion of constraints, and the neutral point balancing. To address this problem, different approaches are analyzed to reduce the complexity of the MPC technique [38–40].

A conventional MPCC technique of the 4L-NNPC converter is discussed in which the optimum switching state is selected in each control loop cycle [41,42]. For this purpose, 216 current predictions are required for each phase. Due to this calculation burden problem, the MPCC technique becomes impractical in the case of a low-speed processor. On the other hand, the cost of the control technique increases if a high-speed processor is used. In short, the time-consuming calculation burden is the main issue in the practical implementation of the conventional MPCC. So, complexity reduction and simplifying the algorithm approaches to solve the computational time issue are better options than conventional MPCC if the performance of the system is not disturbed.

1.3. Contribution and Paper Organization

The main contribution and novelty of this paper is to shorten the control loop cycle time of the conventional MPCC technique for practical implementation and cost reduction. This is achieved by the following steps:

- Analyze the mathematical model, control set, and the performance of 4L-NNPC converters.
- This analysis is used for developing an algorithm, called simplified MPCC, which converts 216 current predictions calculations of the conventional MPCC of 4L-NNPC into one required voltage vector (RVV) calculation for each phase.
- After implementation of this algorithm, the calculation burden is significantly reduced (216×3 to 1×3 calculations) and the performance of the system is not disturbed.
- Consequently, this simplified MPCC technique is much better than the conventional MPCC method, and it contributes to obtaining low-cost and high-performance 4L-NNPC for high-power medium voltage applications.

The rest of the paper consists of five sections. In Section 2, a mathematical model of the 4L-NNPC converter is discussed. The conventional MPCC technique for 4L-NNPC is reviewed in Section 3. The proposed simplified MPCC technique is described in Section 4.

In Section 5, both conventional and simplified techniques are implemented and compared. The conclusion of the paper is given in Section 6.

2. Four-Level Nested Neutral Point Clamped (4-L NNPC) Converter

4L-NNPC Converter [42], as given in Figure 1, is explained for medium-voltage high-power applications. It has a DC voltage source and three legs for three phases; each leg consists of six switches, two diodes, and two flying capacitors. In contrast to the classic four-level converter topologies, the suggested 4L-NNPC converter topology has a smaller number of elements.

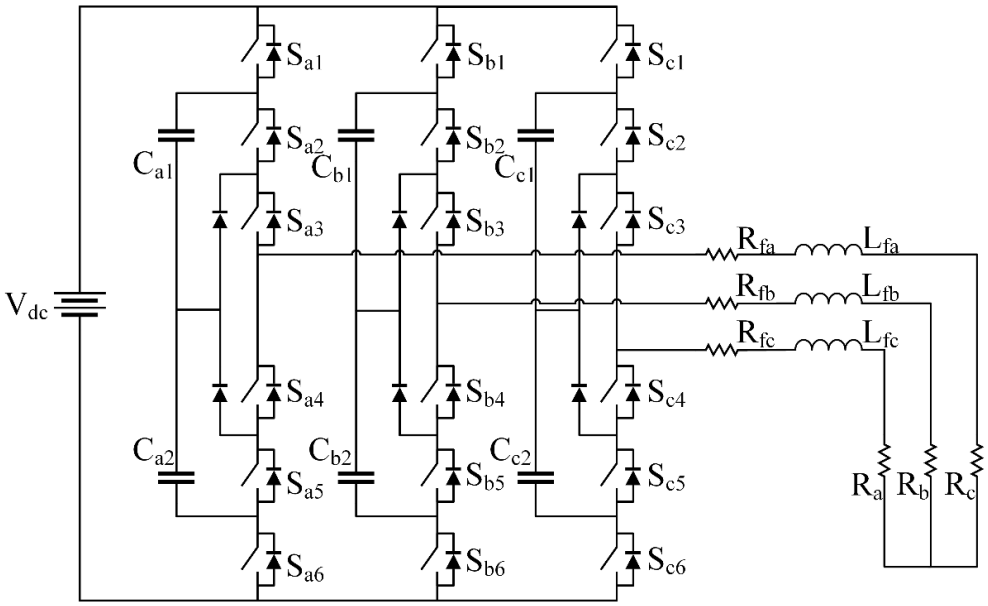

Figure 1. Four-Level Nested Neutral Point Clamped Converter.

It is designed by combining FC and NPC converters, which generate four-level voltages at the output. The capacitors $Cx1$ and $Cx2$, $x = a, b, c$ are charged to $1/3V_{dc}$ to guarantee equally spaced voltage levels. From all 64 possible switching combinations, as 6^2 for six switches in one leg, only six switching states, as shown in Table 1, are chosen to produce four levels of voltage. In this converter, all switches are identically stressed as $1/3V_{dc}$. The redundancy in switch combinations is another benefit of the proposed converter to create higher levels. For instance, there are two extra switching combinations to create voltage levels of $1/3V_{dc}$ and $2/3V_{dc}$.

Table 1. Switching states of the 4L-NNPC with FC and output voltages.

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{Cx1}	V_{Cx2}	V_x
D	1	1	1	0	0	0	No Impact	No Impact	V_{dc}
C2	1	0	1	1	0	0	Charging (ix > 0) Discharging (ix < 0)	No Impact	$\frac{2V_{dc}}{3}$
C1	0	1	1	0	0	1	Discharging (ix > 0) Charging (ix < 0)	Discharging (ix > 0) Charging (ix < 0)	$\frac{2V_{dc}}{3}$
B2	1	0	0	1	1	0	Charging (ix > 0) Discharging (ix < 0)	Charging (ix > 0) Discharging (ix < 0)	$\frac{V_{dc}}{3}$
B1	0	0	1	1	0	1	No Impact	Discharging (ix > 0) Charging (ix < 0)	$\frac{V_{dc}}{3}$
A	0	0	0	1	1	1	No Impact	No Impact	0

2.1. Mathematical Modeling of 4L-NNPC Converter

The mathematical model can be driven by considering the DC supply voltage, switching states, and terminal voltages of any phase. Mostly for simplicity, the upper switches of the converter are considered in the mathematical modeling of the converter. The terminal of the 4L-NNPC converter related to the negative DC bus is represented in terms of a relationship of DC link voltages, FCs voltages, and upper three switching signals as follows [42]:

$$V_{xN} = S_{x1}V_{dc} + (S_{x2} - 1)v_{cx1} + (S_{x3} - 1)v_{cx2} + (1 - S_{x1})(v_{cx1} + v_{cx2}) \quad (1)$$

where v_{cx1} and v_{cx2} are FC voltages and $x = a, b, c$.

2.2. Predictive Model of Load Current

The phase voltages of the 4L-NNPC converter can be driven using Kirchhoff's voltage law as follows:

$$v_{xN} = \left(R_{fx} + R_x\right)i_{ox} + L_{fx}\frac{di_{ox}}{dt} + v_{nN} \quad (2)$$

R_{fx}, $R_{x,}$ and L_{fx} are the filter resistance, output resistance, and filter inductance, respectively. The voltage of the neutral point of load relating to the negative DC bus can be represented as follows:

$$v_{nN} = \frac{1}{3}\sum_{x=a,b,c} v_{xN} \quad (3)$$

The voltages of each phase with respect to the load neutral point can be defined as follows:

$$v_{kn} = v_{kN} - v_{nN} \quad (4)$$

For the MPCC algorithm, the discrete-time model should be derived from the continuous-time Equation (2) that can be implemented on the digital microprocessor. By using the backward Euler method, the first-order derivative gives a better approximation to obtain the discrete-time model. This is represented as follows [42]:

$$\frac{d\mathbf{i_o}}{dt} = \frac{\mathbf{i_o}(n) - \mathbf{i_o}(n-1)}{T_s} \quad (5)$$

where T_s represents the sampling time. By putting Equation (5) into Equation (2) the discrete-time predictive model can be obtained.

$$\mathbf{i_o}(n) = C_v\mathbf{v_o}(n) + C_i\mathbf{i_o}(n-1) \quad (6)$$

where C_v and C_i are constants and defined as:

$$C_v = \frac{T_s}{L_f + \left(R_f + R\right)T_s}, \qquad C_i = \frac{L_f}{L_f + \left(R_f + R\right)T_s} \quad (7)$$

By shifting one future sample in Equation (6), the predicted output current is given as follows:

$$\mathbf{i_o}(n+1) = C_v\mathbf{v_o}(n+1) + C_i\mathbf{i_o}(n) \quad (8)$$

According to Equation (8), the predicted output current $\mathbf{i_o}(n+1)$ depends on the present value of the measured load current $\mathbf{i_o}(n)$ and the predicted output voltage $\mathbf{v_o}(n+1)$ of the inverter. The calculation of the predicted output voltage using Equation (1), required 216 (6^3) switching states, the measured DC link voltage, and the measured FC voltages.

2.3. Predictive Model of FC Voltages

The FC voltages should be maintained at the level of ⅓ Vdc to assure uniformly stepped voltages at the output for reduction of voltage stress of the semiconductor device. A mathematical model of the flying capacitors' voltage is given below [42]:

$$\begin{aligned} v_{Cx1}(t) &= v_{Cx1}(0) + \int_{0+}^{t} i_{Cx1}(t)dt \\ v_{Cx2}(t) &= v_{Cx2}(0) + \int_{0+}^{t} i_{Cx2}(t)dt \end{aligned} \tag{9}$$

The capacitor currents i_{Cx1} and i_{Cx2} can be calculated as follows:

$$\begin{aligned} i_{Cx1} &= (S_{x1} - S_{x2})i_{ox} \\ i_{Cx2} &= (S_{x5} - S_{x6})i_{ox} \end{aligned} \tag{10}$$

To obtain a discrete-time model, Equations (9) and (10) can be driven as:

$$\begin{aligned} i_{Cx1}(n) &= (S_{x1} - S_{x2})i_{ox}(n) \\ i_{Cx2}(n) &= (S_{x5} - S_{x6})i_{ox}(n) \end{aligned} \tag{11}$$

$$\begin{aligned} v_{Cx1}(n+1) &= v_{Cx1}(n) + \tfrac{T_s}{C_{x1}} i_{Cx1}(n) \\ v_{Cx2}(n+1) &= v_{Cx2}(n) + \tfrac{T_s}{C_{x2}} i_{Cx2}(n) \end{aligned} \tag{12}$$

3. Conventional MPCC of 4L-NNPC

A block diagram of the conventional MPCC of the 4L-NNPC converter is shown in Figure 2. There are two main objectives in this method: output current control and FC voltage regulation. For the current control objective, 216 voltage vectors (VVs) are calculated for all possible switching states of the inverter. After that, 216 output currents are predicted using all obtained VVs. The 216 predicted currents are provided to the cost function block for current optimization. For FC voltage regulation, 216 FC voltages are predicted for all possible switching states on the inverter. These predicted FC voltages are provided to the cost function block for optimization. After optimization of output currents and FC voltages, an appropriate switching sequence is applied to the 4L-NNPC inverter.

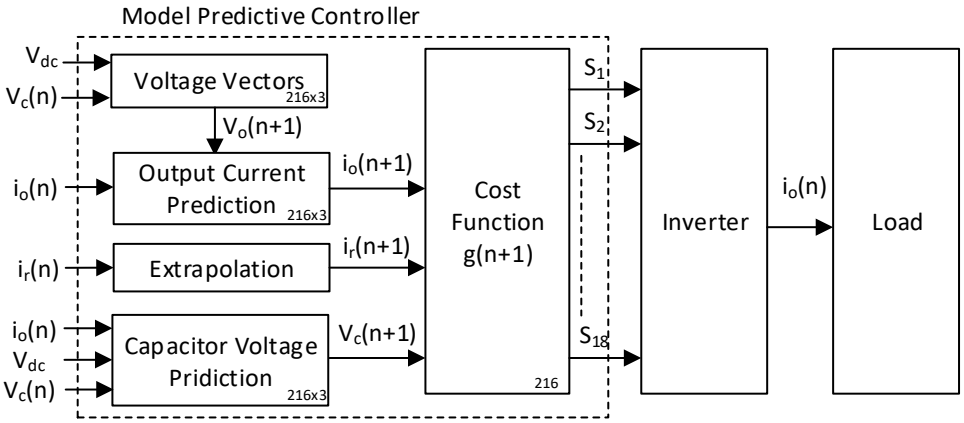

Figure 2. Conventional MPCC for 4L-NNPC Converter.

The flow chart of the conventional MPCC technique for the 4L-NNPC converter is given in Figure 3a. First of all, the measured value of DC link voltage and load currents are needed at the nth instant. User-defined reference currents are taken for the purpose of ease. In the next step, 216 VVs are calculated using Equation (1) for all possible switching states on the inverter. After that, 216 output currents are predicted using Equation (8) for all possible VVs. Similarly, 216 predicted FC voltages are obtained using Equation (12).

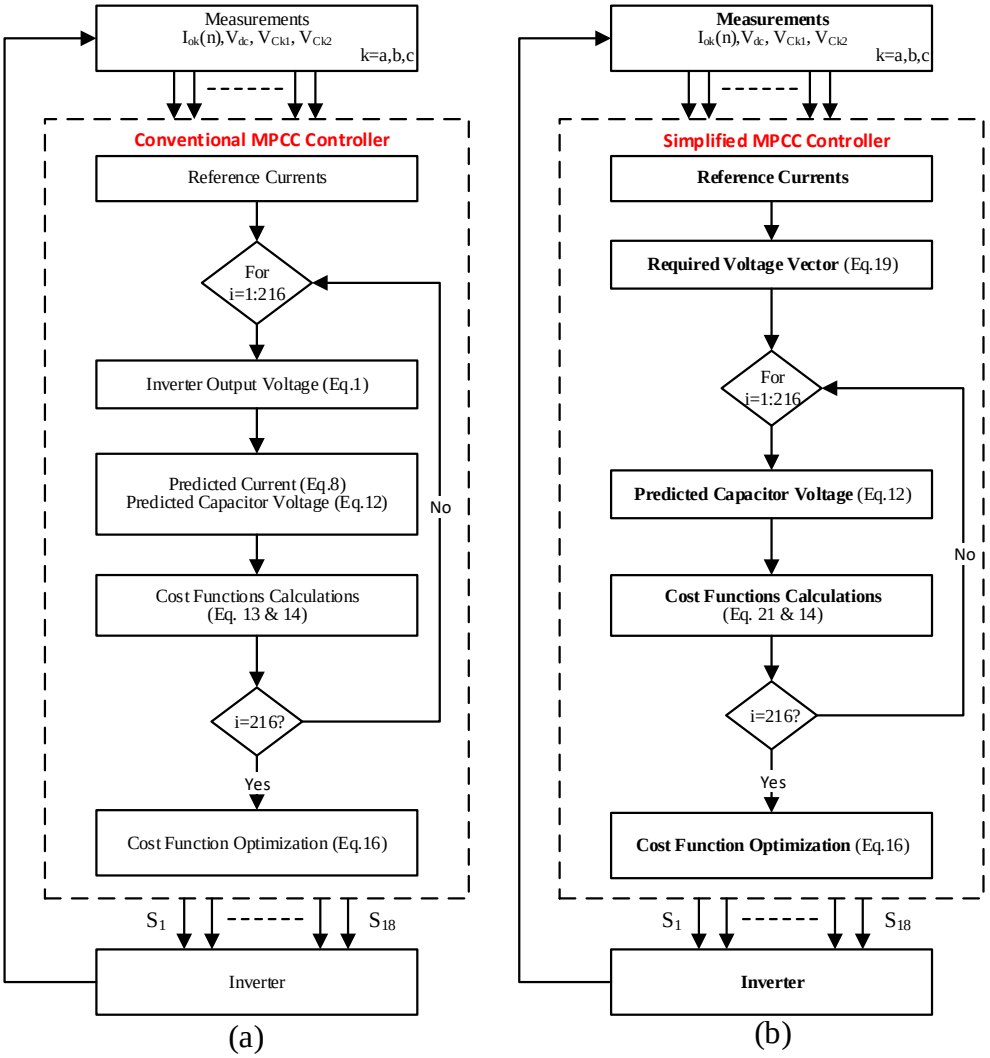

Figure 3. Flow Chart for 4L-NNPC current control, (**a**) Conventional MPCC, (**b**) Simplified MPCC.

After that, two control goals are defined in major cost function g, elimination of error in load current using the sub-cost function g_1 and regulation of FC voltages using the sub-cost function g_2 as follows [42]:

$$g_1(n+1) = \sum_{x=a,b,c} [i^*_{rx}(n+1) - i_{ox}(n+1)]^2 \tag{13}$$

$$g_2(n+1) = \lambda_c \sum_{x=a,b,c} \left\{ \sum_{i=1}^{2} [v^*_{cr} - v^*_{cxi}(n+1)]^2 \right\} \tag{14}$$

where v^*_{cx} is the reference voltages of the flying capacitor and λ_c is the weighting factor which is defined as follows [42]:

$$v^*_{cr} = \frac{1}{3} V_{dc}, \qquad \lambda_c = \frac{i_{o,n}}{v^*_{cx}} \tag{15}$$

where $i_{o,n}$ is the rated value of converter output current. The major cost function can be described in this fashion by bringing together the above two sub-cost functions g_1 and g_2:

$$g(n+1) = g_1(n+1) + g_2(n+1) \tag{16}$$

The fundamental theme of the optimization process is to obtain a cost function near zero. The predicted reference current is compared with 216 predicted load currents. And the reference FC voltage is compared with 216 predicted values of FC voltages. The switching state that belongs to the smallest value of the cost function is chosen for the subsequent interval.

Finally, the conventional MPCC of the 4L-NNPC converter can be summarized by the following mathematical expressions:

$$\begin{cases} \mathbf{i_{o,m}}(n+1) = C_v \mathbf{v_{o,m}}(n+1) + C_i \mathbf{i_o}(n) \\ g_{1,m}(n+1) = \sum\limits_{x=a,b,c} [i^*_{rx}(n+1) - i_{ox,m}(n+1)]^2 \\ g_{2,m}(n+1) = \lambda_c \sum\limits_{x=a,b,c} \left\{ \sum\limits_{i=1}^{2} [v^*_{cr} - v_{cxi,m}(n+1)]^2 \right\} \\ g_m(n+1) = g_{1,m}(n+1) + g_{2,m}(n+1) \\ state : \min g_m(n+1) \\ m = 1, 2, 3, \ldots 216 \end{cases} \tag{17}$$

4. Simplified MPCC of the 4L-NNPC Converter

The block diagram of the simplified MPCC, as shown in Figure 4, is a modified form of the MPCC algorithm used to reduce the calculation burden on the digital microprocessor for real-time implementation. In this technique, only one required voltage vector (RVV) is predicted for the optimization process instead of 216 current predictions per phase. Consequently, the suggested RVV technique simplifies the control process.

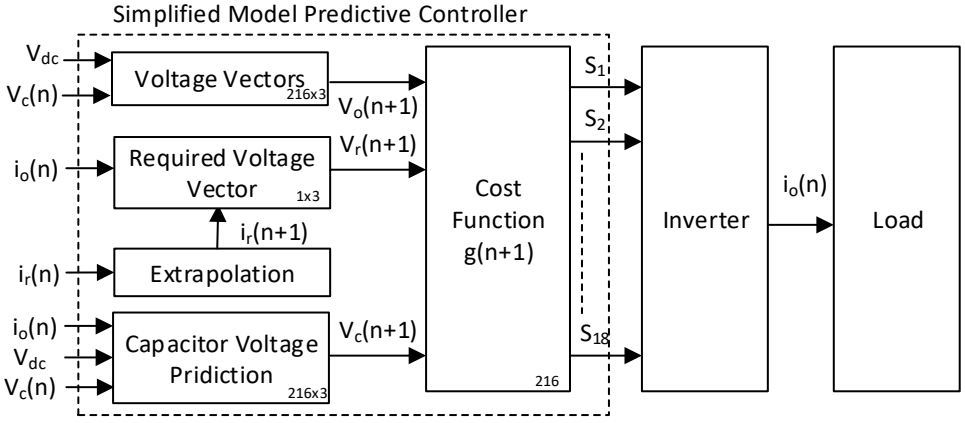

Figure 4. Simplified MPCC for 4L-NNPC Converter.

The main theme of the conventional MPCC of the 4L-NNPC converter is to choose a suitable VV from 216 output VVs using Equation (8) for the next interval that corresponds to the nearly zero error between the predicted output current and the reference output current. For this purpose, all 216 VVs are analyzed for current prediction and the 216 predicted currents are compared in sub-cost function g_1. After cost function optimization, a suitable voltage vector is selected for the next interval.

In the simplified MPCC technique, a required voltage vector (RVV) is obtained that corresponds to the exactly zero output current tracking error. After that, this RVV is compared with all VVs using the sub-cost function, and a suitable voltage vector is chosen for the next interval. In this method, 216 current predictions are eliminated because the suitable voltage vector is directly obtained using RVV.

The required voltage vector can be derived by replacing the predicted output current $\mathbf{i_o}(n+1)$ with the predicted reference $\mathbf{i^*_o}(n+1)$ in Equation (8), which shows that the predicted current is taken exactly equal to the reference current for zero current tracking error.

$$\mathbf{i^*_o}(n+1) = C_v \mathbf{v^*_o}(n+1) + C_i \mathbf{i_o}(n) \tag{18}$$

Rearranging the Equation (19).

$$\mathbf{v}_{\mathbf{o}}^{*}(n+1) = \frac{1}{C_v}[\mathbf{i}_{\mathbf{o}}^{*}(n+1) - C_i \mathbf{i}_{\mathbf{o}}(n)] \tag{19}$$

According to Equation (19), the output current of the converter will be identical to its reference current if the output voltage of the converter is managed to be the same as RVV $\mathbf{v}_{\mathbf{o}}^{*}(n+1)$.

Implementation of the simplified MPCC technique is described using the flow chart given in Figure 3b. According to this flow chart, the first step of the simplified MPCC will be to measure the value of DC link voltages and load currents. The reference signal values for load currents are produced according to the application of the 4L-NNPC converter. Reference currents are user-defined for generality. So, the given technique can be implemented for further application by modifying the reference values.

The reference currents should be predicted to future state because the cost function performs the calculation in an (n + 1)th instant. In case of a very small sampling time, such as $T_s < 20$ µs, there is no need for a reference currents prediction and $\mathbf{i}_{\mathbf{o}}^{*}(n)$ is taken equal to the $\mathbf{i}_{\mathbf{o}}^{*}(n+1)$. When the sampling time is large, such as $T_s > 20$ µs, the given fourth-order Lagrange extrapolation can be used for a reference currents prediction:

$$\mathbf{i}_{\mathbf{o}}^{*}(n+1) = 4\mathbf{i}_{\mathbf{o}}^{*}(n) - 6\mathbf{i}_{\mathbf{o}}^{*}(n-1) + 4\mathbf{i}_{\mathbf{o}}^{*}(n-2) - \mathbf{i}_{\mathbf{o}}^{*}(n-3) \tag{20}$$

In the next step, 216 predicted output currents per phase are eliminated due to one proposed RVV per phase. The RVV can be achieved using Equation (19).

Two control goals are defined in cost function g: the elimination of error in load current, and the regulation of FC voltages. The primary purpose is to diminish the error among predicted load current and reference current, which can be achieved using the sub-cost function g_1 as defined below:

$$g_1(n+1) = \sum_{x=a,b,c} [v_{ox}^{*}(n+1) - v_{ox}(n+1)]^2 \tag{21}$$

According to the sub-cost function g_1, 216 possible VVs are compared with the one proposed RVV. Consequently, 216 errors are generated from the cost function g_1.

The secondary control goal is defined in the sub -cost function g_2: to adjust the FC voltages at a constant level of one-third of DC link voltages. Sub-cost function g_2 is defined in Equation (14). The major cost function can be described in this fashion by bringing together the above two sub-cost functions g_1 and g_2 as given in Equation (16).

The fundamental theme of the optimization process is to obtain a cost function near zero. The RVV is compared with 216 predicted converter voltage vectors in each sampling interval. Similarly, the reference FC voltage is compared with 216 predicted values of FC voltages. The switching state that belongs to the smallest value of the cost function is chosen for the subsequent interval. Finally, the simplified MPCC of the 4L-NNPC converter can be summarized by the following mathematical expressions.

$$\begin{aligned}\{\blacksquare(\mathbf{v\_o}\hat{}*\ (n+1) \quad &= 1/C\_v[\mathbf{i\_o}\hat{}*\ (n+1) - C\_i\ \mathbf{i\_o}\ (n)]@g\_(1,m)\ (n+1) = \textstyle\sum\_(x \\ &= a,b,c)\blacktriangledown[v\_ox\hat{}*\ (n+1) - v\_(\mathrm{o}x,\mathrm{m})\ (n+1)]\hat{}2\ @g\_(2,m)\ (n+1) = \lambda\_c\ \textstyle\sum\_(x \\ &= a,b,c)\blacktriangledown\{\textstyle\sum\_(i=1)\hat{}2\blacktriangledown[v\_cr\hat{}*-v\_(cxi,m)\ (n+1)]\hat{}2\ \}\ @g\_m\ (n+1) \\ &= g\_(1,m)\ (n+1) + g\_(2,m)\ (n+1)@state : \min\llbracket g\_m\ (n+1)\rrbracket@m = 1,2,3,\ldots\ 216) \dashv\end{aligned} \tag{22}$$

It can be observed that 216 calculations of current prediction for each phase are reduced to just one calculation for obtaining the RVV. Consequently, the calculation burden of the microprocessor is significantly reduced.

5. Simulation Results and Discussion

To investigate the simplified and conventional schemes for the 4L-NNPC converter, simulations are performed using MATLAB Simulink. The 4L-NNPC converter parameters and the MPCC parameters are listed in Tables 2 and 3, respectively. The simulation results are analyzed for output voltages, load currents, and regulation of FC voltages. The robustness analysis of simplified and conventional techniques with DC link voltage variations are also discussed.

Table 2. 4L-NNPC converter parameter.

Converter Parameters	Values
Converter rating	5 MVA
Input DC voltage	12.5 KV
Rated current	400 A
Output voltages	7.2 KV
Flying capacitors®	1000 μF
Output frequency (f)	50 Hz
Output inductor (L)	15 mH
Output load®	10 Ω

Table 3. 4L-NNPC converter parameter.

MPCC Parameters	Values
Sampling time	20 μs
Prediction horizon	1
Weighting factor	0.096

5.1. Steady-State Analysis

Figure 5 displays the simulation results of both techniques for the steady-state condition with balanced reference currents and balanced loads for $T_s = 20$ μs, reference currents ($i_{ra} = i_{rb} = i_{rc} = 320$ A) at 50 Hz, and balanced loads ($R_a = R_a = R_a = 10\ \Omega$). It shows that output load currents follow their references with minimum error for both controllers. Output currents and reference currents are compared for percentage error. A very low percentage error of 0.35% is seen in the case of the simplified MPCC technique as compared to 0.86% for the conventional MPCC technique. In the case of steady-state current conditions, simulation time for 5000 samples is analyzed. Computational time is reduced to 1.85 s in the case of the simplified MPCC technique as compared to 2.3 s in that of the conventional MPCC technique. Consequently, calculation time is reduced by 19.56% in the case of a simplified MPCC algorithm as compared to the conventional algorithm. The average switching frequency is calculated at 1237 Hz in the case of the conventional MPCC technique and 1136 Hz in the case of the simplified MPCC technique, which indicates a 8.16% reduction in switching frequency. Total harmonic distortion (THD) in load current is analyzed in a steady-state condition. THD is reduced to 0.29% in the case of the simplified MPCC technique as compared to 0.36% in that of the conventional MPCC technique. The comparison of the proposed and the conventional MPCC technique is given in Table 4 for better understanding. The results shows that the proposed simplified MPCC technique is better than the conventional MPCC technique in all respects.

Table 4. Comparison of conventional and simplified MPCC techniques for steady-state reference currents.

Controller	Time(s)	Error (%)	Frequency (Hz)	THD (%)
Conventional MPCC	2.3	0.86	1237	0.36
Simplified MPCC	1.85↓	0.35↓	1136↓	0.29↓

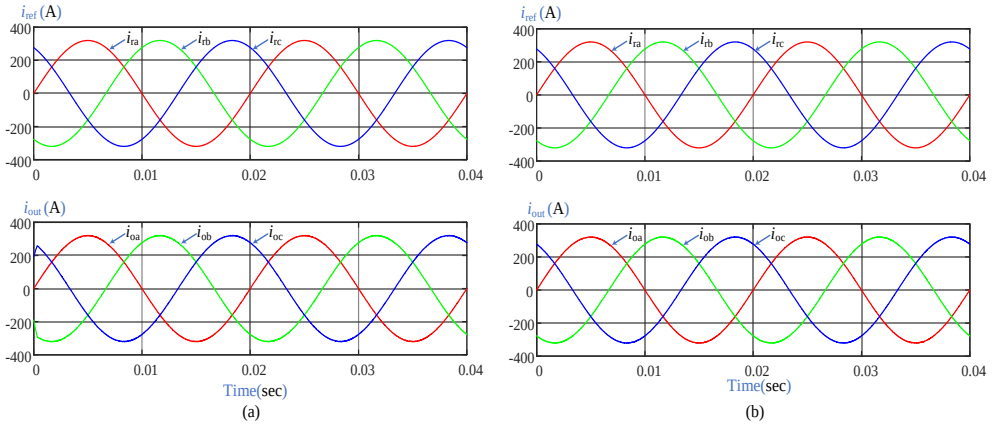

Figure 5. Reference and output currents for steady-state condition; (**a**) Conventional MPCC, (**b**) Simplified MPCC.

Figure 6 displays the FC voltages in the case of steady-state references of load currents. It can be observed from the simulation result that FCs voltages are regulated at the level of $1/3$ of V_{dc} for both controllers. Output phase voltages Vao, phase to phase voltages Vab, and phase to neutral point voltages Van are shown in Figure 7 in steady-state conditions.

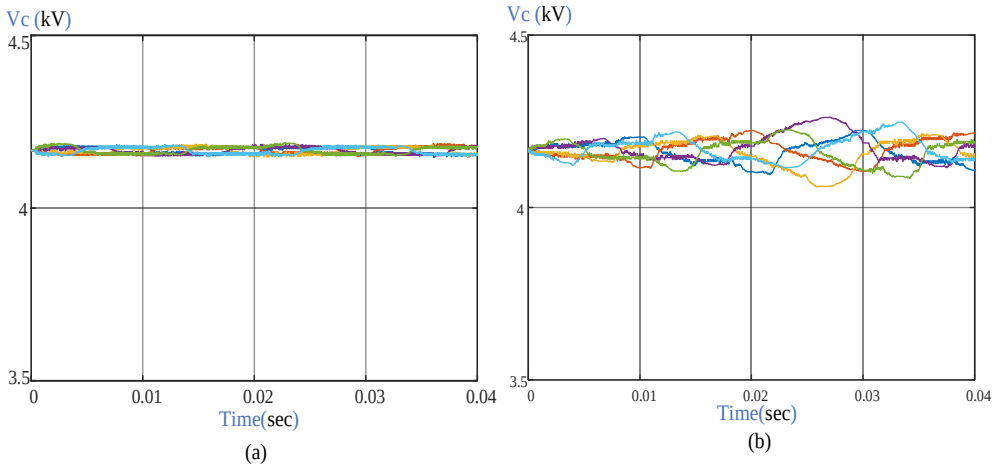

Figure 6. FC voltages for steady-state condition; (**a**) Conventional MPCC, (**b**) Simplified MPCC.

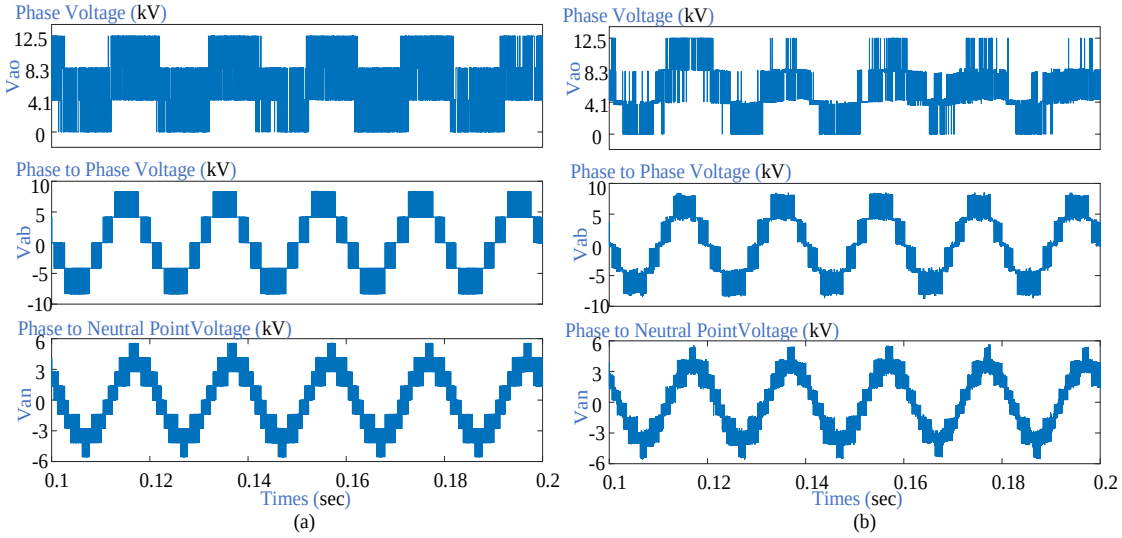

Figure 7. Output voltages of the 4L-NNPC converter; (**a**) Conventional MPCC, (**b**) Simplified MPCC.

5.2. Transient-State Analysis

5.2.1. Balance Reference Step Change

The transient-state analysis is carried out using step change in the reference current from 320 A to 160 A at 50 Hz with balanced loads ($R_a = R_a = R_a = 10\ \Omega$) and sampling time $T_s = 20$ µs. The step change in signal is applied during the interval of $t = 0.12$ s to 0.15 s. Simulation results of load currents and FC voltages are shown in Figure 8 for both controllers. It can be observed that output load currents follow their references well during step change and FCs voltages are also regulated to an acceptable range during transitions. Further analysis is described in Section 5.4.

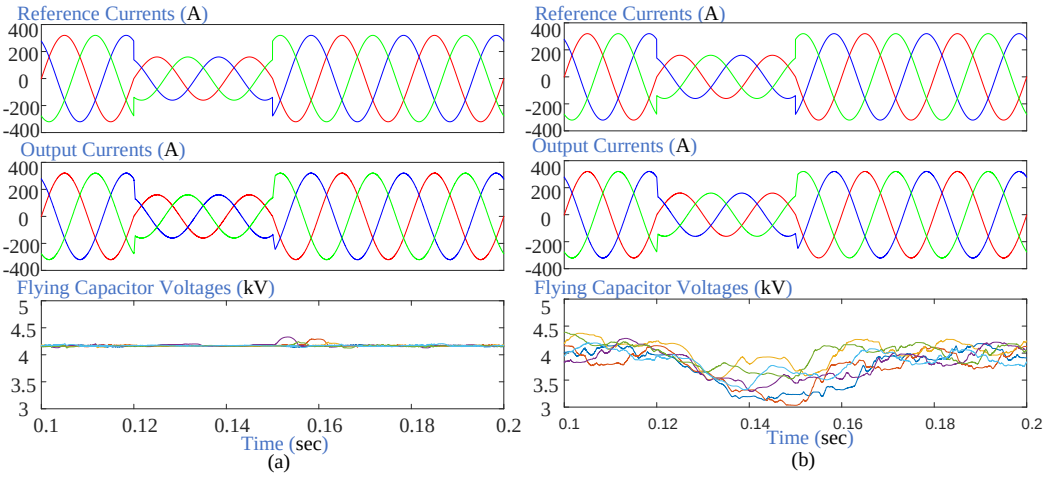

Figure 8. Transient analysis; a step change in reference current; (**a**) Conventional MPCC, (**b**) Simplified MPCC.

5.2.2. Balanced Reference Falling Ramp Change

The transient-state analysis is also carried out using falling ramp change in the reference current from 320 A to 0 A at 50 Hz with balanced loads ($R_a = R_a = R_a = 10\ \Omega$) and sampling time $T_s = 20$ µs. Falling ramp change in reference signals is applied during the interval of $t = 0.12$ to 0.15 s. The simulation result of load currents and FCs voltages during the transition state is given in Figure 9. It shows that output load currents keep tracking their references at an acceptable level, while falling ramp change and FCs voltages are also regulated to an acceptable range during the transition period for both controllers. Further analysis is described in Section 5.4.

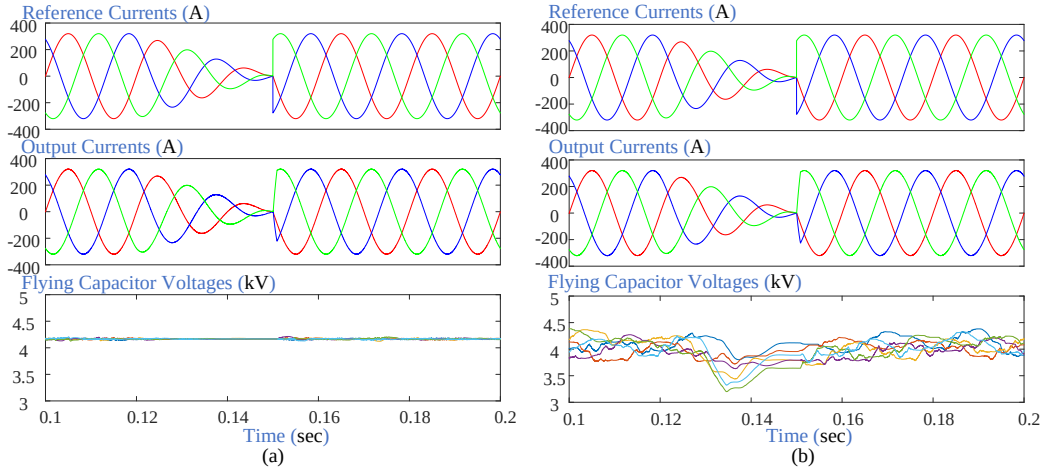

Figure 9. Transient analysis; ramp change in reference current; (**a**) Conventional MPCC, (**b**) Simplified MPCC.

5.3. Robustness Analysis with DC Link Voltage Variations

The robustness of the MPCC technique is analyzed with ramp and step variation in DC bus voltage.

5.3.1. Ramp Change in DC Link Voltage

Ramp alteration in DC link voltage is analyzed for the following parameters: DC link falling ramp change from 12.5 kV to 11 kV, balanced reference currents (320 A at 50 Hz), balanced loads ($R_a = R_a = R_a = 10\ \Omega$), and sampling time $T_s = 20\ \mu s$. Falling ramp change in DC link voltages is applied during the interval of $t = 0.01$ to 0.03 s. Simulation results of load currents, DC link voltages, and FCs voltages during the transition state are is given in Figure 10 for both controllers. It can be seen that load current keeps tracking its references at an acceptable level while falling ramp change in DC link voltages and FCs voltages are also regulated to an acceptable range during the transition period. Further analysis is described in Section 5.4.

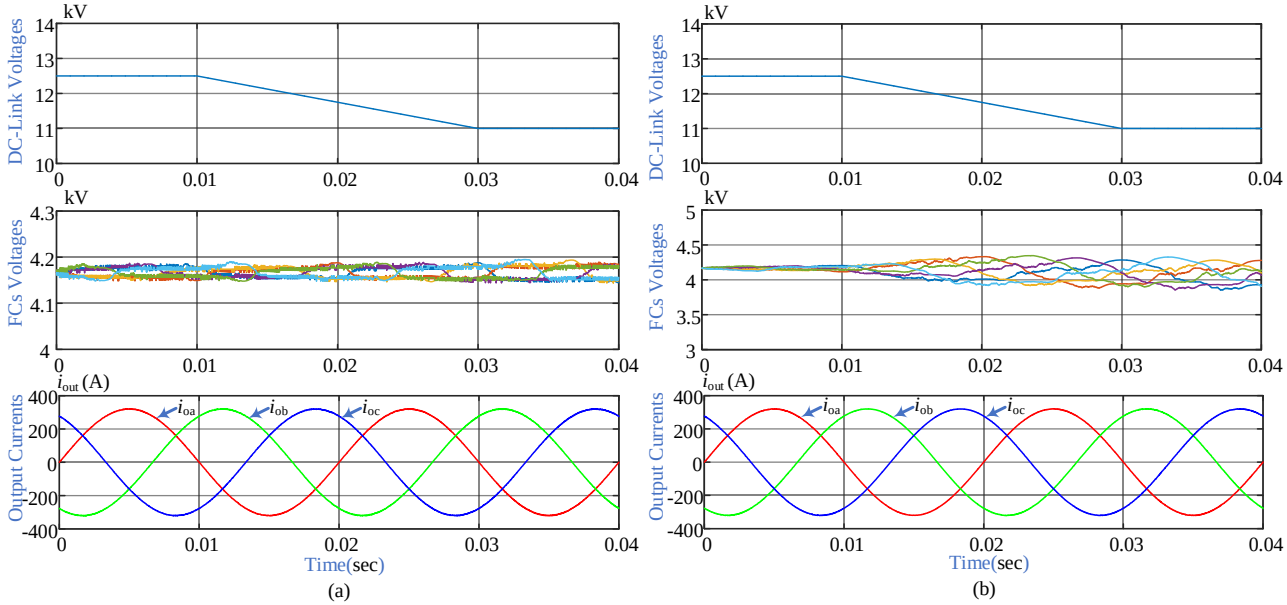

Figure 10. Robustness analysis; ramp change in DC link voltage; (**a**) Conventional MPCC, (**b**) Simplified MPCC.

5.3.2. Step Change in DC Link Voltage

Step alteration in DC link voltage is analyzed using these parameters: DC link step changes 12.5 KV to 11 KV from time 0.01 to 0.02 s, 11 kV to 12 kV from time 0.02 to 0.03 s and 12.5 KV from $t > 0.03$, balanced reference currents 320 A at 50 Hz, balanced loads ($R_a = R_a = R_a = 10\ \Omega$), and sampling time $T_s = 20\ \mu s$. Simulation results of load currents, DC link voltages, and FCs voltages during the transition state are given in Figure 11 for both controllers. It can be seen that load current keeps tracking its references at an acceptable level while step change in DC Link voltages and FCs voltages are also regulated to an acceptable range during the transition period.

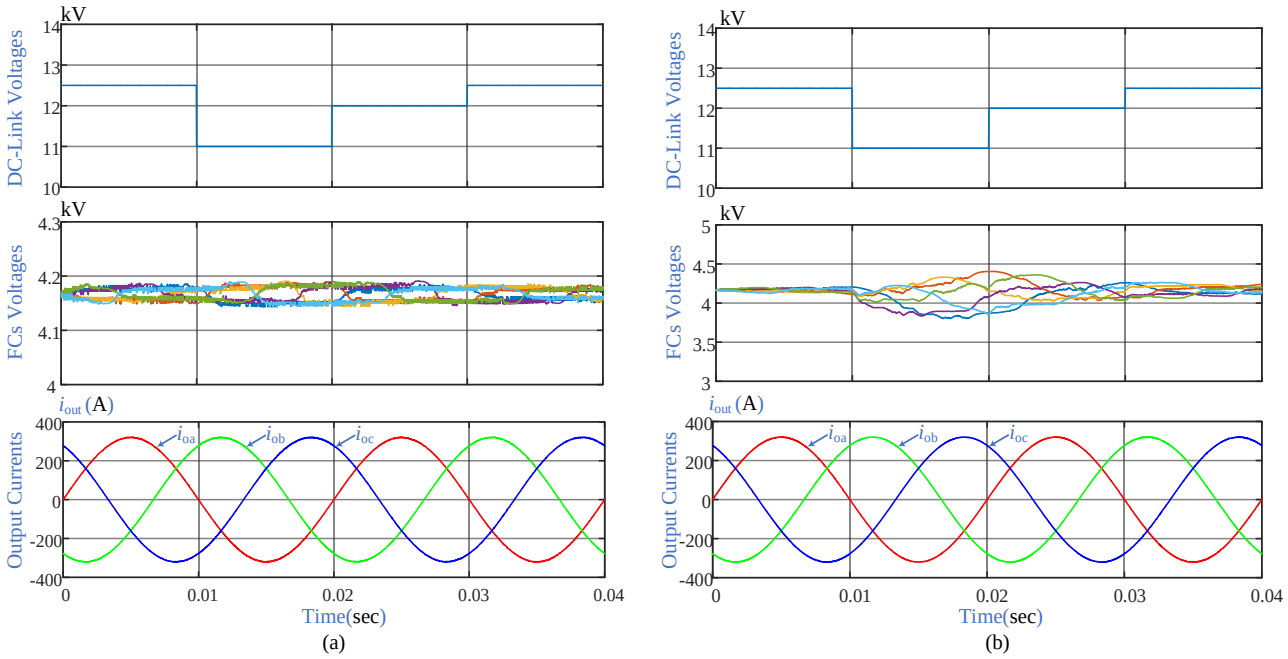

Figure 11. Robustness analysis; step change in DC link voltage; (**a**) Conventional MPCC, (**b**) Simplified MPCC.

5.4. Comparative Analysis

To verify the effectiveness of the proposed MPCC technique, a comparative analysis for different conditions of the reference current and DC link voltages has been done. In the bar chart, different operating conditions mentioned in Table 5 are given along the *x*-axis as follows: A represents steady-state reference current, B represents reference current step change, C represents reference current falling ramp, D represents reference current rising ramp, E represents DC link voltage step change, F represents DC link voltage falling ramp, and G represents DC link voltage rising ramp. All of the comparative analyses are carried out for 5000 sampling instants.

Table 5. Operating conditions for 4L-NNPC converter.

x-Axis Variables	Description
A	Steady-state reference current
B	Reference current step change
C	Reference current falling ramp
D	Reference current rising ramp
E	DC link voltage step change
F	DC link voltage falling ramp
G	DC link voltage rising ramp

Figure 12 shows the computational time comparison between the conventional and simplified MPCC for all operating conditions. MATLAB function is used to measure the computational time of both controllers. The bar chart shows that computational time is reduced in the simplified MPCC technique as compared to the conventional MPCC in all operating conditions. Computational time is reduced to a maximum of 20% in case C (reference current falling ramp change) and a minimum of 17.3% in case E (DC link voltage step change).

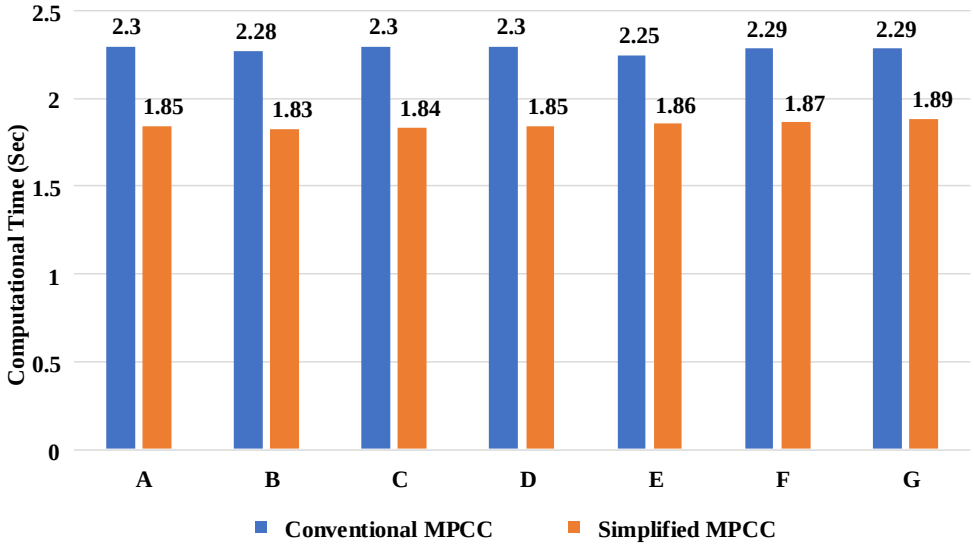

Figure 12. Comparison of computational time for different conditions.

Figure 13 represents a comparative analysis of the conventional and simplified MPCC with respect to the percentage error between the reference current and the output current. The bar chart demonstrates that percentage errors are reduced in the simplified MPCC technique as compared to the conventional MPCC in all operating conditions, which proves the effectiveness of the proposed technique. The percentage error of the current is reduced the most in case A (steady-state reference current), from 0.86% to 0.35%, which shows the 59.3% decrease with respect to the conventional MPCC percentage error. On the other hand, the percentage error of the current is reduced the least in case C (reference current ramp change), from 0.91% to 0.55%, which shows the 39.5% decrease with respect to the conventional MPCC percentage error.

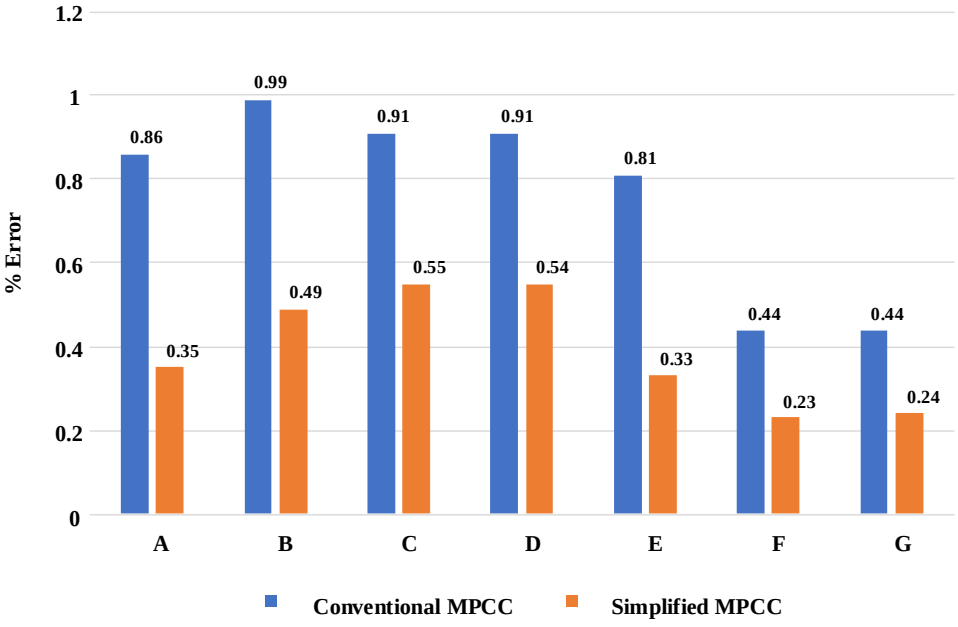

Figure 13. Comparison of current % error for different conditions.

Comparative analysis of the average switching frequency for the conventional and simplified MPCC is expressed in Figure 14. All operating conditions, as mentioned in Table 5, are compared for both the conventional and simplified MPCC techniques. The results show that the average switching frequency is reduced in all operating conditions

for the simplified MPCC technique. The average switching frequency is reduced the most in case F (DC link ramp change), from 1130 to 880 Hz, which shows a 22.1% decrease with respect to the conventional MPCC technique. On the other hand, the average switching frequency of the simplified MPCC is reduced the least in case B (reference current step change), from 1131 to 1132 Hz, which shows the 8.04% decrease with respect to the conventional MPCC technique.

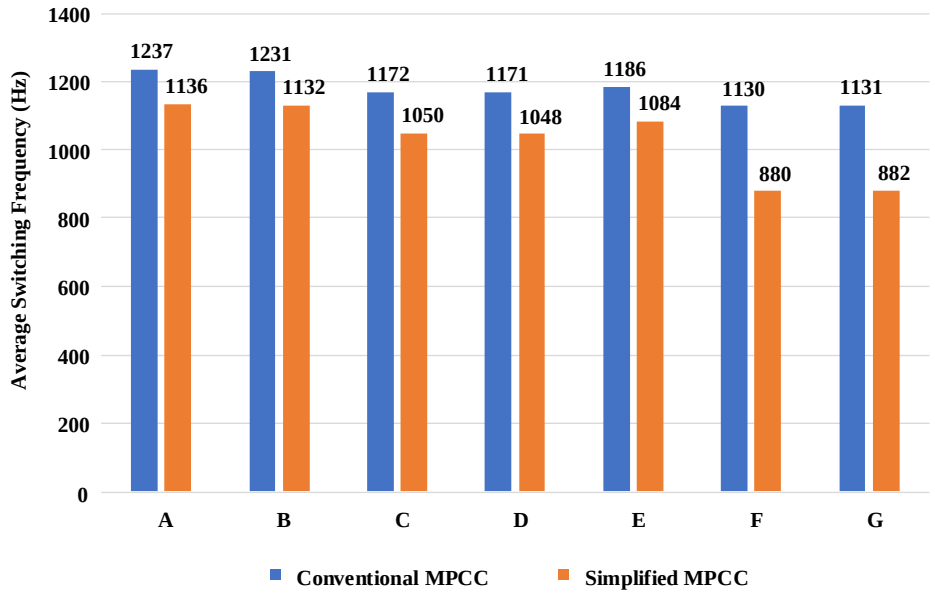

Figure 14. Comparison of average switching frequency for different conditions.

6. Conclusions

An improved and simplified MPCC technique is applied to the 4L-NNPC converter to diminish the calculation burden of the microprocessor caused by the heavy calculations of the conventional MPCC. In this proposed technique, 216 current predictions of the conventional method are converted into one required voltage vector (RVV) prediction for each phase. Consequently, the computational time of the proposed MPCC is reduced due to the reduction of calculations from 216 × 3 to 1 × 3. The results show the computational time of the conventional MPCC is reduced by 19.56% using the proposed MPCC, while keeping a good tracking of output current with respect to the reference current. The switching frequency and THD of the proposed method are reduced by 8.16% and 0.07%, respectively, as compared to the conventional MPCC technique. These results demonstrate that the performance of the simplified MPCC is improved as compared to the conventional MPCC. These results verify that the simplified MPCC algorithm can be employed with low-price processors. Furthermore, the proposed simplified technique is also valid for other converters.

Author Contributions: Conceptualization, R.A.; data curation, M.H.; formal analysis, H.M.M.; funding acquisition, M.A. and S.I.; investigation, M.A. and M.S.; methodology, M.S.R.S.; project administration, H.M.M. and M.A.; supervision, M.H.; validation, M.B.S.; writing—original draft, R.A.; writing—review & editing, H.M.M. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: This work was supported by the Researchers Supporting Project number (RSP2023R467), King Saud University, Riyadh, Saudi Arabia.

Conflicts of Interest: The authors declare no conflict of interest.

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