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Review

A Review of Multilevel Inverter Topologies for Grid-Connected Sustainable Solar Photovoltaic Systems

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Abstract: Solar energy is one of the most suggested sustainable energy sources due to its availability in nature, developments in power electronics, and global environmental concerns. A solar photovoltaic system is one example of a grid-connected application using multilevel inverters (MLIs). In grid-connected PV systems, the inverter's design must be carefully considered to improve efficiency. The switched capacitor (SC) MLI is an appealing inverter over its alternatives for a variety of applications due to its inductor-less or transformer-less operation, enhanced voltage output, improved voltage regulation inside the capacitor itself, low cost, reduced circuit components, small size, and less electromagnetic interference. The reduced component counts are required to enhance efficiency, to increase power density, and to minimize device stress. This review presents a thorough analysis of MLIs and a classification of the existing MLI topologies, along with their merits and demerits. It also provides a detailed survey of reduced switch count multilevel inverter (RSC-MLI) topologies, including their designs, typical features, limitations, and criteria for selection. This paper also covers the survey of SC-MLI topologies with a qualitative assessment to aid in the direction of future research. Finally, this review will help engineers and researchers by providing a detailed look at the total number of power semiconductor switches, DC sources, passive elements, total standing voltage, reliability analysis, applications, challenges, and recommendations.

Keywords: Renewable Energy Sources (RESs); Photovoltaic (PV) systems; Switched Capacitor (SC); Reduced Switch Count Multilevel Inverter (RSC-MLI); Common Ground Switched-Capacitor (CGSC); Reliability

Citation: Nyamathulla, S.; Chittathuru, D. A Review of Multilevel Inverter Topologies for Grid-Connected Sustainable Solar Photovoltaic Systems. *Sustainability* **2023**, *15*, 13376. https://doi.org/10.3390/su151813376

Academic Editor: Mohamed A. Mohamed

Received: 26 July 2023
Revised: 22 August 2023
Accepted: 29 August 2023
Published: 6 September 2023

1. Introduction

Recently, there has been a remarkable rise in the use of grid-supplied power. This can be attributed to an increased number of users and the expansion of high-power sectors. Traditional power production has led to a significant surge in global emissions, thereby causing detrimental effects on the environment. Significant progress has been made in integrating renewable energy sources such as solar and wind into the grid. Welcome to the world of photovoltaic (PV) systems, which have become the top choice for harnessing energy thanks to their incredible potential. In fact, worldwide, grid-connected solar PV capacity has soared to over 635 GW, satisfying approximately 2% of the global energy consumption [1].

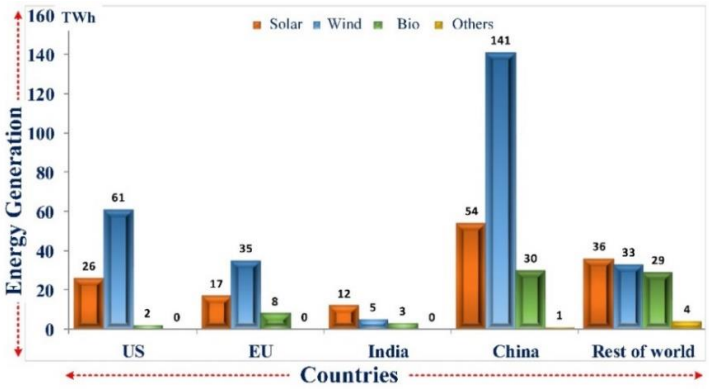
Solar energy is a rapidly growing field, and one crucial aspect that has gained significant importance is power electronics. Researchers are actively engaged in the pursuit of developing highly efficient power electronic converters to enhance the overall performance of solar energy systems. In applications requiring medium and high power, MLIs are increasingly being employed. This is because MLIs provide several inherent advantages over two-level inverters, as mentioned in Table 1.

Table 1. Comparison between two-level and multilevel inverters (MLIs).

Parameter	Two-Level Inverter	MLI
Function at a fundamental frequency	Fails	Operate
Operate at high voltage and current	Operate	Operate
Fault-tolerant operation	Impossible	Possible
Harmonic content	Low	High
Stress on power electronic switches	More	Less
Switching losses	High	Low
Power quality performance	Low	High
Voltage variation rate	High	Low
Generation of voltage in common mode	Higher	Lower
Generation of variable voltage	Not possible	Possible
Capability of functioning without a transformer	No	Yes
Efficiency	Low	High
Input current distortions	High	Low
Voltage applications	Low	High
Structure	Complicated	Modular
Electromagnetic interference	High	Low

It has been predicted that renewable energy would contribute 29% of worldwide power output in 2020, up from 27% in 2019, that renewable energy generation would increase by more than 8% to 8300 TWh by 2021, and that solar PV and wind would account for two-thirds of the growth in renewable energy. The increase in renewable energy alone in China in 2021 was about half of what was predicted, followed by the United States, the European Union, and India, as shown in Figure 1a. China has continued to be the largest PV market, although there is growth in the United States due to continuous federal and state legislative support. In India, new solar PV capacity additions have recovered quickly from COVID-19-related delays in 2021. According to the IEA's 2021 Renewable Energy Market Update, by 2020, renewable energy was the only type of energy whose consumption increased despite the pandemic. To increase worldwide renewable power in 2021 and 2022, the renewable energy sector has looked at new additions. In addition, 270 GW went online in 2021 and 280 GW went online in 2022, continuing the remarkable level of renewable energy additions that are anticipated. This expansion has exceeded the yearly capacity rise record set in 2017–2019 by more than 50%, indicating that renewables have been responsible for 90% of the increase in global capacity in 2021 and 2022, as shown in Figure 1b.

Flexible alternating current transmission systems (FACTSs), customized power devices (CPDs), variable-speed drives (VSDs), active front-end converters (AFCs), and renewable energy sources for power generation are just a few of the many uses for MLIs [2–5]. MLIs can be classified as classical if they use the most common topologies, such as the diode-clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI), and cascaded H-bridge (CHB) multilevel inverter, mentioned in Figure 1c. There has been a lot of interest in these topologies, but their practical implementation is highly impacted by the application, the system that is designed, and costs. The fundamental disadvantage of a DCMLI is its asymmetrical loss distribution. This, in turn, results in an irregular distribution of junction temperature, which, in turn, results in constraints on the inverter's power, current, and switching frequency at maximum junction temperature [6,7].



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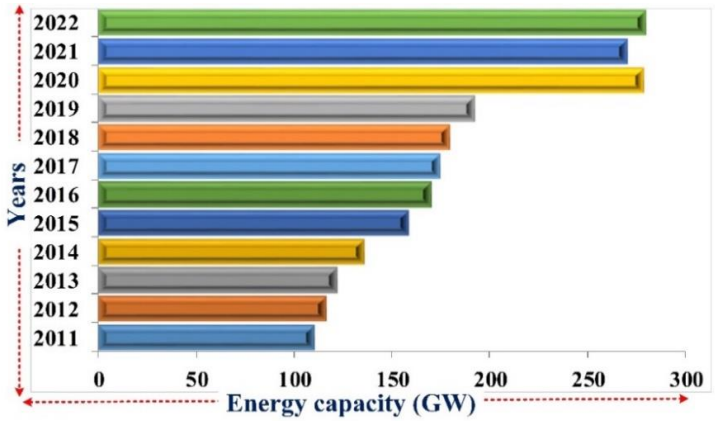

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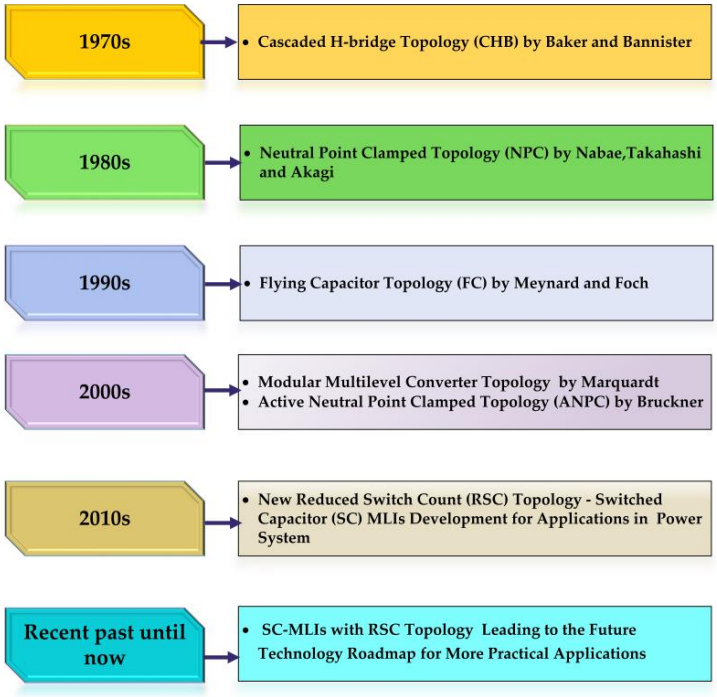


(**c**)

Figure 1. (**a**) Worldwide renewable power generation in 2020–2021; (**b**) net renewable capacity additions, by renewable energy market update 2021—IEA; (**c**) an outlook on the development of various MLI topologies.

Traditional MLIs, on the other hand, need a larger number of components to achieve the same number of output levels, have issues with capacitor voltage balance, and cannot increase their voltages [8]. Different reduced device count MLIs have been presented to address traditional MLIs' high component count [9–14]; however, these MLIs have lacked a voltage-boosting function. To eliminate capacitor voltage imbalance in typical MLIs, complicated control algorithms or multi-output boost converters have been implemented. These methods increase an inverter's weight, complexity, and expense. SC-MLIs minimize the drawbacks of traditional and reduced device count MLIs [15–22].

Researchers have continued to investigate and to develop additional topologies by implementing little or major modifications to conventional MLIs. As a result, MLIs with a lower device count have been developed, and this subset of MLIs has been dubbed RSC-MLIs, which have recently been the subject of many reviews. Newly designed RSC-MLIs for integrating renewable energy sources and driving applications are addressed in [23–25]. The incorporation of switched-capacitor (SC)-based circuits is one of the most widely used methods for designing better MLIs, and rapid progress has been made in the area of SC-MLI development since 2010. Pure SC-based switching circuits use a series–parallel switching conversion technique to take the available fixed DC-link voltage and produce a multilevel voltage using a reduced number of capacitors, power switches, and/or diodes. SC-MLIs are a valuable and interesting solution for many new applications due to the voltage step-up feature they offer, which includes self-voltage balancing for the involved capacitors, which is the result of a single-stage switching operation that eliminates the need for inductors and transformers [26–35]. The following is a list of the primary factors and propensities for SC-MLIs:

1. Maximizing the number of output voltage levels while minimizing the number of semiconductor devices needed.
2. Increasing the overall output voltage gain with single or multiple DC-source configurations.
3. Reducing or controlling the current stress/loss profile of switches with soft charging or pulse-width modulation (PWM)-based techniques for better power density and to improve efficiency.

A wide range of new issues, design requirements, and real-world constraints of conventional MLIs have been highlighted in recent articles [36–45]. Different circuit designs are used to build MLIs using the SC concept. These include single, multiple, mid-point-clamped, and common-grounded (CG)-based DC-source structures [46–55]. Hybrid topological designs that integrate well-known integrated methods such as flying capacitor (FC) and switched boost (SB) technologies into the SC framework significantly raise their performance [56–82].

The significant contributions of this review include:

(1) A complete literature overview and a rigorous analysis of about 200 recently published papers regarding the development, classification, and use of MLI topologies;
(2) A thorough analysis of MLIs and a classification of the existing MLI topologies, along with their merits and demerits.
(3) A detailed survey of reduced switch count multilevel inverter (RSC-MLI) topologies, including their designs, typical features, limitations, and criteria for selection.
(4) A critical analysis and classification of the existing SC-MLI topologies with a qualitative assessment of the merits and downsides of SC-MLIs with well-known applications, and a future roadmap is explored.
(5) An effective summary of multilevel inverters, highlighting the necessity for new or modified multilevel inverters for grid-connected sustainable solar PV systems.
(6) Finally, this review study should help engineers and researchers by providing a detailed look at the total number of power semiconductor switches, DC sources, passive elements, total standing voltage, reliability analysis, applications, challenges, and recommendations.

This review paper includes the following: Section 2 describes grid-connected solar PV systems and MLI background including MLI applications; different types of energy sources integrated with MLI-based systems, motivational factors for generating an RSC-MLI, and assessment parameters are discussed in great length. Section 3 presents the detailed MLI categorization and description of the structure and working principle of features for each reported RSC-MLI topology, and a variety of SC-MLIs with single or multiple DC-source, mid-point-clamped, and CGSC configurations are examined and then compared on several criteria, including the total number of power semiconductor switches, DC sources, passive elements, total standing voltage, efficiencies relative to the number of levels, and the structural motivations behind each concept. Section 4 provides a reliability assessment study to estimate the lifespan of an MLI. Section 5 provides the present challenges and recommendations. Finally, Section 6 concludes the article with some final thoughts.

2. Grid-Connected Solar Photovoltaic System

Massive worldwide energy demand has led to significant usage of fossil fuels, which has affected the environment by increasing greenhouse gas emissions. So, renewable energy resources have gained popularity and growth through producing clean electricity [83–87].

PV cells are used in solar-based technologies to transform the sun's energy into usable power. Figure 2 describes the operation of photovoltaic cells, converters, inverters, and energy control units that make up a system for converting solar energy. Nevertheless, efforts are being made to better understand how to incorporate renewable energy sources into the electricity grid. There has been an increased focus on power converters and their controls because of the importance of their work in transforming electricity and controlling the output power. DC–DC converters are typically used in the initial stage of integrating renewable energy sources into a DC grid. Due to the output voltage variations of renewable energy sources such as wind and solar PVs, this stage must operate at peak efficiency. Hence, it is imperative that the DC–DC converters in the front-end stages exhibit responsive behavior towards such fluctuations in order to operate at their optimal efficiency [88–97]. In small-scale industrial or utility applications, these inverters are frequently employed because of their elevated voltage stress, poor efficiency, elevated operating temperature, and increased pressure capabilities. Multiple inverters are commonly utilized in large-scale, high-power, grid-connected renewable energy systems due to their advantageous characteristics [98–102].

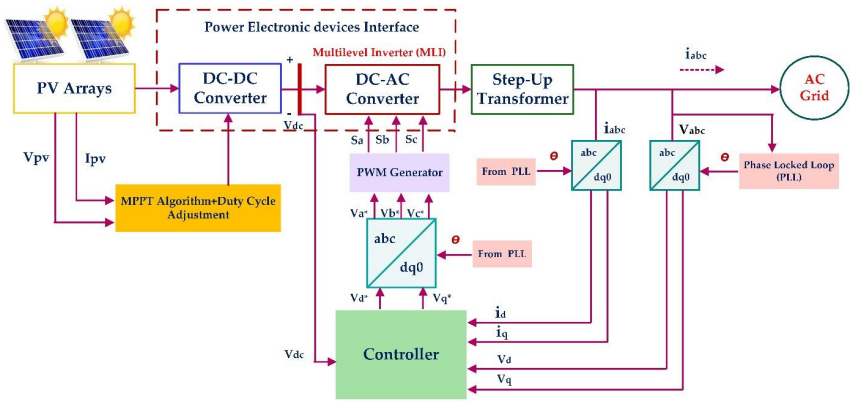


Figure 2. Grid-connected multilevel inverter for solar PV application [103].

An MLI is selected for medium- and high-power applications based on its capability to generate voltage waveforms of superior quality while functioning at a low switching frequency [104–108]. Figure 3 indicates how multilevel inverters have a wide variety of uses in the emerging field of renewable energy, and Figure 4 exhibits the MLI-based system integration of various renewable energy sources being employed and discussed [109–113].

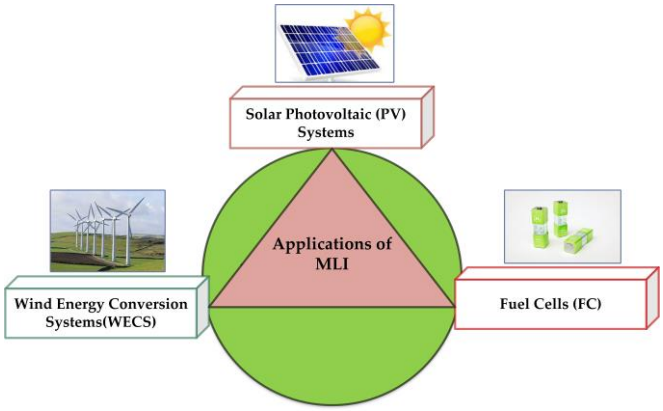


Figure 3. Multilevel inverters have a wide variety of uses in the emerging field of renewable energy.

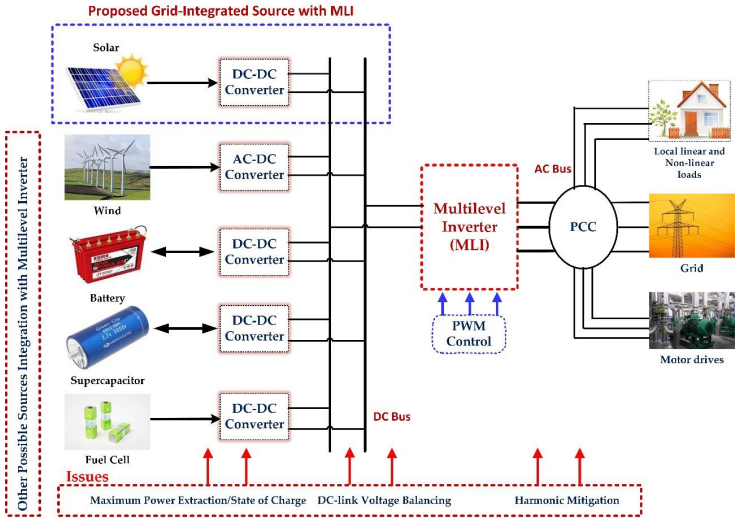


Figure 4. MLI-based system integration of various renewable energy sources [103].

A. Reduced Switch Count Multilevel Inverters (RSC-MLIs): Background

In order to overcome the size and complexity limitations of conventional MLIs, RSC-MLIs have been developed. However, their structural and operational features are affected by changes in their topological arrangement.

(i) Factors Contributing to Motivation

Researchers often consider the following qualities while building a novel RSC-MLI architecture, as shown in Figure 5. The most salient features are enumerated below.

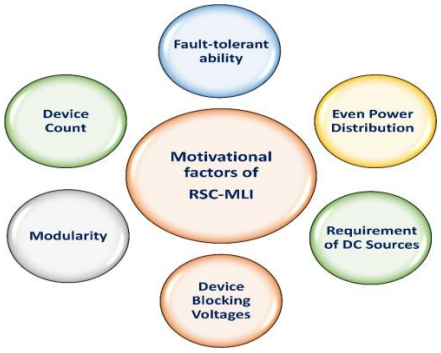


Figure 5. Factors contributing to the motivation for an RSC-MLI.

(ii) Classification

In any physical design, switches and DC-link voltages can be connected in any topology. Often, there is no required architecture, but other times there are ladders, staircases, columns, U-shaped structures, and cascade structures. As can be seen in Figure 6, the resulting RSC-MLIs can be categorized in accordance with their topological and functional properties, as discussed in [114–116].

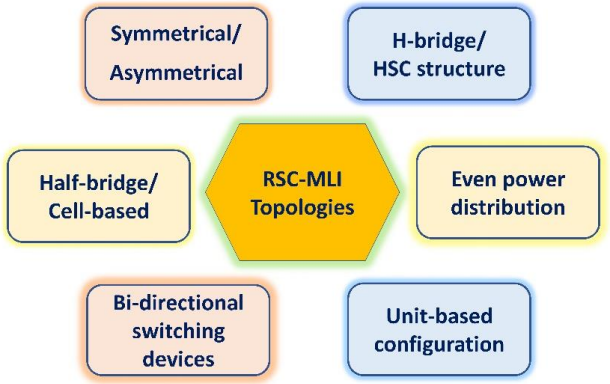


Figure 6. Classification of RSC-MLI topologies.

(iii) The Evaluation Criteria for an MLI

In contrast, this review study takes into consideration broad criteria for rating the proposed topologies:

Several MLI evaluation parameters are context dependent, as shown in Figures 7 and 8, and some of the key features of an MLI that contribute to the different capabilities of the power system are discussed [117–121].

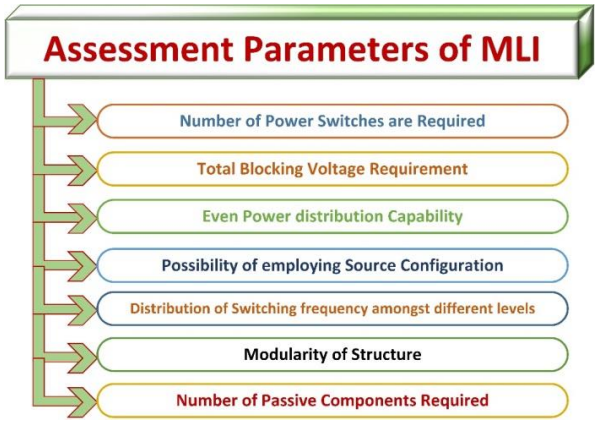


Figure 7. MLI evaluation criteria [103].

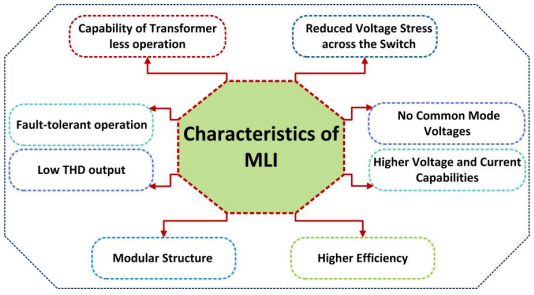


Figure 8. Characteristics of MLIs.

An interconnected multilevel converter system can use renewable energy sources, including solar PV, wind energy, and fuel cells. Their operation, effectiveness, improved power quality, and applications are mostly determined by the control scheme used in the MLI-PWM. Multiple MLI topologies have been suggested in recent years [122–125]. Based on the number of DC sources in their topology, MLIs have been classified as shown in Figure 9, and based on a categorization of the reduced switch in their topology, MLIs have been classified as shown in Figure 10. The NPC-MLI or DC-MLI, FC-MLI, and CHB-MLI are the most prevalent industrial topologies [126–130].

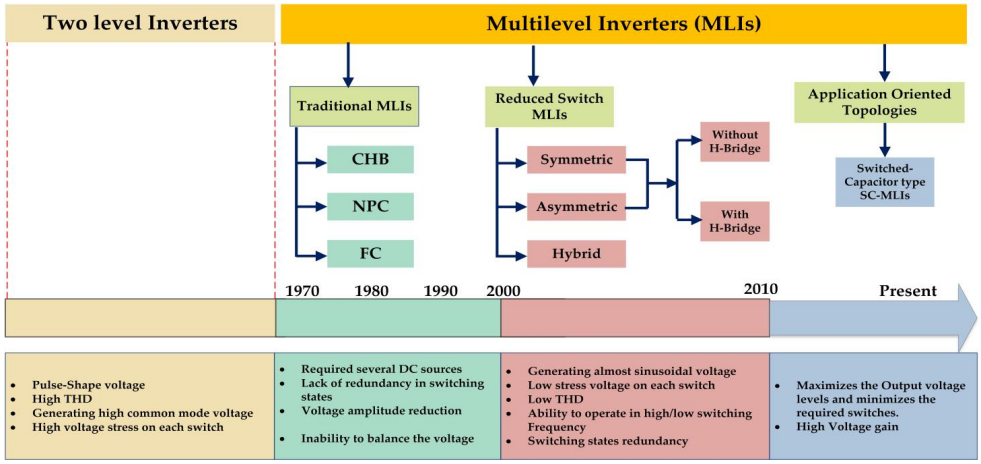


Figure 9. Simplified classification of multilevel inverters.

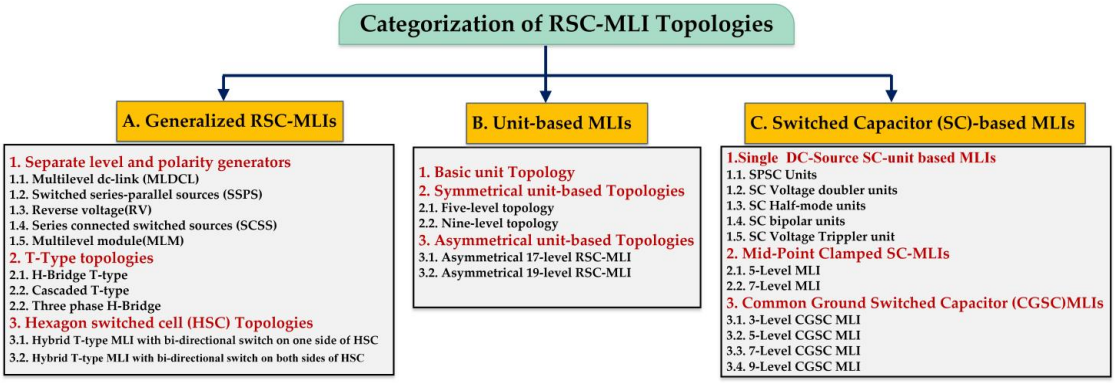


Figure 10. Categorization of reduced switch count MLI topologies.

- Cascaded H-bridge multilevel inverter (CHB-MLI): This topology, which was initially patented by Baker and Bannister [1,39], was thought to be a good alternative to previously reported topologies since it required fewer power components. The series connection of H-bridges with independent DC sources makes up the topology known as the CHB-MLI. Many series-connected H-bridge constructions combine to produce the multilevel stepped waveform. A generic H-bridge cell can be cascaded to create the CHB-MLI that theoretically has an infinite number of layers. Due to its modular design, it effectively corrects the voltage imbalance that can be seen in NPC and FC settings. A CHB typically consists of power conversion cells connected in series on the AC side and individually powered by an isolated DC source from a battery, ultra-capacitor, or fuel cell on the DC side.
- Diode-clamped multilevel inverter (DC-MLI): Nabae, Takashi, and Akagi proposed the diode-clamped multilevel inverter (DC-MLI), also known as the NPC-MLI, in 1981 [73]. The widespread adoption of these inverters can be attributed to their tremendous competency in high-power and medium-voltage operations as well as their relatively high efficiency.

- Flying capacitor multilevel inverter (FC-MLI): Meynard and Foch [25,39] suggested the FC-MLI topology in 1992 to address the issue of static and dynamic sharing of the voltage between semiconductor switches as implemented in the NPC-MLI architecture.

3. Reduced Switch Count Multilevel Inverters (RSC-MLIs) Topologies

A. Generalized RSC-MLI Topologies

Generalized RSC-MLI topologies can be further divided into subcategories depending on the similarity of their structures and the switching devices used. The categorization is as follows:

(1) Separate Level and Polarity Generator Topologies

Each phase-voltage level has its own independent polarity and level generators, which results in an unusually high number of levels. Popular combinations include the MLDCL, SSPS, RV, SCSS, and MLM topologies, according to [2]. Figure 11 depicts the per-phase architecture of these three-source arrangements. An isolated DC supply is used in each basic unit, which uses bidirectional switches to generate levels in the MLM topology. It is important to note that MLDCL and SSPS topologies need identical device-blocking voltages. Adding a new basic unit to an RV, SCSS, or MLM topology increases voltage stress. As a result, the total DC-link voltage is equal to the blocking voltage of each device. Except for the SCSS and MLM topologies, all of these topologies offer symmetric and asymmetric configurations.

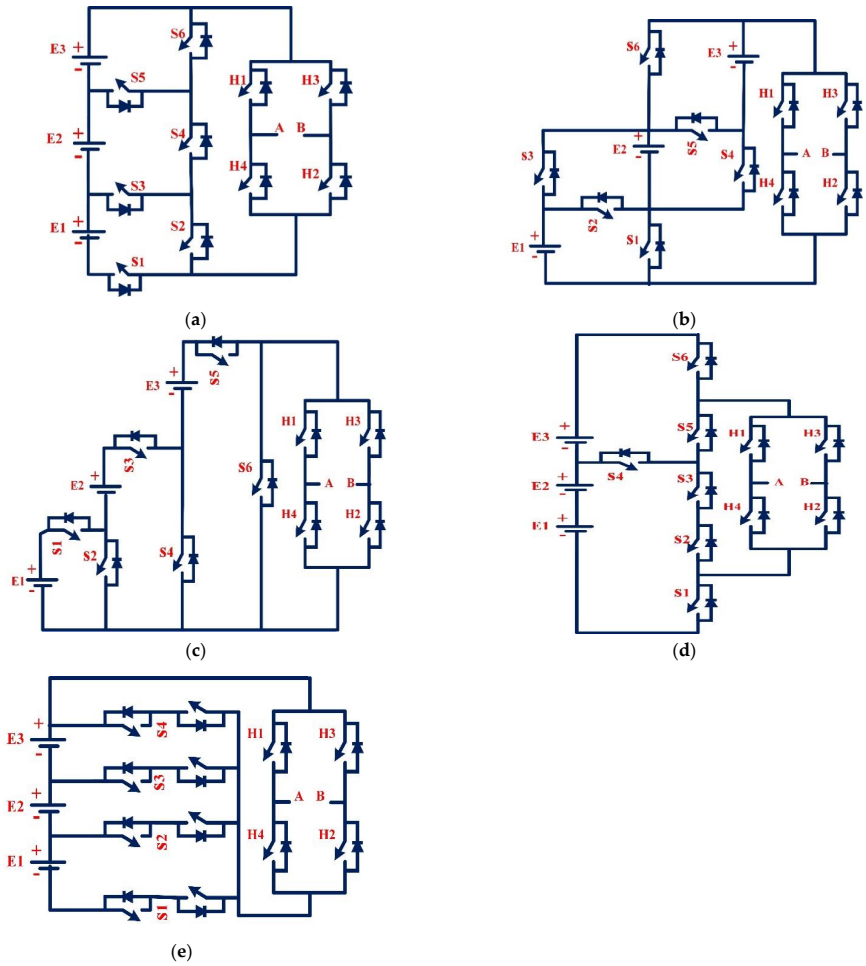


Figure 11. Separate level and polarity generator topologies: (**a**) MLDCL; (**b**) SSPS; (**c**) SCSS; (**d**) RV; (**e**) MLM.

It is acquired from the polarity generator in the SSPS topology since the level generator cannot make it. Only two devices in the level generator are in conduction to obtain any positive or negative voltage level in the SSPS topology depicted in Figure 11b. Because the output voltage is raised by charging all of the DC-link capacitors in series or parallel operation, the output voltage is also increased. This SSPS function is ideal for charging batteries and storing energy. For grid-connected PV systems, series or parallel operation maximizes the use of DC sources. Adding an H-bridge to an SSPS topology RSC-MLI reduces switch counts and further losses. An asymmetrical improvement architecture with a voltage gain is presented by the SSPS topology with minimal modifications. To expand the RV architecture to higher levels, just duplicate the encircling intermediate stage of the level generator illustrated in Figure 11d. In the topologies presented in Figure 11, level generators can only use additive DC source combinations.

(2) T-Type Structure Topologies

A T-type topological structure interconnects numerous DC-link nodes by a phase-leg of full-/half-bridge structures on the burden side. These designs use unidirectional and bidirectional switches. Figure 12 depicts typical T-type topology combinations through complete bridge, cascaded, and half-bridge structures. The T-type with complete bridge construction is the most common, owing to its simplicity and reduced switch count [131,132].

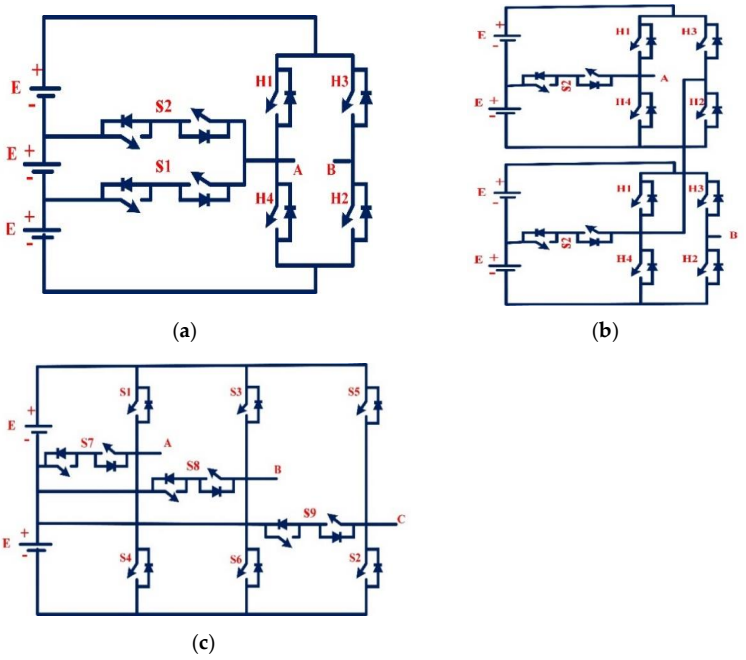


Figure 12. Topologies with T-type structures: (**a**) H-bridge T-type; (**b**) cascaded T-type; (**c**) T-type three-phase half-bridge.

(*i*) T-type MLI: This type of architecture is based on H-bridges and was suggested by [2,133]. The H-bridge is built from the unidirectional switches, and the bidirectional switches connect the H-midpoint bridges to the DC-link voltages. Figure 12a depicts the T-type per-phase configuration with three DC voltage sources. With no redundancies, this topology is merely symmetrical. To increase the topology's flexibility, the number of DC sources can be increased with bidirectional switches or cascade many T-type modules, which allows for uneven voltage ratios and switching redundancy. T-type modules should have the same DC-link voltage. A T-type MLI with two five-level T-type modules cascading is shown in Figure 12b.

(*ii*) Half-leg T-type MLI: Separately, the phase leg is linked to the DC link by bidirectional switches in half-bridge T-type topologies. A three-level

topology is shown in Figure 12c as an example of this structure. To obtain larger levels, just increase the DC sources using bidirectional switches, which may provide even and odd phases of voltage. In Figure 12c, two devices per leg are in conduction at any one moment, and the voltage rating of bidirectional switches is smaller than the devices in a phase-leg. Due to minor conduction losses and a reduced total blocking voltage, this design is preferred over a DCMLI and ANPC in terms of efficiency. Many PV and grid-connected applications have used this design. When an open-circuit switch malfunction occurs, this inverter can be reconfigured to withstand the problem [2,132].

(3) HSC Structure Topologies

A hexagon switch cell (HSC) structure is constructed using unidirectional switches, and the DC link is connected to this structure using bidirectional switches.

(*i*) Topology-I: A mix of T-type with HSC RSC-MLI topology with two stiff DC sources, i.e., ES and ER, on each side of the HSC. Figure 13a illustrates that more bidirectional switches or several modules cascaded together may expand this topology's capabilities further. According to Figure 13a, this topology is similar to the five-level T-type MLI when short-circuiting and open-circuiting the unidirectional switches H5 and H2, as shown. Since there are now unidirectional switches, we can work in asymmetrical configurations with the H-bridge to HSC. Asymmetrical behavior occurs only when ES is less than or equal to the number of elements in the configuration. DC-link capacitors "n" in the asymmetrical design of this architecture can provide (4n + 1) levels of phase voltage. Other voltage levels can be operated by using an asymmetrical arrangement with suitable voltage ratios.

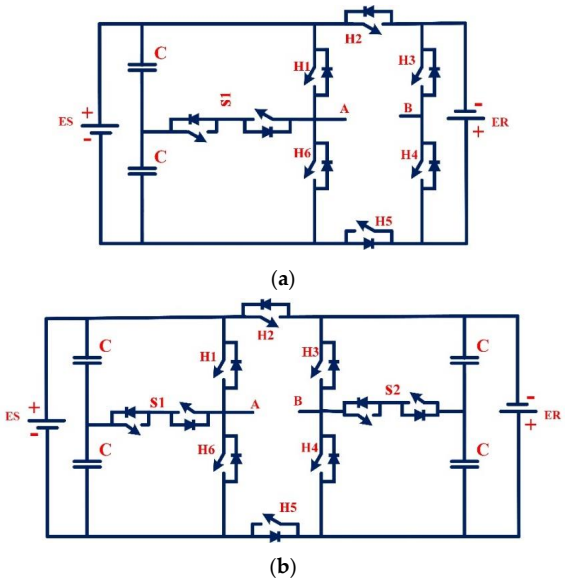


Figure 13. Hybrid T-type topologies and extended HSC structures: (**a**) Hybrid T-type MLI with a bidirectional switch on one side of the HSC; (**b**) hybrid T-type MLI with a bidirectional switch on both sides of the HSC.

(*ii*) Topology-II: Figure 13b shows a configuration that is identical to Topology-I but uses bidirectional switches to connect both sides of the HSC and DC connections. This topology preserves many of the same properties and functions as Topology-I through a pair of unidirectional devices [2].

B. Unit-Based RSC-MLIs

A few authors have developed feasible topologies with drastically reduced switch numbers compared to conventional MLIs to reduce the topological size, price, and complexity. There are a limited number of output voltage values that these topologies can provide. These setups function as RSC-MLIs with fixed topologies and output voltage values.

(1) Basic Unit RSC-MLI Topology

Separate polarity and level generators are used in this H-bridge topology [108,110]. A five-level unipolar voltage can be obtained by using an RSC-MLI basic unit. The basic unit in Figure 14 is made up of three-cell and one-cell structures. The three-cell structure has three voltage sources coupled by five unidirectional switches.

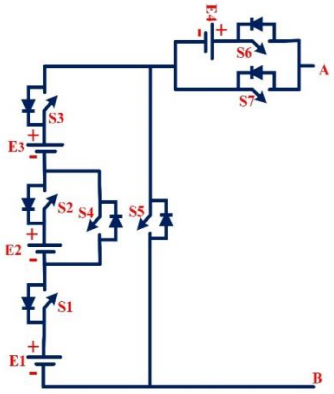
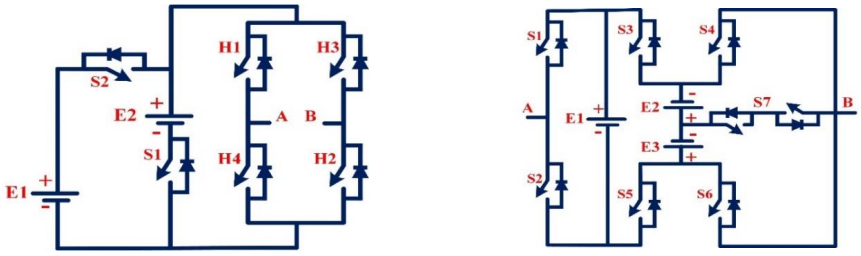


Figure 14. Basic unit RSC-MLI topology.

(2) Symmetrical Unit-Based Topology

There are two unit-based topologies that function with a reduced device sum for a specified number of output voltage levels [2]. These setups are detailed below.

(i) Five-level configuration: To produce nine-level inverters, just cascade two units as indicated in Figure 15a. In each cycle, the cascaded units exchange switching pulses. Consequently, the units perform uniformly.



(**a**) (**b**)

Figure 15. Symmetrical unit-based topologies: (**a**) Five-level; (**b**) nine-level.

(ii) Nine-level configuration: To compare, Topology-I of the hybrid T-type design seems to be comparable, with two DC-link capacitors of identical voltage, as illustrated in Figure 15b.

(3) Asymmetrical Unit-Based Topologies

Figure 16 shows a 17-level MLI circuit with an asymmetrical design. It has ten unidirectional switches with anti-parallel diodes and three asymmetrical DC voltage sources in a 1:2:5 ratio to produce the expected 17-level output voltage. It is described in detail in the aforementioned [134].

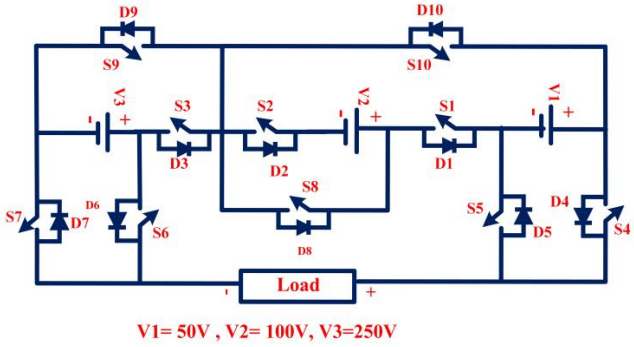


Figure 16. An asymmetrical 17-level RSC MLI.

To produce the desired output voltages of 19 levels in a 1:3:5 ratio [135], an asymmetrical design of the MLI circuit is shown in Figure 17. The design employs ten unidirectional switches with anti-parallel diodes and three asymmetric DC voltage sources. Tables 2 and 3 provide information on how 17-level and 19-level MLIs are built, how they compare with each other, and summarize the various recent topologies. Similarly, Figure 18 compares the parameters of the 17-level MLI topologies that have recently been developed, while Figure 19 compares the parameters of the 19-level MLI topologies that have recently been developed [134–137].

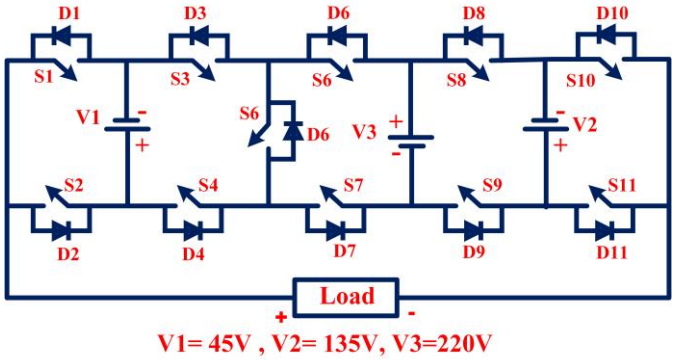


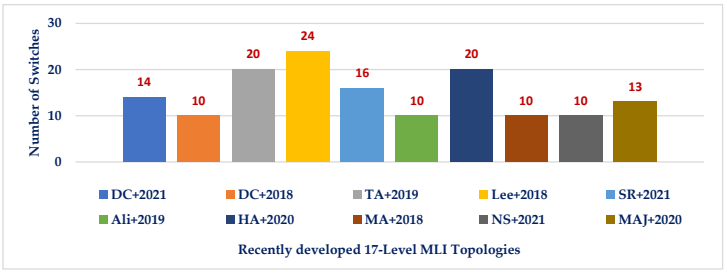
Figure 17. An asymmetrical 19-level RSC MLI.

Table 2. Parametric comparisons of the recently developed 17-level MLIs.

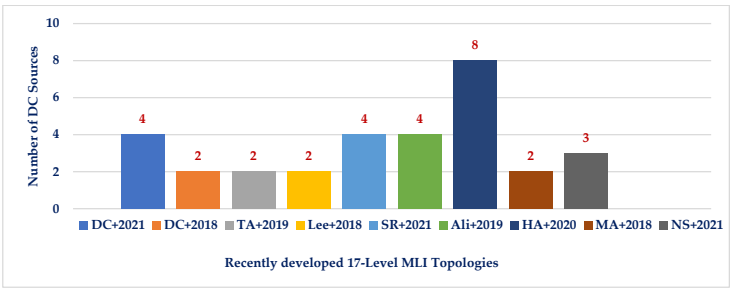
Topologies	N_{SWT}	N_{DCS}	N_L	N_{CAP}	N_{DK}	TSV_{PU}	Transformer-Less Interfacing Capability	Leakage Current Limiting Capability	FCC/L	CF/L	
										α = 1.5	α = 0.5
[3]	14	4	17	4	14	11	No	No	3.05	4.02	3.38
[138]	10	2	17	4	20	-	No	No	3.88	-	-
[139]	20	2	17	4	20	-	No	No	3.88	-	-
[140]	24	2	17	4	24	-	No	No	4.48	-	-
[5]	16	4	17	4	14	11	No	No	3.17	4.14	3.5
[141]	10	4	17	0	10	36	No	No	1.41	9.18	4.94
[142]	20	8	17	0	20	36	No	No	4	7.17	5.05
[143]	10	2	17	0	10	40	No	No	1.35	9.88	5.18
[134]	10	3	17	0	10	12	No	No	1.94	3.92	3.66
17-Level SC-MLI [144]	13	0	17	4	13	5.6	Yes	Yes	2.11	2.02	1.69

Table 3. Parametric comparisons of the recently developed 19-level MLIs.

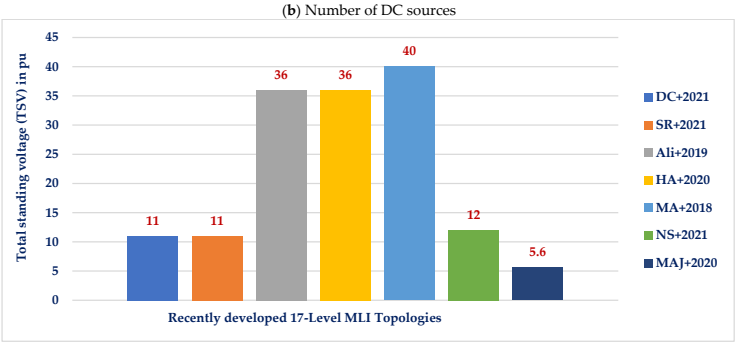
Topologies	N_L	N_{SWT}	N_{DK}	N_{DCS}	FCC/L	TSV_{PU}	Efficiency (%)	CF/L	
								α = 0.5	α = 1.5
[145]	19	12	11	1	1.26	7.55	87.72	1.46	1.85
[146]	19	10	19	2	1.63	8.88	-	1.86	2.33
[147]	19	22	22	8	2.73	8.22	93.49	2.95	3.38
[148]	19	11	19	5	1.84	8	-	2.05	2.47
[149]	19	10	10	2	1.15	6.88	-	1.33	1.7
[150]	19	11	11	4	1.36	5.77	97.38	1.52	1.82
[136]	19	13	13	3	1.52	6.66	93.67	1.70	2.05
[135]	19	11	11	3	1.31	4.66	97.38	1.43	1.68



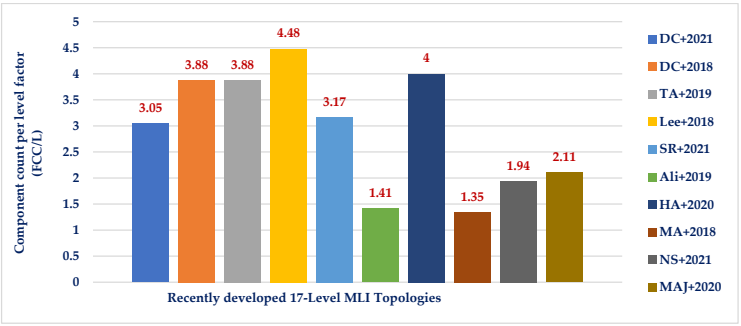
(**a**) Number of switches



(**b**) Number of DC sources

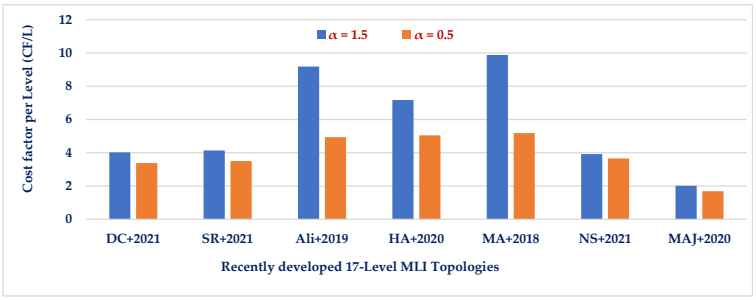


(**c**) Total standing voltage



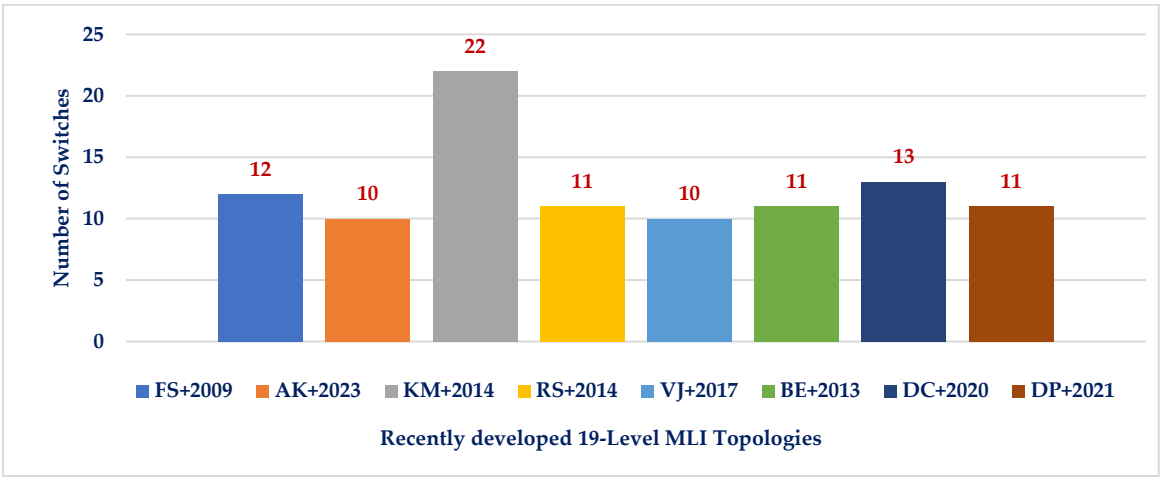
(**d**) Factor of component count per level

Figure 18. *Cont.*

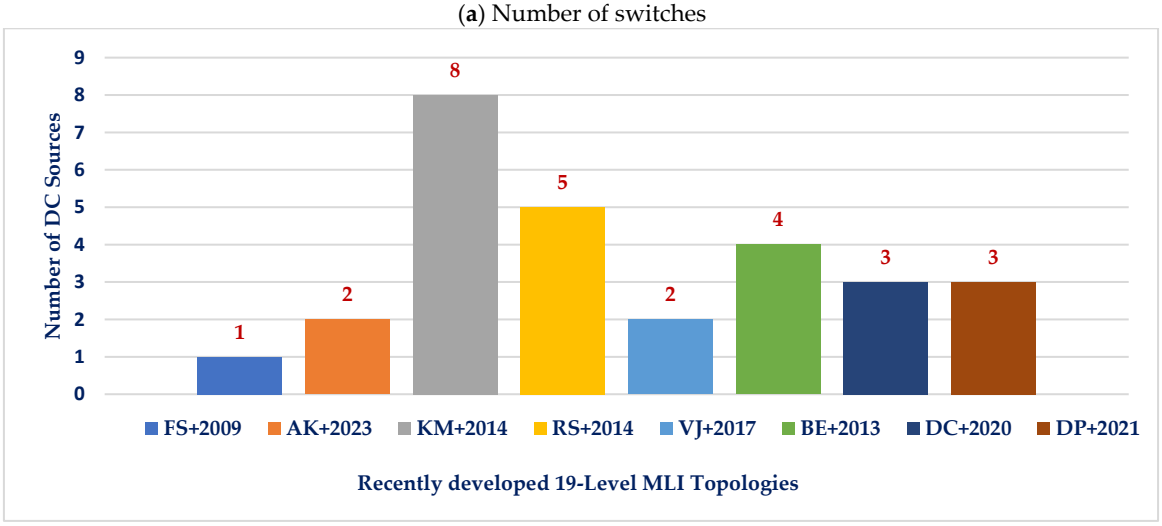


(**e**) Cost factor per level

Figure 18. Parametric comparisons of recently developed 17-level MLI topologies [3,5,134,138–144].

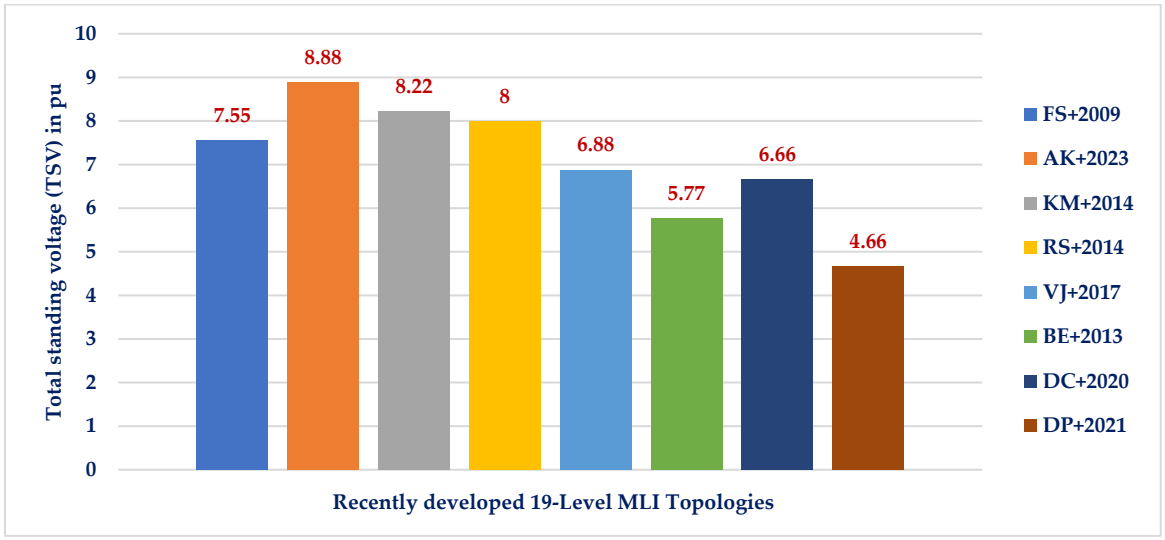


(**a**) Number of switches

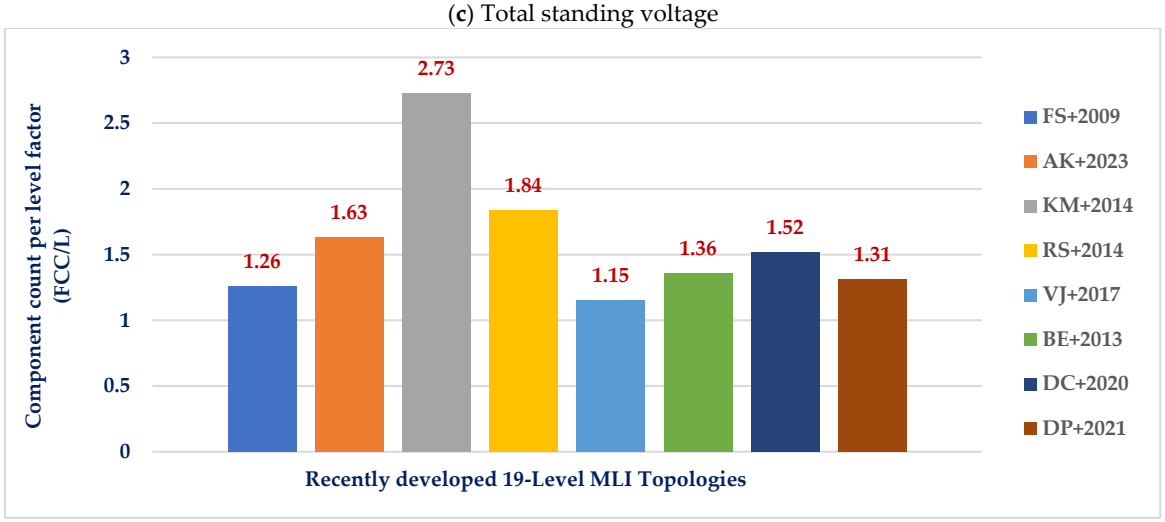


(**b**) Number of DC sources

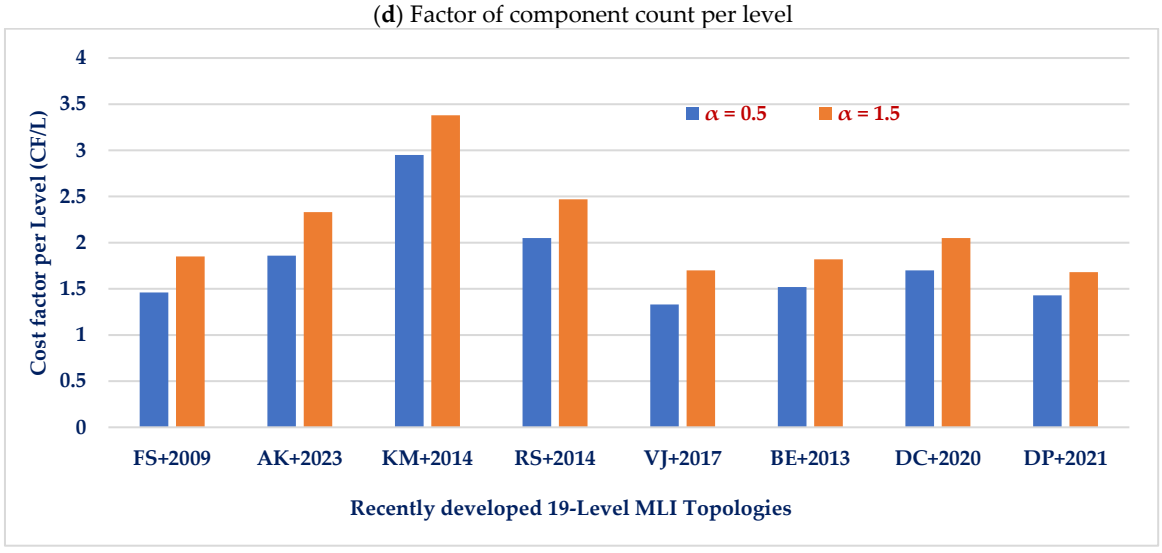
Figure 19. *Cont.*



(**c**) Total standing voltage

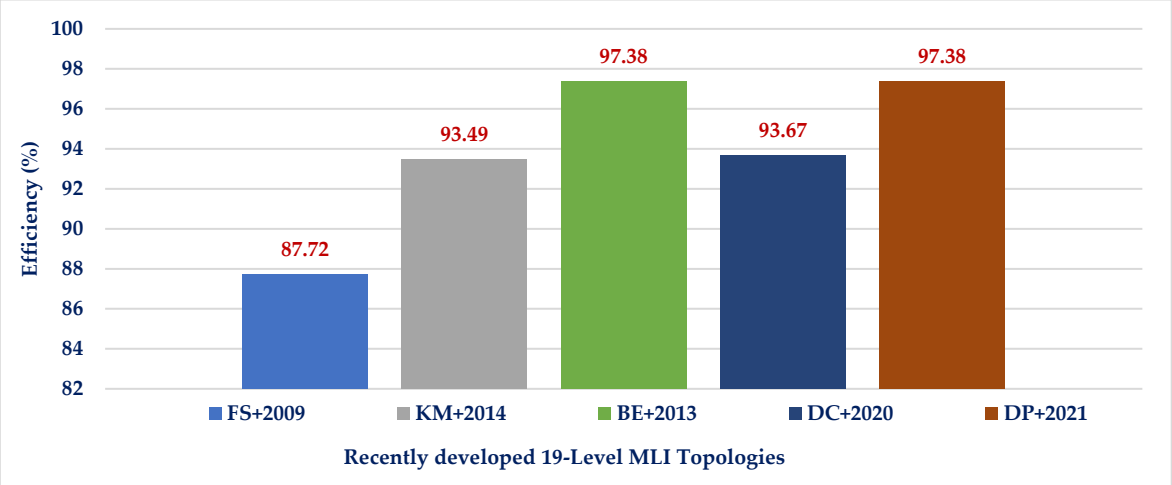


(**d**) Factor of component count per level



(**e**) Cost factor per level

Figure 19. *Cont.*



(**f**) Efficiency

Figure 19. Parametric comparisons of recently developed 19-Level MLI topologies [135,136,145–150].

a. Power loss efficiency calculations:

Power losses are the main constraints in inverters, such as conduction losses (P_{Cond}) and switching losses (P_{Swi}) [134–136]. The net amount of conduction losses can be obtained by considering losses in the IGBT switch (P_{CIGBT}) and anti-parallel diode (P_{CDI}) in the current conduction state and is represented as follows:

$$P_{Cond}(t) = P_{CIGBT}(t) + P_{CDI}(t) \tag{1}$$

$$P_{Cond}(t) = \left\{\left[V_{IGBT} + R_{DI} i_n^{\beta}(t)\right] + \left[V_{DI} + R_{DI} i_n(t)\right]\right\} i_n(t) \tag{2}$$

where V_{IGBT}, V_{DI}, and i_n are the *IGBT* threshold voltages and peak current, respectively. If the diodes (N_{DI}) and switches (N_{IGBT}) are conducted at the same intervals (t), R_{IGBT} and R_{DI} are the IGBT and diode on-state resistance, respectively, β is the IGBT constant. The average power loss is:

$$P_{Cond} = \frac{1}{2\pi} \int_0^{2\pi} \{N_{IGBT}(t) \mathrm{P_{CIGBT}}(t) + N_{DI}(t) P_{CDI}(t)\} dt \tag{3}$$

The energy losses such as energy turn-on (E_{non}) and turn-off (E_{noff}) for IGBT turn-on and -off states during power consumption are:

$$E_{noff} = \frac{1}{6} V_{IGBTj} I t_{off} \tag{4}$$

$$E_{non} = \frac{1}{6} V_{IGBTj} I' t_{on} \tag{5}$$

The j is the loss in *IGBT* and t_{noff} and t_{non} are the turn-on and -off, E_{noff} and E_{non} I and I' of the *IGBT* switches, respectively.

$$P_{Swi} = f\left\{\sum_{j=1}^{N_{IGBT}} \left[\sum_{j=1}^{N_{nonj}} E_{nonji} + \sum_{j=1}^{N_{noffj}} E_{noffji}\right]\right\} \tag{6}$$

The N_{nonj} and *Nnoffj* are IGBT turn-on and -off *j*th time intervals with fundamental (*f*) in one complete cycle.

$$P_{Tloss} = P_{cond} + P_{swi} \tag{7}$$

To calculate the inverter efficiency by Equation (8):

$$\%\eta = \frac{P_{outn}}{P_{inn}} = \frac{P_{outn}}{P_{outn} + P_{Tloss}} \times 100 \tag{8}$$

where both P_{outn} and P_{inn} are abbreviations used to denote output and input power, respectively. The output power can be calculated using Equation (9) as follows:

$$P_{outn} = V_{rms} \times I_{rms} \tag{9}$$

b. Switch stress total standing voltage (TSV) calculations:

To produce the largest blocking voltage via each switch, the multilevel inverter is crucial, and the TSV is the most essential factor in switch selection. There is a pairing between the maximum voltage across the switches and the TSV values. A voltage-blocking stress has been applied across the switch. Differences in voltage stress exist between unidirectional and bidirectional switches.

According to [134], it is possible to calculate the TSV per unit (TSV_{PU}) as:

$$TSV_{PU} = \frac{V_{TSV}}{V_{omax}} \tag{10}$$

c. Cost function (CF) parameter calculations:

The cost function (CF) can be used to make educated guesses about the financial viability of various MLI design alternatives, which is useful for highlighting budgetary constraints and showcasing design tradeoffs. The following equation provides a means through which the cost factor can be determined:

$$CF = (N_{SWT} + N_{DD} + N_{CAP} + N_{DCS} + N_{DK} + \alpha TSV_{PU}) \tag{11}$$

where N_{SWT} indicates the number of switches, N_{DD} indicates the number of diodes, N_{CAP} indicates the number of capacitors, N_{DCS} indicates the number of DC sources, N_{DK} indicates the number of driver circuits, and TSV_{PV} indicates the total standing voltage, if TSV_{PU} is multiplied by the "α" weighting factor. In order to calculate the cost function (CF) can be used Equation (12) can be used as follows:

$$CF = (N_{SWT} + N_{DK} + N_{DCS} + \alpha TSV_{PU}) \tag{12}$$

For the best cost factor computation, 0.5 and 1.5 will be explored. The component count per level factor (FCC/L) can be calculated by using Equation (13):

$$\text{FCC/L} = \frac{(N_{SWT} + N_{DCS} + N_{CAP} + N_{DD} + N_{DK})}{Levels} \tag{13}$$

C. Switched capacitor (SC) unit-based topologies

Basically, a DC source, diodes, capacitors, and switches make up the building blocks of an "SC unit". SPSC units, SC voltage doubler units, SC half-mode units, SC bipolar units, and SC voltage triple units are all subsets of basic SC units. The SC-MLIs can be categorized as single and multiple DC-source SC-MLIs, mid-point-clamped SC-MLIs, common ground switched-capacitor (CGSC)-based MLIs, and hybrid SC-MLIs [151–161].

1. Single DC-source SC-Unit-based MLIs

   a. SPSC Units

There are two main types of SPSC units utilized in SC-MLIs, and they are depicted in Figure 20; Figure 20a depicts the minimal component count for Type-I of this device, which consists of just two switches, one capacitor, and one power diode [162–166]. The output voltage can be set to one of two discrete positive values, V_{DC} or $2V_{DC}$, depending on the

value of the input DC source. SPSC Unit-II, represented in Figure 20b, employs the same capacitor charging and discharging principle, although with an extra capacitor and a power switch in place of the diode and four-quadrant switch. The SPSC Unit-I is different from the SPSC Unit-II in that it can only send power in one direction. Furthermore, unlike the SPSC Unit-I, the SPSC Unit-II uses charged capacitor voltages to create both discrete voltage levels, which eliminates the possibility of a DC offset during the formation of the output voltage level in SC-MLIs. In this case, in addition to the paralleled conventional power switches in SPSC Unit-II, four-quadrant power switches with a back-to-back connection of two standard MOSFETs can be employed [167–171].

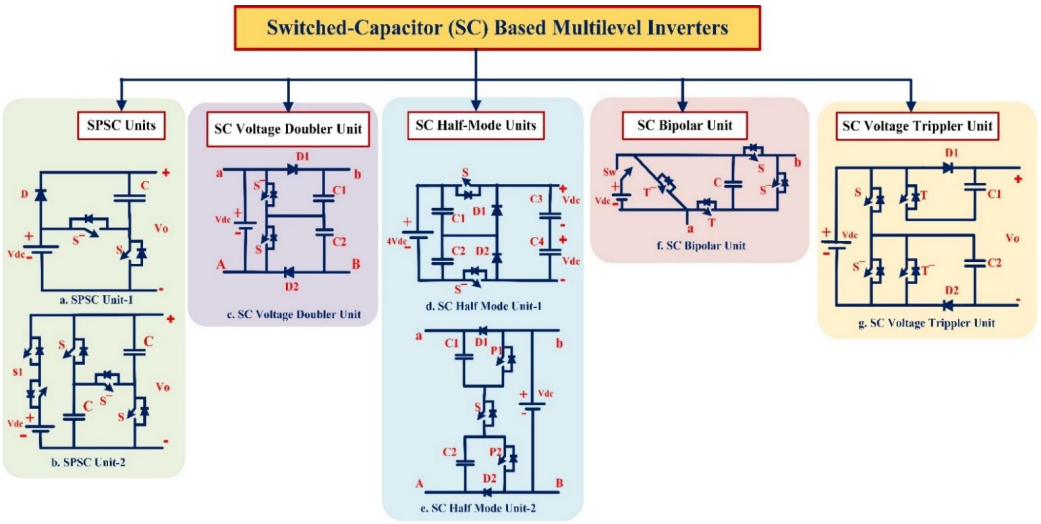


Figure 20. Categorization of different SC-based basic units.

b. SC Voltage Doubler Unit

A voltage doubler SC unit, as shown in Figure 20c, is a two-port converter that utilizes a single DC source, two capacitors, two complementary power switches, and two power diodes. Each capacitor has its own charging channel, which includes a diode and a power switch. Being a two-port SC-based basic unit, it can provide five different DC-link voltages, including 0 V_{DC}, $\pm V_{DC}$, and $\pm 2V_{DC}$. This fundamental SC unit's adaptability to operation comes at the expense of a lack of bidirectional power flow capacity [172–176].

c. SC Half-Mode Units

When using an SC half-mode device, the DC-link capacitors can be charged to a voltage that is only a small multiple of the DC-input source's voltage. Several other SC half-mode units have been introduced recently, as illustrated in Figure 20d. This is connected to the charging activities of the capacitors in the SC half-mode Unit-I; two fixed values of discrete DC-link voltages are required at its output, and this requires four DC-link capacitors, two complementary switches, and two diodes. Using a capacitive charging channel consisting of two diodes and a single power switch, the capacitors in this setup are charged to half the main DC-link voltage, earning this configuration the designation SC half-mode Unit-II, as shown in Figure 20e.

d. SC Bipolar Unit

The SC bipolar unit, shown in Figure 20f, has the ability to generate bipolar output voltage levels, such as $0V_{DC}$, $\pm V_{DC}$. In this device, just one DC-link capacitor is required to be charged in parallel to the input DC-source voltage, whereas five power switches are required for the entire operation.

e. SC Voltage Tripler Units

Basic units based on SC technology give SC-MLI topologies with voltage increases that are three times the normal value. Figure 20g shows the functioning concept of the most common type of SC voltage tripler unit. It is comprised of two DC-link capacitors, two power diodes, and four power switches [177–181]. As can be observed, both capacitors in this device are charged by the DC input. Table 4 provides a comparative study of different single DC source SC-MLIs [151], Table 5 describes the comparative study of different SC-MLIs with two asymmetric DC sources, and Table 6 provides a comparative study of cross-connected asymmetrical 15-level SC-MLIs [182–186].

Table 4. Comparative study of different single DC source SC-MLIs.

Type of SC-MLI	No. of Levels/THD	Overall Voltage Gain/Caps Voltage	TSV (pu)/MVS	Reported Rated Efficiency	No. of Components		
					S	D	C
FB based [153]	7/19.5%	3/V_{DC} (3)	6/3V_{DC}	85%@1kHz/5W	10	0	3
HB based [169]	7/7%	3/V_{DC} (2)	5.66/3V_{DC}	92.2%@50Hz/500W	9	4	2
HB/NPP based [172]	7/16.2%	1.5/0.5V_{DC} (2)	6/V_{DC}	95.5%@50Hz/250W	10	0	2
HB based [173]	7/11.2%	4/V_{DC} (2), 2V_{DC} (2)	5.5/4V_{DC}	96.5%@50Hz/270W	12	0	4
HB based [162]	7/13.7%	1.5/V_{DC} (2)	5.33/V_{DC}	96.6%@50Hz/600W	10	0	2
FB based [151]	7/2.8%	3/V_{DC} (2)	6/3V_{DC}	92.1%@50Hz/150W	9	1	2
FB based [174]	9/3.1%	2/V_{DC} (2)	5.75/2V_{DC}	94.2%@1kHz/200W	9	2	2
FB based [175]	9/13.8%	4/V_{DC} (1), 2V_{DC} (1)	5.25/4V_{DC}	NA%@50Hz/NA	9	2	2
HB/NPP based [176]	9/12.5%	2/0.5V_{DC} (2)	5.5/2V_{DC}	NA%@50Hz/400W	11	0	2
HB/NPP based [36]	9/8.8%	2/V_{DC} (1), 0.5V_{DC} (2)	5.5/2V_{DC}	97.4%@50Hz/1kW	12	0	3
HB/NPP based [37]	9/10.2%	2/V_{DC} (1), 0.5V_{DC} (2)	5.5/2V_{DC}	98%@50Hz/1kW	10	1	3
HB based [165]	11/6.8%	5/V_{DC} (2), 3V_{DC} (2)	5/6V_{DC}	95.5%@50Hz/220W	9	4	4
HB based [166]	13/11%	6/V_{DC} (2), 3V_{DC} (2)	5.5/6V_{DC}	95.5%@50Hz/500W	10	4	4
HB/NPP based [177]	13/5.3%	3/V_{DC} (2), 0.5V_{DC} (2)	6/3V_{DC}	NA%@50Hz/1kW	12	4	3
HB based [178]	13/7.2%	6/V_{DC} (2), 3V_{DC} (1)	6/3V_{DC}	NA%@50Hz/NA	13	2	3
HB based [38]	13/7.7%	6/V_{DC} (1), 2V_{DC} (2)	5/3V_{DC}	94%@50Hz/1kW	15	0	3
HB/NPP based [160]	17/NA	8/V_{DC} (2), 2V_{DC} (2), 4V_{DC} (2)	4.25/8V_{DC}	95.5%@50Hz/1kW	10	4	6
HB based [179]	17/3.9%	8/V_{DC} (1), 2V_{DC} (2), 4V_{DC} (2)	4.25/8V_{DC}	94.5%@50Hz/80W	10	5	5
HB based [180]	21/4.8%	10/V_{DC} (2), 2V_{DC} (4), 4V_{DC} (2)	5/2V_{DC}	NA%@50Hz/NA	20	8	8
HB based [181]	21/4.5%	10/V_{DC} (2), 2V_{DC} (4), 4V_{DC} (2)	5/2V_{DC}	NA%@50Hz/NA	20	12	10

Table 5. Comparative study of different SC-MLIs with two asymmetric DC sources.

Type of SC-MLI	No. of Levels/THD	Overall Voltage Gain/CapsVoltage	TSV (pu)/MVS	Asymmetric Amplitude of DC-Sources	No. of Components		
					S	D	C
SCC-Mode-I [43]	11/NA	1.25/V_{DC}	4.2/4V_{DC}	V_{DC} and 3V_{DC}	11	0	1
SCC-Mode-II [43]	11/9.3%	1.67/2V_{DC}	4.4/2V_{DC}	V_{DC} and 2V_{DC}	11	0	1
Figure 1 [49]	15/4.7%	1.75/V_{DC}	8.5/7V_{DC}	V_{DC} and 3V_{DC}	10	1	1
Figure 1 [47]	17/4.8%	1.6/2V_{DC}, 1.5V_{DC} (1)	4.5/8V_{DC}	2V_{DC} and 3V_{DC}	12	1	3
Figure 1 [44]	19/8.9%	1.8/4V_{DC} (2)	4.89/9V_{DC}	V_{DC} and 4V_{DC}	13	0	2
Figure 1 [47]	21/4.3%	2/V_{DC} (2), 4V_{DC} (2)	5/10V_{DC}	V_{DC} and 4V_{DC}	14	0	4
Figure 1 [52]	25/1.8%	2/V_{DC}, 4V_{DC}	10/10V_{DC}	V_{DC} and 5V_{DC}	12	2	2
Figure 3 [44]	29/NA	2/V_{DC} (2), 2.5V_{DC}	4.64/14V_{DC}	V_{DC} and 2.5V_{DC}	18	0	3
Figure 12 [182]	31/NA	4/V_{DC} (2), 4V_{DC} (2)	5.5/15V_{DC}	V_{DC} and 4V_{DC}	14	2	4
Figure 13f SCC [183]	31/NA	3/V_{DC} (2), 4V_{DC} (2)	5.6/15V_{DC}	V_{DC} and 4V_{DC}	16	0	4
Figure 13g SCC [184]	49/NA	4/V_{DC} (3), 4V_{DC} (3)	7.25/24V_{DC}	V_{DC} and 4V_{DC}	18	2	6
Figure 3 [185]	49/NA	2/V_{DC} (2), 5V_{DC} (2)	6/24V_{DC}	V_{DC} and 5V_{DC}	18	2	4
Figure 4 [44]	49/NA	2/V_{DC} (2), 5V_{DC} (2)	5/24V_{DC}	V_{DC} and 5V_{DC}	20	0	4

Table 6. Parametric comparisons of cross-connected 15-level SC-MLIs.

Topologies	N_{Lev}	N_{Swt}	N_{DK}	N_{DC}	N_C	N_{Dio}	V_{TB}/N_L	Efficiency (%)
[187]	15	10	10	5	0	1.26	-	93.73
[188]	15	14	14	1	4	1.63	4.86	-
[189]	15	10	9	4	0	2.73	4.6	97.5
[190]	15	8	8	3	0	1.84	2	95.2
[191]	15	10	9	3	0	1.15	2.26	-
[192]	15	10	10	5	0	1.36	1.06	90
Figure 1 [186]	15	10	8	2	2	1.31	3.6	96.3

4. Mid-Point-Clamped SC-MLIs

High-frequency variable CMV, which results from the varying numbers of HB legs used in the aforementioned single and multiple DC-source SC-MLIs to invert the SC unit/generalized SCC output voltage polarity, is one of the main issues that prevents their widespread use, for example, in grid-tied PV systems. Since their output voltage is monitored at the neutral point of the DC connection, mid-point-clamped MLIs are a common choice in this scenario. While a multilevel output voltage waveform is generated by a single input DC source, the leakage current problem in grid-tied PV applications is significantly reduced. The identical capacitors used in the DC links of single-phase MLIs may be used in three-phase systems. Table 7 provides a comparative study of different mid-point-clamped SC-MLIs [187–197].

Table 7. Comparative study of different mid-point-clamped SC-MLIs.

Type of SC-MLI	No. of Levels/THD	TSV (pu)/MVS	Reported Rated Efficiency	No. of Components		
				S	D	C
SC [56,159]	4/41.4%	$2.66/1.5V_{DC}$	97%@1kW	4	2	4
ABNPC [57]	5/NA	$5/V_{DC}$	98.5%@1.2kW	6	2	3
ABNPC [60]	5/NA	$6/0.5V_{DC}$	NA@50W	10	0	3
ABNPC [62]	5/NA	$6/0.5V_{DC}$	97.5%@800W	6	2	4
ABNPC [81]	5/NA	$6/1.5V_{DC}$	97.1%@1kW	8	2	4
ABNPC [82]	6/20.2%	$4.4/3V_{DC}$	95.8%@450W	6	4	5
Sym SC [172]	7/12.2%	$5/V_{DC}$	97%@150W	9	1	3
ABNPC [61]	7/NA	$5.33/V_{DC}$	96%@50W	9	0	3
ABNPC [66]	7/19.3%	$5.3/2V_{DC}$	96.7%@250W	9	0	3
Dual T-type [70]	7/NA	$7.33/2V_{DC}$	98%@100W	10	0	4
ABNPC [71]	7/NA	$6.66/V_{DC}$	97%@100W	10	0	4
ABNPC [74]	7/NA	$4.66/V_{DC}$	97.8%@400W	8	2	4
Dual T-type [61]	9/NA	$10/V_{DC}$	96%@50W	12	0	3
ABNPC [72]	9/NA	$5/0.5V_{DC}$	97%@500W	10	4	4
ABNPC [73]	9/NA	$10/2V_{DC}$	98%@400W	11	4	3
ABNPC [75]	9/4.1%	$5/V_{DC}$	97.1%@400W	10	2	2
Asym SC [56]	15/5.5%	$5/2V_{DC}$	97%@150W	12	2	4
9-Level SC-MLI [198]	9/1.07%	$8.5\ V_{DC}$	98.03%@583.91W	10	4	4
15-Level MC-MLI [199]	15/5.66%	$7\ V_{DC}$	94.1%@113.75W	9	4	3
MM-STC [200]	9/9.28%	$4\ V_{DC}$	98.65%@321.35W	8	8	0
17-Level SC-MLI [201]	17/NA	$5/2V_{DC}$	96.5%@434.7W	16	10	4

a. Five-Level mid-point-clamped SC-based inverter

The five-level mid-point clamped-based MLI approach, as shown in Figure 21a, involves adding two capacitors, C3 and C4, and a four-quadrant power switch "*p*" to a standard 3L NPC-based inverter to provide five distinct levels of output voltage.

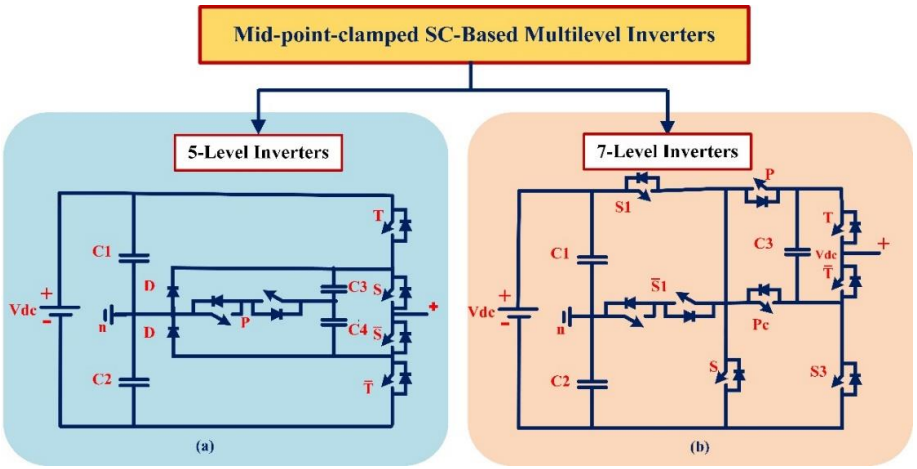


Figure 21. Mid-point-clamped SC-based inverters: (**a**) 5-Level inverter, (**b**) 7-Level inverter.

b. Seven-Level mid-point-clamped SC-based inverter

The seven-level mid-point-clamped inverter proposed in [79] and depicted in Figure 21b is another example of this topology, although one that employs nine rather than eight switches. Figure 22 shows the comparison of the efficiency of SC-MLI with multi-source MLIs [198], and Figure 23 shows the measured efficiency of the 19-level SC-MLI at different frequency ranges [144,198–201].

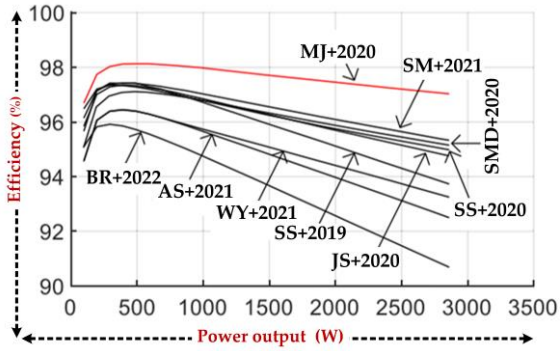


Figure 22. Comparison of the efficiency of SC-MLI with multi-source MLIs [61,68,72–74,151,172,198].

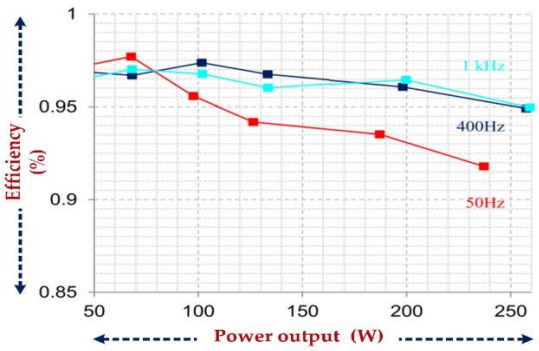


Figure 23. Measured efficiency of the 19-level SC-MLI at different frequency ranges.

5. Common Ground Switched-Capacitor (CGSC)-Based MLIs

Mid-point clamped MLIs can minimize leakage current in transformer-less grid-tied PV systems. HF-CMV in midpoint-clamped MLIs is from DC-link capacitors. To eliminate CMV, CGSC-based MLIs have been proposed, where the input DC source's ground and the grid's neutral point are directly coupled. No leakage current can flow through the system because the parasitic capacitance between the negative terminal of the input DC source, such as PV panels, and the ground sees a grounded potential instead of a fluctuating HF-CMV. This converter is also called a three-port single-DC source inverter or a transformer-less inverter with double grounding. Table 8 provides a comparative study of different CGSC-based MLIs, and Table 9 provides comparative study of different hybrid MLIs [194–196].

Table 8. Comparative study of different CGSC-based MLIs.

Type of SC-MLI	No. of Levels/THD	Overall Voltage Gain/Caps Voltage	TSV (pu)/MVS	Reported Rated Efficiency	No. of Components		
					S	D	C
[86]	5/NA	$2/V_{DC}$ (1), $2V_{DC}$ (1)	$4.5/2V_{DC}$	98.1%@600W	6	2	2
[89]	5/NA	$2/V_{DC}$ (1), $2V_{DC}$ (1)	$6/2V_{DC}$	96%@40W	7	2	2
[90]	5/35.4%	$2/V_{DC}$ (2)	$5/2V_{DC}$	98%@600W	8	1	2
[92]	5/NA	$2/V_{DC}$ (1), $2V_{DC}$ (1)	$5/2V_{DC}$	98%@600W	11	0	4
[93]	5/NA	$2/V_{DC}$ (1), $2V_{DC}$ (1)	$6.5/2V_{DC}$	97.5%@600W	8	2	3
[94]	5/NA	$2/V_{DC}$ (2)	$5.5/2V_{DC}$	98.3%@600W	8	0	2
[99]	5/36.4%	$2/V_{DC}$ (1), $2V_{DC}$ (1)	$6.5/2V_{DC}$	97.5%@330W	8	1	2
[102]	5/NA	$2/V_{DC}$ (2)	$6/2V_{DC}$	96.7%@1kW	9	0	2
[102]	5/NA	$1/0.5V_{DC}$ (2)	$6/V_{DC}$	97%@500W	6	1	2
[94]	7/NA	$3/V_{DC}$ (3)	$6/3V_{DC}$	98.3%@600W	11	0	2
[95]	7/NA	$3/V_{DC}$ (2), $2V_{DC}$ (1), $3V_{DC}$ (1)	$6/3V_{DC}$	98%@800W	6	4	4
[97]	7/NA	$3/V_{DC}$ (1), $2V_{DC}$ (2)	$5.33/3V_{DC}$	NA@1kW	8	4	3
[98]	9/NA	$4/V_{DC}$ (4)	$6/4V_{DC}$	NA@275W	17	4	4
[102]	9/NA	$4/V_{DC}$ (4)	$6/4V_{DC}$	NA@1kW	17	0	4

Table 9. Comparative study of different hybrid MLIs.

Type of SCMLI	No. of Levels/THD	Overall Voltage Gain/Caps Voltage	TSV (pu)/MVS	Reported Rated Efficiency	No. of Components		
					S	D	C
CGSC based [105]	5/NA	$1/V_{DC}$ (1), $0.5V_{DC}$ (1)	$4/V_{DC}$	95.8%@1.2kW	6	1	2
ABNPC based [106]	7/NA	$1/0.5V_{DC}$ (2), V_{DC} (1), $0.5V_{DC}$ (1)	$5/V_{DC}$	98%@2.2kW	8	2	4
ABNPC based [107]	7/NA	$1/0.5V_{DC}$ (2), V_{DC} (1), $0.5V_{DC}$ (1)	$5.5/V_{DC}$	NA	10	0	4
ABNPC based [112]	7/NA	$0.5/0.5V_{DC}$ (2), $0.33V_{DC}$ (2)	$6/0.5V_{DC}$	NA	11	0	4
HB based [108]	9/NA	$2/V_{DC}$ (2), $0.5V_{DC}$ (1)	$6/2V_{DC}$	96.4%@500W	8	2	3
HBSC based [109]	9/13.5%	$2/V_{DC}$ (1), $0.5V_{DC}$ (1)	$6/V_{DC}$	97.3%@330W	11	0	2
HBSC based [110]	9/NA	$2/V_{DC}$ (1), $0.5V_{DC}$ (1)	$5/2V_{DC}$	96.5%@330W	8	1	2
HBSC based [111]	9/NA	$2/V_{DC}$ (1), $0.5V_{DC}$ (1)	$5.5/2V_{DC}$	96.6%@600W	8	1	2
HBSC based [114]	9/9.4%	$2/V_{DC}$ (1), $0.5V_{DC}$ (1)	$5.5/V_{DC}$	96.5%@800W	10	0	2
CGSC based [116]	9/NA	$2/V_{DC}$ (2), $0.5V_{DC}$ (1)	$5/2V_{DC}$	97.5%@1.2kW	9	1	3
CGSC based [117]	5/NA	$2/V_{DC}$ (1), $2V_{DC}$ (1)	$6/2V_{DC}$	97.5%@700W	7	2	2

a. Three-level CGSC-based inverter

The inverters are based on CGSC and have been recently practiced. Taking into consideration Figure 24a, [202] proposed a three-level CGSC-based inverter with five power switches and a virtual DC-link capacitor, where the capacitor, C, was charged to the input DC source, Vdc, during the positive and zero levels of the output voltage and discharged during the generation of the negative output voltage. Siwakoti-H inverters were proposed in [203] that reduced the number of switching devices for this type of three-level CGSC-based inverter, as illustrated in Figure 24b,c, where one additional diode was employed in Type-I of this converter and two RB-IGBTs were used in its Type-II variation. In [204], a three-level, four-switch CGSC-based inverter is presented; the virtual DC-link capacitor is charged indirectly to Vdc through a diode-aided CPC cell.

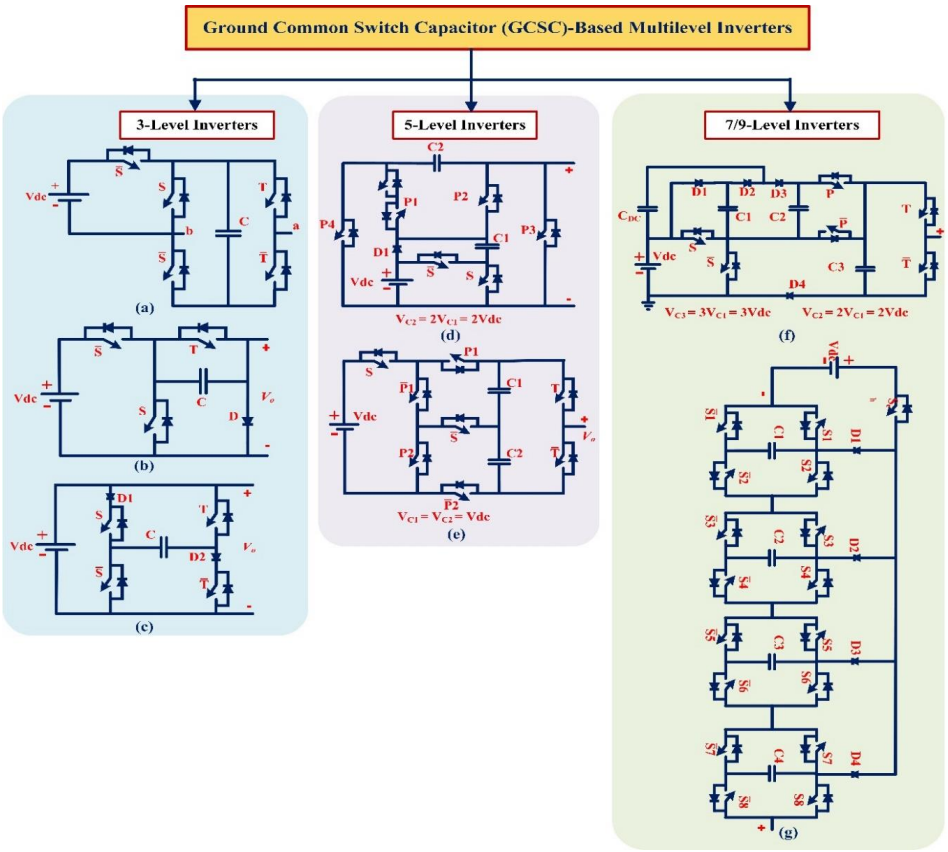


Figure 24. CGSC-based inverters: (**a**–**c**) Three-level inverters; (**d**,**e**) five-level inverters; (**f**) seven-level inverter; (**g**) nine-level inverter.

b. Five-level CGSC-based inverter

There are two distinct CGSC-based inverter topologies, as can be seen in Figure 24d,e, one employing six power switches and the other employing eight power switches, both of which are capable of producing five levels of double voltage conversion gain output. A five-level CGSC-based inverter, recently presented by Ardashir et al. [197], is comprised of six power switches. The negative output voltage levels are generated using a similar virtual DC-link SC approach, but the total gain of the voltage conversion is unity.

c. Seven-level CGSC-based inverter

The authors of [134] described a further inverter design based on a seven-level CGSC by considering Figure 24f, with fewer switches. By charging capacitors C1, C2, and C3 to Vdc, 2Vdc, and 3Vdc, respectively, the whole seven-level inverter output voltage range can be made with a voltage gain of three. This construction is based on the virtual DC-link

principle, just like the aforementioned five-level CGSC-based inverters. Only six power switches are needed, but an extra four power diodes are essential. Since C2 and the input DC source are connected in series, C3 can be charged from either. This charging action is feasible both at zero and at the highest positive output voltage level, +3 Vdc, just as in the five-level CGSC-based inverters given in [86–91]. Additionally, in positive and negative half-cycles of the output voltage, the direction of the load current charges and discharges the DC-link capacitor Cdc. As a result, a higher Cdc and C3 capacitance may be required to reduce the voltage ripple caused by these lengthy discharging cycles.

d. Nine-Level CGSC-based inverter

A nine-level quadruple-voltage-gain CGSC-based inverter is shown in Figure 24g. The consistent MVSs across all the FB-cell switches and the lowered balanced voltage value of the related capacitors make this a compelling design, despite the high number of switching devices it employs. Because bigger values of the capacitance are required in the case of increased power injection requirements, the converter's lengthy discharging cycle for the capacitors may be a major drawback.

The scope of use for SC-MLIs can be expanded as shown in Figure 25, and SC-MLIs are appealing for grid-tied PV-based low-power applications because of their single-stage voltage step-up capability, despite their pulsing input current [86–88]. Other developed applications of SC-MLIs with restricted output power performance include motor drives, electric vehicles, energy storage systems, and balancing in battery strings.

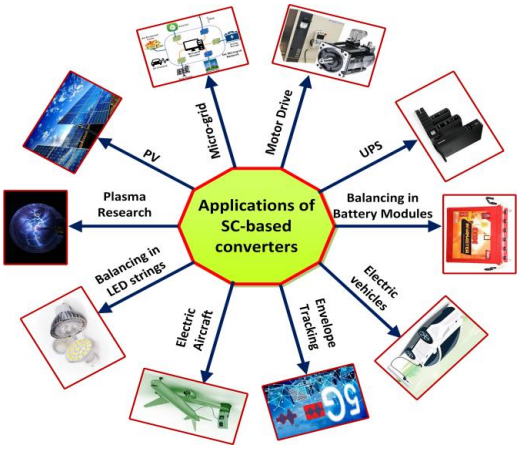


Figure 25. Various applications of SC-based multilevel converters/inverters.

As can be seen in Figure 26, we take into consideration ten characteristics to present a comprehensive qualitative overview of the circuit properties of various SC-MLIs.

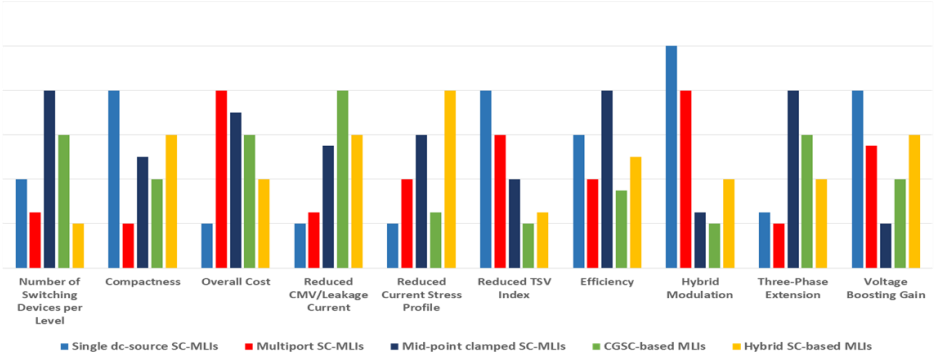


Figure 26. Qualitative comparison analysis of different SC-MLIs in various characteristics.

6. Modulation Techniques

Modulation techniques typically involve a carrier signal and a modulator waveform with different waveform parameters. By adjusting the characteristics of a carrier signal using a reference signal, modulation can be used to control the switching time of the switches in the MLIs. Harmonic reduction and switching losses, both of which can be controlled by modulation methods, are two of the things that affect the overall efficiency of a multilevel inverter. The modulation index plays an important role in all control systems. The THD fluctuates with a modulation ratio (either too much or too little). There are a variety of methods in the literature that may be used based on the switching frequency, whether fundamental or high frequency. Figure 27 shows several MLI modulation control techniques.

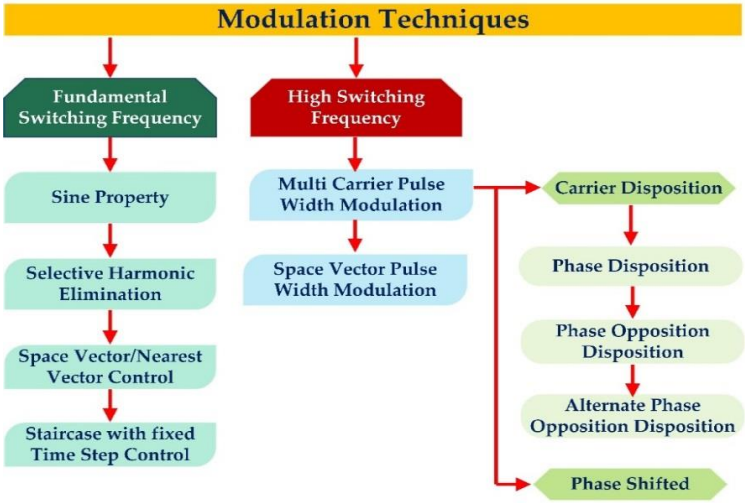


Figure 27. Multilevel inverter modulation control techniques.

Table 10 provides a comprehensive study of conventional MLI topologies; Table 11 offers the merits and demerits of new multilevel inverter topologies; Table 12 provides the applications of MLI topologies; and Table 13 provides information on a comprehensive examination study of traditional and new multilevel inverter topologies.

Table 10. The advantages of switched-capacitor multilevel inverters (SC-MLIs) over conventional multilevel inverters.

Advantages	Switched-Capacitor Multilevel Inverters (SC-MLIs) [36,38,68,90,91,99,151,198,201]	Conventional Multilevel Inverters (DC-MLI, FC-MLI & CHB-MLI) [1,2,11,31,39,106,205]
Reduced component count	Fewer power electronic components required	More components needed
Cost	Fewer components lead to lower costs and increased reliability	A higher component count might lead to increased cost and complexity
Higher efficiency	Fewer components and simplified control can contribute to higher efficiency	Higher component count and more complex control might lead to lower efficiency
Compact design	Modular and compact designs are possible	The size might be larger
Modular structure	Scalable and adaptable design by adding or removing capacitor modules	Limited scalability
Simplified control	Simple control strategy due to switched capacitors	Control complexity may be higher
Voltage balancing	Inherent voltage balancing	Requires active balancing
Improved reliability	A simpler structure and fewer components can result in improved overall reliability	Complex structures and more components might lead to increased failure points

Table 10. *Cont.*

Advantages	Switched-Capacitor Multilevel Inverters (SC-MLIs) [36,38,68,90,91,99,151,198,201]	Conventional Multilevel Inverters (DC-MLI, FC-MLI & CHB-MLI) [1,2,11,31,39,106,205]
Reduced EMI	Potentially lower EMI	EMI considerations may be higher
Low-power applications	Well-suited for applications with lower power requirements	Suitable for a range of power levels, but complexity might be overkill for lower power applications
Improved waveform quality	Inherent voltage balancing leads to improved output waveform quality	Output waveform might require additional filtering to achieve desired quality.

Table 11. Benefits and restrictions of new multilevel inverter topologies.

MLI Topology	Benefits	Restrictions
RVDC-C [205]	• A more modular framework • Asymmetric or symmetric source configurations are possible • Cells may share electricity equally • Can be used at the basic switching frequency	• Independent DC sources are required
Developed H-bridge [31]	• To produce greater levels of output, it only requires a small number of switches	• Why equality of load sharing across sources is impractical. • An asymmetrical arrangement is required • Independent DC sources are required
SCU [151]	• High modularity, equal load sharing across sources • Works with both symmetric and asymmetric sources	• Control complex • Capacitor performance problem • DC sources must be isolated
DCC [1]	• There is the option of using an asymmetric source arrangement • This device has a basic construction and a high degree of modularity	• Cell-to-cell power transfer is impossible • Various voltage switches are required • Requires independent DC.
CPCC [205]	• It may be used with either an asymmetrical or symmetrical source arrangement • It is feasible to distribute electricity equally across cells in a symmetrical design	• No need for fundamental frequency shifting. • Requires various voltage switches.
CIC [205]	• Minimal switching and conductor losses • Modular construction	• It requires both isolated and non-isolated DC supply, and it cannot be used with asymmetric source configurations
Hybridtopology [31,43,51]	• Low-, medium-, and high-voltage applications are all well-served by this component • Switching frequency at the fundamental level can be applied	• A lot of work is required to manage this • Switches with various voltage ratings are required • This does not apply to a trinary-source setup • Isolated DC power supply are required
HERC-C [205]	• Simple and very modular structure • Power distribution across modules may be done on an equal basis • Switching and conduction losses have been • minimized significantly	• It is not possible to use a trinary source configuration
Cascaded half- bridge [11,33]	• Modular and simplified design • All that is needed is a single, isolated DC supply • Switch rating stays constant as the number of levels increases • Totally eliminates common-mode leakage current in solar PV	• Balancing capacitors is a delicate process that needs further attention • High losses in switching • It is not feasible to share authority equally • It is feasible to set up a source in an asymmetrical fashion.

Table 11. *Cont.*

MLI Topology	Benefits	Restrictions
SSSC [151]	• Switches with the same power rating are needed • A reduction in switch count without an increase in switch rating • Equality of power can be achieved	• The structure is complicated • Capacitor dynamics prevent it from operating at its basic switching frequency
SADC [151]	• Simple Architecture and it can function at the highest voltage-rated switch	• No two sources can share the burden equally • A variety of switches are required • A DC source of uneven magnitudes is needed for this application
CCS [11,33]	• Suitable for low-, medium-, and high-voltage applications • Simple construction	• Sources needed to be mandatorily asymmetric
Staircase cascaded [33]	• Structural flexibility • Low conduction losses • Low-, medium-, and high-voltage applications • Non-isolated DC input levels	• Requires switches of different voltage rating • Equal distribution of power among sources cannot be attained • Asymmetric source configuration is not possible
Reduced switch type [205]	• Asymmetric arrangement is also feasible • High efficiency • Simple basic module layout for many levels	• DC power sources must be kept separate • Various switches have different blockings • Voltage ratings
Cascade unit based [11]	• Has a modular design • Can be swapped at the fundamental frequency • Asymmetric source setup is another option.	• It is impossible to have an equal distribution of power • Switches with various voltage ratings are required

Table 12. Applications of MLI topologies.

MLI Type	Applications
NPC [72,79]	• Drives • RESs • Power conversion
FC [205]	• RES • Drives
ANPC [57]	• Solar PV systems • Filters
CHB [11,33]	• Power systems • RES • Motor Drives
HCHB [31,43,51]	• Drives • RES
MLDCL [12]	• Permanent magnet motor drives for below 100 KW • Solar PV and fuel cell incorporation
SSPS [151]	• RES • Drives • Traction

Table 12. *Cont.*

MLI Type	Applications
T-type [68]	• Drives • RES • Railways (traction)
N-type [1]	• RES • Medium voltage level industries
CCHB [1,11,33]	• Drives • Power conversion • RES
RV [2,205]	• Power conversion • High voltage DC transmission systems
MLM [205]	• RES
CCS [11,33]	• Solar PV systems
PUC [205]	• Drives • RES
CBSC [151,205]	• RES
M-type [1]	• High voltage DC transmission systems • Wind energy conversion systems

Table 13. Comprehensive examination study of traditional and new multilevel inverter topologies (n_{level} = number of levels in phase voltage).

Topology	Unidirectional Switches (N_{sw})	Bidirectional Switches	DC Sources (N_{DC})	Capacitors (N_{cap})	H-Bridge	Highest Switch Rating	Total StandingVoltage Requirement (p.u.)
CHB-MLI [11,31]	$2 * (n_{level} - 1)$	0	$\frac{(n_{level}-1)}{2}$	0	-	VDC	$2 * (n_{level} - 1) * VDC$
NPC-MLI [72,73]	$2 * (n_{level} - 1)$	0	1	$(n_{level} - 1)$	No	VDC	$2 * (n_{level} - 1) * VDC$
FC-MLI [205]	$2 * (n_{level} - 1)$	0	1	$\frac{n_{level}}{2} * (nlevel - 1)$	No	$2 * VDC$	$2 * (n_{level} - 1) * VDC$
RVDC-MLI [1,2]	$3 * (n_{level} - 1)$	0	$\frac{.}{(n_{level} - 1)}{2}$	0	No	$2 * VDC$	$\frac{11}{4} * (n_{level} - 1) * VDC$
H-bridge MLI [31,45,51]	$2 * (\log_2 (n_{level} + 1))$	0	$(\log_2 (nlevel + 1) - 1)$	0	No	$\frac{n\ level-1}{2} * VDC$	$2 * (n_{level} - 1) * VDC$
SCU-MLI [151,205]	$3 * (\log_3 (\frac{n_{level}+1}{2})) + 4$	0	$\mathrm{Log}_3 (\frac{n_{level}+1}{2})$	$\log 3 * (\frac{n\ level+1}{2})$	Yes	$\frac{n\ level-1}{2} * VDC$	$\frac{11}{4} * (n_{level} - 1) * VDC$
DCC-MLI [1,2,133]	$\frac{5*(n_{level}*21)}{6}$	0	$\frac{.}{(n_{level} - 1)}{3}$	0	Yes	$3 * VDC$	$\frac{7*n_{level}-9}{2} * VDC$
CPCC-MLI [11,33,205]	$\frac{2*(n_{level}-1)}{3}$	$\frac{(n_{level}-1)}{3}$	$\frac{.}{(n_{level} - 1)}{2}$	0	No	$\frac{3*(n_{level}-7)}{N_{sw}}$	$\frac{10}{3} * (n_{level} - 1) * VDC$
CIC-MLI [11]	$\frac{2*(n_{level}+8)}{3}$	0	$\frac{(n_{level}-1)}{2}$	0	No	$2 * VDC$	$(3 * n_{level} - 7) * VDC$
Hybrid MLI [31,43,51]	$\frac{3*(n_{level}-1))}{4}$	$\frac{(n\ level-1)}{8}$	$\frac{(n_{level}-1)}{4}$	$\frac{(n_{level}-1)}{4}$	No	$2 * VDC$	$\frac{13}{8} * (n_{level} - 1) * VDC$
HERC-MLI [11,33,205]	$\frac{(3*n_{level}-1)}{2}$	1	$\frac{(n_{level}-1)}{2}$	0	No	$2 * VDC$	$\frac{15}{4} * (n_{level} - 1) * VDC$

Table 13. *Cont.*

Topology	Unidirectional Switches (N_{sw})	Bidirectional Switches	DC Sources (N_{DC})	Capacitors (N_{cap})	H-Bridge	Highest Switch Rating	Total Standing Voltage Requirement (p.u.)
CHB-MLI [11]	$(n_{level} + 1)$	0	1	$\frac{(n_{level}+1)}{2}$	No	$2 * VDC$	$(n_{level} + 3) * VDC$
SSSC-MLI [151]	$(5 * n_{level} - 1)$	0	1	$(n_{level} - 1)$	No	VDC	$(5 * n_{level} - 1) * VDC$
SADC-MLI [151,205]	$\frac{(n_{level}-1)}{3}$	$\frac{(n_{level}-1)}{12}$	$\frac{(n_{level}-1)}{4}$	0	No	$10 * VDC$	$\frac{9}{4} * (n_{level} - 1) * VDC$
CCS-MLI [33,205]	6	$\frac{(n_{level}-5)}{2}$	2	$\frac{(n_{level}-9)}{2} + 2$	No	$2 * VDC$	$\frac{1}{4} * (n_{level} - 1) * VDC$
RSC-MLI [205]	6	$\frac{(n_{level}-1)}{2}$	$\frac{(n_{level}-1)}{2}$	0	Yes	$2 * VDC$	$\frac{7}{2} * (n_{level} - 1) * VDC$

(' $*$ ' indicates the multiplication operation).

7. Reliability Assessment

Reliability assessment is the process of estimating a device's lifespan and chance of failure. Reliability is vital to a system's seamless operation. Manufacturing companies work with reliability analyses to build durable, high-performing, and low-maintenance goods. This idea of "reliability" includes various aspects for assessing a device's reliability. Figure 28 shows reliability categories and how to calculate system reliability [103,144,206,207].

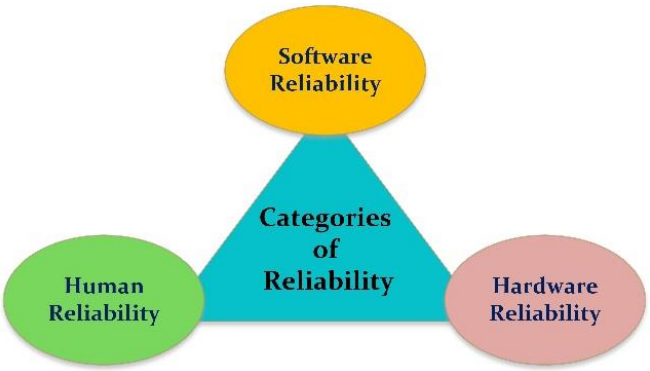


Figure 28. Reliability classifications.

Lifespan estimation is crucial, and a device's or part's lifespan can be estimated by calculating the mean time to failure. A high MTTF suggests reliability. The MTTF can be calculated using MIL-HDBK 217E. These standard handbooks will help calculate a device's failure rate (FR) and mean time between failures (MTTF). Reliability depends on several aspects. Figure 29 shows a system's reliability influence factors.

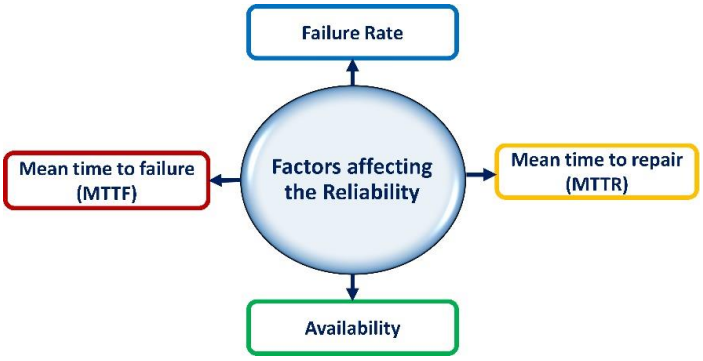


Figure 29. Reliability influence factors.

(a) Reliability

"Reliability" can be defined as the ability of an object to perform its intended function within specified conditions and time frames. This attribute is commonly assessed by quantifying the probability or frequency of failures.

(b) Failure

The system fails when it stops doing the requested task. Thus, the time it takes something to function without breaking down is frequently unpredictable. Failure can be quick or delayed. A sudden failure is called cataleptic failure.

(c) Failure Rate (FR)

The "failure rate" is a crucial aspect in the assessment of system reliability. The chance of failure at a specific moment can be determined by utilizing the "failure rate" function.

(d) Mean Time to Failure (MTTF)

The MTTF measures how long an item or system lasts, on average, before breaking down. This malfunction has rendered the device useless. The MTTF is often provided among components with hourly or thousand-hour service life requirements.

(e) Mean Time to Repair (MTTR)

The MTTR is the typical amount of time needed to repair broken equipment, and its value is directly proportional to the quantity of care it receives [103].

(f) Availability and Average Availability

Availability is the probability that a system will be functional at a particular moment.

The FR and MTTF are the most crucial metrics for this reliability analysis. As the FR is time invariant, it can be used to describe D(t) [103]. The FR is a statistical measure of the frequency with which a failure happens within a certain time frame. Combining the above failure rates, the exponential distribution is utilized to obtain the probability distribution function. The proportion of attempts that fail is also represented by "λ" as follows.

$$P\ (t, \lambda) = \lambda\ e^{-\lambda t} \tag{14}$$

The reliability function can be obtained from Equation (15):

$$D\ (t, \lambda) = e^{-\lambda t} \tag{15}$$

The failure in time (FIT) is a metric for estimating the "failure rate" which is defined as the average number of failures per time interval:

$$1\ \text{FIT} = 10^{-9}\ \text{failure/hour} \tag{16}$$

$$MTTF = \int_{0}^{+\infty} D(t)dt. \tag{17}$$

$$MTTF = \frac{1}{\lambda} \tag{18}$$

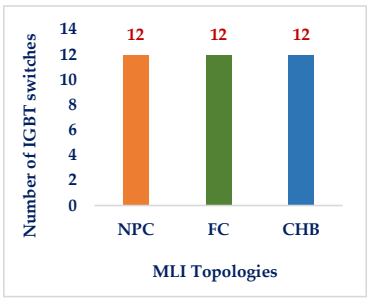
Using MIL-HDBK-217E specifications, Table 14 calculates FR [103]. Based on device counts, power electronic circuits can determine their MTTFT [103]. The MTTFT decreases as device numbers increase. The MTTFT increases with the component count. The inverter topologies are evaluated by the number of components needed. The reliability features (FR and MTTF) are calculated using the approximation technique [103] and summarized in Tables 14 and 15, as well as graphically represented in Figure 30.

Table 14. Failure rates of each component by using the approximation method [103].

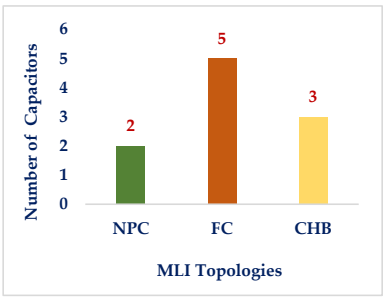
SI. No.	Components	Failure Rate (Failures/Hour)
1.	Switches	250×10^{-9}
2.	Diodes	100×10^{-9}
3.	Capacitors	300×10^{-9}

Table 15. Expected mean failure time for three standard inverters.

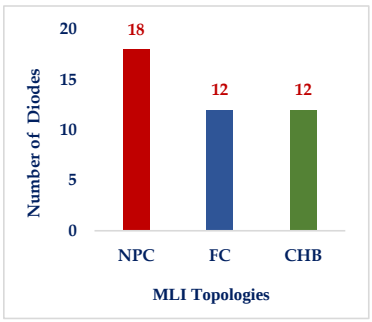
Components	NPC [103]	FC [103]	CHB [103]
IGBTs	4800 (12)	4800 (12)	1200 (12)
Capacitors	600 (2)	1500 (5)	1200 (3)
Diodes	1800 (18)	1200 (12)	1200 (12)
Total FITs	7200	7500	3600
Failure rate (failure/10^6 h)	7.2	7.5	3.6
MTTF (hours)	138,888	133,333	277,777



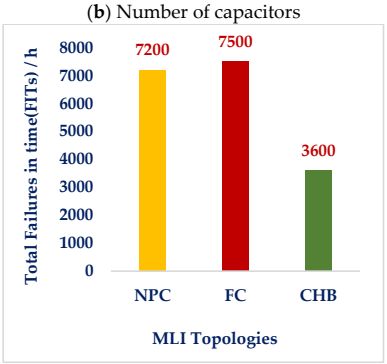
(**a**) Number of switches



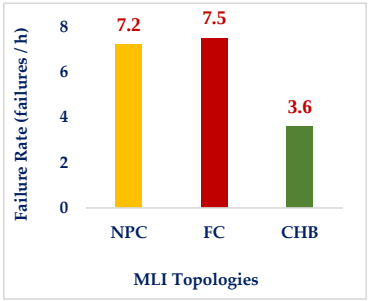
(**b**) Number of capacitors



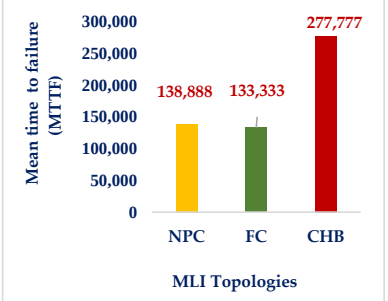
(**c**) Number of diodes



(**d**) Total failures in time



(**e**) Failure rate



(**f**) Mean time to failure

Figure 30. List of comparisons among three basic MLI topologies [103].

Calculation of the overall *MTTF* for power electronic circuits involves estimation of the cumulative failure rate of the constituent circuit parts. In order to obtain the total failure rate, denoted as λ_{Total}, it is necessary to multiply the number of components such as switches, diodes, and capacitors by their respective FR values, as specified in Equation (19):

$$\lambda_{Total} = (\lambda_S \times N_{SWT}) + (\lambda_D \times N_{DIO}) + (\lambda_C \times N_{CAP}) \quad (19)$$

The total *MTTF* of the circuit can be calculated by Equation (20):

$$MTTF_{Total} = \frac{1}{\lambda_{Total}} \quad (20)$$

The *MTTF* of power electronic circuits can be determined by considering the number of device counts. When there are a large number of device counts, the related total mean time to failure ($MTTF_{Total}$) is reduced. A higher $MTTF_{Total}$ is observed when the number of components is lower. In this study, the main aim is to evaluate the average duration of inverter topologies by considering the number of components needed for every individual topology.

8. Challenges and Recommendations

The utilization of renewable energy systems in power grids has been enhanced due to advancements in power electronics devices and related technologies. However, challenges remain pertaining to electricity quality, grid reliability, and security. In order to ensure the quality of grid power, a multitude of standards and guidelines have been established for grid-connected RES. Based on the reviewed literature, it is understood that additional research is required in the following areas:

Challenges:

- The evaluation of the performance of these novel topologies in grid-integrated applications is imperative, as the majority of them have not yet been examined in the context of grid-connected Renewable Energy Sources (RESs).
- MLI control and modulation systems should be more robust, flexible, and fault tolerant.
- In recent times, researchers and industries have begun to develop hybrid topologies in order to successfully address power quality challenges and to meet demanding grid standards in a cost-efficient manner.
- More research is needed on quantitative approaches for solving MLI nonlinear systems.
- New voltage balancing techniques must be employed in MLIs to minimize capacitor size and to increase inverter power density.
- Resonant converters with single DC source MLIs are suggested.
- It is imperative for smart grid systems to include the integration of microgrid load interactions with MLIs as an essential component.
- However, because of the lower TSV, new RSC-MLI topologies need to be created to boost their appropriateness for both solar PV and wind energy integration.
- Renewable energy sources are increasingly evolving towards a future smart grid as they are integrated into networks utilizing appropriate MLIs, and for MLI topology creation and control, this poses considerable hurdles. There have been many breakthroughs in this sector.

Recommendations:

- The roadmap in Figure 31 shows SC-MLIs' future progress. In addition to exploring new topologies with higher voltage conversion gain, future SC-MLIs can consider factors such as fewer switching devices, reduced MVS and TSV index across switches, improved performance during high pulsating inrush current, and lower cost.
- A modern MLI performance analysis for many practical applications cannot measure all failure prediction parameters and limits the ageing information of PV inverters. Hence, Figures 32 and 33 are the proposed and future road maps for the reliability study of PV inverters.

- In grid-connected solar PV systems, safe and reliable operation of the multilevel inverter depends on the use of suitable safety mechanisms and control strategies, which are listed in Table 16.

Table 16. Grid-fault challenges and recommendations for multilevel inverters in grid-connected solar PV systems.

Grid-Fault Conditions (Challenges)	Multilevel Inverter Response (Recommendations)
Overvoltage [34,163]	• The output voltage magnitude can be controlled by reducing the modulation index • Enable voltage regulation control
Under voltage [34,163]	• The output voltage magnitude can be controlled by reducing the modulation index • Reactive power injection is required to maintain grid voltage
Frequency deviation [34,163,194]	• The output frequency of the inverter can be adjusted by activating the frequency control loop • Frequency adaptive control algorithms are activated
Voltage sag [163,194]	• Voltage support methods, such as reactive power injection, can be used • Inverter may maintain grid voltage by drawing power from DC-link capacitors • Dynamic voltage restorer support during sag periods
Voltage swell [163,194]	• Inverter reduces the output voltage to mitigate excessive power generation during the swell
Grid disconnect [163,194]	• Inverter switch.hes to island mode (if applicable) and operates as a stand-alone system or shuts down safely • Reconnection to the grid after stabilization
Short circuit [34,163,194]	• In order to eliminate faults and restore inverter functionality, fast disconnect and reconnect procedures are required • Short-circuit protection algorithms activated
Grid outage [34,163,194]	• Inverter disconnects from the grid to ensure islanding protection • May switch to an internal control mode to provide power to local loads
Harmonic distortion [34,163,194]	• Activate harmonic filtering control to mitigate harmonics in inverter output • Implement active and passive filtering strategies to mitigate harmonics

Figure 31. Perception evaluation and future development of SC-MLIs.

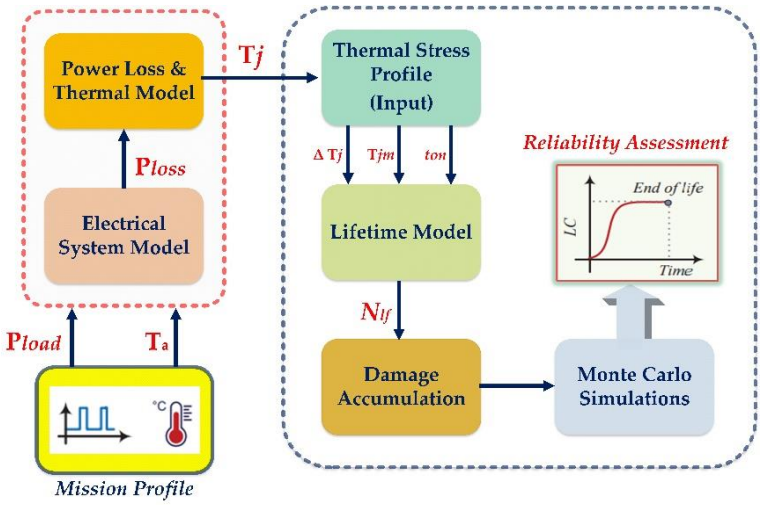


Figure 32. Monte Carlo-based reliability study of PV inverters [103].

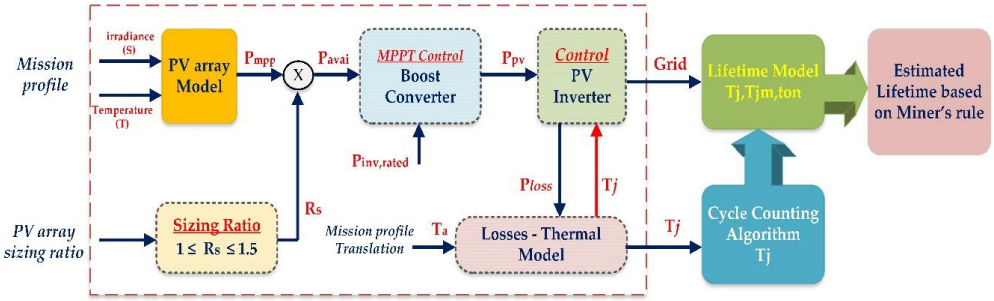


Figure 33. PV system mission profile translation diagram by PV array size ratio Rs consideration [103].

9. Conclusions

This review provides an efficient summary of multilevel inverters to emphasize the necessity for new or modified multilevel inverters for grid-connected sustainable solar PV systems. Firstly, this review presented a detailed survey of reduced switch count multilevel inverter (RSC-MLI) topologies, including their designs, typical features, limitations, assessment parameters, and selection for particular applications. Secondly, this review presented a comprehensive analysis of MLIs and a classification of the existing MLI topologies, along with their merits and demerits. Thirdly, this review also included a survey of SC-MLI topologies with a qualitative assessment to aid in the direction of future research due to their variety of applications such as inductor-less or transformer-less operation, enhanced voltage output, improved voltage regulation, low cost, reduced circuit components, size, and less electromagnetic interference. Lastly, this review serves as a valuable resource for

engineers and researchers because it provides a detailed look at parametric comparisons of the total number of power semiconductor switches, DC sources, passive elements, total standing voltage, reliability assessment, applications, challenges, and recommendations.

Author Contributions: Conceptualization and methodology, S.N.; validation, D.C.; formal analysis, S.N.; investigation, D.C.; resources, D.C.; data curation, S.N.; writing—original draft preparation, S.N.; writing—review, S.N.; editing, D.C.; visualization, D.C.; supervision, D.C.; project administration, D.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: This review has no information related to it.

Acknowledgments: The authors further thank the Vellore Institute of Technology in Vellore, India, for their assistance and also the authors wish to thank the particular copyright holders for allowing approval to use the pictures, graphics, tables, and figures in this work.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

MLIs	Multilevel inverters
RES	Renewable energy sources
NPC	Neutral point clamped
SC-MLI	Switched-capacitor multilevel inverters
DC-MLI	Diode-clamped multilevel inverters
DCC	Developed cascaded cell based
PUC	Packed U-cell
N_{SWT}	Number of switches
N_{DCS}	Number of DC sources
N_L	Number of levels
N_{DIO}	Number of diodes
N_{CAP}	Number of capacitors
N_{DK}	Number of driver circuits
TSV_{PU}	Total standing voltage per unit
CF/L	Cost function
FCC/L	Component count factor per level
CHB-MLI	Cascaded H-bridge multilevel inverter
PV	Photovoltaic
SDCS	Separate DC source
MPPT	Maximum power point tracking
THD	Total harmonic distortion
EMI	Electromagnetic interference
MMC	Modular multilevel converter
FC-MLI	Flying-capacitor multilevel inverter
CSD	Cascaded switched diode
CPCC	Cascaded predictive current control
CCHB	Cross-connected half-bridges
CCS	Cross-connected source based
MCSI	Multilevel current-source inverter
ASD	Adjustable speed drives
AFC	Active front-end converters
CPD	Custom power devices
ANPC	Active neutral point clamped
ABNPC	Active boost neutral point clamped
PWM	Pulse width modulation
CGSC	Common-grounded switched-capacitor
FACTS	Flexible alternating current transmission systems

MLDCL	Multilevel DC-link
SSPS	Switched series-parallel sources
SPSC	Series–parallel switched-capacitor
SSSC	Single-source switched-capacitor
SADC	Symmetric–asymmetric DC sources based
RV	Reverse voltage
RVDC-C	Reduced variety of DC voltage sources based cascaded
HERC-C	Highly efficient and reliable configuration based cascaded
SCSS	vSeries-connected switched sources
SCU	Switched-capacitor Unit
MLM	Multilevel module
HBSC	Half-bridge switched-capacitor
SCC	Switched-capacitor converters

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