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A Robust Control Scheme for Dynamic Voltage Restorer with Current Limiting Capability

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Abstract: In this paper, a second order sliding mode control scheme is utilized for outer voltage loop of a three-phase fault current limiter-based dynamic voltage restorer (FCL-DVR) instead of a conventional proportional integral/proportional resonance (PI/PR) controller. The new control strategy improves the dynamic performance of the FCL-DVR against voltage distortion. Furthermore, by using the proposed robustness controller, the FCL-DVR can smoothly switch between the FCL and DVR operation modes. Compared with other existing control schemes, the proposed control strategy for the FCL mode can still work well under a large fault current. The MATLAB/Simulink simulation results demonstrate that the proposed control strategy is robust to voltage harmonics, sag and swell. They also show that the proposed control scheme can effectively limit the fault current in different scenarios.

Keywords: fault current limiter-based dynamic voltage restorer (FCL-DVR); grid-side converter (gsc); nonlinear control scheme; second-order sliding mode control

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1. Introduction

Power quality issues such as voltage dip, voltage swell, unbalance, and harmonic pollution are the main concerns of power grids [1,2]. Nowadays, the integration of the large scale of renewable energy and other nonlinear loads further deteriorates these voltage-relevant power quality issues [3,4]. At present, a variety of voltage compensation devices have developed for the suppression of voltage-relevant power quality issues [5]. Among these devices, the dynamic voltage restorer (DVR) is favored because of its resistance to voltage dip, voltage swell, and harmonic disturbances [6]. Short circuit faults are another significant concern of power grids as they can impact the stability and safety of power grid significantly. To protect the electrical equipment from load faults, protection schemes are always implemented. Fuses, circuit breakers, bypass circuits, and fault current limiters (FCLs) are the most common types of protection schemes [7]. Fuses are cheap, small and reliable, but are disposable and require manual replacement, so are always used in low voltage systems that do not require high power supply reliability [8]. Circuit breakers, on the other hand, are the most commonly used protection devices, and can be repeatedly used and automatically reset, but have the disadvantages of larger size, higher price and the requirement of frequent maintenance [9]. Bypass circuits such as fast mechanical or solid-state switches can also be used to protect series compensation devices during a fault [10]. However, their performance against large fault currents is poor, meaning that the fault can still cause damage to electrical equipment. FCLs, compared with the above-mentioned protection devices, have the advantage of low loss, quick response and fast recovery. Therefore, FCLs have been an attractive choice for power industries [11,12].

Based on above description, it is natural to consider combining FCLs and DVRs to form a fault current limiter-based dynamic voltage restorer (FCL-DVR), which can suppress the voltage-relevant power quality issues and limit the load current at the same time. At present, there are a few FCL-DVR schemes proposed in existing publications [13–15]. One

study [13] introduces a double functional type FCL-DVR, which can not only compensate voltage but also limit load current. This scheme limits the fault current mainly by a filter inductor, and, as a result, it is not appropriate for a large fault current. Another study [14] further proposes a bridge-type FCL-DVR, which can maintain good performance for large fault currents. Nevertheless, the power loss of the bridge-type FCL-DVR is very high, and the control scheme is relatively complex. To reduce the power loss, an energy-efficient FCL-DVR is presented in [15], but this type of scheme relies on a very complex control scheme because the shunt and series converter need to switch control schemes when the FCL-DVR changes its operating mode. In [16], a model predictive control scheme is present for the UPQC-FCL, where the system can smoothly switch between the FCL and UPQC modes. However, the number of switches of the topology is relatively high. In [17], an FCL-DVR with a reduced number of components (six switches) is present, while the total power losses cannot be neglected.

From Table 1, the proposed FCL-DVR system can compensate the voltage sag/swell and limit the fault currents simultaneously. Additionally, the power loss of the proposed system is very low when compared with the system in [13,17].

Table 1. Comparison results with other FCL systems.

Reference	Number of Line Transformers	Number of Switches in 3 Phase	Power Losses	Compensation Voltage Sag	Limiting Fault Current Ability
[13]	2	24	High	yes	yes
[16]	0	34	N/A	yes	Yes
[17]	1	6	Medium	yes	yes
Proposed system	1	12	N/A	yes	yes

Accordingly, a smooth control scheme for an FCL-DVR is still desired. Generally, a proportional resonance (PR) controller is enough to mitigate the grid voltage harmonics in the FCL-DVR due to its good performance in tracking the sinusoidal quantity [13]. To improve the dynamic performance of DVR, J. Li, et al. have proposed an observer-based adaptive control scheme for a UPS system [18], which performs well under distorted load currents. In [16], a model predictive control scheme is presented to smooth the switching process between the FCL and UPQC modes. However, the switching frequency is not fixed in the proposed model's predictive control. In addition, due to the advantages of the convergence in finite time, suppression of smooth disturbances of arbitrary shape and suppression of chattering, the second order sliding model control has been widely used in power electronics [19,20]. In [21], a super twisting sliding mode control is used in the DVR, where good dynamic performance and good load voltage quality are achieved under a distorted grid voltage. However, the above control schemes are not applicable when the FCL-DVR switches between the FCL and DVR modes.

Accordingly, a three-phase FCL-DVR with second-order sliding mode control scheme is designed in this paper. The proportional integral/proportional resonance (PI/PR) regulator for the outer voltage loop in series converter of the FCL-DVR is replaced by a second-order sliding mode control scheme while the PI/PR regulator for the inner current loop is kept. The control scheme of the series converter in FCL-DVR is switched in FCL or DVR modes while the control scheme of the shunt converter always remains unchanged. The new FCL-DVR control is extremely robust to external disturbances and can effectively suppress the vibration caused by the switching function. The simulation experiments confirm the effectiveness of the designed second-order sliding mode nonlinear controller.

In summary, the main contributions are listed as follows:

1. A smooth control scheme is presented for the series and shunt converter of an FCL-DVR, where the frequent switching of control schemes can be avoided.

2. A second-order sliding mode control scheme is proposed to improve the robustness of the FCL-DVR system. The stability analysis of the proposed controller is introduced.

2. Operation Principle of FCL-DVR

2.1. Topology of FCL-DVR

A typical FCL-DVR is shown in Figure 1. As one can see, the FCL-DVR system mainly consists of a series converter (made up of a three-phase voltage source converter), a shunt converter (made up of a three-phase voltage source converter), a line frequency transformer, filters on the AC sides of two converter and a DC-link capacitor. The series converter is connected to load through the fundamental frequency transformer, which mainly aims at compensating voltage and limiting current. The shunt converter connects to the power grid, which mainly provides the energy absorbed or released by the series converter under voltage compensation mode or current limiting mode.

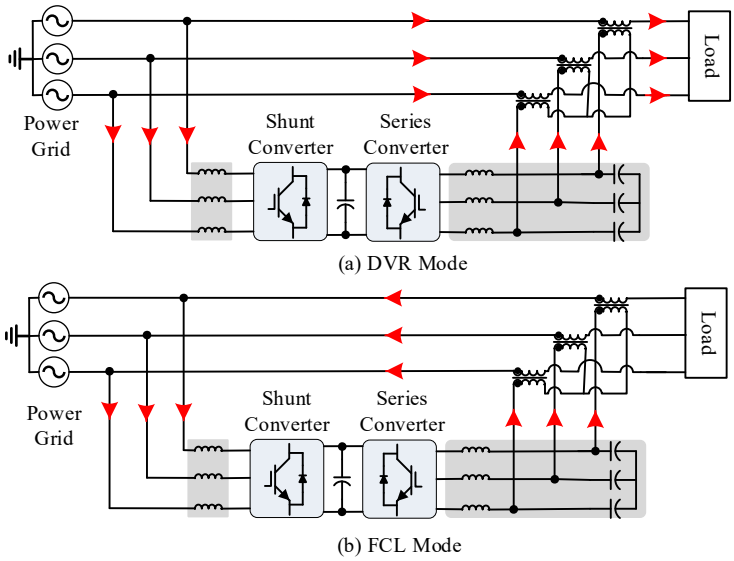

Figure 1. Topology of the three-phase FCL-DVR.

2.2. FCL-DVR Operation Mode

According to the operating principle of the FCL-DVR, its operation mode can be categorized into three types.

2.2.1. Normal Operation Mode

An FCL-DVR will work in the normal operation mode when there are no power grid voltage disturbances and load faults.

2.2.2. DVR Operation Mode

The series converter will work in the DVR operation mode when there are voltage dips, voltage swells, or harmonic disturbances. It will inject voltage into the grid side to maintain the load voltage. Meanwhile, the shunt converter provides the required power for the normal operation of the series converter. Under the DVR mode, the power grid will supply the load, where the currents direction of the FCL-DVR system is seen in Figure 1a.

2.2.3. The FCL Operation Mode

The series converter on the faulted phase works in the current source mode to limit the fault current, while the series converter on the normal phases works as a voltage source to maintain the load voltage. In all likelihood, the shunt converter will still provide the required power for the normal operation of the series converter. Under the DVR mode, the

power grid will supply the load, where the current direction of the FCL-DVR system is seen in Figure 1a.

3. Mathematical Model of FCL-DVR

The equivalent circuit of the FCL-DVR is shown in Figure 2. According to Figure 2, the mathematical model of the series converter in the ABC frame can be established as follows:

$$\begin{cases} C_{\mathrm{se}}\frac{dv_{\mathrm{sea}}}{dt} = i_{\mathrm{se}a} - i_{\mathrm{Sa}} \\ C_{\mathrm{se}}\frac{dv_{\mathrm{seb}}}{dt} = i_{\mathrm{se}b} - i_{\mathrm{Sb}} \\ C_{\mathrm{se}}\frac{dv_{\mathrm{sec}}}{dt} = i_{\mathrm{sec}} - i_{\mathrm{Sc}} \\ L_{\mathrm{se}}\frac{di_{\mathrm{sea}}}{dt} = -R_{\mathrm{se}}i_{\mathrm{se}a} - v_{\mathrm{se}a} + v_{\mathrm{i}a} \\ L_{\mathrm{se}}\frac{di_{\mathrm{seb}}}{dt} = -R_{\mathrm{se}}i_{\mathrm{se}b} - v_{\mathrm{se}b} + v_{\mathrm{i}b} \\ L_{\mathrm{se}}\frac{di_{\mathrm{sec}}}{dt} = -R_{\mathrm{se}}i_{\mathrm{sec}} - v_{\mathrm{sec}} + v_{\mathrm{ic}} \end{cases} \tag{1}$$

where $v_{\mathrm{sec}}(x(\{a,b,c\}))$ represents the voltage injected into the power grid; i_{Sx} is the grid current; i_{sex} represents series converter's filter inductor current for the series converter. v_{ix} represents the output voltage of the series-side converter; L_{se} and C_{se} represent the filter inductance and the filter capacitance of the series converter's front-end filter; and R_{se} is the equivalent resistance.

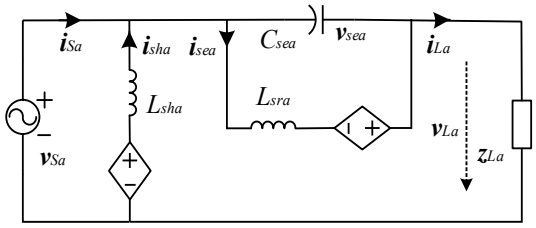

Figure 2. FCL-DVR system A phase equivalent circuit.

According to Kirchhoff's law, the relationship between load voltage and power grid voltage can be written as:

$$\begin{cases} v_{\mathrm{L}a} = v_{\mathrm{S}a} + v_{\mathrm{Se}a} \\ v_{\mathrm{L}b} = v_{\mathrm{S}b} + v_{\mathrm{Se}b} \\ v_{\mathrm{L}c} = v_{\mathrm{S}c} + v_{\mathrm{Sec}} \end{cases} \tag{2}$$

where v_{sx} and v_{Lx} represent the grid voltage and load voltage, respectively.

4. Second-Order Sliding Mode Control Scheme of FCL-DVR

The FCL-DVR is mainly used to maintain the load voltage's frequency, magnitude, and balance in DVR mode and also to limit load fault current in FCL mode. This section introduces a second-order sliding mode control scheme to improve FCL-DVR's dynamic features under DVR and FCL modes. The control diagram for the FCL-DVR is shown in Figure 3.

In the DVR mode, the load voltage should be controlled as:

$$\begin{cases} v^*_{\mathrm{L}a} = V_{\mathrm{L}}\sin(\omega t) \\ v^*_{\mathrm{L}b} = V_{\mathrm{L}}\sin\left(\omega t - \frac{2}{3}\pi\right) \\ v^*_{\mathrm{L}c} = V_{\mathrm{L}}\sin\left(\omega t + \frac{2}{3}\pi\right) \end{cases} \tag{3}$$

where v_L represents the desired load voltage amplitude, which is equal to the rated power grid voltage. ωt represents the phase angle of the power grid voltage.

In the FCL operation mode, the inductor current is controlled as:

$$\begin{cases} i^*_{sea} = I_{se}\sin(\omega t) \\ i^*_{seb} = I_{se}\sin\left(\omega t - \frac{2}{3}\pi\right) \\ i^*_{sec} = I_{se}\sin\left(\omega t + \frac{2}{3}\pi\right) \end{cases} \tag{4}$$

where I_{se} represents the desired value of the inductor current.

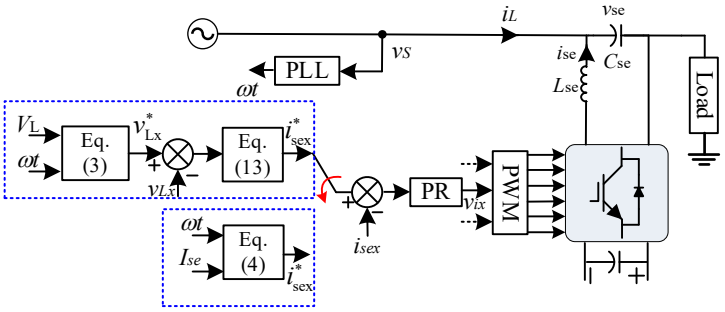

Figure 3. Control block diagram of FCL-DVR.

4.1. Design of Second-Order Sliding Mode Controller of Outer Voltage Control Loop

4.1.1. Design of the Integral Sliding Surface of the Outer Voltage Control Loop

According to (1)–(2), the dynamics of the FCL-DVR load voltage can be described as:

$$\frac{dv_{La}}{dt} = \frac{1}{C_{se}}\left(i_{sea} - i_{Sa} + C_{se}\frac{dv_{Sa}}{dt}\right) \tag{5}$$

Define the tracking error as:

$$e_{La} = v_{La} - v^*_{La} \tag{6}$$

where * represents the reference value of the corresponding variable.

According to (5), the integral sliding surface of the DC voltage is designed as:

$$s_{La} = e_{La} + \lambda_{La}\int e_{La}dt \tag{7}$$

where λ_{La} represents a positive sliding mode coefficient.

4.1.2. Design of the Outer Voltage Loop's Control Law

Super-twisting algorithm (STA) [22–24] has the advantages of restraining vibration and quick convergence and has therefore been widely used in systems with relative order 1. In the double-closed control loop of FCL-DVR, the outer voltage loop provides reference value I^*_{sea} of inductor current for current control loop. To realize the second-order sliding mode control, the global control law I^*_{sea} mainly includes the equivalent control term and STA term. Therefore, the global control law can be defined as follows:

$$I^*_{sea} = I_{sea(eq)} + I_{sea(st)} \tag{8}$$

Equivalent control term can be obtained by solving the following equation

$$\dot{S}_{La} = 0 \tag{9}$$

Combine (5), (7) and (9), and the equivalent control terms can be expressed as:

$$I_{sea(eq)} = C_{se}\left(\dot{v}^*_{La} - \lambda_{La}e_{La} - \frac{dv_{Sa}}{dt}\right) + i_{Sa} \tag{10}$$

where the STA item can be designed as follows:

$$I_{\mathrm{se}a(\mathrm{st})} = C_{\mathrm{se}} u_{\mathrm{st}} \tag{11}$$

$$\begin{cases} u_{\mathrm{st}} = -\varepsilon_{1a} |s_{\mathrm{L}a}|^{\frac{1}{2}} \mathrm{sgn}(s_{\mathrm{L}a}) + \rho_{\mathrm{L}a} \\ \dot{\rho}_{\mathrm{L}a} = -\varepsilon_{2a} \mathrm{sgn}(s_{\mathrm{L}a}) \end{cases} \tag{12}$$

where ε_{1a} and ε_{2a} represent the positive constant, $\mathrm{sgn}(\cdot)$ represents the symbol function.

Substituting (11) and (12) into (8), the expression of the reference current for the inner current control loop of DVR can be expressed as:

$$I_{\mathrm{se}a(\mathrm{eq})} = C_{\mathrm{se}} \left(\dot{v}^{*}_{\mathrm{L}a} - \lambda_{\mathrm{L}a} e_{\mathrm{L}a} - \frac{dv_{\mathrm{S}a}}{dt} \right) + i_{\mathrm{S}a} - C_{\mathrm{se}} \varepsilon_{1a} |s_{\mathrm{L}a}|^{\frac{1}{2}} \mathrm{sgn}(s_{\mathrm{L}a}) - C_{\mathrm{se}} \varepsilon_{2a} \int \mathrm{sgn}(s_{\mathrm{L}a}) \tag{13}$$

The control law for phase B and phase C can be obtained in the same manner.

4.1.3. Stability Analysis

Considering the internal disturbance and external disturbance, (5) can be rewritten as:

$$\frac{dv_{\mathrm{L}a}}{dt} = \frac{d\hat{v}_{\mathrm{L}a}}{dt} + d \tag{14}$$

where d represents the total disturbance, and $\hat{}$ represents the rated values of corresponding variables. Due to the physical constraints of the practical system, it can be assumed that there is a boundary for the perturbation, that is:

$$|d| < \varepsilon \tag{15}$$

Substitute (14) into (7), then the first-order differential of the integral sliding mode surface s_{La} can be rewritten as [8]:

$$\dot{s}_{\mathrm{L}a} = \dot{e}_{\mathrm{L}a} + \lambda_{\mathrm{L}a} e_{\mathrm{L}a} = \dot{\hat{e}}_{\mathrm{L}a} + \lambda e_{\mathrm{L}a} + d \tag{16}$$

Therefore, substitute (13) into (16), then the closed-loop system can be described as:

$$\begin{cases} \dot{s}_{\mathrm{L}a} = -\varepsilon_{1a} |s_{\mathrm{L}a}|^{\frac{1}{2}} \mathrm{sgn}(s_{\mathrm{L}a}) + \rho_{\mathrm{L}a} + d \\ \dot{\rho}_{\mathrm{L}a} = -\varepsilon_{2a} \mathrm{sgn}(s_{\mathrm{L}a}) \end{cases} \tag{17}$$

To inspect the stability of the closed-loop system, the Lyapunov function [24] is designed as follows:

$$\begin{aligned} V &= 2\varepsilon_{2a} |s_{\mathrm{L}a}| + \tfrac{1}{2} \rho_{\mathrm{L}a}^2 + \tfrac{1}{2} \left[\varepsilon_{1a} |s_{\mathrm{L}a}|^{0.5} \mathrm{sgn}|s_{\mathrm{L}a}| - \rho_{\mathrm{L}a} \right]^2 \\ &= \boldsymbol{\xi}_a^T \mathbf{P}_a \boldsymbol{\xi}_a \end{aligned} \tag{18}$$

where

$$\boldsymbol{\xi}_a = \begin{bmatrix} |s_{La}|^{\frac{1}{2}} \mathrm{sgn}(s_{La}) \\ \rho_{La} \end{bmatrix}$$

$$\mathbf{P}_a = \frac{1}{2} \begin{bmatrix} 4\varepsilon_{2a} + \varepsilon_{1a}^2 & -\varepsilon_{1a} \\ -\varepsilon_{1a} & 2 \end{bmatrix}$$

then, the differential of Lyapunov function V can be calculated as (19)

$$\dot{\mathbf{V}} = -\frac{1}{|s_{La}|^{\frac{1}{2}}} \boldsymbol{\xi}_a^T \mathbf{Q}_a \boldsymbol{\xi}_a + \frac{d}{|s_{La}|^{\frac{1}{2}}} \mathbf{q}_a^T \boldsymbol{\xi}_a \tag{19}$$

where

$$\mathbf{Q}_a = \frac{\varepsilon_{1a}}{2}\begin{bmatrix} 2\varepsilon_{2a} + \varepsilon_{1a}^2 & -\varepsilon_{1a} \\ -\varepsilon_{1a} & 1 \end{bmatrix}$$

$$\mathbf{q}_a = \frac{\varepsilon_{1a}}{2}\begin{bmatrix} 2\varepsilon_{2a} + 0.5\varepsilon_{1a}^2 \\ -0.5\varepsilon_{1a} \end{bmatrix}$$

In practice, there is a boundary for the perturbation $|d| < \varepsilon$, and, according to [24], (19) can be further written as:

$$\dot{\mathbf{V}} \leq -\frac{1}{|s_{La}|^{\frac{1}{2}}}\boldsymbol{\xi}_a^T \boldsymbol{\Lambda}_a \boldsymbol{\xi}_a \tag{20}$$

where

$$\boldsymbol{\Lambda}_a = \frac{\varepsilon_{1a}}{2}\begin{bmatrix} 2\varepsilon_{2a} + \varepsilon_{1a}^2 - \left(\frac{4\varepsilon_{2a}}{\varepsilon_{1a}}\right)\varepsilon & -(\varepsilon_{1a} + 2\varepsilon) \\ -(\varepsilon_{1a} + 2\varepsilon) & 1 \end{bmatrix}$$

To ensure the stability of the designed controller, a matrix $\boldsymbol{\Lambda}_a$ should be designed as a positive semidefinite matrix to ensure $\dot{\mathbf{V}} \leq 0$. Therefore, the following conditions should be satisfied:

$$\begin{cases} \varepsilon_{1\mathrm{d}} > 2\varepsilon \\ \varepsilon_{2\mathrm{d}} > \varepsilon_{1\mathrm{d}}\frac{5\varepsilon_{1\mathrm{d}}\varepsilon + 4\varepsilon^2}{2(\varepsilon_{1\mathrm{d}} - 2\varepsilon)} \end{cases} \tag{21}$$

4.1.4. Parameters of the Sliding Mode Control

The second-order sliding mode controller for the outer voltage loop in FCL-DVR mainly includes three sliding mode coefficients: λ_{La}, ε_{1a} and ε_{2a}. As can be seen from Formula (6), the coefficient λ_{La} has a direct impact on the dynamic response of the closed-loop system. A large λ_{La} leads to a fast dynamic response, but will easily cause an overshoot; A small λ_{La} will slow the dynamic response of the system. Therefore, the coefficient λ_{La} must be selected reasonably. The principle of the selection of λ_{La} has been introduced in [18]. Additionally, in order to ensure the stability of the designed controller, ε_{1a} and ε_{2a} can be determined by (21).

4.2. Design of Inner Current Loop's PR Controller

The main objectives of the inner current loop include: (1) the stable tracking of the output of the load voltage in the DVR mode, to achieve the goal of maintaining the load voltage stability; (2) In FCL mode, the desired inductor current's reference value is tracked to limit the load fault current. In order to track inductive current reference, the current inner ring uses a PR controller, which can be written as:

$$G_{PR}(s) = k_p + \frac{k_r s}{s^2 + (hw)^2} \tag{22}$$

where k_p and k_r represent the controller gain. The PR regulator is able to adjust the current error in a steady-state mode at zero, in the h-order harmonic frequency. Integration is performed using the proportional gain k_p and resonant gain k_i, where the resonant component is a quadratic resonance filter with resonant frequency equal to hw with zero damping coefficient and can be used to determine the selectivity of the filter. In practice, the bandwidth can be expanded to reduce sensitivity to frequency changes in the grid. In addition, the detailed parameters design is shown in [25].

5. Simulation Results

MATLAB/Simulink simulations are conducted in this section to verify the correctness and effectiveness of the proposed second-order sliding mode control scheme. The parameters of the FCL-DVR and its control setting are listed in Tables 2 and 3, respectively. As a comparison, the simulation results for an FCL-DVR with conventional PR regulator are also presented.

Table 2. The FCL-DVR parameters used for the simulation.

Parameters	Values
Grid voltage	380 V
Grid angular frequency	314 rad/s
Series converter's filter capacitance	80 μF
Series converter's filter inductance	6 mH
DC capacitance	4000 μF
DC voltage	800 V
Grid equivalent resistance	0.5 Mh
Load resistance	10 kHz

Table 3. Control parameters used for the simulation.

Control Parameters	Values
Second-order sliding mode controller	
λ_{La}	46
ε_{1a}	6173
ε_{2a}	2.162×10^6
PR controller	
k_p	2
k_r	800

Figures 4 and 5 show the simulation results of the FCL-DVR with the proposed second-order sliding mode controller under the distorted grid voltage, and they include the grid voltage v_s, load voltage v_L, and series injected voltage v_{se}. As seen in Figure 4, when the grid voltage is distorted, the DVR injects a compensation voltage into the power grid through the series converter. With the compensation of the series converter, the grid voltage contains small harmonics so that it remains a sinusoidal signal. Figure 5 presents the simulation results of the three-phase FCL-DVR with conventional PR regulator under distorted voltage. The results in Figure 5 indicate the conventional PR control scheme cannot guarantee a sinusoidal load voltage when the grid voltage is distorted within [0.1, 0.14] s. Hence, the results verify that the proposed second-order sliding mode controller is superior to the conventional PI/PR controller in terms of restraining the harmonic distortion.

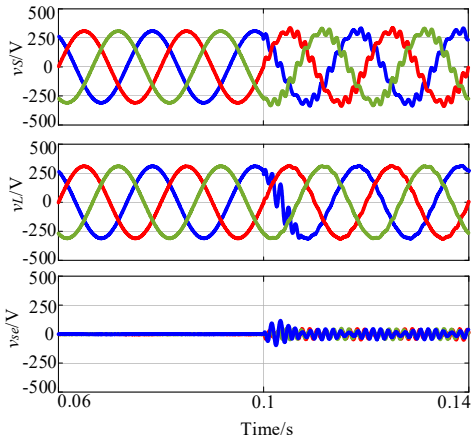

Figure 4. Simulation waveform of FCL-DVR under the second-order sliding mode control scheme under distorted grid voltage.

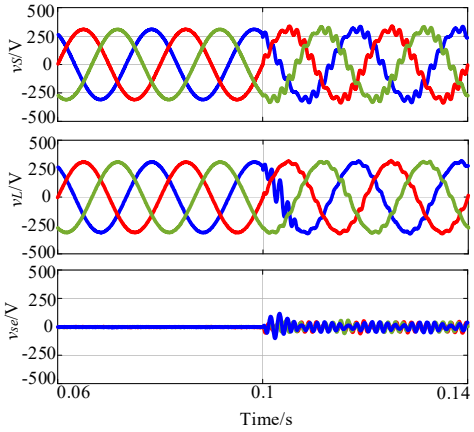

Figure 5. Simulation waveform of FCL-DVR under the PR scheme under distorted grid voltage.

Figures 6 and 7 show the simulation results of three-phase FCL-DVRs with second-order sliding mode controller and PR controller in a grid with a voltage dip and voltage swell. As seen from these two figures, both control schemes result in sinusoidal, balanced, and constant-magnitude voltages after short transients. Nevertheless, the proposed second-order sliding mode controller reduces the transient time and the overshooting compared with the conventional PR control at 0.1 and 0.14s. Therefore, the proposed second-order sliding mode controller has a better dynamic feature.

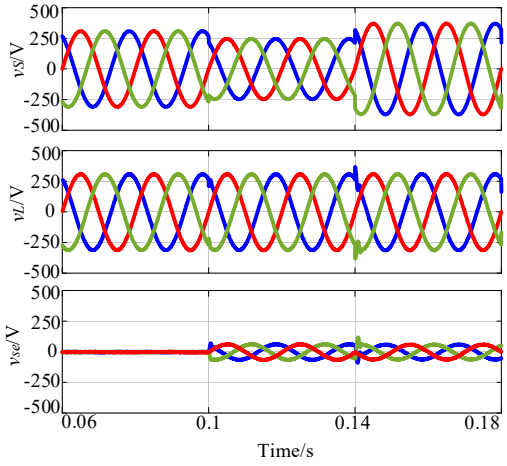

Figure 6. FCL-DVR simulation waveform under the second-order sliding mode control scheme during the power grid voltage sag and temporary swell.

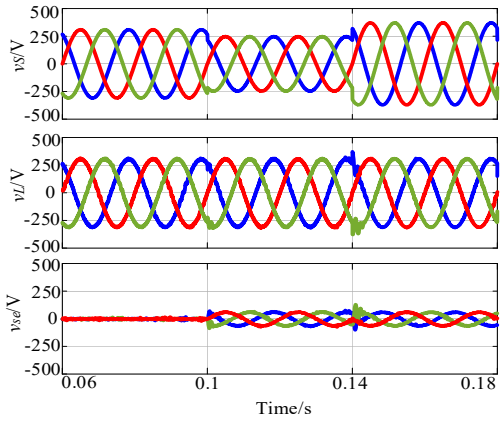

Figure 7. Simulation waveform of FCL-DVR under PR scheme during temporary voltage sag and temporary swell.

Figure 8 illustrates the simulation results of the FCL-DVR under a phase-A fault. One can see from the figure that the three-phase FCL-DVR switches from the DVR mode to the current limiter mode at 0.1 s after the phase-A fault occurs. In such a condition, the phase-A load voltage reduces to almost 0 because phase A is shorted. As a result, the load current is contained to the desired values. When the fault disappears, the three-phase FCL-DVR will switch back to DVR mode, and the load voltage and current return to normal.

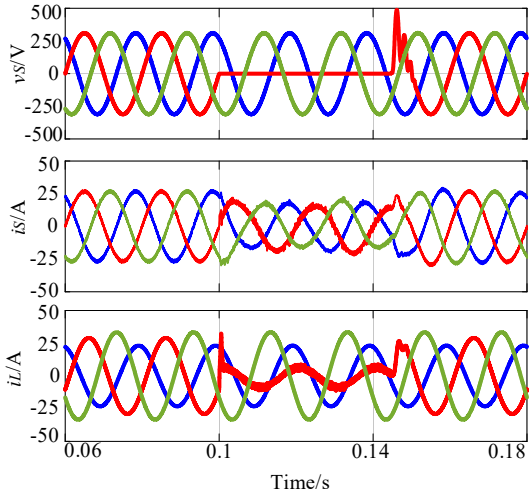

Figure 8. A Simulation waveform of FCL-DVR during phase ground failure.

Figure 9 gives the simulation of a three-phase FCL-DVR under three-phase grounding fault. The figure indicates that the three-phase FCL-DVR will switch from the DVR mode to current limiter mode at 0.1 s after the three-phase grounding fault is detected. For such a case, the load voltage for three phases reduces to almost 0, and, as a result, grid current declines to almost 0, and the load current is maintained at desired values. After the fault disappears, the three-phase FCL-DVR will switch back to DVR mode, and the load voltage and current will return to normal values.

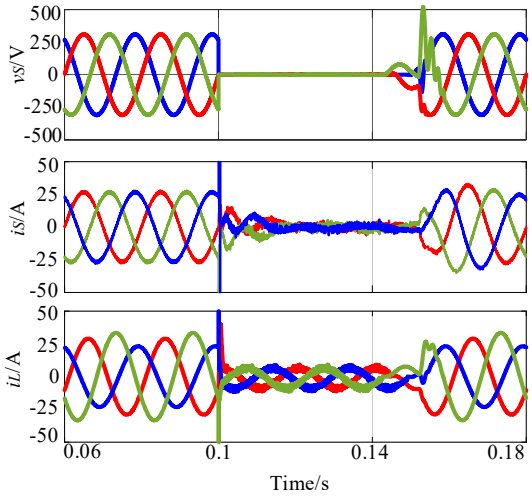

Figure 9. Simulation waveform of the FCL-DVR during a three-phase ground failure.

6. Conclusions

To effectively improve the robustness of the three-phase FCL-DVR load voltage controller, this paper proposes a new second-order sliding mode controller. Compared with three-phase DVR in which the series converter applies PI/PR for the outer voltage loop and inner current loop, the new control scheme has a better resistance to grid voltage disturbance. The main conclusions for this paper are:

(1) A second-order sliding mode controller can result in a better resistance to voltage disturbance than the conventional PI/PR regulator.
(2) A second-order sliding mode controller can have a better dynamic feature than the conventional PI/PR regulator as the second-order sliding mode controller reduces the response time and overshooting.
(3) The FCL-DVR with a second-order sliding controller can maintain the large fault current by switching the control mode from DVR to FCL.

MATLAB/Simulink simulation results verify the good robustness and superior fault flow limiting capability of the proposed scheme.

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