



Communication Effect of Gate Bias Stress on the Electrical Characteristics of Ferroelectric Oxide Thin-Film Transistors with Poly(Vinylidenefluoride-Trifluoroethylene)

Bon-Seong Gu¹, Eun-Seo Park¹, Jin-Hyuk Kwon^{2,*} and Min-Hoi Kim^{1,2,*}

- Department of Creative Convergence Engineering, Hanbat National University, Daejeon 34158, Republic of Korea
 Research Institute of Printed Electronics & 3D Printing Industry University Cooperation Foundation
- ² Research Institute of Printed Electronics & 3D Printing, Industry University Cooperation Foundation, Hanbat National University, Daejeon 34158, Republic of Korea
- * Correspondence: jhkwon@hanbat.ac.kr (J.-H.K.); mhkim8@hanbat.ac.kr (M.-H.K.); Tel.: +82-42-821-1973 (M.-H.K.)

Abstract: We investigated the effect of gate bias stress (GBS) on the electrical characteristics of ferroelectric oxide thin-film transistors (FeOxTFTs) with poly(vinylidenefluoride-trifluoroethylene). Generally, conventional oxide thin-film transistors (OxTFTs) with dielectric gate insulators exhibit a small negative shift under negative gate bias stress (NBS) and a large positive shift under positive gate bias stress (PBS) in transfer characteristic curves. In contrast, the FeOxTFTs show a small positive shift and a large negative shift under NBS and PBS, respectively. It was confirmed that sufficient changes in the electrical characteristics are obtained by 10 min NBS and PBS. The changed electrical characteristics such as threshold voltage shift, memory on- and memory off-current were maintained for more than 168 h after NBS and 24 h after PBS. It is deduced that, since the dipole alignment of the ferroelectric layer is maximized during GBS, these changes in electrical properties are caused by the remnant dipole moments still being retained during the gate sweep. The memory on- and memory off-current are controlled by GBS and the best on/off current ratio at 10⁷ was obtained after NBS. By repeatedly alternating NBS and PBS, the electrical characteristics were reversibly changed. Our results provide the scientific and technological basis for the development of stability and performance optimization of FeOxTFTs.

Keywords: ferroelectric; oxide TFT; P(VDF-TrFE); gate bias stress; threshold voltage shift

1. Introduction

Oxide thin-film transistors (OxTFT) have attracted great attention due to their high field-effect mobility, high optical transparency, and solution processability [1–4]. In order to examine the electrical stability of OxTFTs, numerous studies about the characteristic variations caused by long-term gate bias stress (GBS), such as negative gate bias stress (NBS), positive gate bias stress (PBS), and negative bias illumination stress (NBIS), have been conducted [5,6]. In conventional OxTFTs, NBS and PBS typically induce negative and positive threshold voltage (V_T) shifts, respectively [5].

Recently, various attempts have been made to exploit OxTFTs as a ferroelectric or charge trap memory device [7,8]. Ferroelectric oxide thin-film transistors (FeOxTFTs), which use ferroelectrics as a gate insulator, facilitate programing and erasing operations at relatively low voltages compared to charge trap transistors [9]. Representatives of ferroelectrics for gate insulators include lead zirconate titanate, silicon-doped hafnia, and poly(vinylidenefluoride-trifluorethylene) (P(VDF-TrFE)). Since P(VDF-TrFE) thin films can be fabricated via a facile low-cost solution process, P(VDF-TrFE) has been actively studied thus far [10–12]. Previously, studies on the improvement of the retention characteristics of the FeOxTFT memories with solution-processed P(VDF-TrFE) insulator have also being conducted using the solution-processed indium-gallium-zinc oxide (IGZO) semiconductor [13].



Citation: Gu, B.-S.; Park, E.-S.; Kwon, J.-H.; Kim, M.-H. Effect of Gate Bias Stress on the Electrical Characteristics of Ferroelectric Oxide Thin-Film Transistors with Poly(Vinylidenefluoride-Trifluoroethylene). *Materials* **2023**, *16*, 2285. https://doi.org/10.3390/ ma16062285

Academic Editor: Linfeng Lan

Received: 6 February 2023 Revised: 7 March 2023 Accepted: 10 March 2023 Published: 12 March 2023



Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). In an array architecture where multiple memory devices are integrated, a voltage for the operation of a certain cell is simultaneously applied to the gates of other constituent cells [14]. Especially, in the case of NAND-type ferroelectric memories explored recently, positive or negative read voltages should be continuously applied to the devices for the pass states of FeOxTFTs [15]. Although there is a growing need for investigating the effect of GBS in ferroelectric memory devices, GBS-induced variations in the memory characteristics of FeOxTFTs have not yet been studied.

In this work, we investigated the effect of GBS on the electrical characteristics of solution-processed FeOxTFTs with P(VDF-TrFE). First, we compared the NBS and PBS characteristics of OxTFTs in both bottom-gate and top-gate configurations applying dielectric and ferroelectric polymers. Moreover, the effect of GBS time on the electrical characteristics of the devices and the electrical sustainability of the GBS-induced characteristic changes were examined. It was found that the memory on- and off-currents can be controlled through the application of GBS, and the FeOxTFT with P(VDF-TrFE) exhibited the highest on/off current ratio at $\approx 10^7$ after being subjected to NBS. Lastly, the reversibility of the characteristic changes by repeatedly alternated NBS and PBS were tested.

2. Materials and Methods

An IGZO solution was prepared by dissolving indium nitrate hydrate, gallium nitrate hydrate, and zinc nitrate hydrate into 2-methoxyethanol with an In:Ga:Zn molar ratio of 4:3:2. The solution was stirred for 8 h at 60 °C and then filtered through a syringe filter. A poly(methyl methacrylate) (PMMA) solution was prepared by dissolving PMMA in toluene at 5 wt.%. A P(VDF-TrFE) solution was prepared by dissolving P(VDF-TrFE) (75/25) into cyclopentanone at 10 wt.%.

Figure 1a–c show the schematic diagrams of the bottom-gate top-contact OxTFT with dielectric gate insulator, top-gate bottom-contact OxTFT with dielectric gate insulator, and top-gate bottom-contact FeOxTFT with ferroelectric gate insulator, respectively. For bottomgate top-contact OxTFT (Figure 1a), the IGZO solution was first spin-coated on a substrate (i.e., heavily p-doped silicon with thermally grown 200 nm-thick silicon dioxide) at 3000 rpm for 30 s with subsequent two-step thermal treatment: for 10 min at 110 °C and then for 3 h at 500 °C. Lastly, 120 nm thick aluminum source/drain electrodes were thermally deposited on the IGZO layer through a shadow mask. For top-gate bottom-contact OxTFT with dielectric gate insulator (Figure 1b), the IGZO solution was first spin-coated on an indium-tin-oxide source/drain-patterned substrate at 3000 rpm for 30 s with subsequent two-step thermal treatment: for 10 min at 110 °C and then for 3 h at 500 °C. The PMMA solution was then spin-coated on the IGZO layer at 3000 rpm for 30 s with subsequent thermal treatment for 1 h at 90 °C. Lastly, a 120 nm thick aluminum gate electrode was thermally deposited on the PMMA layer through a shadow mask. For top-gate bottomcontact FeOxTFT with ferroelectric gate insulator (Figure 1c), the IGZO solution was first spin-coated on an indium-tin-oxide source/drain-patterned substrate at 3000 rpm for 30 s with subsequent two-step thermal treatment: for 10 min at 110 °C and then for 3 h at 500 °C. The P(VDF-TrFE) solution was spin-coated on the IGZO layer at 3000 rpm for 30 s with subsequent thermal treatment for 2 h at 140 °C. Lastly, a 120 nm thick aluminum gate electrode was thermally deposited on the P(VDF-TrFE) layer through a shadow mask. In the case of the devices with the top-gate configuration, since aluminum source/drain electrodes can be oxidized due to the high temperature for the IGZO thermal treatment, the indium-tin-oxide source/drain electrodes with relatively good thermal stability were used instead of aluminum source/drain electrodes.



Figure 1. The device structures for (**a**) the conventional bottom-gate OxTFT with a dielectric gate insulator, (**b**) top-gate OxTFT with a dielectric gate insulator, and (**c**) top-gate OxTFT with a ferroelectric gate insulator. The transfer characteristic curves of (**d**) the conventional bottom-gate OxTFT with the dielectric gate insulator (i.e., silicon dioxide), (**e**) top-gate OxTFT with the dielectric gate insulator (i.e., PMMA), and (**f**) top-gate OxTFT with the ferroelectric gate insulator (i.e., P(VDF-TrFE)) after 1-h NBS and 1-h PBS.

All electrical characterizations for the transistors were carried out using a semiconductor analyzer (Hewlett Packard, HP 4551A). Gate voltages ($V_{\rm G}$) of -50 V and 50 V were applied to the transistors for NBS and PBS, respectively (Figure S1d, Supplementary Materials).

3. Results and Discussion

First, we compared our FeOxTFT with other OxTFTs having conventional dielectric gate insulators. Figure 1d shows the transfer characteristic curves of the bottom-gate OxTFT with conventional dielectric gate insulator after NBS and PBS. The $V_{\rm G}$ of -50 V and 50 V were applied to the devices for the NBS and PBS, respectively, for 1 h. Each transfer characteristic curve after GBS was measured by sweeping $V_{\rm G}$ from -50 to 50 V in 2 V increments at constant drain voltage (V_D) = 5 V. IGZO-based TFTs usually exhibit n-type operation [16–18]. Our devices also clearly exhibited n-type operation. While the curve moves to the negative direction after NBS, a large positive shift (>10 V) is shown after PBS. With the PMMA gate insulator (i.e., a conventional polymer dielectric), the transfer curve of the top-gate OxTFT shows small negative and large positive shift under NBS and PBS, respectively, as shown in Figure 1e. This is because holes are trapped by NBS and electrons are trapped by PBS in field-effect transistors [19,20]. For NBS, the trapped holes that act as positive charges further accumulate free electrons in the channel region, which shifts the $V_{\rm T}$ and transfer curve of an n-type device in the negative direction. For PBS, the trapping of electrons reduces free electrons, which shifts the $V_{\rm T}$ and transfer curve in the positive direction. Moreover, the trapped electrons hinder the charge accumulation for channel formation, which further shifts the $V_{\rm T}$ and transfer curve in the positive direction (Figure S2, Supplementary Materials). Under NBS, a small electric field is applied to the gate insulator due to depletion of IGZO during NBS, resulting in only a small or negligible negative shift [21,22]. Therefore, with dielectric gate insulators, both bottom- and top-gate OxTFT show conventional transfer curve shift by GBS.

In contrast, with a ferroelectric P(VDF-TrFE) gate insulator, the device shows nonconventional transfer curve shift as shown in Figure 1f. First, after NBS, a small positive curve shift and reduced off-current were observed. For PBS, a large negative curve shift appeared, resulting in the off-current being significantly increased compared to the initial curve. That is, the FeOxTFT shows a GBS-induced characteristic change, which is opposite to the case with dielectric gate insulators. While the off-current is significantly increased by the PBS, the gate current maintained a comparable level without showing a discernible variation (Figure 1f). In addition, the linear mobility values were calculated (Figure S1, Supplementary Materials) [23].

In order to investigate the variation in the electrical characteristics of the FeOxTFTs according to the GBS time, the transfer characteristic curves were measured as the GBS time increases, shown in Figure 2a,d. The measurements were conducted by acquiring the transfer characteristic curves with the accumulated GBS time of 10 min, 20 min, 30 min, 40 min, 50 min, 60 min, and 120 min, under the GBS of $V_{\rm G} = -50$ V and 50 V for the NBS and PBS, respectively. Each transfer characteristic curve after GBS was measured by sweeping $V_{\rm G}$ from -50 to 50 V and back in 2 V increments and 2 V decrements at constant $V_{\rm D}$ = 5 V. The double sweeping measurement was conducted to understand the memory characteristics of the ferroelectric transistors. As shown in Figure 2b,c,e,f, $V_{\rm T}$ at forward sweep ($V_{\rm T,F}$), $V_{\rm T}$ at reverse sweep ($V_{\rm T,R}$), memory on-current ($I_{\rm M,ON}$), and memory off-current (I_{M,OFF}) of the transfer curves under NBS and PBS were obtained, respectively. Here, we defined $V_{\rm TF}$ and $V_{\rm TR}$ as a voltage where the drain current is 15 μ A during forward and backward sweeps [24]. I_{M,ON} and I_{M,OFF} were defined as the current values where the $V_{\rm G}$ is -10 V during forward and backward sweeps. Under NBS, $V_{\rm LF}$ and $V_{\rm T,R}$ shows only small changes as seen in Figure 2b, and $I_{\rm M,ON}$ exhibits negligible change shown in Figure 2c. However, $I_{M,OFF}$ shows a large decrease even under 10 min of NBS and saturated with additional GBS thereafter. In contrast, when PBS is applied, $V_{\rm T,F}$ and $V_{T,R}$ were moved to the negative direction more than about 15 V as shown in Figure 2e. In Figure 2f, $I_{M,ON}$ and $I_{M,OFF}$ are increased, and notably a large increase of about 10³ times was observed. That is, when NBS and PBS are applied, unlike the OxTFT with dielectric gate insulator showing negative and positive shift, the FeOxTFT rather shows positive and negative shift respectively. Note again that, in the OxTFT with dielectric gate insulators, the GBS-induced characteristic change originated from the trapped charges by the gate field. However, it has been reported that trap density in P(VDF-TrFE) interfaced with the oxide semiconductor was low [25]. In addition, due to the effect of the remnant ferroelectric dipole moments, counterclockwise hysteresis, rather than clockwise hysteresis, appears by trapped charges. During the $V_{\rm G}$ sweeping in the transfer characteristic measurement, which proceeds for a short time (<15 s), ferroelectric dipole moment alignment is not achieved in the entire ferroelectric layer. During $V_{\rm G}$ sweeping, the ferroelectric dipole moments are aligned according to the gate electric field in the relatively high crystalline region. However, under long GBS, the additional ferroelectric dipole moments are aligned even in the region where the alignment of ferroelectric dipole moments is difficult under short gate bias. The GBS possibly suppresses partial disorder in the P(VDF-TrFE) layer, which leads to the alignment of the additional ferroelectric dipole moments [26]. After this GBS, if a $V_{\rm G}$ is swept for a short time, the additional ferroelectric dipole moments aligned by the previous GBS do not change along the $V_{\rm G}$ (Figure S3, Supplementary Materials). For example, under PBS, ferroelectric dipole moments are formed in an upward direction in our top-gate FeOxTFTs. During the gate sweep after PBS, even if the $V_{\rm G}$ becomes negative, exceeding the coercive voltage, the additional ferroelectric dipole moments maintain an upward direction instead of a downward direction (Figure S2, Supplementary Materials). Therefore, by these unswept ferroelectric dipole moments, the drain current is increased and the transfer curve is negatively shifted.



Figure 2. (a) Transfer characteristic curves, (b) $V_{\rm T}$, and (c) $I_{\rm M,ON}$ and $I_{\rm M,OFF}$ under NBS as increasing GBS time, (d) transfer characteristic curves, (e) $V_{\rm T}$, and (f) $I_{\rm M,ON}$ and $I_{\rm M,OFF}$ under PBS. $I_{\rm M,ON}$ and $I_{\rm M,OFF}$ are the current at $V_{\rm G}$ of -10 V during forward and backward sweeps.

In order to find out the electrical sustainability of the GBS-induced characteristic changes (i.e., how long the changed properties of the FeOxTFTs due to GBS are maintained), the transfer characteristic curves were measured corresponding to the elapsed time as shown in Figure 3a,d. After applying the GBS of $V_{\rm G} = -50$ V and 50 V for the NBS and PBS, respectively to the devices, the transfer characteristic curves were acquired with the elapsed time of 1 h, 24 h, 48 h, 96 h, and 168 h. The transfer characteristics were measured by sweeping $V_{\rm G}$ from -50 to 50 V and back in 2 V increments and 2 V decrements at constant $V_{\rm D} = 5$ V. For the case of NBS, since the change of $V_{\rm T,F}$, $V_{\rm T,R}$, and $I_{\rm M,ON}$ by NBS were small, a significant change according to the elapsed time was not observed; see Figure 3b,c. The value of $I_{\rm OFF}$ significantly reduced by NBS was maintained for 168 h. For the case of PBS, $V_{\rm T,F}$, $V_{\rm T,R}$, $I_{\rm M,ON}$, and $I_{\rm M,OFF}$, which showed large changes due to PBS, varied close to the initial values as time passed, as shown in Figure 3e,f. In detail, after 24 h, the characteristics of FeOxTFT changed by PBS are maintained to some extent, but after 96 h, the values become similar to the transfer curve values in the initial state.

To investigate the memory characteristics of the FeOxTFTs, the retention characteristics of I_D were measured as shown in Figure 4a. The device was programmed by applying the high V_G of 50 V and -50 V, and then, the $I_{M,ON}$ and $I_{M,OFF}$ were measured with the V_G of 0 V for the initial measurement and with the V_G of -10 V for the post-NBS and post-PBS measurements. The V_G of -50 V and 50 V for the NBS and PBS, respectively, were applied to the device for 1 h. $I_{M,ON}$ and $I_{M,OFF}$ were well retained during 1000 s for the initial (no bias), NBS, and PBS cases. It was noted that in the case of NBS, $I_{M,OFF}$ shows a decreasing value over time, which occurs when the holes charged in ferroelectric in erasing operation are discharged during retention measurement. $I_{M,ON}$, $I_{M,OFF}$, and $I_{M,OFF}$ of the FeOxTFTs after 10³ s are presented in Figure 4b. In the initial FeOxTFT, $I_{M,ON}$ and $I_{M,OFF}$ shows 388.9 µA and 1.6 µA, respectively, and thus an $I_{M,ON}/I_{M,OFF}$ value of 2.5 × 10² is

obtained. In the case of NBS, a significantly improved $I_{M,ON}/I_{M,OFF}$ value of 10^7 is shown due to largely reduced $I_{M,OFF}$. For PBS, while $I_{M,ON}$ increases, $I_{M,OFF}$ increases excessively, resulting in a reduced $I_{M,ON}/I_{M,OFF}$ value of 0.4×10^2 compared to the NBS case.



Figure 3. (a) Transfer characteristic curves, (b) V_{T} , (c) $I_{M,ON}$ and $I_{M,OFF}$ according to elapsed time after NBS, (d) transfer characteristic curves, (e) V_{T} , (f) $I_{M,ON}$ and $I_{M,OFF}$ according to elapsed time after PBS.

In order to study the reversibility of the GBS effect, the NBS and PBS were applied alternately and repeatedly as shown in Figure 4c. The transfer characteristic curves were obtained with applying the first NBS (GBS #1), first PBS (GBS #2), second NBS (GBS #3), second PBS (GBS #4), and third NBS (GBS #5) in sequence. In Figure 4d, $I_{M,ON}$ and $I_{M,OFF}$ repeatedly decrease after NBS and increase after PBS. This means that the direction of the unswept ferroelectric dipole moments during the gate sweeping can be controlled reversibly by GBS (Figure S3, Supplementary Materials). The repeatedly alternated NBS and PBS further suppressed the partial disorder [26], which eventually enabled the reversible rotation of the additional ferroelectric dipole moments. In a real memory array circuit, a larger value of $I_{M,ON}$ and $I_{M,OFF}$ or a larger value of $I_{M,ON}/I_{M,OFF}$ is preferred according to the number of memory elements connected together and the connected circuit in the next stage. Therefore, using NBS and PBS, the performance of the PeOxTFTs is reversibly optimized. Future work needs to investigate the origin of the partial disorder in P(VDF-TrFE) layers and the mechanism for the alignment of additional ferroelectric dipole moments.



Figure 4. (a) Retention characteristics of the FeOxTFT initial and after NBS and PBS. (b) $I_{M,ON}$, $I_{M,OFF}$, and $I_{M,ON}/I_{M,OFF}$ of the FeOxTFT initial after 1000 s. (c) Transfer characteristic curves. (d) The $I_{M,ON}$ and $I_{M,OFF}$ of the initial FeOxTFT and those subjected to repeatedly alternated NBS and PBS.

4. Conclusions

The FeOxTFT with a P(VDF-TrFE) gate insulator exhibited small variations in $V_{\rm T}$ and $I_{\rm M,ON}$, and a large reduction in $I_{\rm M,OFF}$ under the NBS, while exhibiting a large negative shift in $V_{\rm T}$, and large increases in $I_{\rm M,ON}$ and $I_{\rm M,OFF}$ under the PBS. The large variations in $V_{\rm T}$, $I_{\rm M,ON}$, and $I_{\rm M,OFF}$ under the GBS were attributed to the alignment of the additional ferroelectric dipole moments in the P(VDF-TrFE) layer. In the sustainability tests, the $V_{\rm T}$, $I_{\rm M,ON}$, and $I_{\rm M,OFF}$ changed by the NBS were maintained for more than 168 h, and those changed by the PBS for 24 h. In the retention tests, the $I_{\rm M,ON}$, and $I_{\rm M,OFF}$ of the initial FeOxTFT and those subjected to the NBS and PBS were well retained for 1000 s. Moreover, the $I_{\rm M,ON}$ and $I_{\rm M,OFF}$ of the FeOxTFT tended to increase and to decrease, respectively, with the application of the repeatedly alternated NBS and PBS. This indicates that the reversibility of the GBS effect was obtained by repeatedly alternating the NBS and PBS. These results will contribute to improving the electrical stability and performance of FeOxTFTs.

Supplementary Materials: The following supporting information can be downloaded at: https: //www.mdpi.com/article/10.3390/ma16062285/s1, Figure S1: (a–c) The device structures, (d) the circuit diagram for the GBS, and the linear-scale transfer characteristic curves of (e) the conventional bottom-gate OxTFT with the dielectric gate insulator (i.e., silicon dioxide), (f) top-gate OxTFT with the dielectric gate insulator (i.e., PMMA), and (g) top-gate OxTFT with the ferroelectric gate insulator (i.e., P(VDF-TrFE)) after 1-h NBS and 1-h PBS; Figure S2: The energy band diagrams for the OxTFT and FeOxTFT subjected to the PBS and NBS; Figure S3: Schematic diagrams for the ferroelectric dipole changes in the P(VDF-TrFE) layer in the PBS and NBS cases. Author Contributions: Conceptualization, B.-S.G., J.-H.K. and M.-H.K.; methodology, B.-S.G., E.-S.P. and M.-H.K.; validation, B.-S.G. and E.-S.P.; formal analysis, B.-S.G., J.-H.K. and M.-H.K.; investigation, B.-S.G. and E.-S.P.; writing—original draft preparation, B.-S.G., J.-H.K. and M.-H.K.; writing—review and editing, J.-H.K. and M.-H.K. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the research fund of Hanbat National University in 2022.

Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available due to privacy.

Conflicts of Interest: The authors declare no conflict of interest.

References

- 1. Hsu, C.-M.; Tzou, W.-C.; Yang, C.-F.; Liou, Y.-J. Investigation of the high mobility IGZO thin films by using co-sputtering method. *Materials* **2015**, *8*, 2769–2781. [CrossRef]
- Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* 2004, 432, 488–492. [CrossRef] [PubMed]
- 3. Kim, S.J.; Yoon, S.; Kim, H.J. Review of solution-processed oxide thin-film transistors. *Jpn. J. Appl. Phys.* 2014, 53, 02BA02. [CrossRef]
- 4. Ji, D.; Jang, J.; Park, J.H.; Kim, D.; Rim, Y.S.; Hwang, D.K.; Noh, Y.-Y. Recent progress in the development of backplane thin film transistors for information displays. *J. Inf. Disp.* **2021**, *22*, 1–11. [CrossRef]
- 5. Cho, E.N.; Kang, J.H.; Kim, C.E.; Moon, P.; Yun, I. Analysis of bias stress instability in amorphous InGaZnO thin-film transistors. *IEEE Trans. Device Mater. Reliab.* 2010, *11*, 112–117. [CrossRef]
- Lee, H.; Lee, S.; Kim, Y.; Siddik, A.B.; Billah, M.M.; Lee, J.; Jang, J. Improvement of stability and performance of amorphous indium gallium zinc oxide thin film transistor by zinc-tin-oxide spray coating. *IEEE Electron. Device Lett.* 2020, 41, 1520–1523. [CrossRef]
- Hasan, M.M.; Islam, M.M.; Bukke, R.N.; Tokumitsu, E.; Chu, H.-Y.; Kim, S.C.; Jang, J. Improvement of amorphous InGaZnO thin-film transistor with ferroelectric ZrOx/HfZrO gate insulator by 2 step sequential Ar/O₂ treatment. *IEEE Electron. Device Lett.* 2022, 43, 725–728. [CrossRef]
- Kim, H.-R.; Kim, G.-H.; Seong, N.-J.; Choi, K.-J.; Kim, S.-K.; Yoon, S.-M. Comparative studies on vertical-channel chargetrap memory thin-film transistors using In-Ga-Zn-O active channels deposited by sputtering and atomic layer depositions. *Nanotechnology* 2020, *31*, 435702. [CrossRef]
- 9. Kim, M.-K.; Kim, I.-J.; Lee, J.-S. CMOS-compatible ferroelectric NAND flash memory for high-density, low-power, and high-speed three-dimensional memory. *Sci. Adv.* **2021**, *7*, eabe1341. [CrossRef]
- Sun, Y.; Xie, D.; Zhang, X.; Xu, J.; Li, X.; Li, X.; Dai, R.; Li, X.; Li, P.; Gao, X. Temperature-dependent transport and hysteretic behaviors induced by interfacial states in MoS2 field-effect transistors with lead-zirconate-titanate ferroelectric gating. *Nanotechnology* 2016, 28, 045204. [CrossRef] [PubMed]
- Mulaosmanovic, H.; Ocker, J.; Müller, S.; Schroeder, U.; Müller, J.; Polakowski, P.; Flachowsky, S.; van Bentum, R.; Mikolajick, T.; Slesazeck, S. Switching kinetics in nanoscale hafnium oxide based ferroelectric field-effect transistors. ACS Appl. Mater. Interfaces 2017, 9, 3792–3798. [CrossRef]
- 12. Chen, X.; Han, X.; Shen, Q.D. PVDF-based ferroelectric polymers in modern flexible electronics. *Adv. Electron. Mater.* 2017, 3, 1600460. [CrossRef]
- Boampong, A.A.; Cho, J.-H.; Choi, Y.; Kim, M.-H. Enhancement of the Retention Characteristics in Solution-Processed Ferroelectric Memory Transistor with Dual-Gate Structure. J. Nanosci. Nanotechnol. 2021, 21, 1766–1771. [CrossRef]
- 14. Kim, M.-H.; Lee, G.J.; Keum, C.-M.; Lee, S.-D. Concept of rewritable organic ferroelectric random access memory in two lateral transistors-in-one cell architecture. *Semicond. Sci. Technol.* **2014**, *29*, 025004. [CrossRef]
- 15. Park, H.W.; Lee, J.G.; Hwang, C.S. Review of ferroelectric field-effect transistors for three-dimensional storage applications. *Nano Sel.* **2021**, *2*, 1187–1207. [CrossRef]
- 16. Yamada, N.; Ino, R.; Tomura, H.; Kondo, Y.; Ninomiya, Y. High-mobility transparent p-type CuI semiconducting layers fabricated on flexible plastic sheets: Toward flexible transparent electronics. *Adv. Electron. Mater.* **2017**, *3*, 1700298. [CrossRef]
- 17. Chen, H.; Cao, Y.; Zhang, J.; Zhou, C. Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors. *Nat. Commun.* **2014**, *5*, 1. [CrossRef]
- 18. Yatsu, K.; Lee, H.-A.; Kim, D.H.; Park, I.-J.; Kwon, H.-I. Highly stable oxide thin-film transistor-based complementary logic circuits under X-ray irradiation. *ACS Appl. Electron. Mater.* 2022, *4*, 3606–3614. [CrossRef]
- Suresh, A.; Muth, J. Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors. *Appl. Phys.* Lett. 2008, 92, 033502. [CrossRef]
- Li, Y.; Pei, Y.; Hu, R.; Chen, Z.; Zhao, Y.; Shen, Z.; Fan, B.; Liang, J.; Wang, G. Effect of channel thickness on electrical performance of amorphous IGZO thin-film transistor with atomic layer deposited alumina oxide dielectric. *Curr. Appl. Phys.* 2014, 14, 941–945. [CrossRef]

- Jeong, Y.; Song, K.; Kim, D.; Koo, C.Y.; Moon, J. Bias stress stability of solution-processed zinc tin oxide thin-film transistors. *J. Electrochem. Soc.* 2009, 156, H808. [CrossRef]
- Kim, J.S.; Kang, S.; Jang, Y.; Lee, Y.; Kim, K.; Kim, W.; Lee, W.; Hwang, C.S. Investigating the Reasons for the Difficult Erase Operation of a Charge-Trap Flash Memory Device with Amorphous Oxide Semiconductor Thin-Film Channel Layers. *Phys. Status Solidi* (*RRL*)—*Rapid Res. Lett.* 2021, *15*, 2000549. [CrossRef]
- Abiram, G.; Thanihaichelvan, M.; Ravirajan, P.; Velauthapillai, D. Review on perovskite semiconductor field-effect transistors and their applications. *Nanomaterials* 2022, 12, 2396. [CrossRef] [PubMed]
- 24. Ortiz-Conde, A.; Sánchez, F.G.; Liou, J.J.; Cerdeira, A.; Estrada, M.; Yue, Y. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* 2002, 42, 583–596. [CrossRef]
- 25. Pecunia, V.; Banger, K.; Sirringhaus, H. High-Performance Solution-Processed Amorphous-Oxide-Semiconductor TFTs with Organic Polymeric Gate Dielectrics. *Adv. Electron. Mater.* **2015**, *1*, 1400024. [CrossRef]
- Lee, T.Y.; Lee, K.; Lim, H.H.; Song, M.S.; Yang, S.M.; Yoo, H.K.; Suh, D.I.; Zhu, Z.; Yoon, A.; MacDonald, M.R.; et al. Ferroelectric polarization-switching dynamics and wake-up effect in Si-doped HfO₂. ACS Appl. Mater. Interfaces 2019, 11, 3142–3149. [CrossRef] [PubMed]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.