

## Article

# Common-Mode Voltage Reduction Method Based on Variable Sampling Frequency Finite Control Set-Model Predictive Control for PMSM Drive Systems

Yoon-Seong Lee <sup>1</sup>, Kyoung-Min Choo <sup>2</sup>, Chang-Hee Lee <sup>3</sup>, Chang-Gyun An <sup>1</sup>, Junsin Yi <sup>1</sup> and Chung-Yuen Won <sup>1,\*</sup>

<sup>1</sup> Department of Electrical and Computer Engineering, College of Information and Communication Engineering, Sungkyunkwan University, Suwon 16419, Republic of Korea; ysl2@skku.edu (Y.-S.L.); acg1643@skku.edu (C.-G.A.); junsin@skku.edu (J.Y.)

<sup>2</sup> Electric Propulsion Research Center, Korea Electrotechnology Research Institute (KERI), Changwon 51541, Republic of Korea; chuchoo@keri.re.kr

<sup>3</sup> Dawonsys Co., Ltd., Anyang 15655, Republic of Korea; chlee@dawonsys.com

\* Correspondence: woncy@skku.edu

**Abstract:** In this article, a finite control set-model predictive control (FCS-MPC) with variable sampling time is proposed. A zero-voltage vector appears in the dead time between specific voltage vectors, resulting in an unintentionally large common-mode voltage. Herein, a large common-mode voltage was suppressed, and the load current was controlled using a voltage vector combination that did not cause a zero-voltage vector in dead time. Additionally, to improve the total harmonic distortion (THD) of the load current, the intersection of the predicted current and the command current by all the voltage vectors (VVs) in the combination is confirmed. The VV where the intersection occurs is selected as the optimal VV. This optimal VV is applied to the point where the predicted current and the reference current intersect. The applicable range of the sampling time should be selected by considering the calculation time and number of switching. Through the proposed FCS-MPC strategy, not only can the common-mode voltage be limited to within  $\pm V_{dc}/6$ , but an improved THD can also be obtained compared to the existing method using fixed sampling. The proposed method was verified through PSIM simulation and experimental results.

**Keywords:** voltage source inverter (VSI); finite control set-model predictive control (FCS-MPC); common-mode voltage (CMV)



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## 1. Introduction

Voltage source inverters (VSIs) have recently been widely utilized in various energy conversion systems. VSIs, comprising advanced power switching devices, offer improved power quality based on rapid switching operations [1–5]. However, as the switching operations of VSIs accelerate, the issue of common-mode voltage (CMV) tends to increase. Therefore, various approaches have been proposed to reduce the CMV in VSI systems.

One method for suppressing CMV is the use of an active CMV filter [6]. However, hardware solutions, including active CMV filters, require additional auxiliary components, such as common-mode transformers or additional switches [7,8]. Consequently, the system volume increases, and the optimal design of the filter becomes complex. Because of these demands, it has not been considered an attractive option.

Alternatively, finite-control set-model predictive control (FCS-MPC) has been studied as a way to reduce CMV without additional hardware. All switching states of the two-level voltage source inverter (2L-VSI) and CMV voltages are shown in Table 1. Zero-voltage vectors (ZVVs) induce peak CMV; thus, CMV can be mitigated by excluding the ZVV and synthesizing the reference voltages. To replace ZVVs, voltage vectors (VVs) with the same magnitude and opposite direction can be used [9]. However, an indiscriminate VV

synthesis without consideration of the dead time interval can lead to unintended peak CMV occurrences.

**Table 1.** CMV in 2L-VSI.

VV		Switching State ( $S_a, S_b, S_c$ ) <sup>1</sup>	CMV Level
ZVV	$V_0$	(0, 0, 0)	$-V_{dc}/2$
Non-ZVV	$V_1$	(1, 0, 0)	$-V_{dc}/6$
	$V_2$	(1, 1, 0)	$+V_{dc}/6$
	$V_3$	(0, 1, 0)	$-V_{dc}/6$
	$V_4$	(0, 1, 1)	$+V_{dc}/6$
	$V_5$	(0, 0, 1)	$-V_{dc}/6$
	$V_6$	(1, 0, 1)	$+V_{dc}/6$
ZVV	$V_7$	(1, 1, 1)	$+V_{dc}/2$

<sup>1</sup>  $S_i$  ( $i = a, b, c$ ) is a switching function that takes on the values "1" or "0"; if  $S_a = 1$ , the upper switch turns on and the lower switch has the complementary value.

In [10], reference voltages were synthesized, excluding vector transitions that induce peak CMV during the dead time interval. In this case, as the number of available non-ZVVs decreases, the total harmonic distortion (THD) of the load current increases.

In [11–18], the CMV was reduced using a fixed switching frequency. With a fixed switching frequency, lower THD can be achieved with higher switching frequencies, but, unfortunately, switching losses increase simultaneously. In the case of FCS-MPC, where switching vectors are determined at each sampling period, increasing the sampling frequency also leads to an increase in switching losses.

This article proposes a CMV reduction strategy based on variable sampling frequency FCS-MPC. Considering the dead time interval and excluding cases where the peak CMV occurs during vector transitions, a limited number of VV combinations are used to reduce the CMV. The cost function is constructed based on the predicted errors in the  $d$ -axis and  $q$ -axis, and the intersection of the reference current and the predicted current is predicted to determine the next sampling point. Because the predicted current error has a minimum value at the intersection point, the proposed variable sampling method can achieve a low THD for the load current. Consequently, the proposed method can minimize CMV between  $+V_{dc}/6$  and  $-V_{dc}/6$  and achieve lower switching losses and THD compared to fixed sampling frequency methods.

The remainder of this article is organized as follows. Section 2 reviews current control using FCS-MPC for conventional CMV reduction methods. Section 3 presents VV combinations that do not induce peak CMV, while considering the dead time interval. The proposed CMV reduction strategy based on the variable sampling frequency FCS-MPC is described in Section 4. The simulation results and experimental findings validating the proposed FCS-MPC strategy are presented in Sections 5 and 6, respectively. Finally, Section 7 concludes this article.

## 2. Review of Conventional FCS-MPC for CMV Reduction

As shown in Figure 1, the CMV is represented based on the pole voltages  $v_{an}$ ,  $v_{bn}$ , and  $v_{cn}$  of the VSI:

$$v_{CM} = (v_{an} + v_{bn} + v_{cn})/3. \quad (1)$$

The stator voltage equation of a permanent magnet synchronous machine (PMSM) drive system, which includes stator impedance, is expressed as follows:

$$v_s = R_s i + L_s \frac{di}{dt} + E_s, \quad (2)$$

where  $R_s$ ,  $L_s$ , and  $E_s$  represent the stator resistance, stator inductance, and back electromotive force (EMF), respectively. In this case, because the FCS-MPC is based on a discretized

model, the differentiation of the load current is approximated using Euler’s approximation as follows:

$$\frac{di}{dt} = \frac{i(k+1) - i(k)}{T_s} \tag{3}$$

where  $i(k)$  represents the  $k$ -th sampled current, and  $T_s$  indicates the sampling period.

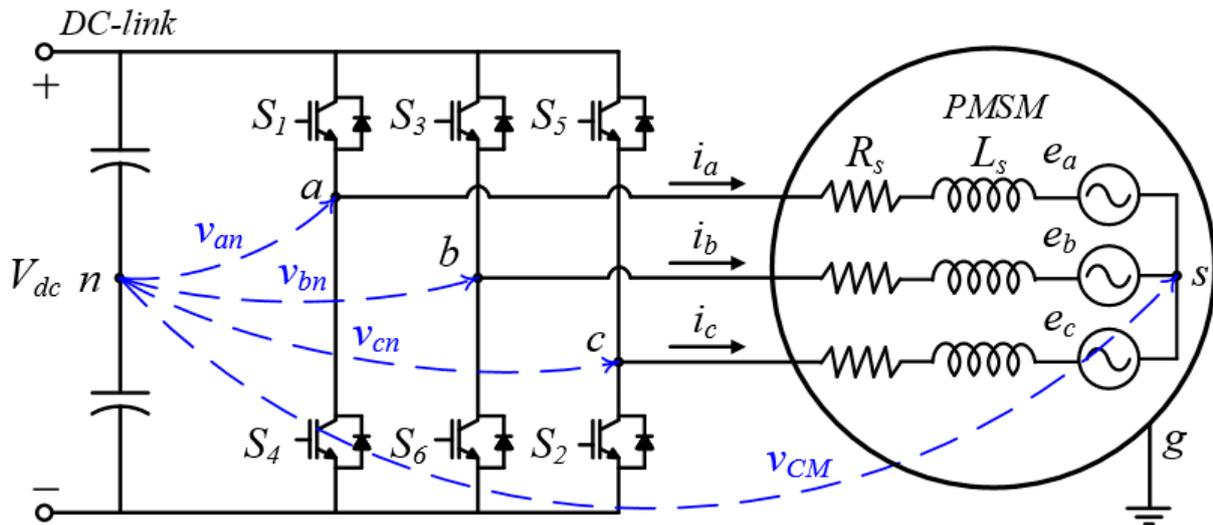


Figure 1. CMV in 2-level voltage source inverter.

By substituting (3) into (2), the predicted future current can be obtained as follows:

$$i(k+1) = \left(1 - \frac{R_s \cdot T_s}{L_s}\right) \times i(k) + \frac{T_s}{L_s} (v_s(k) - E_s(k)) \tag{4}$$

By applying seven VVs to the  $k$ -th sampled  $v(k)$ , seven future currents can be predicted. The predicted future currents can be substituted for the d-axis and q-axis predicted currents, and the current error is the difference between the  $i(k+1)$  and the reference currents along each axis. Therefore, cost function  $g$  can be expressed as follows:

$$g = |i_d^*(k+1) - i_d(k+1)| + |i_q^*(k+1) - i_q(k+1)| \tag{5}$$

Selecting the vector that minimizes cost function  $g$  and applying it during the sampling period minimizes the error between the predicted future currents and actual sampled currents at each sampling instance. Figure 2 illustrates reference values  $i_{ref-d}^*$ ,  $i_{ref-q}^*$ , predicted d-axis and q-axis current waveforms resulting from various VVs.

However, using the ZVV to synthesize the reference voltages leads to a peak CMV. Therefore, to limit the magnitude of CMV to  $|V_{dc}/6|$ , only a non-ZVV was applied to synthesize the reference voltages. Figure 3 shows the future predicted currents along the d-axis with the ZVV and two non-ZVVs applied, respectively. When the ZVV was applied, the future prediction error, represented by  $Err_{zero-d}$ , was smaller than the errors  $Err_{x-d}$  and  $Err_{y-q}$  when the other two non-ZVVs were applied. This suggests that the ZVV is the optimal VV. However, to mitigate CMV, an alternative,  $V_x$ , is applied. The intentional application of a non-ZVV results in significant current ripple and current error compared with the optimal VV. Therefore, the THD of the load current increased.

To reduce current ripple, two methods have been proposed: applying a high sampling frequency and synthesizing two non-ZVVs within a single sampling interval. Figure 4 depicts the predicted current waveforms for both methods. When setting a short sampling period, the inverter outputs the optimal VV with the minimum cost function at each sampling instance, resulting in a low current ripple and current error, but incurring significant

switching losses. In addition, synthesizing two non-ZVVs within one sampling interval also increases the switching losses owing to VV changes.

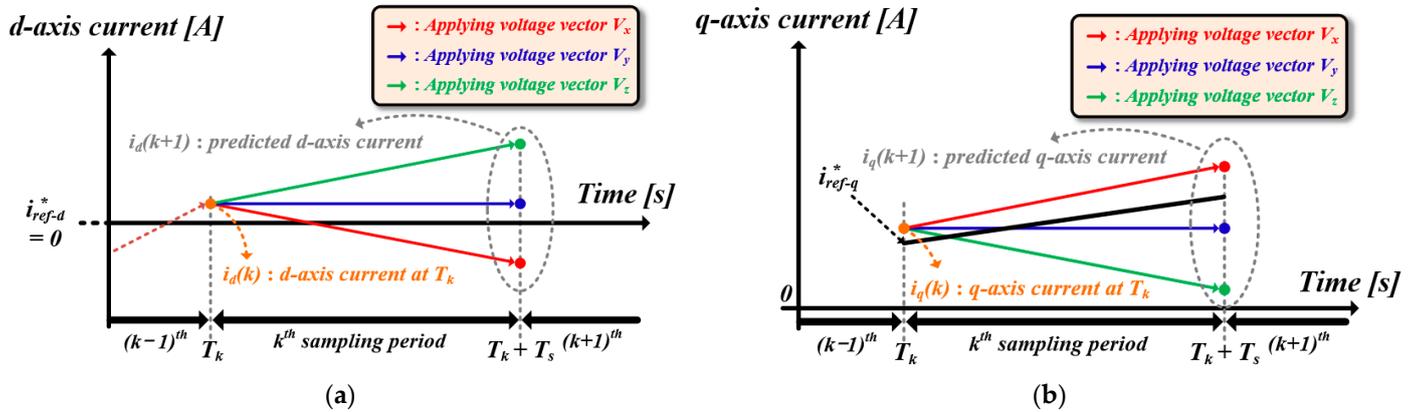


Figure 2. Predicted d-axis and q-axis currents by VVs: (a) predicted d-axis currents and (b) predicted q-axis currents. \* expresses the reference value.

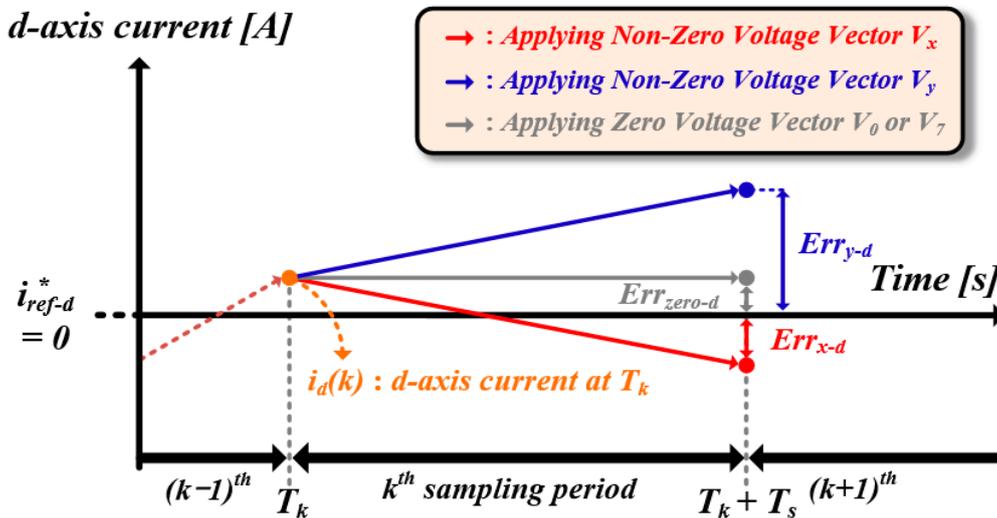


Figure 3. Future predicted current applying ZVV and two non-ZVVs, respectively. \* expresses the reference value.

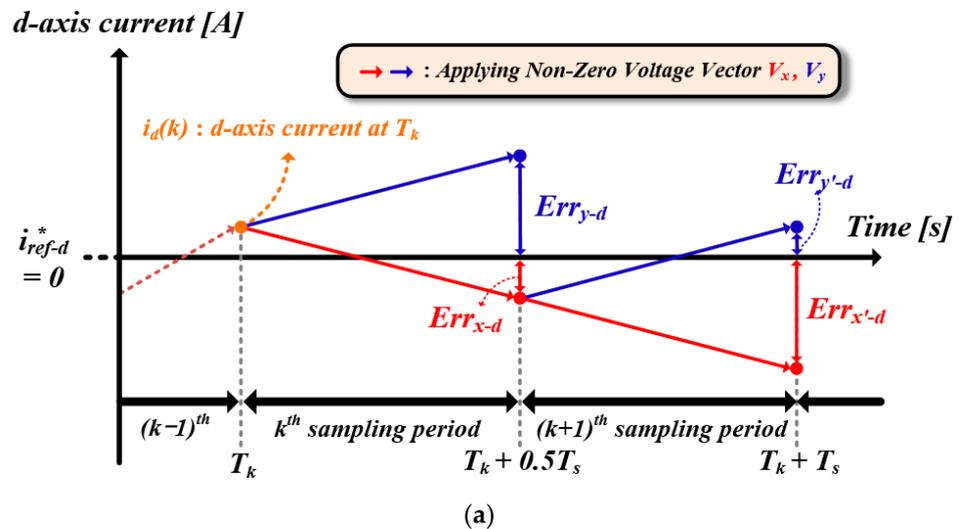
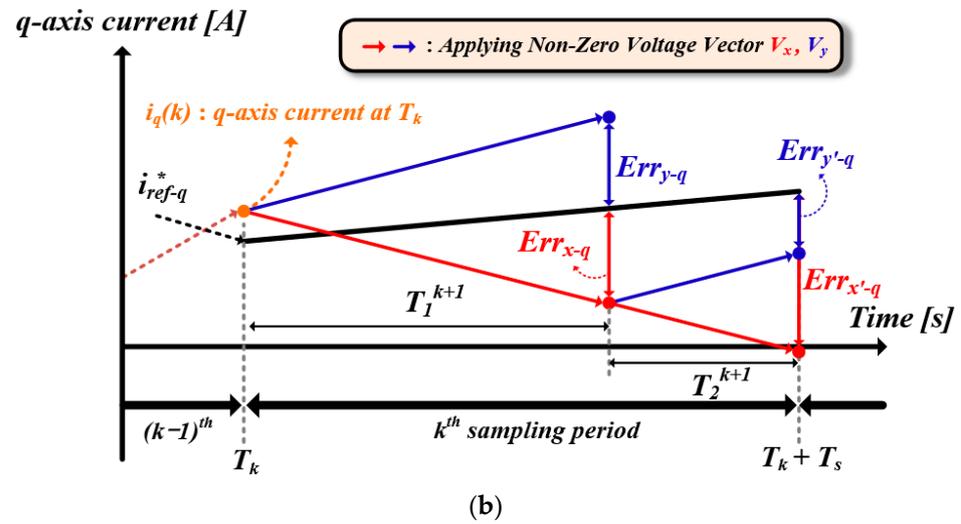


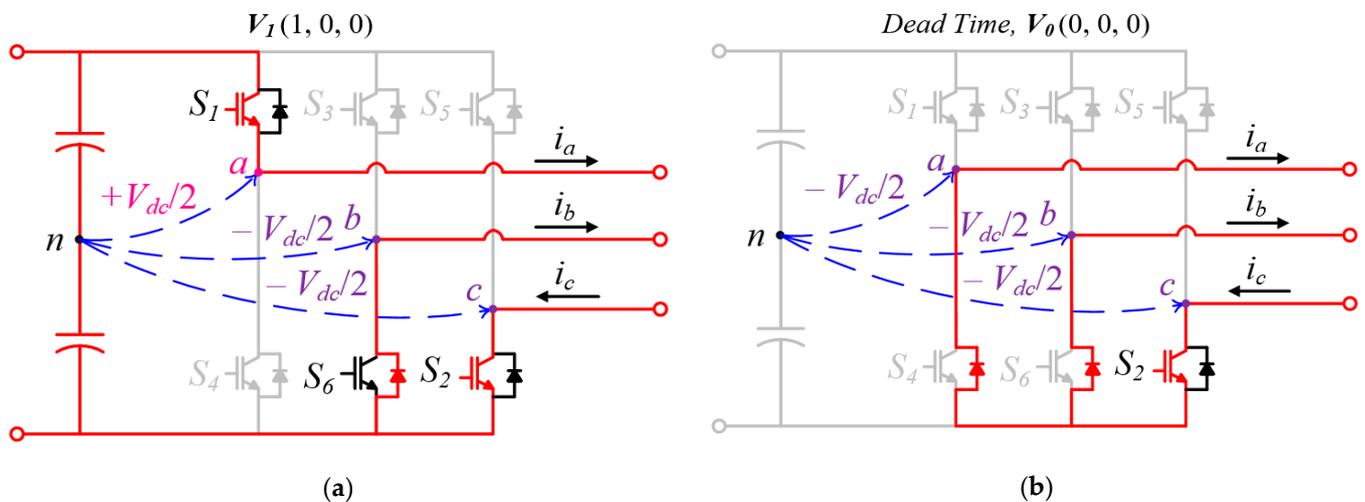
Figure 4. Cont.



**Figure 4.** FCS-MPC for reducing current ripple: (a) applying a high sampling frequency and (b) synthesizing two non-ZVVs within one sampling interval. \* expresses the reference value.

### 3. Consideration of the Dead Time Interval

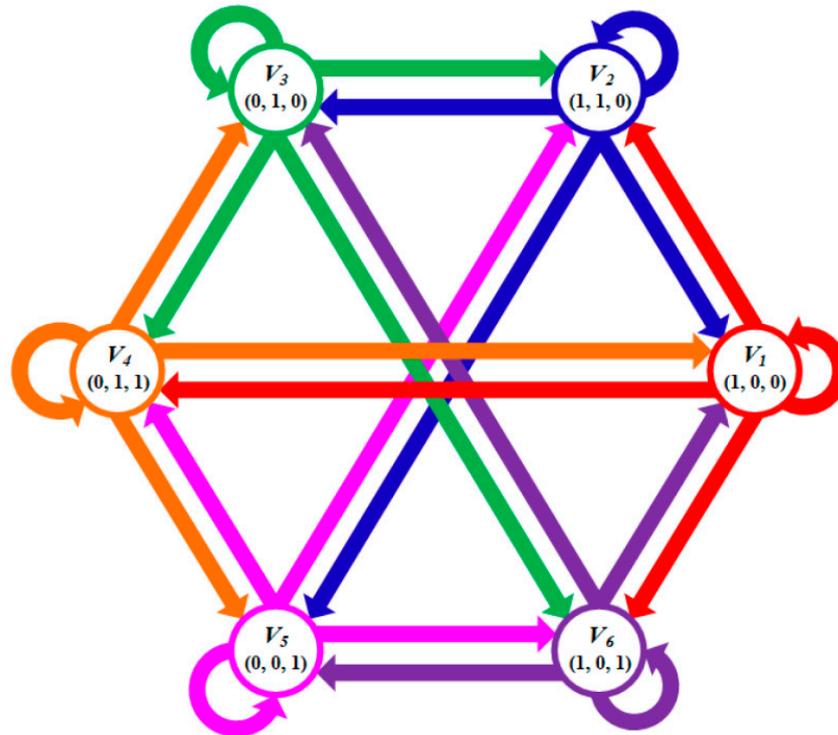
Despite excluding the ZVV from the reference VV synthesis process to mitigate the CMV, an unintended peak CMV occurred when the circuit was configured with the same switching states as the ZVV during the dead time interval. Therefore, the peak CMV could not be completely eliminated without considering the dead time between switching state transitions. Therefore, it is necessary to consider the vector transitions that result in the peak CMV. For instance, Figure 5 illustrates the VV transition where the switch state becomes  $V_0$  (0,0,0) during the dead time. During the switch state  $V_1$  (1,0,0),  $S_1$  is on, whereas  $S_6$  and  $S_2$  are on. During the dead time interval from  $V_1$  (1,0,0) to  $V_3$  (0,1,0),  $S_1$  and  $S_6$  turn off. In this case, both the top and bottom switches of phase  $a$  are off, and the current  $i_a$  flows through the reverse-parallel diode at  $S_4$ . Therefore, during this dead time interval, the CMV has a peak value of  $V_{dc}/2$ . Table 2 lists the VV transitions that result in the peak CMV during the dead time. As shown in Table 2, the peak CMV occurs during transitions between odd or even vectors. Hence, to eliminate the peak CMV, the algorithm should be designed to alternate between odd and even VVs for the output. Figure 6 shows all the VV transitions with a CMV of  $|V_{dc}/6|$ .



**Figure 5.** VV transition where the switch state becomes  $V_0$  during the dead time: (a) circuit configuration for  $V_1$  and (b) circuit configuration for dead time interval between  $V_1$  and  $V_3$ .

**Table 2.** VV transitions that result in peak CMV during the dead time.

Present VV	$V_1$	$V_2$	$V_3$
Future VV	$V_3, V_5$	$V_4, V_6$	$V_1, V_5$
Present VV	$V_4$	$V_5$	$V_6$
Future VV	$V_2, V_6$	$V_1, V_3$	$V_2, V_4$

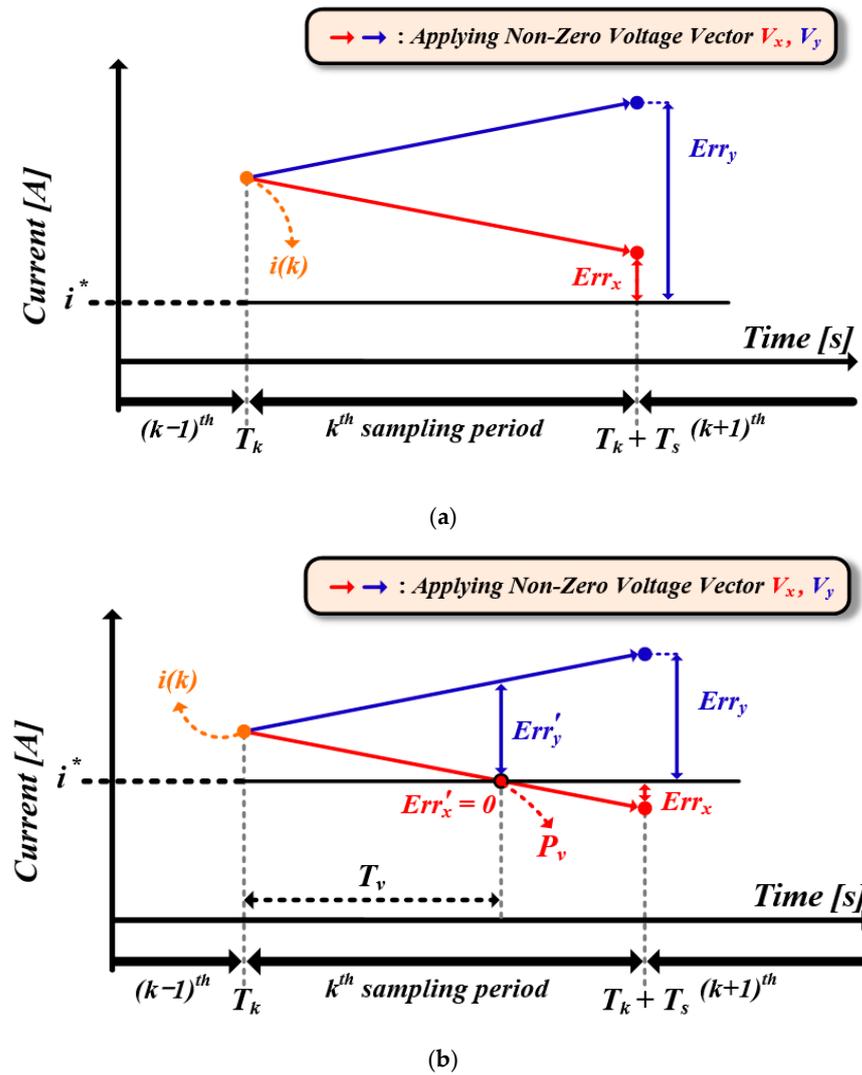
**Figure 6.** All the VV transitions with a CMV of  $|V_{dc}/6|$ .

#### 4. Proposed FCS-MPC with Variable Sampling for CMV Reduction

In this section, we propose the FCS-MPC for CMV reduction based on variable sampling, aiming not only to improve the current THD, but also to reduce the number of switching events compared to fixed sampling methods. This section establishes how the cost function has its minimum at the intersection of the reference current and future predicted current, and the sampling time when the cost function is minimized by considering both  $d$ -axis and  $q$ -axis.

##### 4.1. Minimum Value of Cost Function in Proposed Method

Figure 7 shows both cases where intersections between the predicted future current and the reference current are present and absent. In cases where there is no intersection within the sampling interval, maintaining the existing sampling period yields the smallest cost function value. Conversely, when there is an intersection, the smallest cost function value is attained at the intersection point  $P_v$ . Therefore,  $P_v$  yields the smallest current ripple and current error.



**Figure 7.** Cases where intersections between the predicted future current and the reference current are present and absent: (a) intersection absent and (b) intersection present.

#### 4.2. Calculation of Variable Sampling Period

The intersection between the predicted future current and the command current was obtained using the error equation. Expressing the current as a function of time using (2) yields the following:

$$i(t) = i(k) \times e^{-\frac{R_s}{L_s} T_s} + \frac{v_s(k) - E_s(k)}{R_s} \left(1 - e^{-\frac{R_s}{L_s} T_s}\right), \quad (6)$$

where  $i(k)$  represents the initial value of the current, i.e., the currently measured value. Defining the current error equation over time as (7), the current error equation can be expressed as (8):

$$Err(t) = i^*(t) - i(t), \quad (7)$$

$$Err(t) = i^*(t) - i(k) \times e^{-\frac{R_s}{L_s} T_s} + \frac{v_s(k) - E_s(k)}{R_s} \left(1 - e^{-\frac{R_s}{L_s} T_s}\right), \quad (8)$$

where  $i^*(t)$  denotes the reference current. Therefore, the intersection point  $T_v$  between the predicted future current and commanded current is expressed as follows:

$$T_v = \frac{L_s}{R_s} \times \frac{i(k) - i^*}{\left[i(k) - \frac{v_s(k) - E_s(k)}{R_s}\right]} \quad (9)$$

However, because current control occurs on both the d-axis and q-axis, consideration of both axes is necessary. Figure 8 illustrates a scenario with an intersection on only one axis. When the current error on the q-axis was zero, the error on the d-axis was significant. Thus, because the errors on each axis are independent, effectively reducing the current ripple requires sampling when the sum of the errors on both axes is minimized. The current error equations for each axis are as follows:

$$Err_d(t) = i_d^*(t) - i_d(k) \times e^{-\frac{R_s}{L_d} T_s} + \frac{v_{s,d}(k) - E_{s,d}(k)}{R_s} \left(1 - e^{-\frac{R_s}{L_d} T_s}\right), \quad (10)$$

$$Err_q(t) = i_q^*(t) - i_q(k) \times e^{-\frac{R_s}{L_q} T_s} + \frac{v_{s,q}(k) - E_{s,q}(k)}{R_s} \left(1 - e^{-\frac{R_s}{L_q} T_s}\right). \quad (11)$$

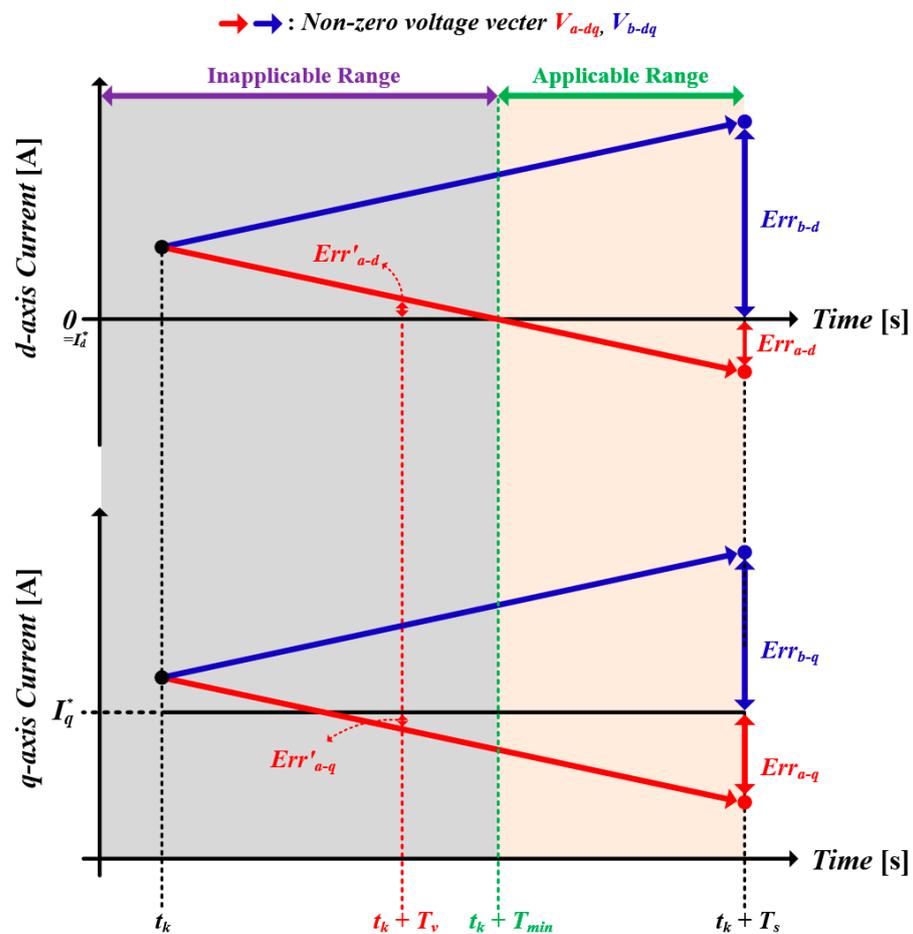


Figure 8. Interval in which variable sampling can be applied.

The time  $T_v$  at which the sum of the current errors is minimized can be found through differentiation and is expressed as follows:

$$T_v = \frac{i_d^*(t) - i_d(k) \times J_d + i_q^*(t) - i_q(k) \times J_q}{[J_q(k)^2 - (J_d(k))^2]}, \quad (12)$$

where  $J_d(k)$  and  $J_q(k)$  are

$$J_d(k) = \frac{R_s \times i_d(k) - v_{s,d}(k) + E_{s,d}(k)}{L_d}, \quad (13)$$

$$J_q(k) = \frac{R_s \times i_q(k) - v_{s,q}(k) + E_{s,q}(k)}{L_q}. \quad (14)$$

#### 4.3. Applicable Range of Variable Sampling

To implement a variable sampling period, the computations involved in predicting future currents must be considered. Without considering the time required for computation, outputting VVs at the points of the minimum cost function may degrade the current characteristics. Figure 8 illustrates the interval in which variable sampling can be applied. For instance, if the point with the minimum cost function is within an inapplicable region, sampling should occur at  $t_k + T_{min}$ , the point within the applicable range that minimizes the cost function, to prevent degradation of the current characteristics. Therefore, in this case, the sampling period was set to  $T_{min}$ . Conversely, if the point with the minimum cost function is within the applicable region, sampling is performed at  $t_k + T_v$ , which is the computed sampling point. Therefore, the sampling period was  $T_v$ .

The FCS-MPC algorithm incorporating the proposed variable sampling period is depicted in Figure 9. First, the MPC computation was performed considering only four specific non-ZVVs. Then, the intersection between the command current and the predicted future current was confirmed. If there were no intersections, the sampling period was set to  $T_s$ . If there was an intersection,  $T_{min}$  and  $T_v$  were compared to determine the sampling period. In this article, the default  $T_s$  was set to 100 [ $\mu$ s], and  $T_{min}$  was set to 50 [ $\mu$ s].

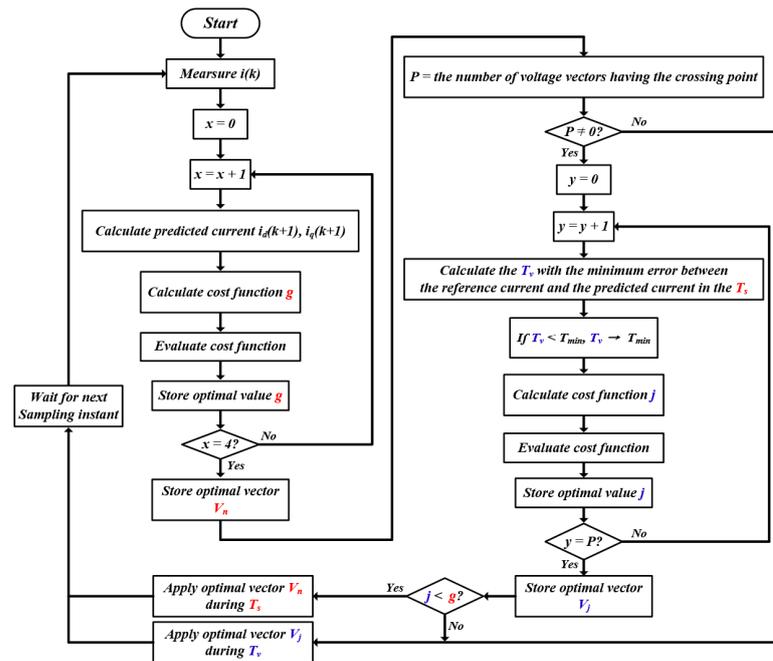


Figure 9. FCS-MPC algorithm for CMV reduction with proposed variable sampling period.

## 5. Simulation Results

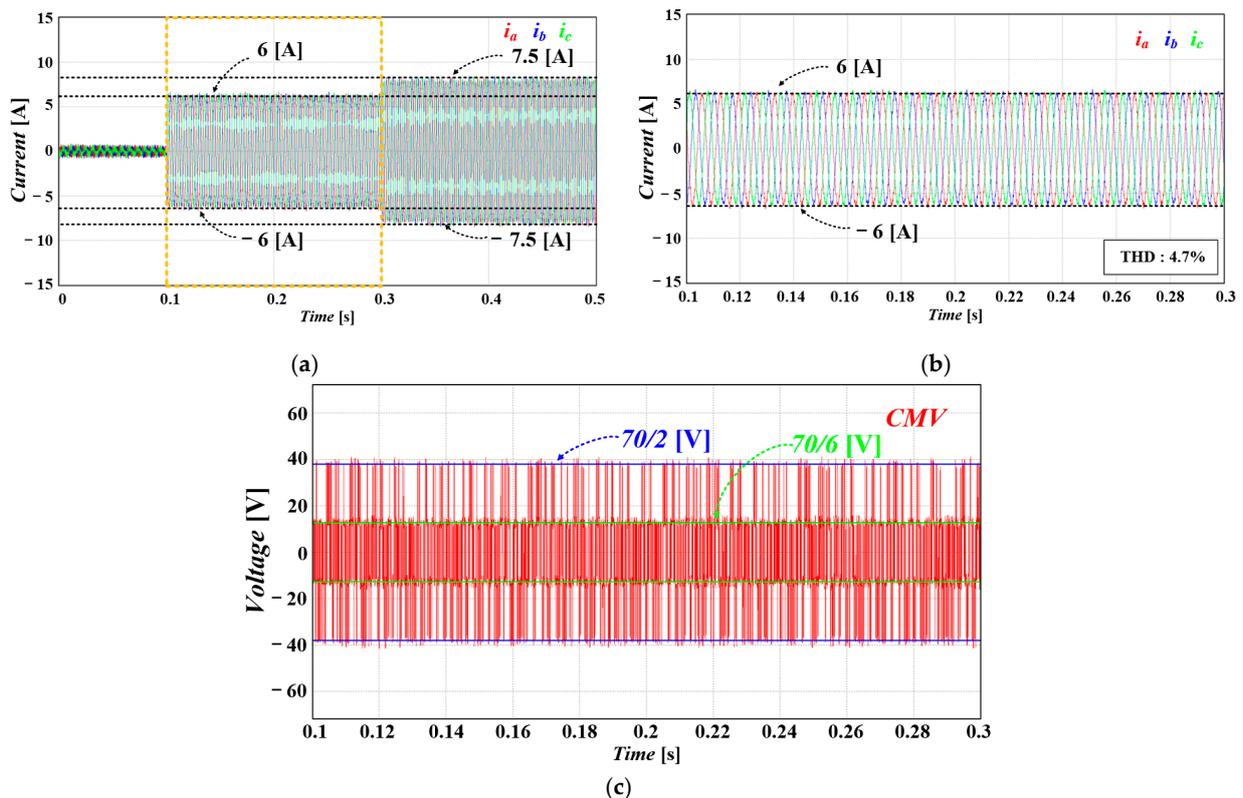
The proposed FCS-MPC method was simulated using a surface-mounted permanent magnet synchronous motor (SPMSM) drive system with the Power SIM program at 750 [rpm], with q-axis current references set to 0 [A], 6 [A], and 7.5 [A]. The simulation parameters are presented in Table 3. The fixed sampling was simulated at 10 and 20 kHz, and the sampling frequency for the proposed method was between 10 and 20 kHz. The simulation results are presented in the following order: FCS-MPC for current control, FCS-MPC excluding ZVV, FCS-MPC excluding ZVV considering dead time (sampling frequencies: 10 and 20 kHz), and the proposed FCS-MPC with a variable sampling frequency between 10 and 20 kHz.

**Table 3.** Simulation parameters of proposed FCS-MPC method.

Parameter	Description	Value	Unit
$V_{dc}$	DC-Link Voltage	70	V
$P_{rate}$	Rated Power	1.1	kW
$\omega_{rate}$	Rated Speed	1500	rpm
$I_{rate}$	Rated Current	9.5	A
$T_{rate}$	Rated Torque	7.0	Nm
$p$	Number of Poles	24	-
$R_s$	Stator Resistance	0.18	$\Omega$
$L_s$	Stator Inductance	3.4	mH
$V_{pk}/krpm$	Peak Line-to-Line Back EMF Constant	43.5	V/krpm

### 5.1. FCS-MPC for Current Control

Figure 10 shows the simulation results of MPC with both ZVVs and non-ZVVs applied. The sampling frequency was fixed at 10 kHz. Figure 10b represents the magnified waveforms of the highlighted part in Figure 10a. Because the FCS-MPC for current control utilizes all applicable VVs, it always outputs the optimal VVs with the minimum cost function, resulting in a current THD of 4.7%. Figure 10c illustrates the CMV from 0.1 t to 0.3 t when the q-axis current reference is 6 [A]. As ZVV usage and transitions between VVs were not considered, the CMV ranges up to the maximum value of  $\pm 70/2$  [V]. In the case of MPC, where VVs are used without restriction to synthesize the reference VV, a low THD can be obtained; however, it should be noted that a peak CMV occurs.

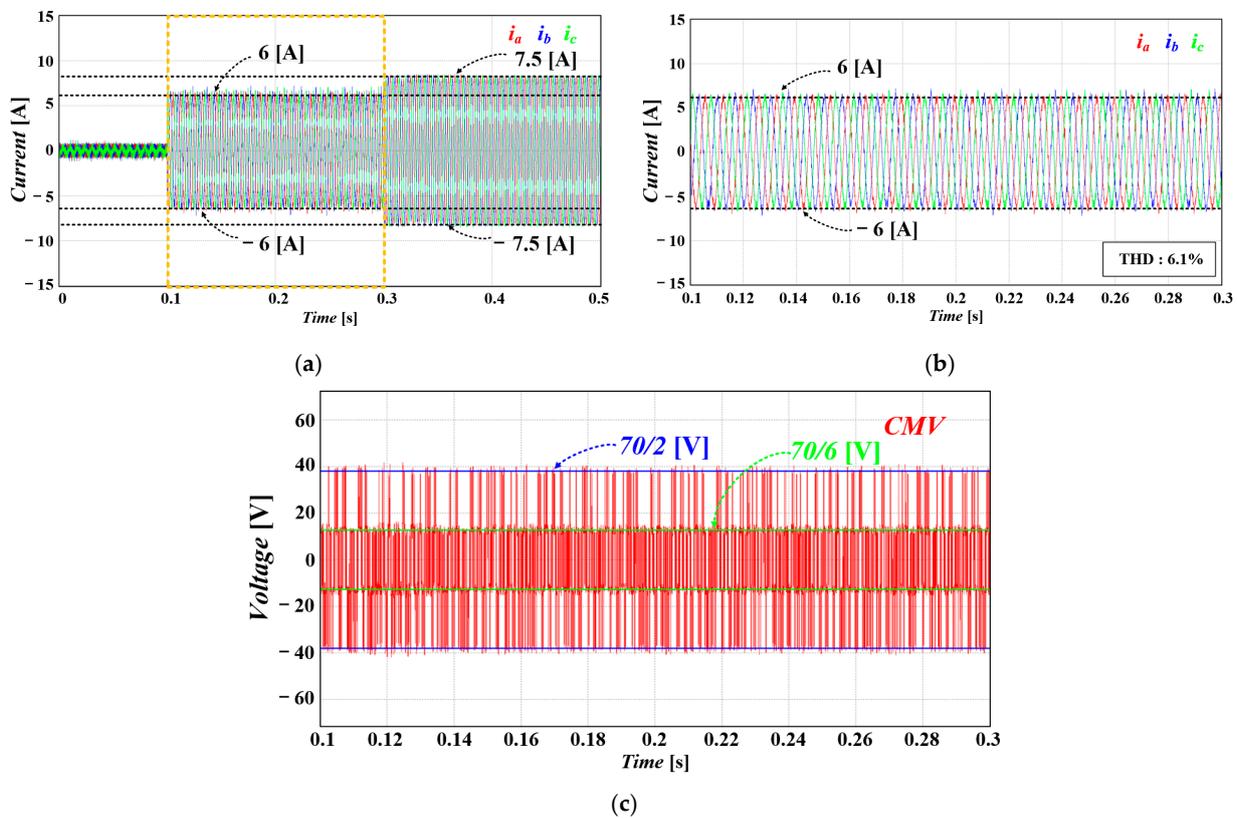


**Figure 10.** Simulation results of FCS-MPC for current control with both ZVVs and non-ZVVs applied: (a)  $i_a$ ,  $i_b$ , and  $i_c$ ; (b) magnified waveforms of (a); and (c) CMV.

### 5.2. FCS-MPC Excluding ZVV

Figure 11 shows the simulation results of FCS-MPC using only non-ZVVs. The sampling frequency was fixed at 10 kHz for comparison with that described in Section 5.1.

Figure 11b shows that the current THD is 6.1%, which is higher than that shown in Figure 10b. Because of the process of synthesizing the reference VV excluding ZVVs, VVs other than ZVVs were selected as the optimal VV and applied, leading to increased current error. This means that VVs with larger cost functions than those in Section 5.1 are selected as the optimal VV.



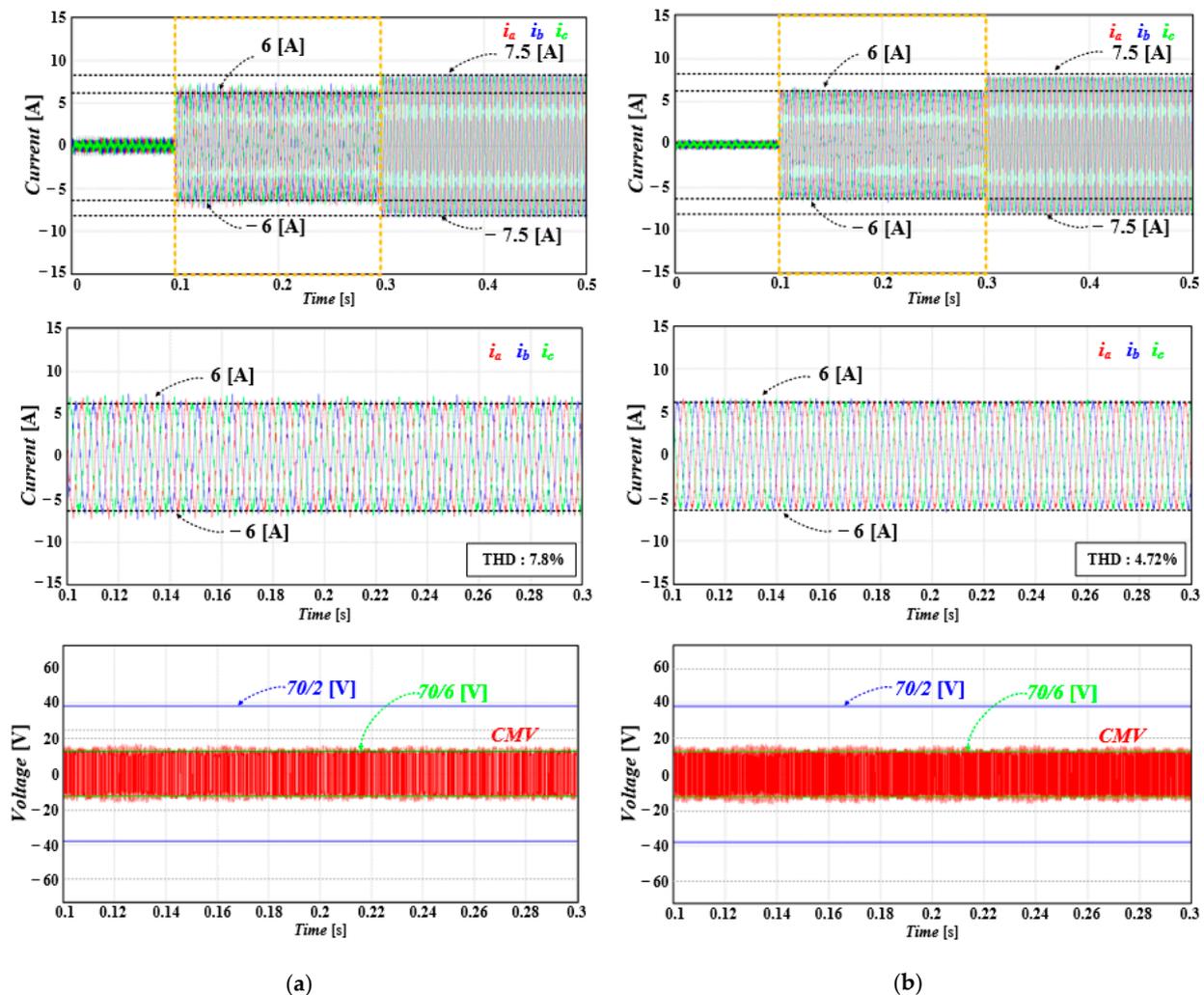
**Figure 11.** Simulation results of FCS-MPC using only non-ZVVs: (a)  $i_a$ ,  $i_b$ , and  $i_c$ ; (b) magnified waveforms of (a); and (c) CMV.

Figure 11c shows the CMV when synthesizing the command voltage excluding non-ZVVs. Excluding ZVVs reduced the occurrence of CMV with the maximum value of  $\pm 70/2$  [V]. However, because vector combinations with the same circuit as ZVVs were not excluded during the dead time interval, the resulting peak CMV remained unresolved.

### 5.3. FCS-MPC Excluding ZVV with the Consideration of Dead Time (Sampling Frequencies: 10 kHz, 20 kHz)

Figure 12 shows the simulation results of FCS-MPC using only non-ZVVs and considering the dead time interval. In addition, simulations were conducted by changing the sampling frequency to 10 and 20 kHz to compare the results with varying sampling frequencies. Figure 12a represents the simulation results for a sampling frequency of 10 kHz. Only four VVs are available for synthesizing the reference voltage. Therefore, VVs with larger cost functions than those in Section 5.2 must be selected. For example, when  $v(k)$  is  $V_1$ ,  $v(k+1)$  should be selected from  $V_1$ ,  $V_2$ ,  $V_4$ , and  $V_6$ . This is because the selection of other VVs may induce the peak CMV. Therefore, although peak CMV removal was possible, it resulted in a high THD of 7.8%. Figure 12b shows the simulation results when the sampling frequency was increased to 20 kHz to reduce THD. Owing to the higher sampling frequency, the THD of the load current decreased by 3.08% to 4.72% compared to when the sampling frequency was 10 kHz. However, in the case of the FCS-MPC, an increase in sampling frequency implies an increase in switching frequency. Therefore, changing the sampling

frequency to 20 kHz increased the switching losses compared with having the sampling frequency at 10 kHz.



**Figure 12.** Simulation results of FCS-MPC using only non-ZVVs and considering the dead time interval: (a) simulation results with a sampling frequency of 10 kHz and (b) simulation results with a sampling frequency of 20 kHz.

#### 5.4. Proposed FCS-MPC for CMV Reduction with Variable Sampling Frequency

Figure 13 shows the simulation results of the FCS-MPC for CMV reduction with the proposed variable sampling frequency. As shown in Figure 13b, the THD of the load current is improved by 2.92% to 4.88% compared with the conventional method with a fixed sampling frequency of 10 kHz. Furthermore, Figure 13c shows that the proposed method utilizes only non-ZVVs and considers the dead time interval to output future VVs. Therefore, it can perfectly eliminate the peak CMV. Figure 13d shows the ramp function, which resets at each sampling point, and the value before the reset  $i$  indicates the variable sampling period. The proposed method determines the sampling period between the minimum value of 50 [ $\mu$ s] and the maximum value of 100 [ $\mu$ s], and the determined sampling period is when the cost function has a minimum value for both the d-axis and q-axis errors. Therefore, the current error is minimized at the determined sampling points, resulting in a low THD. Consequently, compared to the conventional method with a fixed sampling frequency of 20 kHz, although the THD increased by 0.16%, it had fewer switching.

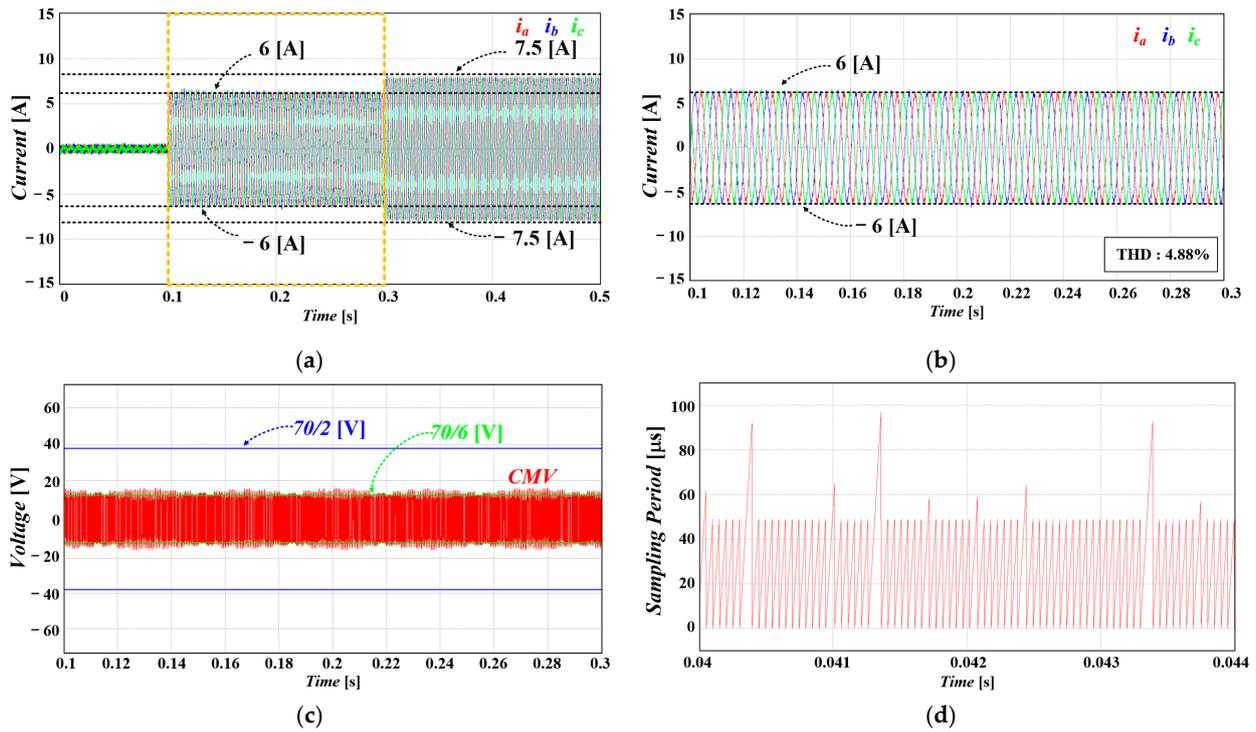


Figure 13. Simulation results of FCS-MPC for CMV reduction with the proposed variable sampling frequency: (a)  $i_a$ ,  $i_b$ , and  $i_c$ ; (b) magnified waveforms of (a); (c) CMV; and (d) sampling period.

### 6. Experimental Results

To validate the performance of the proposed FCS-MPC method, experiments were conducted using a motor-generator (M-G) set. Figure 14 illustrates the M-G set and 2L-VSI used in the experiment. The experimental parameters were identical to the simulation parameters, and the proposed algorithm was implemented using a TMS320F28377S from Texas Instruments (Dallas, TX, USA). Using the proposed method, the load motor (DC motor) was controlled in the speed control mode, whereas the target motor, a PMSM, was controlled in the torque control mode.

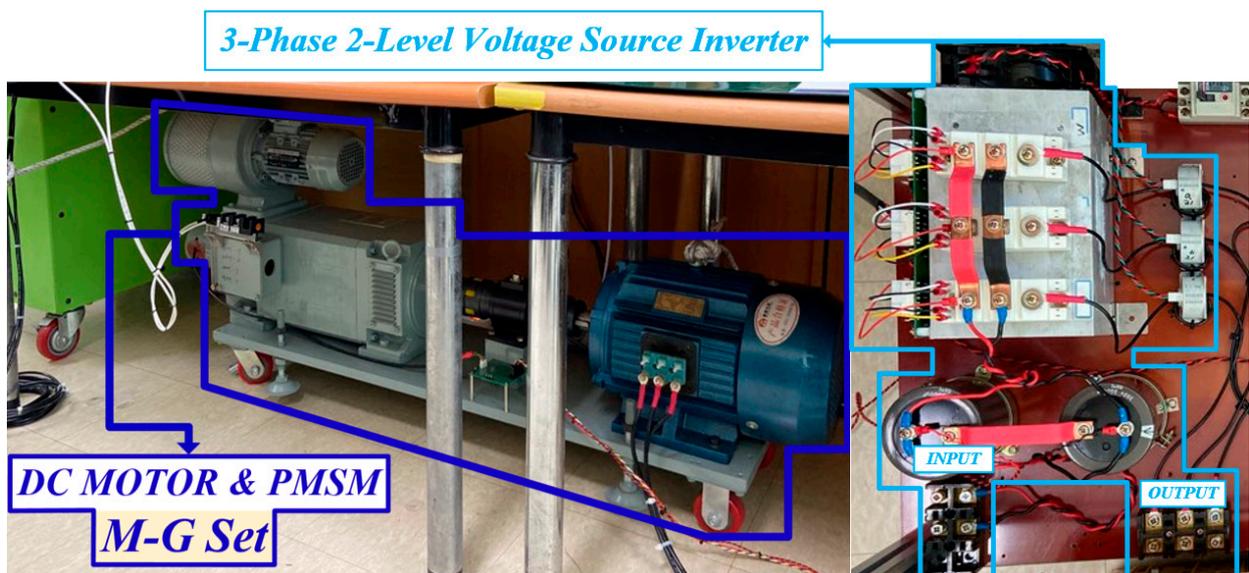
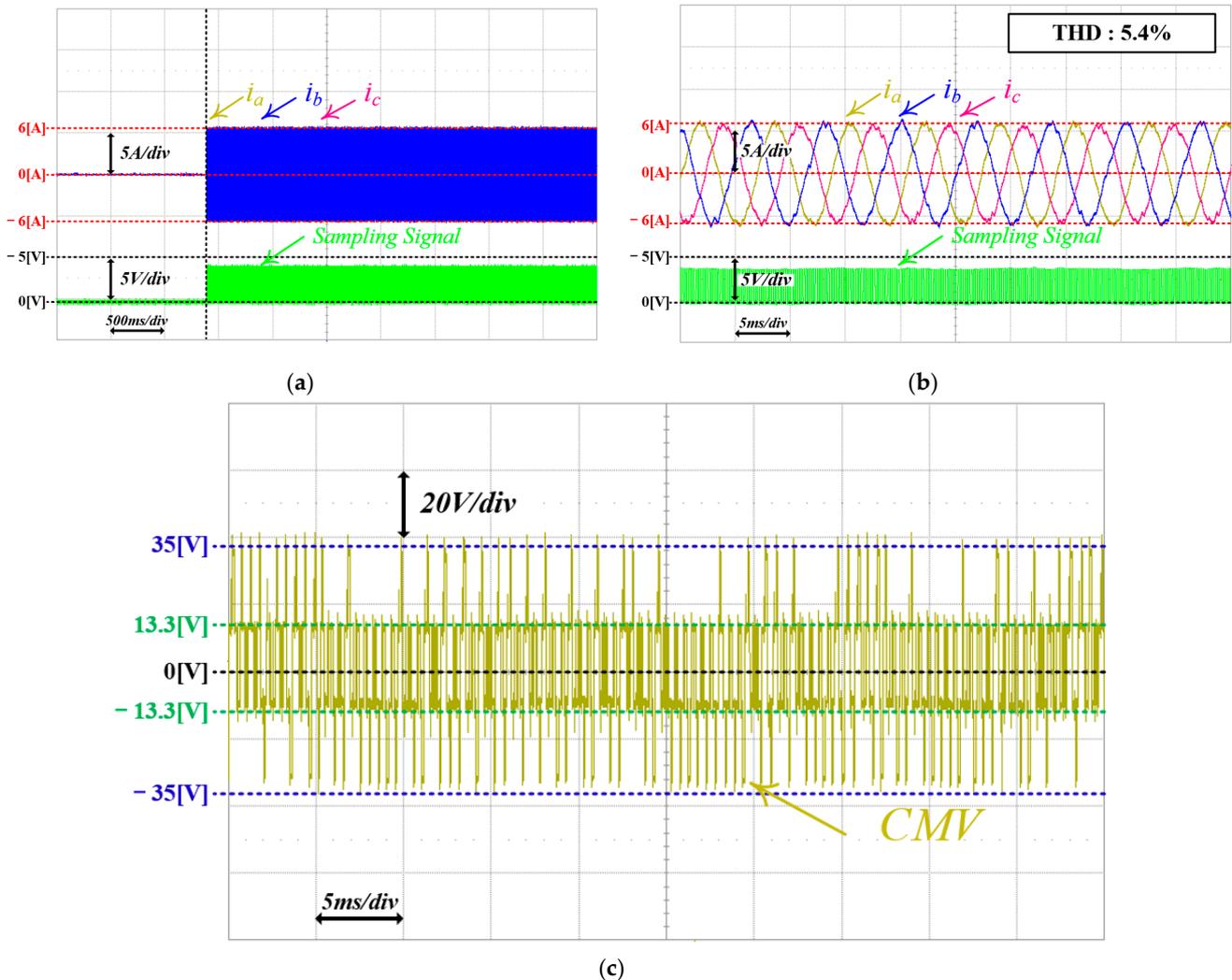


Figure 14. Experiment equipment and 2L-VSI.

### 6.1. FCS-MPC for Current Control

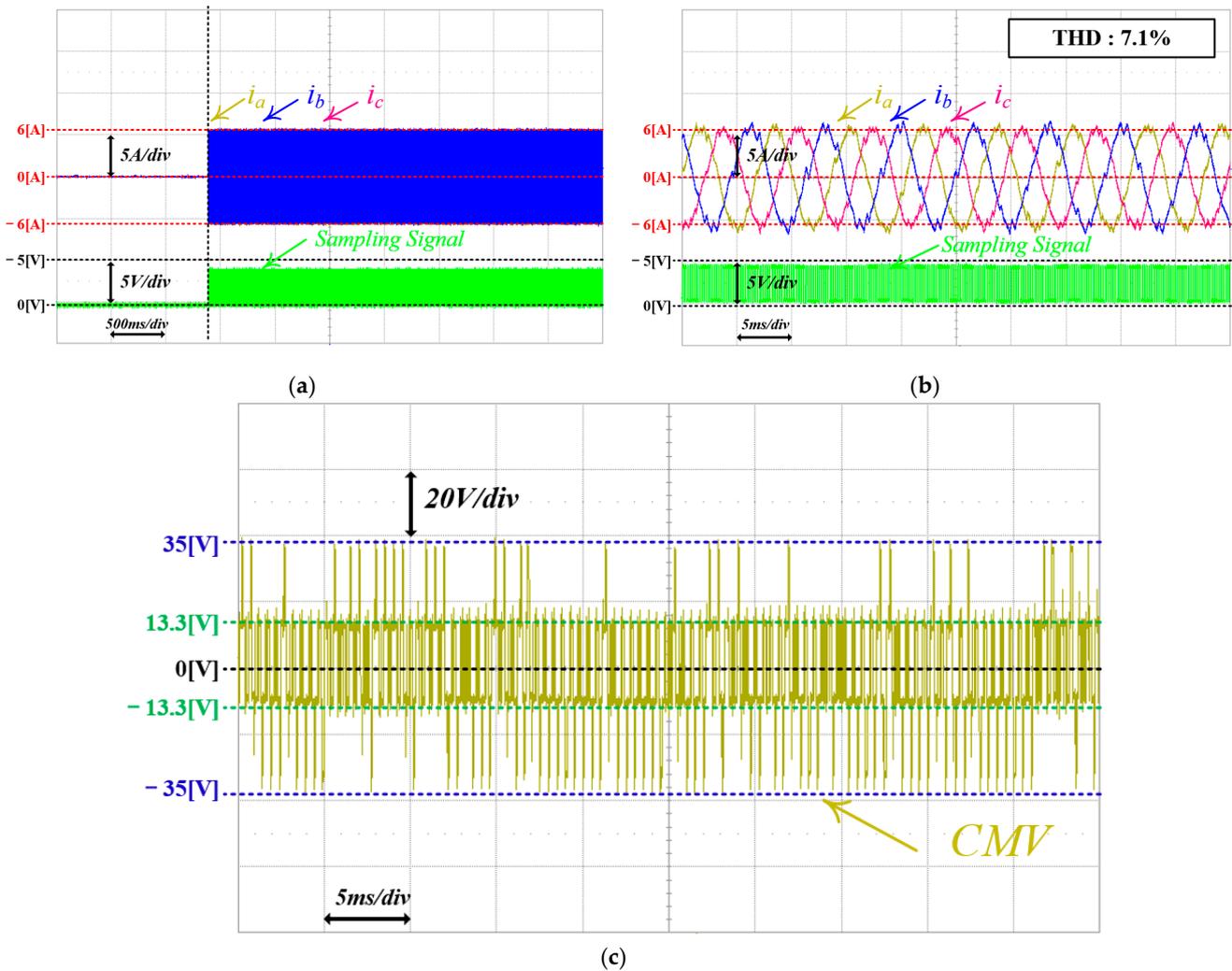
Figure 15 shows the experimental results for the FCS-MPC with current control at 750 [rpm]. Figure 15b shows a magnified waveform of Figure 15a. As shown in Figure 15, the FCS-MPC for current control determines the optimal VVs without constraints on the VV selection. Therefore, the THD of the load current was 5.4%. Figure 15c illustrates the CMV of FCS-MPC for current control. Due to unrestricted VV selection, peak CMV occurring at the ZVV or dead time intervals is not mitigated, resulting in  $\pm V_{dc}/2$  being observed.



**Figure 15.** Experimental waveforms for FCS-MPC for current control: (a)  $i_a$ ,  $i_b$ ,  $i_c$ , and sampling signal; (b) magnified waveforms of (a); and (c) CMV.

### 6.2. FCS-MPC Excluding ZVV

Figure 16 shows the experimental results for FCS-MPC, excluding the ZVV, in the reference VV synthesis. As shown in Figure 16b, which is an enlarged waveform of Figure 16a, this method excludes the selection of the ZVV in the reference VV synthesis process, resulting in larger current errors compared to the method that synthesizes using all VVs. Consequently, it exhibited a the load current THD of 7.1%, which was 1.7% higher than that of the FCS-MPC for current control. Figure 16c illustrates the CMV of the FCS-MPC excluding the ZVV. In comparison with Figure 15c, although fewer occurrences of peak CMV were visible owing to the exclusion of the ZVV in the command VV synthesis, the complete elimination of the peak CMV was not achieved, as it still includes cases with CMV during dead time intervals.



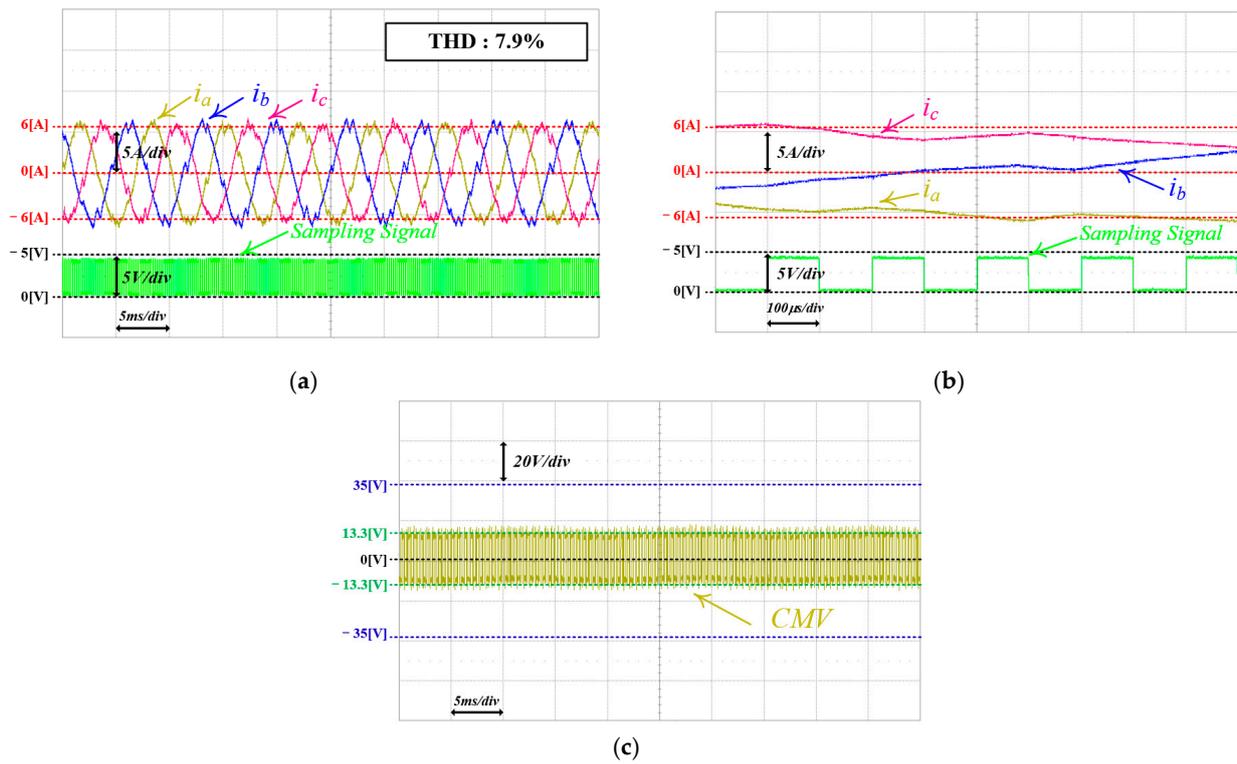
**Figure 16.** Experimental waveforms of FCS-MPC excluding ZVV: (a)  $i_a$ ,  $i_b$ ,  $i_c$ , and sampling signal; (b) magnified waveforms of (a); and (c) CMV.

### 6.3. FCS-MPC Excluding ZVV with the Consideration of Dead Time Interval (Sampling Frequencies: 10 kHz, 20 kHz)

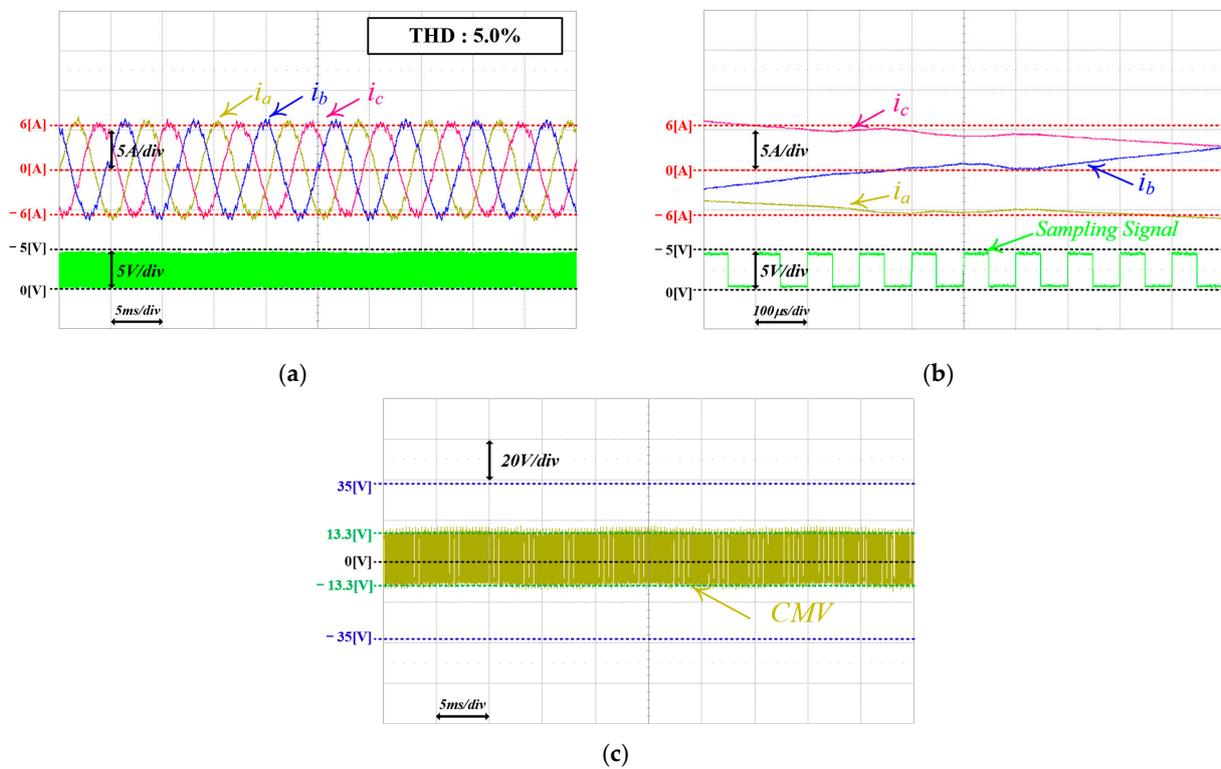
Figure 17 depicts the experimental results of FCS-MPC for CMV reduction using only non-ZVVs, considering dead time intervals, with a sampling frequency of 10 kHz. This approach synthesizes the reference VVs, excluding ZVVs. Additionally, by excluding the switching state transitions that cause the peak CMV during the dead time interval, the options for selecting future VVs were minimized to four. Therefore, as shown in Figure 17a, the THD of the load current is relatively high at 7.9%.

Figure 18 depicts the experimental results of the same FCS-MPC implementation as shown in Figure 17, but with an increased sampling frequency of 20 kHz. Compared to the case with a sampling frequency of 10 kHz, the THD of the load current decreased from 2.9% to 5.0%. However, this reduction was accompanied by an increase in CMV fluctuations and switching frequency.

All possible cases in which the CMV occurred were excluded from both sets of experiments presented in this subsection. Therefore, the CMV is always limited to approximately  $\pm 13.3$  [V], rather than  $\pm V_{dc}/2$  or  $\pm V_{dc}/6$ , ensuring that the CMV does not reach  $+V_{dc}/2$  or  $-V_{dc}/2$ .



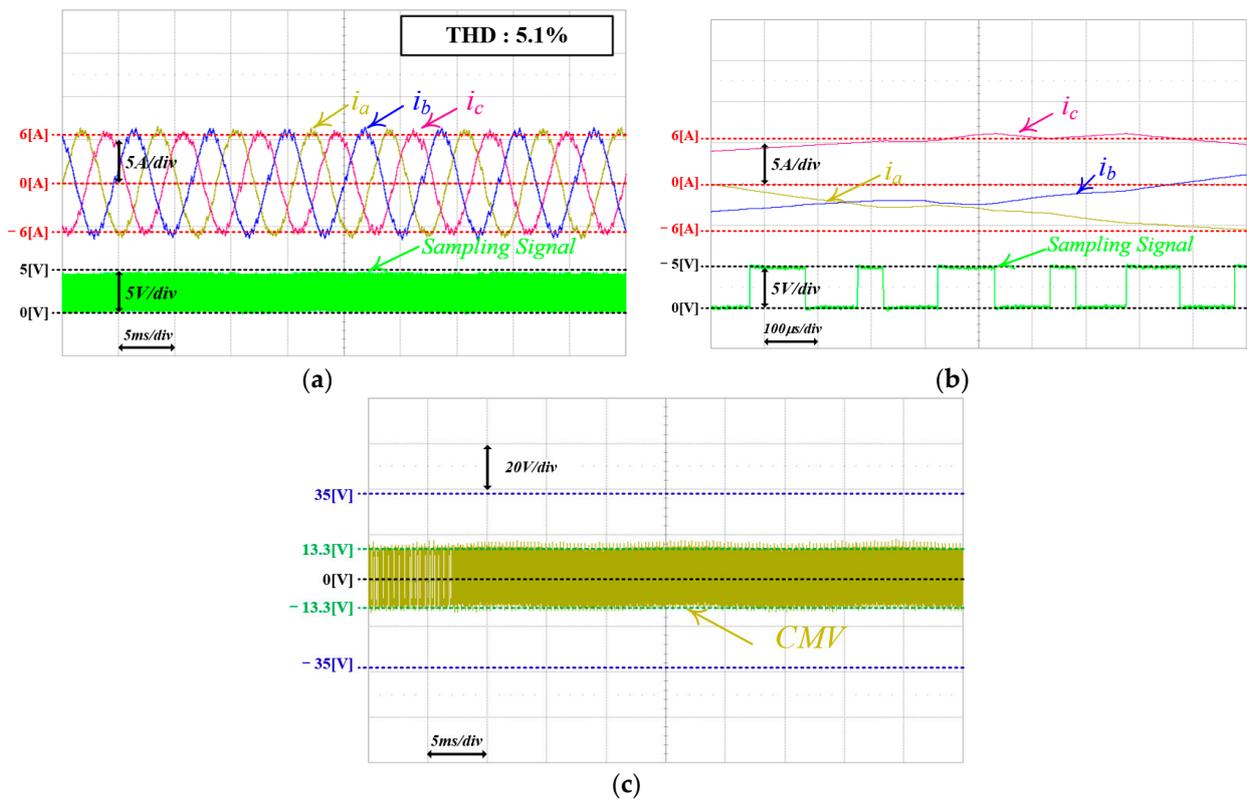
**Figure 17.** Experimental waveforms of FCS-MPC for CMV reduction using only non-ZVVs, considering dead time intervals (sampling frequency: 10 kHz): (a)  $i_a$ ,  $i_b$ ,  $i_c$ , and sampling signal; (b) magnified waveforms of (a); and (c) CMV.



**Figure 18.** Experimental waveforms of FCS-MPC for CMV reduction using only non-ZVVs, considering dead time intervals (sampling frequency: 20 kHz): (a)  $i_a$ ,  $i_b$ ,  $i_c$ , and sampling signal; (b) magnified waveforms of (a); and (c) CMV.

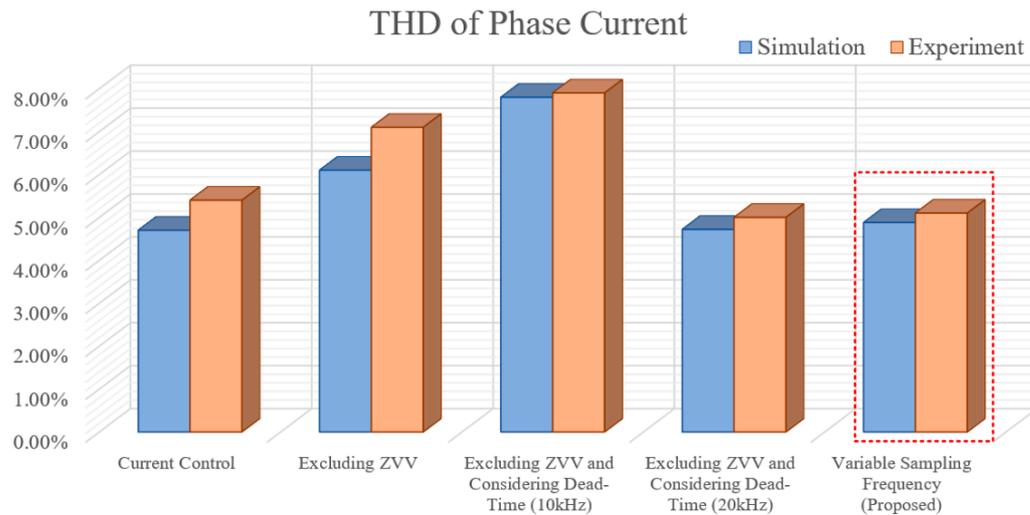
#### 6.4. Proposed FCS-MPC for CMV Reduction with Variable Sampling Frequency

Figure 19 illustrates the experimental results of the FCS-MPC with the proposed variable sampling frequency for CMV reduction. As shown in Figure 19a, the proposed approach predicts and measures the points with the smallest current errors on the d-axis and q-axis, thereby ensuring a low THD. Consequently, the THD of the load current with the proposed approach was 5.1%, which is 2.8% lower than that shown in Figure 17a. In Figure 19b, though slightly higher by 0.1% compared to that in Figure 18a, the sampling period is variable between 50 and 100 [ $\mu$ s], and there are fewer switching than in Figure 18b. Moreover, to limit the CMV to within  $\pm 13.3$  [V], the number of selectable future VVs was maintained at four. Thus, as shown in Figure 19c, applying the proposed method results in a maximum CMV of  $|\pm 13.3|$  [V].



**Figure 19.** Experimental waveforms of the FCS-MPC with the proposed variable sampling frequency for CMV reduction: (a)  $i_a$ ,  $i_b$ ,  $i_c$ , and sampling signal; (b) magnified waveforms of (a); and (c) CMV.

Figure 20 presents a comparison of the THD of the load currents for various FCS-MPC methods implemented through simulation and experimental results in this article. When compared to the FCS-MPC method for CMV reduction with a sampling frequency of 10 kHz, both in the simulation and experimental results, the THD of load currents with the proposed method decreased by over 2.8%. While the THD of the load currents slightly increased by approximately 0.1% compared to that of the FCS-MPC method for CMV reduction with a sampling frequency of 20 kHz, the switching state changes decreased from 92 to 76 per load current cycle.



**Figure 20.** FCS-MPC algorithm for CMV reduction with proposed variable sampling time.

## 7. Conclusions

This article proposes a variable sampling frequency-based FCS-MPC method with CMV reduction. For reference VV synthesis, both ZVV and VV transitions with the same circuit as the ZVV during the dead time interval were excluded. As a result, although the number of selectable future VVs decreased to four, it was possible to eliminate the peak CMV. Additionally, by confirming the intersection of the reference current and the predicted future current and deriving the point where the cost function composed of the  $d$ -axis and  $q$ -axis current errors is minimized, sampling is changed to that point. As shown in Table 4, this variable sampling compensates for the increase in the THD of the load current caused by the reduced options for the future VVs by up to 2.8% compared to a fixed sampling frequency of 10 kHz. Moreover, compared to a fixed sampling frequency of 20 kHz, it has a slightly higher load current THD, and the advantage of reducing the number of switching state changes by 16 per cycle of load current. The performance of the proposed FCS-MPC was validated by comparing it with the simulation and experimental results of conventional methods. The proposed method provides a good solution for reducing the current THD and minimizing the switching frequency.

**Table 4.** Comparison between conventional and proposed methods.

Methods	Current Control	Excluding ZVV	Excluding ZVV and Considering Dead Time (10 kHz)	Excluding ZVV and Considering Dead Time (20 kHz)	Variable Sampling Frequency (Proposed)
THD of Load Current	5.4%	7.1%	7.9%	5.0%	5.1%
Switching State Changes	46	47	45	92	76

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