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A Three-Phase Multilevel Inverter Synthesized with 31 Levels and Optimal Gating Angles Based on the GA and GWO to Supply a Three-Phase Induction Motor

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Abstract: A three-phase multilevel inverter (MLI), synthesized with 31 levels in regard to its output voltage, is used to provide the AC supply to a three-phase, squirrel cage induction motor. The gating angles required for the 30 power switches on the MLI are optimized using both the genetic algorithm (GA) and the grey wolf optimizer (GWO), in which the optimal angles are determined through solving the trigonometric equations taken from Fourier analysis to target the minimum total harmonic distortion (THD) at the MLI output. A simulation model and an experimental prototype are developed for performance analysis and validation. The results demonstrate that the MLI is effectively able to produce 31 levels of three-phase AC output voltage, with the THD not exceeding 5% when loaded with a resistive load and a three-phase induction motor. The voltage and current are measured and recorded for different loads and operating conditions, including the amount of energy consumed by the load. The results of the frequency analysis demonstrate that most of the triple harmonics, which can harm the efficiency of the inverter, are cancelled.

Keywords: DC/AC (inverter); power converter; GA algorithm; GWO algorithm; induction motor

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1. Introduction

Three-phase multilevel inverters (MLIs) are used in applications that require a medium or high level of electrical power [1,2]. The control circuit in these inverters changes the output voltage through changing the number of levels used and the frequency of the output voltage, making them important power sources in many electrical systems. One of the main tasks in MLI applications is the need to power a three-phase induction motor, which are widely employed in numerous applications [3,4]. Recently, these inverters have been used in important applications in the field of renewable energy [5–7]; furthermore, they are also an essential component in the modern vehicle industry [8]. Researchers have been working hard to develop efficient controllers for inverters through enhancing the gating signals for the switches and reducing the number of switches required, to achieve the minimum amount of losses resulting from on and off states [9–14]. In this research, a three-phase MLI with 31 levels is designed, simulated, and implemented, using a Spartan 3E FPGA controller with an optocoupler, in order to drive the switches in a three-phase inverter. The genetic algorithm [15,16] and the grey wolf optimization algorithm [17,18] are employed as artificial intelligence techniques to solve and optimize the switching angles in this three-phase MLI. The remainder of this paper is organized as follows: The proposed topology of the three-phase MLI is shown in Section 2. The details of the methods employed are presented in Section 3. A MATLAB simulation analysis and its results are discussed in

Section 4. A prototype and the experimental results are presented in Section 5 and, finally, the conclusions from the work are provided in Section 6.

2. Multilevel Inverter Topologies

Researchers are contributing to design topologies to reduce the switch count in MLIs for better utilization of such inverters and higher efficiency. The classification of these topologies in terms of the structure and selection, for medium power inverters and for PV energy system applications, has been a valuable consideration in recent decades. A basic unit in the proposed three-phase inverter topology is based on a basic unit reported by [19], and in recent times it is known as a hexagonal switch cell (HSC), as shown in Figure 1. An extended HSC unit with four DC sources, as reported by [20], is shown in Figure 2. The topology has the merits of a simplified structure. The maximum output voltage is (E_{S2} + E_{R2}) and the minimum output voltage is −(E_{S2} + E_{R2}). This topology can easily be extended to include a higher number of levels. It only requires unidirectional switches. E_{S1} and E_{R1} cannot be switched on together as an addition or subtraction. The same applies to E_{S2} and E_{R2}. By selecting E_{S1} = Vdc, E_{S2} = 5Vdc, E_{R1} = 2Vdc, and E_{R2} = 10Vdc, a 31-level output voltage can be produced.

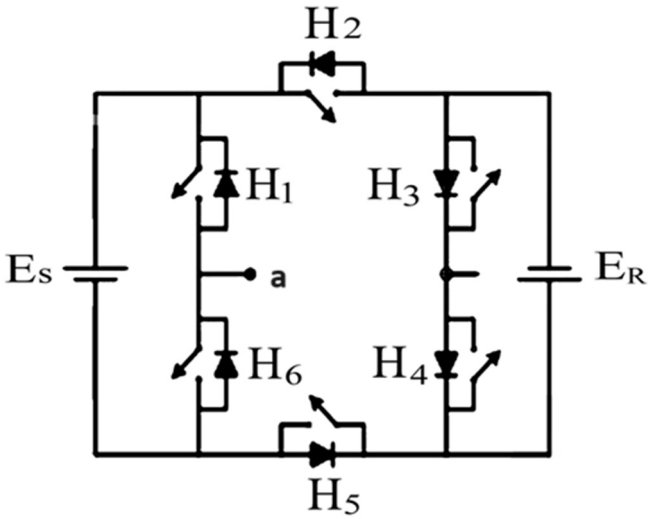


Figure 1. Basic unit in the inverter structure.

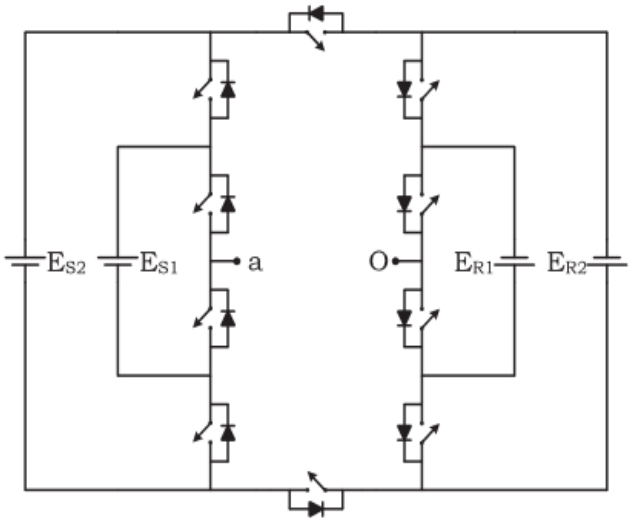


Figure 2. Extended HSC unit.

A comparison of different basic units in a cascaded connection is shown in Table 1, in terms of the number of levels, number of switches, number of DC sources, number of phases (single or three-phase inverter), and advantages and disadvantages.

Table 1. Basic units in a cascaded connection.

Topology	No. of Levels	No. of Switches	No. of DC Sources	No. of Phases	Advantages	Disadvantages
[19]	7	6	2	1 phase	Simple structure	Isolated DC sources
[21]	9	11	4	1 phase	Cells share power equally	Switches withstand different voltage ratings
[22]	17	12	4	1 phase	Symmetric and asymmetric topology	Complex control
[23]	17	10	4	1 phase	Modular structure	Lower number of switches increases power rating
Proposed/ phase	31	10	4	3 phase	Simple and modular structure suitable for cascaded topologies; requires switches with unidirectional operation	Switches exposed to various voltage ratings

The proposed topology for the three-phase MLI with a reduced number of switches consists of 10 switches (MOSFETs or IGBTs) and 4 DC sources for each single phase, resulting in a total of 30 switches and 12 DC sources for the three-phase implementation, as shown in Figure 3.

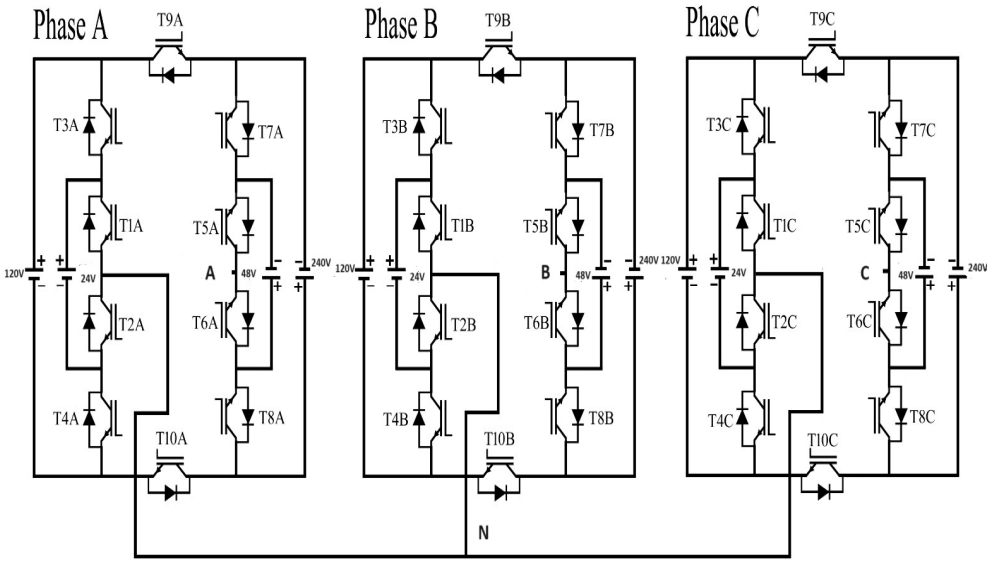


Figure 3. Proposed topology of the three-phase, 31-level MLI.

To illustrate the principle of fabricating the multilevel inverter output, Figure 4 presents the output voltage of a nine-level inverter with four angles (α_1, α_2, α_3, and α_4). These angles are determined by solving trigonometric equations resulting from a Fourier analysis of the output voltage of the inverter. The Fourier series of a staircase periodic function can be expressed [24] as follows:

$$v_0(t) = \frac{a_o}{2} + \sum_{k=0}^{n} a_n \cos(nwt) + b_n \sin(nwt) \quad (1)$$

where a_o is the average value of the output voltage, and a_n and b_n are even and odd components of the periodic staircase signal, respectively. The staircase waveform possesses a quarter wave symmetry, which sets the a_o , a_n and the even b_n values to zero, and simplifies Equation (1) to the following:

$$v_0(t) = \sum_{i=1,3,5,7,9,11.....}^{n} b_n \sin(nwt) \quad (2)$$

$$b_n = \frac{4V_{dc}}{n\pi} \left[\int_{\alpha_1}^{\frac{\pi}{2}} \sin(nwt) d(wt) + \int_{\alpha_2}^{\frac{\pi}{2}} \sin(nwt) d(wt) + \int_{\alpha_{m-1}}^{\frac{\pi}{2}} \sin(nwt) \right] \quad (3)$$

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{k=1,3,5,7,9,11.....}^{m} \cos(n\alpha_k) \quad (4)$$

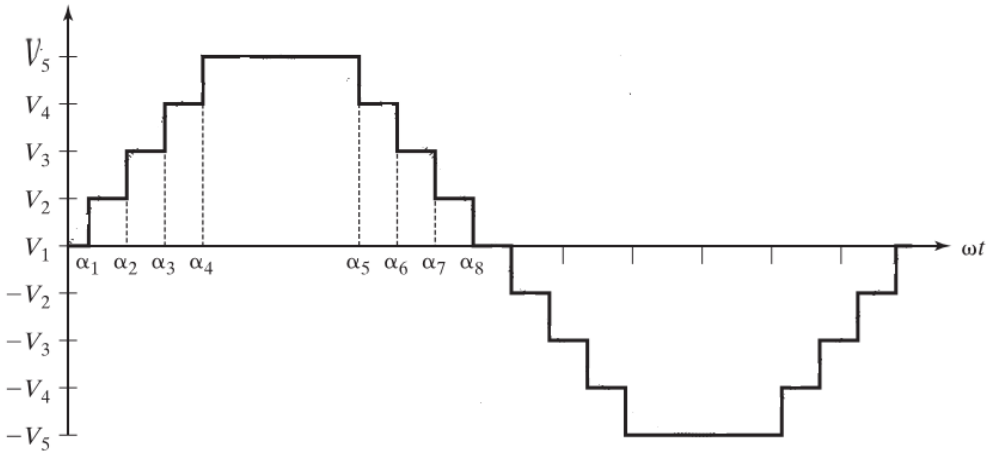


Figure 4. A nine-level inverter and its timing instants.

These equations can be solved for any number of levels in the MLI. In a three-phase system, the triple harmonics (3rd, 9th, 15th . . .) are eliminated implicitly. To eliminate other harmonics (e.g., the 5th, 7th, 9th, and 11th harmonics), the following equations are solved for the optimum values of the gating angles:

$$b_1 = \frac{4V_{dc}}{\pi} \{\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4)\} = V_{fund} \quad (5)$$

$$b_5 = \frac{4V_{dc}}{5\pi} \{\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4)\} = 0 \quad (6)$$

$$b_7 = \frac{4V_{dc}}{5\pi} \{\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4)\} = 0 \quad (7)$$

$$b_{11} = \frac{4V_{dc}}{5\pi} \{\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4)\} = 0 \quad (8)$$

where V_{fund} is the fundamental output voltage. Intelligent algorithms are employed to find the optimal solution for the values of these angles, relying on the selective harmonic elimination (SHE) technique with the restriction $\alpha_1 < \alpha_2 < \frac{\pi}{2}$. The other timing instants for one complete cycle of the output voltage are derived from these two angles.

3. Artificial Intelligence Algorithms

Artificial intelligence (AI) algorithms work efficiently to solve mathematical problems, resulting in an improvement in the performance of engineering systems [25]. In this research, the genetic algorithm (GA) and the grey wolf optimization (GWO) algorithm are used to find the optimum switching angles for the inverter. A curve fitting principle

is employed to determine the optimum solution between these two algorithms. For a three-phase inverter system with 31 levels, 15 angles are required for Phase A, and phase shifts of 120° and 240° are set for Phase B and Phase C, respectively. The inverter is operated at a modulation index of M = 0.7. Other values in the modulation index can be implemented following the same principle, which are summarized in Table 2.

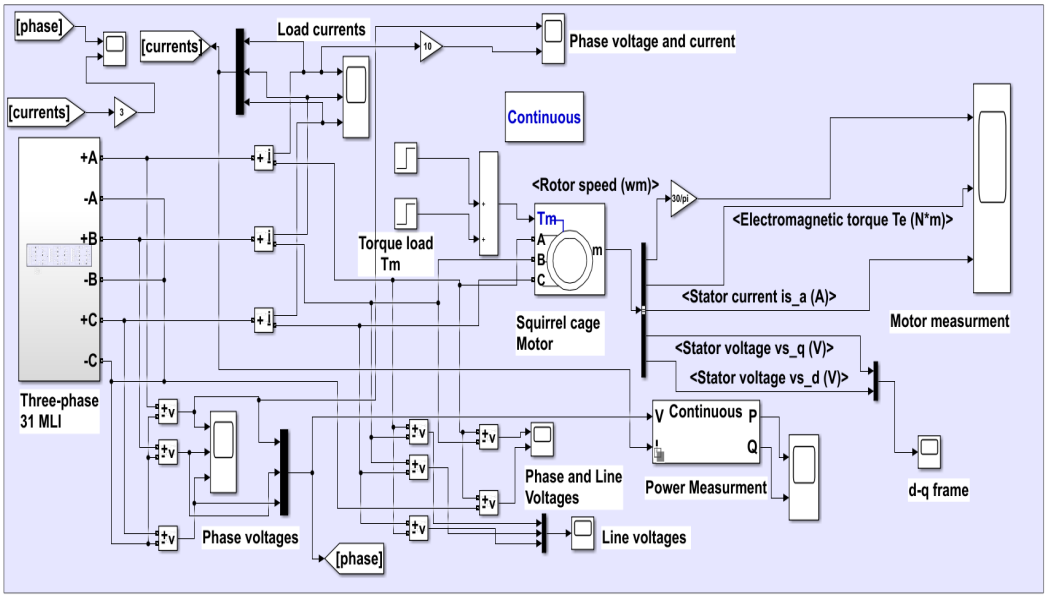
Table 2. Switching angles for a 31-level inverter.

Angle	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}	α_{11}	α_{12}	α_{13}	α_{14}	α_{15}
GA	3.3	6.1	13.1	16.7	23.1	27.2	33.5	38.7	45.5	52.2	58.5	66.2	74.7	83.8	85
GWO	1.2	11.8	23.3	32.2	42.2	50.6	58.9	67.4	71.2	79.6	80.4	85.1	85.9	86	86
Optimum	2.4	5.21	8.42	14.2	16.3	22.6	27.4	31.6	37.1	42.9	50.5	58.4	67.4	78.6	85

4. Results

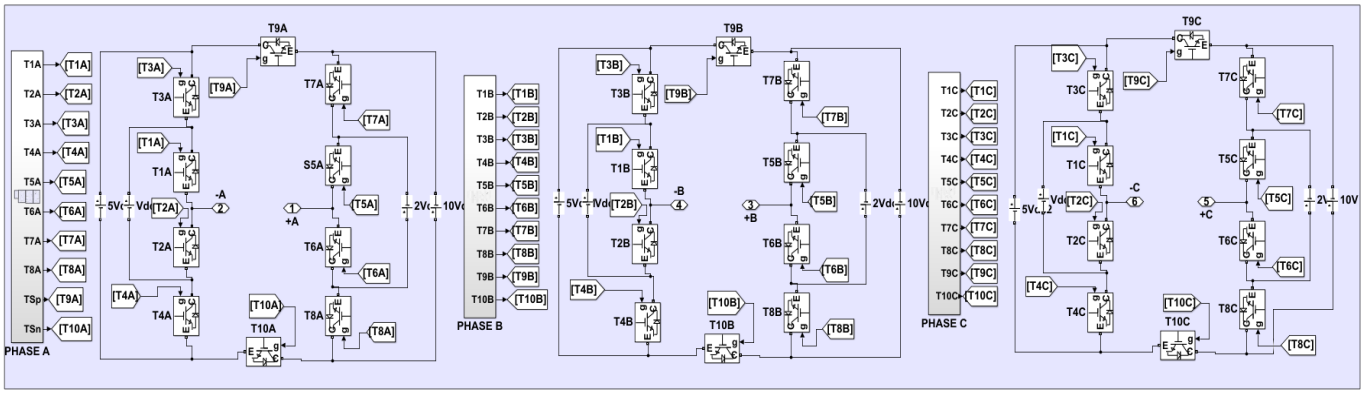
4.1. Simulation Results

The proposed three-phase, 31-level MLI was built and simulated using the MATLAB Simulink software version R2019a, using the optimized angles provided in Table 1. The three single-phase inverters are Y-connected to form a three-phase 50 Hz AC supply source, as shown in Figure 3. Each phase has 10 power switches (IGBTs) and 4 DC sources. The IGBTs work in complementary mode. Switches T2, T4, T6, T8, and T10 complement T1, T3, T5, T7, and T9, respectively. A voltage of V_{DC} = 24 V is used for each staircase level. The other three DC sources are $2V_{DC}$ = 48 V, $5V_{DC}$ = 120 V, and $10V_{DC}$ = 240 V. To generate 31 levels in the inverter output voltage, multiple paths are chosen for the electrical current to pass through the power switches. Here, several DC sources are used; either adding them together, subtracting them from each other, or using individual sources. The peak output phase voltage = 15 (level) × 24 V (one staircase voltage) = 360 V. The peak line voltage = 580 V and $V_{L(RMS)}$ = 410 V. The three-phase induction motor specifications used for the simulation are as follows: squirrel cage (5.4 HP, 4 KW, 50 Hz, 1430 RPM). The Simulink model of the 31-level, three-phase MLI connected to a three-phase squirrel cage induction motor load is shown in Figure 5a. The block diagram consists of three main circuits, each of which has devices attached to measure the voltage, current, and other variables.



(**a**)

Figure 5. *Cont.*



(**b**)

Figure 5. (**a**) Simulink model of the 31-level, three-phase MLI connected to a three-phase motor. (**b**) Simulink model of the three-phase, 31-level MLI showing the gating signals.

The first circuit is a three-phase inverter, as shown in Figure 5b, which consists of a three star-connected single-phase inverter. There are 30 insulated gate bipolar transistors (IGBTs) with diodes and 12 DC sources. The output terminals of the three-phase inverter are points (+A, +B, and +C), while points (−A, −B, and −C) are connected to form the neutral point in the star connection.

The second circuit involves the operation of the switches based on artificial intelligence algorithms and will be detailed later. The load circuit is the third part and consists of a static load represented by a different set of resistors and a dynamic load represented by a three-phase squirrel cage induction motor. The detailed fabrication of the gating periods in Phase A is shown in Table 3; the asterisk (*) represents the complementary mode.

Table 3. Switch state for the positive half period.

T1 T2 *	T3 T4 *	T5 T6 *	T7 T8 *	T9 T10 *	Level	Duration	Shift
1	1	1	1	1	0	α_1	0
0	1	1	1	1	1	$\alpha_2 - \alpha_1$	α_1
1	1	0	1	1	2	$\alpha_3 - \alpha_2$	α_2
0	1	0	1	1	3	$\alpha_4 - \alpha_3$	α_3
1	0	1	1	1	4	$\alpha_5 - \alpha_4$	α_4
0	0	1	1	1	5	$\alpha_6 - \alpha_5$	α_5
1	0	0	1	1	6	$\alpha_7 - \alpha_6$	α_6
0	0	0	1	1	7	$\alpha_8 - \alpha_7$	α_7
1	1	1	0	1	8	$\alpha_9 - \alpha_8$	α_8
0	1	1	0	1	9	$\alpha_{10} - \alpha_9$	α_9
1	1	0	0	1	10	$\alpha_{11} - \alpha_{10}$	α_{10}
0	1	0	0	1	11	$\alpha_{12} - \alpha_{11}$	α_{11}
1	0	1	0	1	12	$\alpha_{13} - \alpha_{12}$	α_{12}
0	0	1	0	1	13	$\alpha_{14} - \alpha_{13}$	α_{13}
1	0	0	0	1	14	$\alpha_{15} - \alpha_{14}$	α_{14}
0	0	0	0	1	15	$\pi - 2\alpha_{15}$	α_{15}
1	0	0	0	1	14	$\alpha_{15} - \alpha_{14}$	$\pi - \alpha_{15}$
0	0	1	0	1	13	$\alpha_{14} - \alpha_{13}$	$\pi - \alpha_{14}$
1	0	1	0	1	12	$\alpha_{13} - \alpha_{12}$	$\pi - \alpha_{13}$
0	1	0	0	1	11	$\alpha_{12} - \alpha_{11}$	$\pi - \alpha_{12}$
1	1	0	0	1	10	$\alpha_{11} - \alpha_{10}$	$\pi - \alpha_{11}$
0	1	1	0	1	9	$\alpha_{10} - \alpha_9$	$\pi - \alpha_{10}$

Table 3. *Cont.*

T1 T2 *	T3 T4 *	T5 T6 *	T7 T8 *	T9 T10 *	Level	Duration	Shift
1	1	1	0	1	8	$\alpha_9 - \alpha_8$	$\pi - \alpha_9$
0	0	0	1	1	7	$\alpha_8 - \alpha_7$	$\pi - \alpha_8$
1	0	0	1	1	6	$\alpha_7 - \alpha_6$	$\pi - \alpha_7$
0	0	1	1	1	5	$\alpha_6 - \alpha_5$	$\pi - \alpha_6$
1	0	1	1	1	4	$\alpha_5 - \alpha_4$	$\pi - \alpha_5$
0	1	0	1	1	3	$\alpha_4 - \alpha_3$	$\pi - \alpha_4$
1	1	0	1	1	2	$\alpha_3 - \alpha_2$	$\pi - \alpha_3$
0	1	1	1	1	1	$\alpha_2 - \alpha_1$	$\pi - \alpha_2$
1	1	1	1	1	0	α_1	$\pi - \alpha_1$

A detailed Simulink model of the switching controls is shown in Figure 6. The gating signals for phases B and C are derived from Phase A, by adding phase shifts of 120° and 240°, respectively.

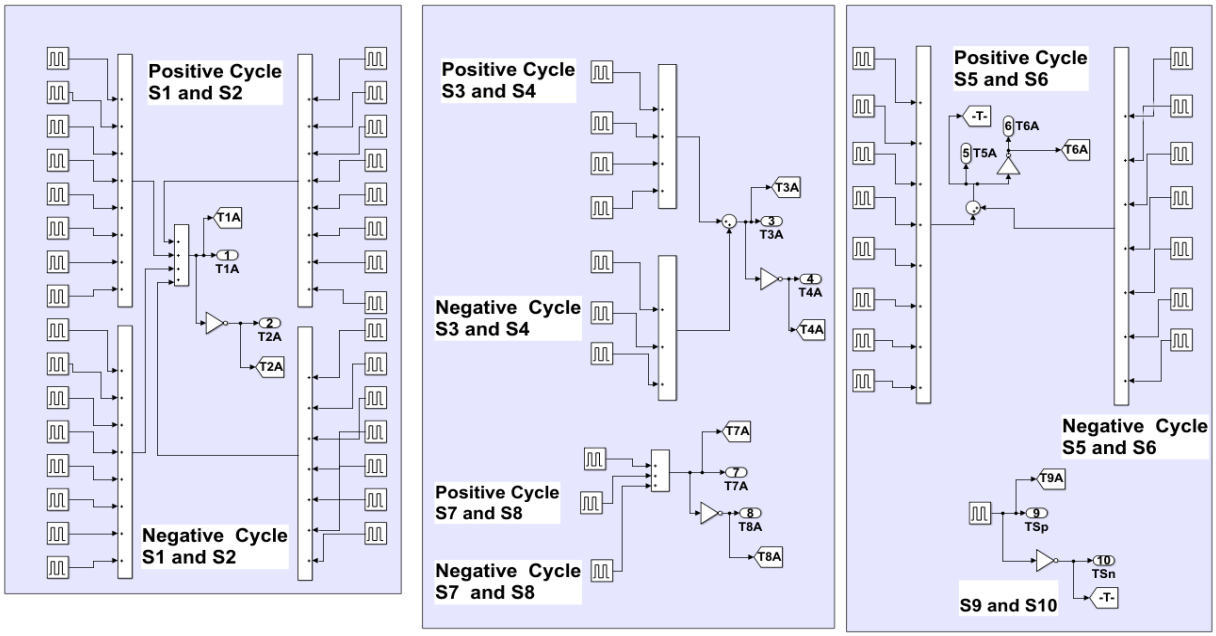


Figure 6. Fabrication of the gating periods for Phase A.

The three-phase output and line voltages for the 31-level MLI are shown in Figure 7 and Figure 8 respectively.

The phase currents supplied by the 31-level MLI to the induction motor are shown in Figure 9. The current from 0 to 1 sec is about 4.25 A (rms) when the motor is operating at no load. When the motor is subjected to an external 20 Nm load at an instance from 1 s to 2 s, the current increases to 11.3 A (rms). Finally, from 2 s to 3 s, the current increases to about 24 A (rms), when the motor is subjected to a 40 Nm load. Figure 10 shows a phase shift of about 36° between the supply voltage and the current, indicating a lagging power factor of 0.81.

Figure 11 shows the measurements for the three-phase squirrel cage induction motor, consisting of the motor speed, electromagnetic torque, and stator current. The motor reaches the base speed of about 1500 rpm at no load. This speed is then reduced because of the external load applied at an instance between 1 s and 2 s. The stator current increases from no load to higher values to reflect the load torque applied. The power consumed consists of active power, P, and reactive power, Q, as shown in Figure 12.

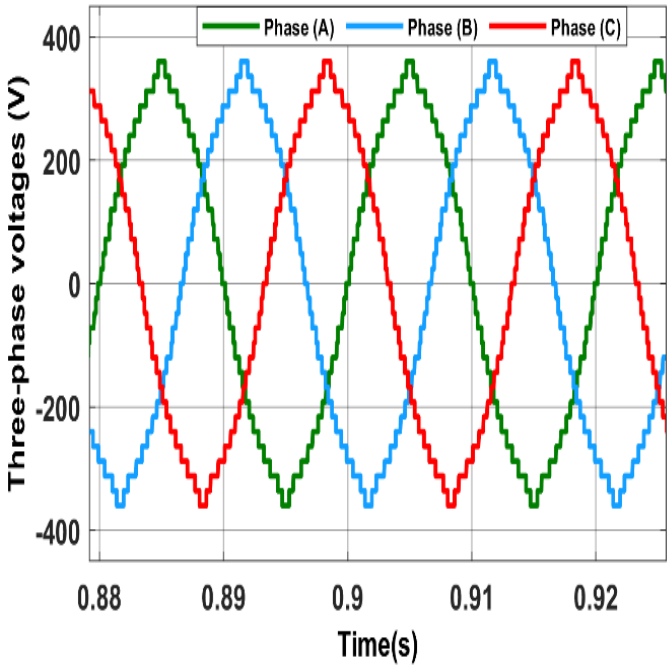


Figure 7. Phase voltages from the simulation.

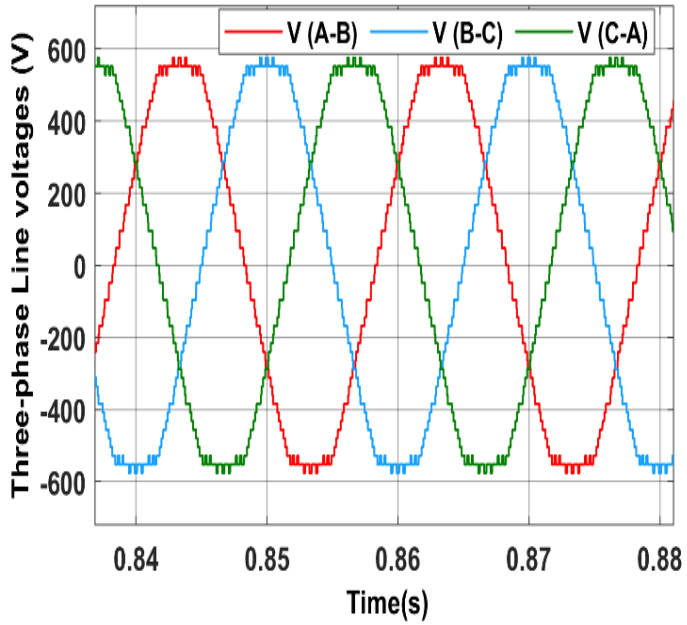


Figure 8. Line voltages from the simulation.

The fast Fourier transform toolbox in the MATLAB software revealed that the harmonic content in the inverter's phase voltage is relatively low; the total harmonic distortion THD is about 4.69%, and the recorded value of the line voltage THD is 4.05%, as shown in Figures 13 and 14, respectively. The motor is considered to be an inductive load that filters some harmonics, resulting in a low harmonic distortion THD of 1.54% for the motor current, as shown in Figure 15. Figure 16 shows values for the DC component = 0.002039 and some of the harmonic contents, which have low values compared to the fundamental 50 Hz component.

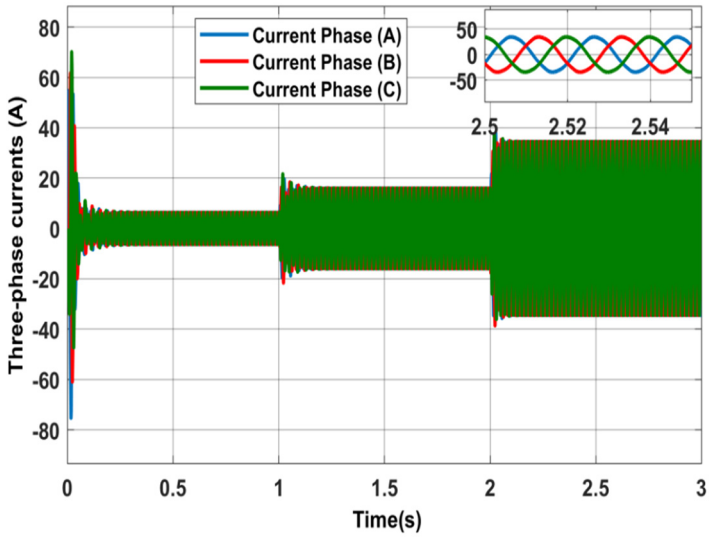


Figure 9. Squirrel cage motor currents.

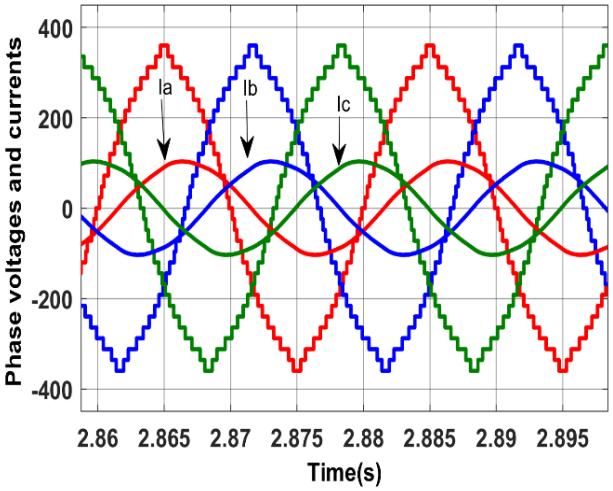


Figure 10. Phase shift between the voltages and currents.

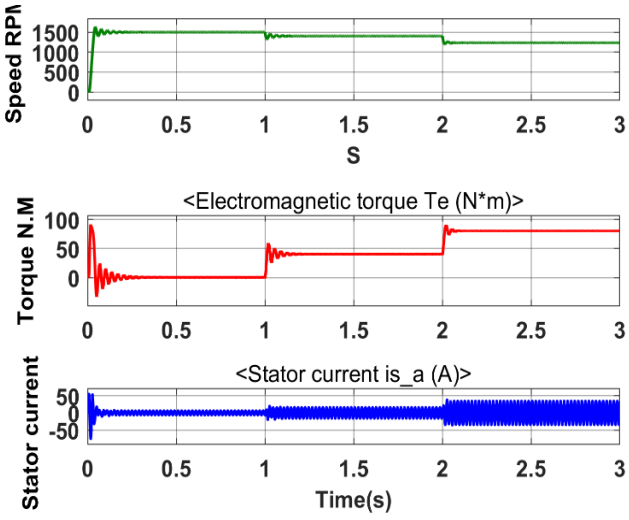


Figure 11. Motor measurements at different loads.

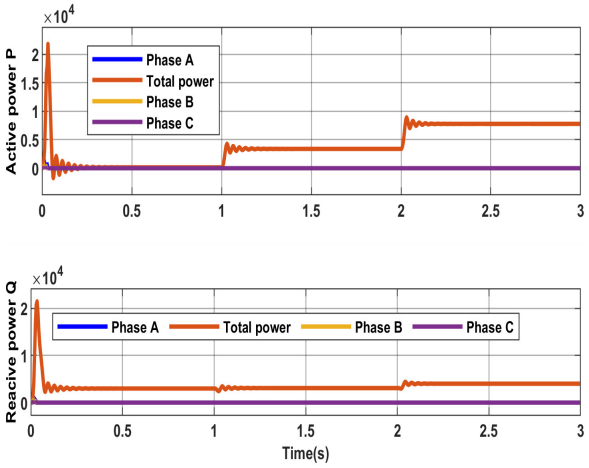


Figure 12. Power consumed by the load.

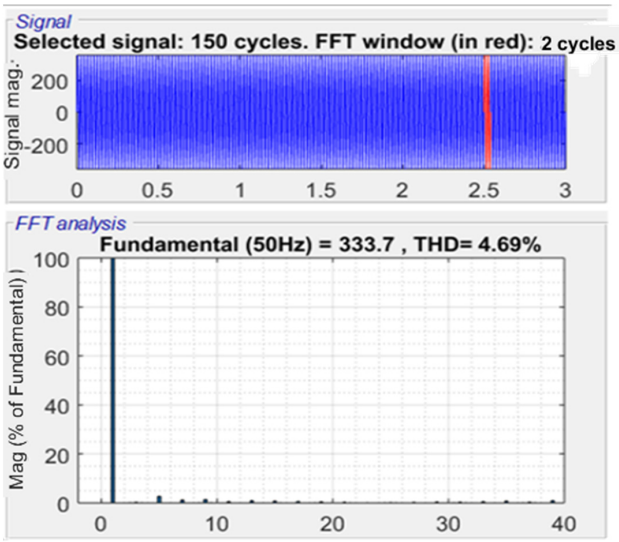


Figure 13. Phase voltage.

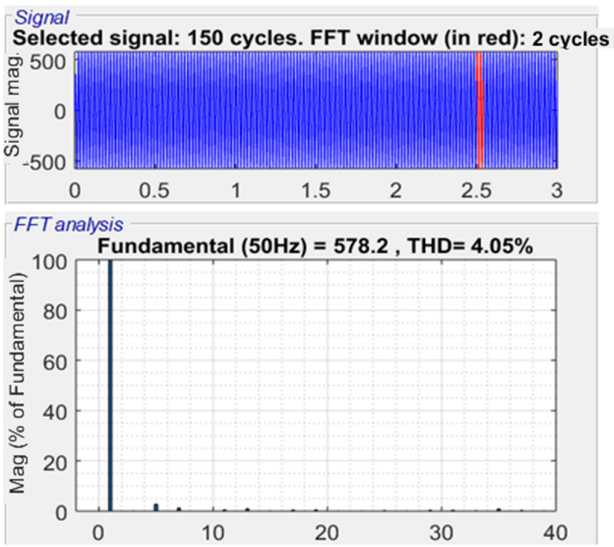


Figure 14. Line voltage harmonic content.

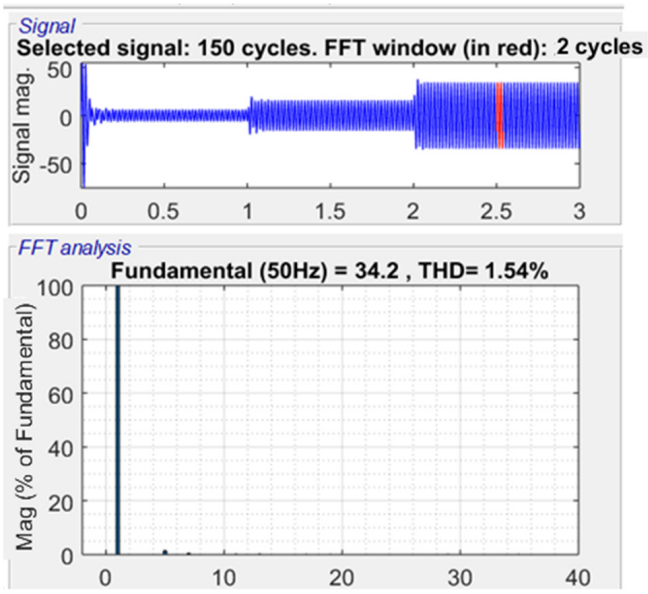


Figure 15. Current harmonic content.

```
Sampling time      = 3.28987e-05 s
Samples per cycle  = 608
DC component       = 0.002039
Fundamental        = 34.2 peak (24.18 rms)
THD                = 1.54%

     0 Hz   (DC):          0.01%    270.0°
    25 Hz                 0.02%    -48.2°
    50 Hz   (Fnd):      100.00%    -28.7°
    75 Hz                 0.03%    160.7°
   100 Hz   (h2):         0.01%    166.2°
   125 Hz                 0.01%    170.1°
   150 Hz   (h3):         0.01%    174.3°
   175 Hz                 0.01%    176.4°
   200 Hz   (h4):         0.01%    181.3°
   225 Hz                 0.00%    193.4°
   250 Hz   (h5):         1.45%    -84.4°
   275 Hz                 0.00%    152.2°
   300 Hz   (h6):         0.00%    159.2°
   325 Hz                 0.00%    156.6°
   350 Hz   (h7):         0.47%     93.5°
   375 Hz                 0.00%    188.0°
   400 Hz   (h8):         0.00%    181.8°
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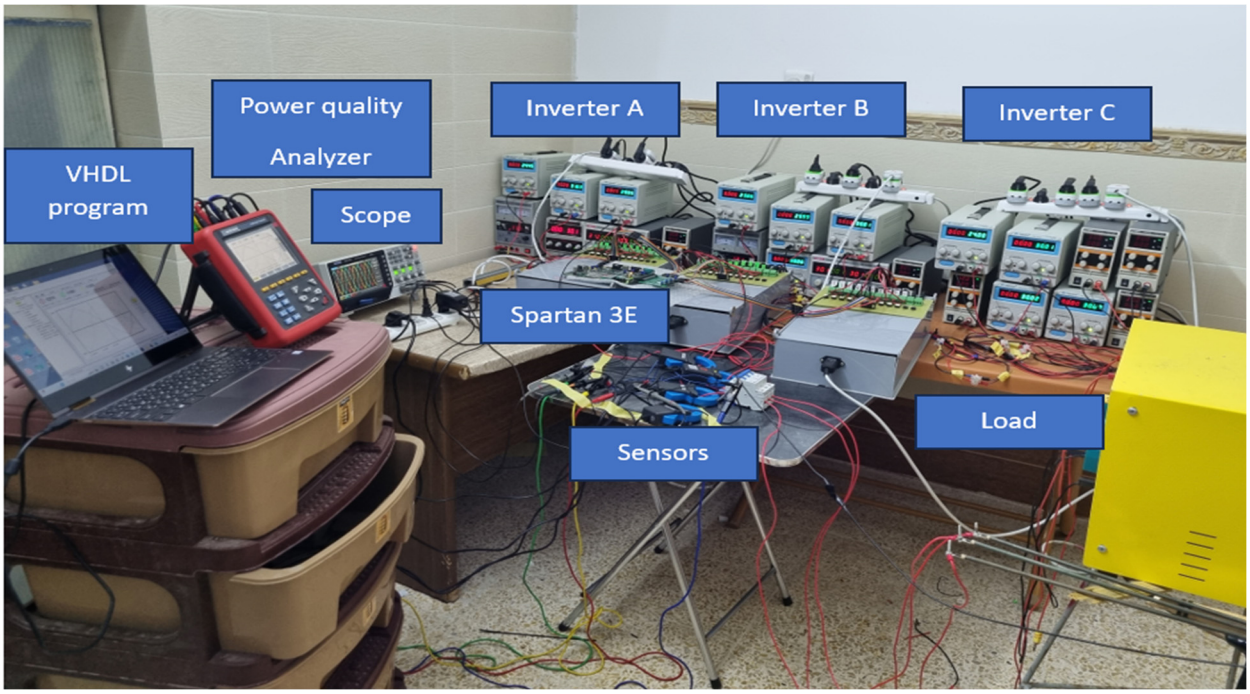
Figure 16. List of harmonics content in inverter current.

4.2. Practical Results

4.2.1. Generating Gating Pulses

The Spartan 3E controller is used as the processor unit in the experiment. The clock frequency of the controller is 50 MHz; therefore, the period of each clock is 20 ns. To cover one 50 Hz AC supply cycle at the inverter output, a total of 20 ms/20 ns = 1,000,000 clocks linked to the Spartan 3E controller are required. A prototype of the proposed three-phase, 31-level MLI is designed and built, as shown in Figure 17a. The operation of 30 switches is programmed using the Spartan 3E controller through writing a program in the VHDL language, then running a simulation such that the appropriate pulses can operate the switches. The simulated pulses for one cycle of operation are shown in Figure 17b.



(**a**)

(**b**)

Figure 17. (**a**) Experimental set up for the implementation of the proposed three-phase, 31-level MLI. (**b**) Spartan 3E simulated pulses for the IGBTs.

The corresponding number of pulses for each optimized angle, as shown in Table 1, is provided in Table 4.

Table 4. Corresponding pulse counts by the Spartan 3E clocks for the 15 angles.

α_1 = 6778	α_2 = 14,472	α_3 = 23,389	α_4 = 39,472	α_5 = 45,445	α_6 = 62,889	α_7 = 76,278	α_8 = 87,917
α_9 = 103,056	α_{10} = 119,222	α_{11} = 140,361	α_{12} = 162,278	α_{13} = 187,389	α_{14} = 218,445	α_{15} = 236,111	

Table 5 details the IGBT states for the positive half cycle of Phase A. The IGBT states for phases B and C are determined by considering a 120° phase shift between the three phases. The asterisk (*) represents the complementary mode.

Table 5. IGBT states for the positive half cycle of phase A.

	T1	T3	T5	T7	T9	Duration	
	T2 *	T4 *	T6 *	T8 *	T10 *		PHASE A
1	1	1	1	1	1	α_1	$0 \rightarrow 6778$
2	0	1	1	1	1	$\alpha_2 - \alpha_1$	$6779 \rightarrow 14{,}472$
3	1	1	0	1	1	$\alpha_3 - \alpha_2$	$14{,}473 \rightarrow 23{,}389$
4	0	1	0	1	1	$\alpha_4 - \alpha_3$	$23{,}390 \rightarrow 39{,}472$
5	1	0	1	1	1	$\alpha_5 - \alpha_4$	$39{,}473 \rightarrow 45{,}445$
6	0	0	1	1	1	$\alpha_6 - \alpha_5$	$45{,}446 \rightarrow 62{,}889$
7	1	0	0	1	1	$\alpha_7 - \alpha_6$	$62{,}890 \rightarrow 76{,}278$
8	0	0	0	1	1	$\alpha_8 - \alpha_7$	$76{,}279 \rightarrow 87{,}917$
9	1	1	1	0	1	$\alpha_9 - \alpha_8$	$87{,}918 \rightarrow 103{,}056$
10	0	1	1	0	1	$\alpha_{10} - \alpha_9$	$103{,}057 \rightarrow 119{,}222$
11	1	1	0	0	1	$\alpha_{11} - \alpha_{10}$	$119{,}223 \rightarrow 140{,}361$
12	0	1	0	0	1	$\alpha_{12} - \alpha_{11}$	$140{,}362 \rightarrow 162{,}278$
13	1	0	1	0	1	$\alpha_{13} - \alpha_{12}$	$162{,}279 \rightarrow 187{,}389$
14	0	0	1	0	1	$\alpha_{14} - \alpha_{13}$	$187{,}390 \rightarrow 218{,}445$
15	1	0	0	0	1	$\alpha_{15} - \alpha_{14}$	$218{,}446 \rightarrow 236{,}111$
16	0	0	0	0	1	$\pi - 2\alpha_{15}$	$236{,}112 \rightarrow 263{,}890$
17	1	0	0	0	1	$\alpha_{15} - \alpha_{14}$	$263{,}891 \rightarrow 281{,}557$
18	0	0	1	0	1	$\alpha_{14} - \alpha_{13}$	$281{,}558 \rightarrow 312{,}613$
19	1	0	1	0	1	$\alpha_{13} - \alpha_{12}$	$312{,}614 \rightarrow 337{,}725$
20	0	1	0	0	1	$\alpha_{12} - \alpha_{11}$	$337{,}726 \rightarrow 359{,}643$
21	1	1	0	0	1	$\alpha_{11} - \alpha_{10}$	$359{,}644 \rightarrow 380{,}783$
22	0	1	1	0	1	$\alpha_{10} - \alpha_9$	$380{,}784 \rightarrow 396{,}950$
23	1	1	1	0	1	$\alpha_9 - \alpha_8$	$396{,}951 \rightarrow 412{,}089$
24	0	0	0	1	1	$\alpha_8 - \alpha_7$	$412{,}090 \rightarrow 423{,}729$
25	1	0	0	1	1	$\alpha_7 - \alpha_6$	$423{,}730 \rightarrow 437{,}120$
26	0	0	1	1	1	$\alpha_6 - \alpha_5$	$437{,}121 \rightarrow 454{,}564$
27	1	0	1	1	1	$\alpha_5 - \alpha_4$	$454{,}565 \rightarrow 460{,}538$
28	0	1	0	1	1	$\alpha_4 - \alpha_3$	$460{,}539 \rightarrow 476{,}622$
29	1	1	0	1	1	$\alpha_3 - \alpha_2$	$476{,}623 \rightarrow 485{,}540$
30	0	1	1	1	1	$\alpha_2 - \alpha_1$	$485{,}541 \rightarrow 493{,}235$
31	1	1	1	1	1	α_1	$493{,}236 \rightarrow 500{,}000$

A VHDL file, based on the data in Table 4, used to obtain the 31-level MLI is uploaded to the Spartan 3E controller. The controller outputs 30 gating signals. These gating signals are fed to the 30 appropriate power switches. The 10 power switches in each phase's circuitry are designed to work in complementary mode, as shown in Figure 18 for Phase A. Also shown are the 120° phase shifts between phases A, B, and C. A dead time of 4 μsec is added between the outgoing and incoming switches, in order to avoid all possible short circuits.

4.2.2. The Proposed 31-Level MLI Operating at No Load

The system is operated at no load to monitor the phase and line voltage. Figure 19a shows the three-phase output voltage at 50 Hz and 122 Vrms. The line voltage (Vab) is shown in Figure 19b at 50 Hz and 210 Vrms.

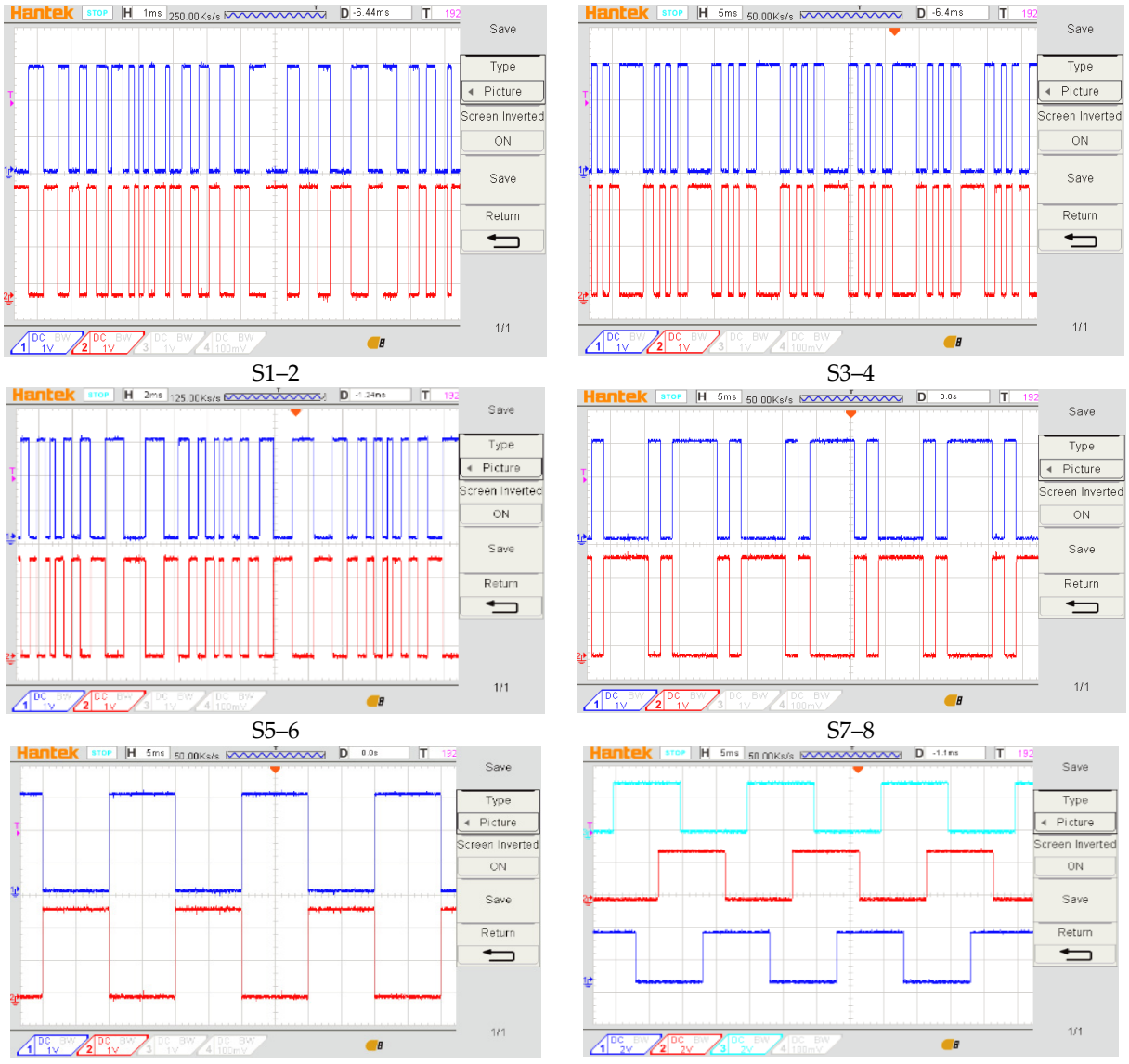
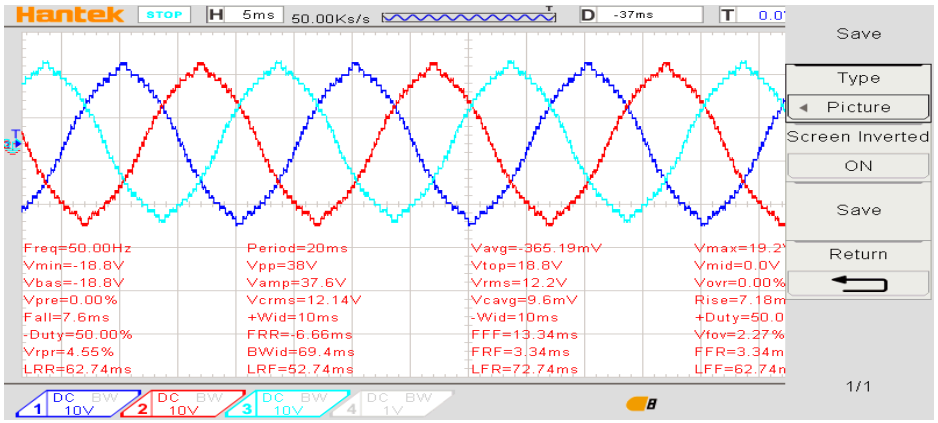
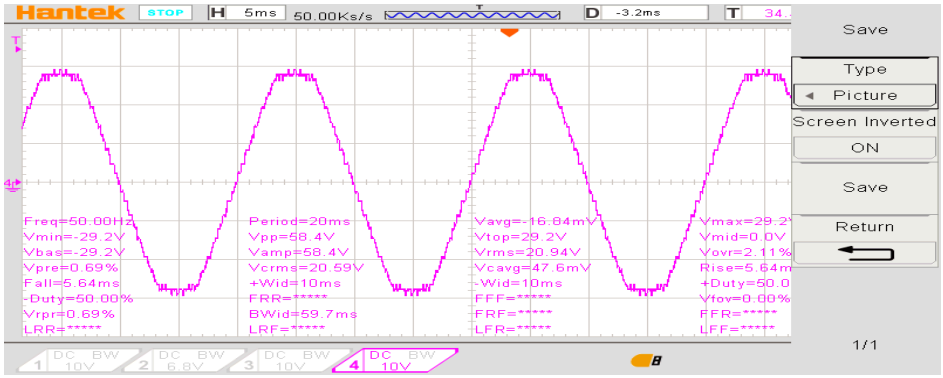


Figure 18. Gating pulses for the IGBTs in Phase A and the phase shift between phases.



(**a**)

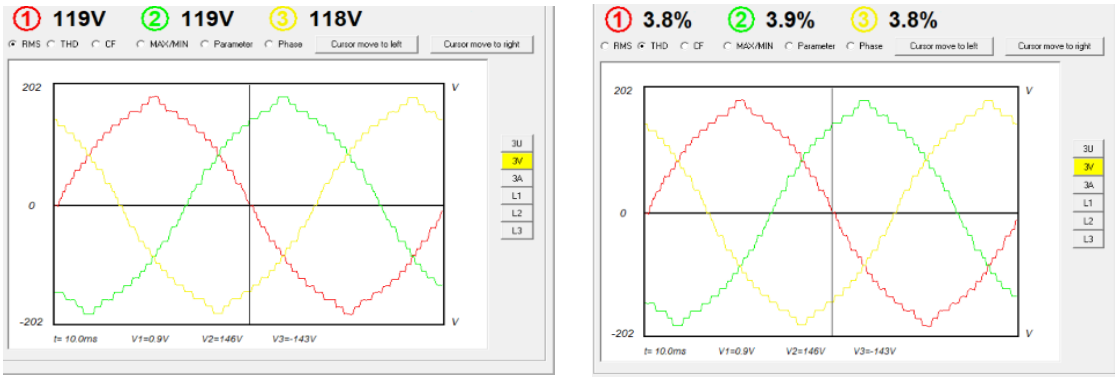
Figure 19. *Cont*.



(**b**)

Figure 19. Phase and line voltage of the proposed three-phase, 31-level MLI at no load. (**a**) Phase voltage (scale ×10), (**b**) line voltage (Vab) (scale ×10).

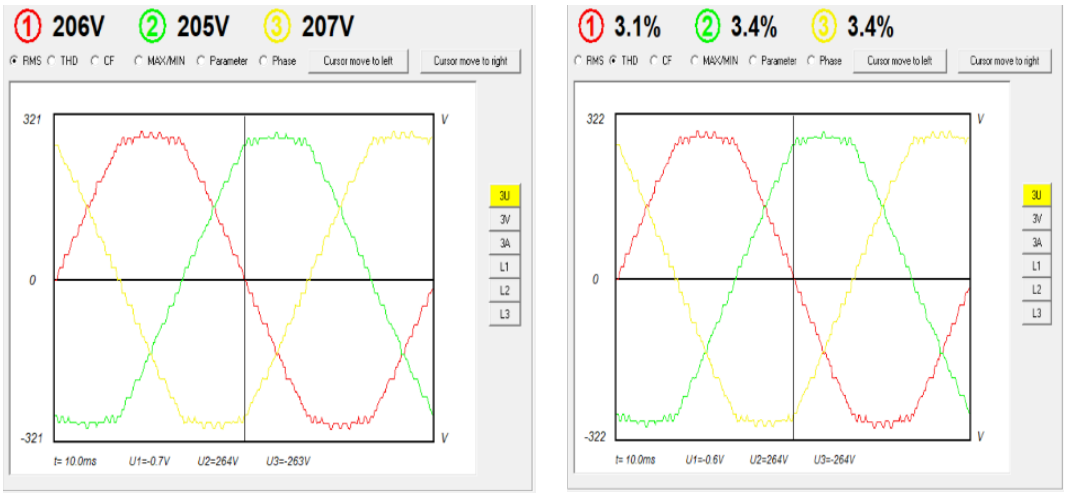
The power and quality analyzer HZCR-5000 is used to record the results. The three-phase voltage, THDs, and phase shift between the phases are shown in Figure 20a, and Figure 20b respectively.



(**a**) (**b**)

Figure 20. The three-phase voltage and THDs at no load: (**a**) phase voltage, (**b**) phase THDs.

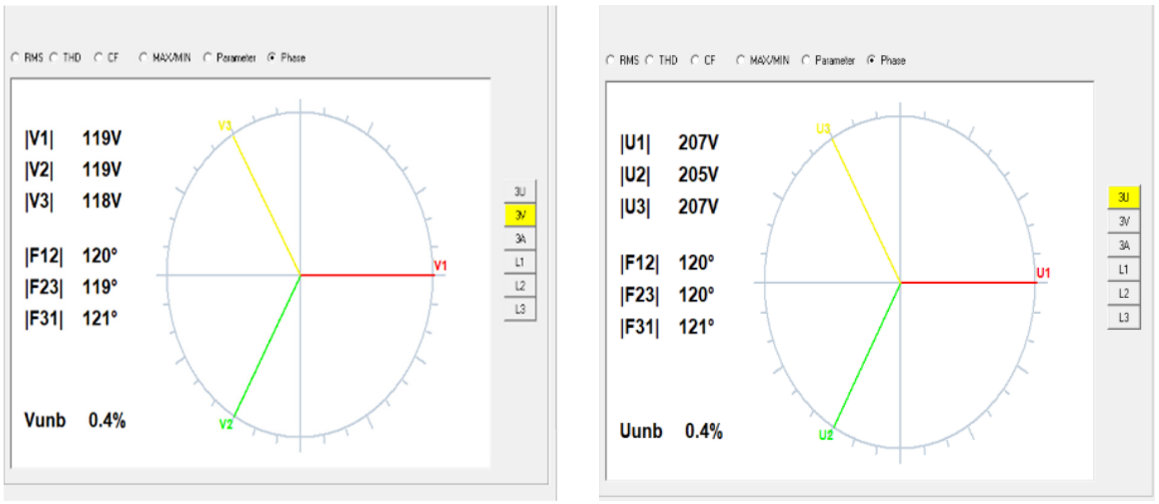
The line voltage, THDs, and phase shift between the phases are shown in Figure 21a, and Figure 21b respectively.



(**a**) (**b**)

Figure 21. Line voltage and THDs at no load: (**a**) line voltage, (**b**) line voltage THDs.

The phase shifts between the three-phase and the three-line voltage are shown in Figure 22a and Figure 22b, respectively. The voltage unbalance is very low and about 0.4%.



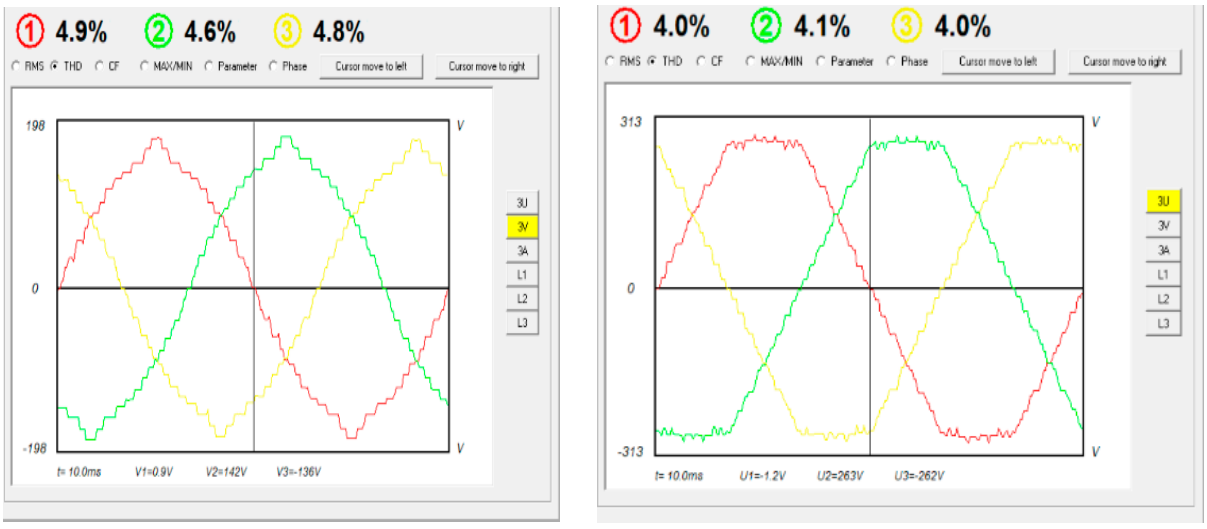
(**a**) (**b**)

Figure 22. Phase shift (**a**) phase voltage shift (**b**) line voltage shift.

4.2.3. Load Test

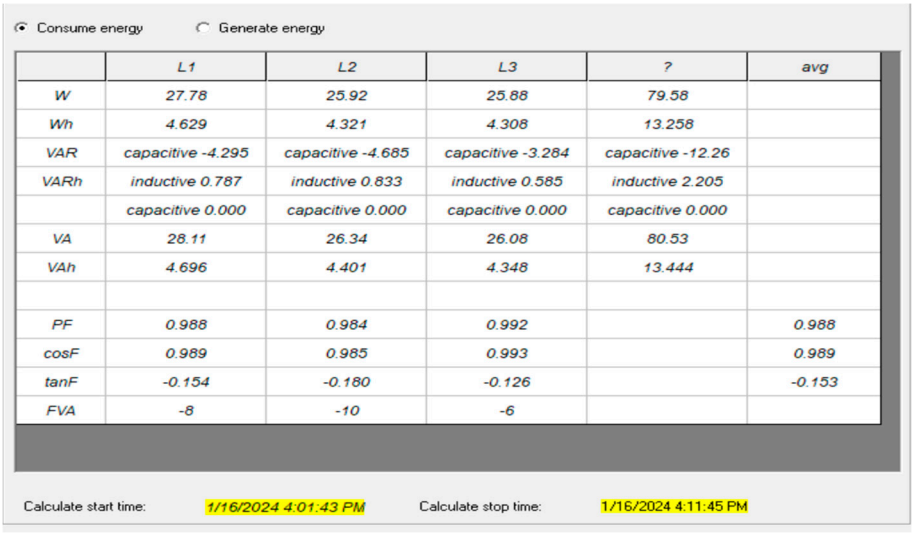
The load test is divided into two parts: a static load using a three-phase resistive load and a dynamic load using a three-phase squirrel cage induction motor. In the static load test, a Y-connected resistive load is connected to the output terminals of the 31-level MLI. The THD of the phase and line voltage are well below the 5% limit, as shown in Figure 23a,b, respectively. The details of the consumed power are shown in Figure 23c, where the power factor is almost at unity due to the purely resistive load.

The three phase currents in Figure 24a have an average THD value below 5%, which is compatible with the respective voltage values. The relationship between the phase voltage and current in the Phase A supply is shown in Figure 24b. The other phases responded with very similar characteristics. Figure 24c shows the phase difference between the three phase currents. Although the load is resistive, there is a small value difference in the phase between the voltage and current, which is normal in practical work. The voltage unbalance is recorded as 1.2%, which is a low value.



(**a**) (**b**)

Figure 23. *Cont.*



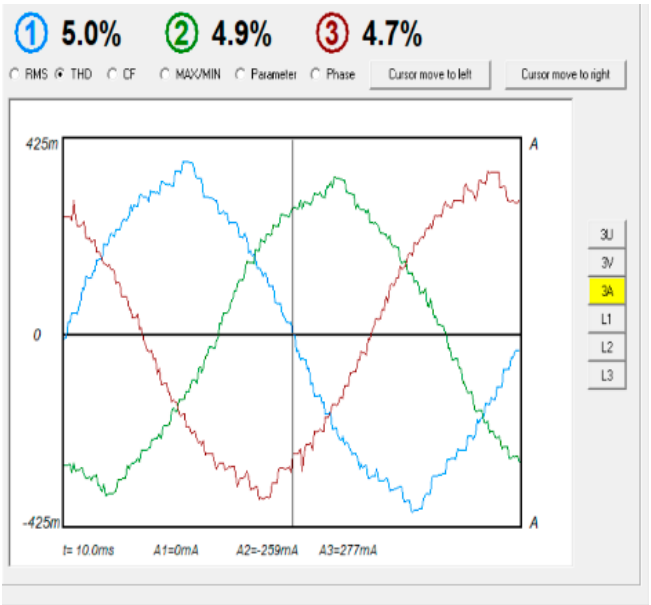
	L1	L2	L3	?	avg
W	27.78	25.92	25.88	79.58	
Wh	4.629	4.321	4.308	13.258	
VAR	capacitive -4.295	capacitive -4.685	capacitive -3.284	capacitive -12.26	
VARh	inductive 0.787	inductive 0.833	inductive 0.585	inductive 2.205	
	capacitive 0.000	capacitive 0.000	capacitive 0.000	capacitive 0.000	
VA	28.11	26.34	26.08	80.53	
VAh	4.696	4.401	4.348	13.444	
PF	0.988	0.984	0.992		0.988
cosF	0.989	0.985	0.993		0.989
tanF	-0.154	-0.180	-0.126		-0.153
FVA	-8	-10	-6		

(**c**)

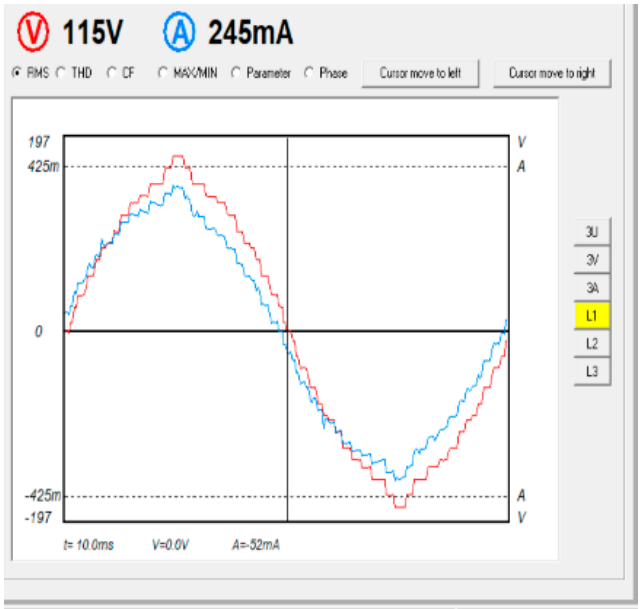
Figure 23. Phase and line voltage values of the THDs and consumed power for a resistive load: (**a**) phase voltage (resistive load) THDs, (**b**) line voltage THDs, (**c**) consumed power.

A three-phase squirrel cage motor is used in the dynamic load test. The motor has the following specifications: three-phase induction motor (SIEMENS) 220/380 Δ/Y, 0.18 kW, 1315 rpm, 50 Hz. When the motor is at no load, the 31-level MLI supplies a relatively small three-phase current of about 0.25 A per phase, as shown in Figure 25a. The relationship between phase voltage and current in phase B is shown in Figure 25b. The current can be seen to lag behind the voltage, as the load is now inductive. The recorded THDs are less than 5%, as shown in Figure 25c.

The harmonic analysis is shown in Figure 26a, Blue color for phase A, green for phase B, and grey for phase C, where most of the triple harmonics were either eliminated or exist at low values. The power consumed by the motor, as in Figure 26b, shows the effect of the inductive load on the total VAR power.

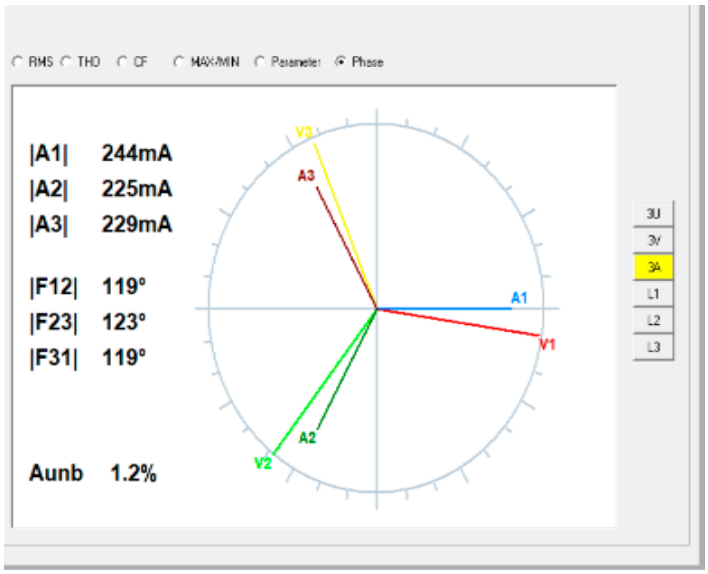


(**a**)



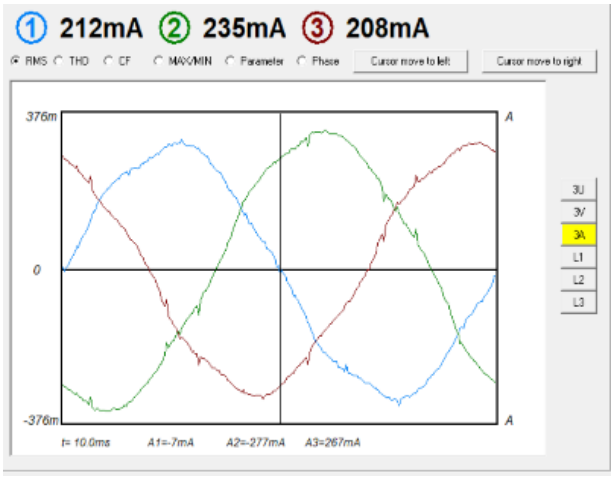
(**b**)

Figure 24. *Cont.*

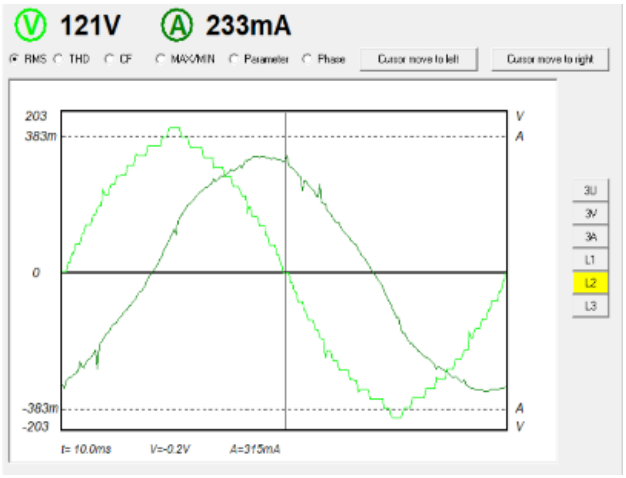


(**c**)

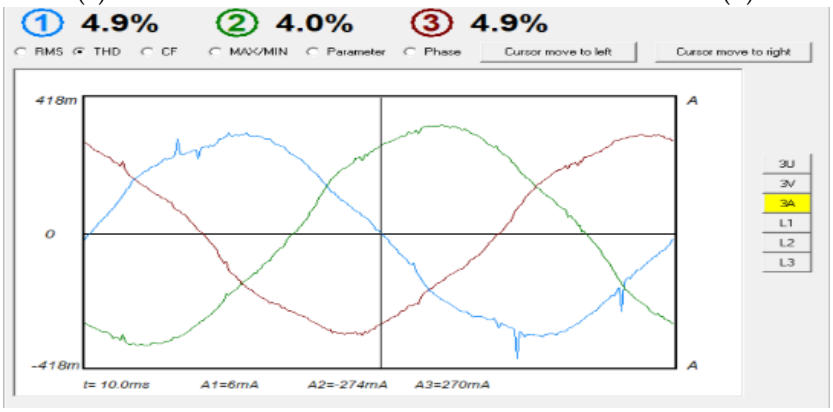
Figure 24. Phase current results for a resistive load: (**a**) phase currents (THDs) for a resistive load, (**b**) voltage–current relationship, (**c**) phase shift between the phase currents.



(**a**)

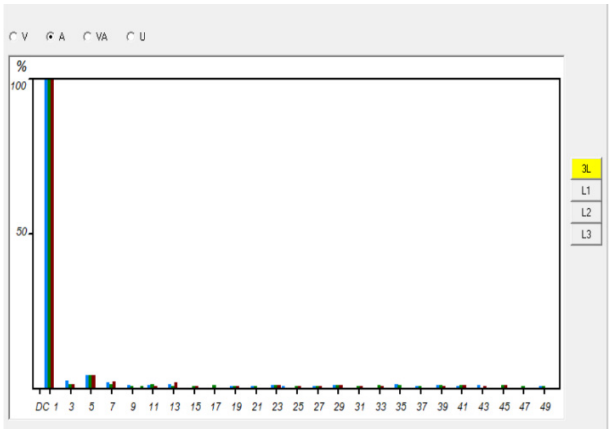


(**b**)



(**c**)

Figure 25. Motor currents at no load: (**a**) phase currents, (**b**) voltage–current phase shift, (**c**) motor current THDs.



(**a**)

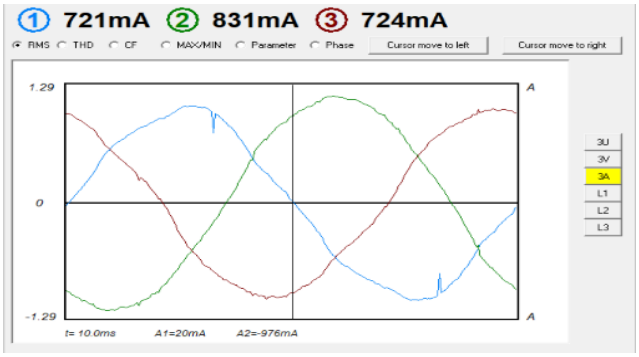
Consume energy Generate energy

	L1	L2	L3	?	avg
W	10.01	9.894	6.284	26.19	
Wh	0.000	0.000	0.000	0.000	
VAR	inductive 23.56	inductive 26.15	inductive 23.67	inductive 73.37	
VARh	inductive 0.000	inductive 0.000	inductive 0.000	inductive 0.000	
	capacitive 0.000	capacitive 0.000	capacitive 0.000	capacitive 0.000	
VA	25.59	27.96	24.49	78.04	
VAh	0.000	0.000	0.000	0.000	
PF	0.391	0.353	0.256		0.333
cosF	0.392	0.355	0.258		0.335
tanF	2.353	2.642	3.766		2.920
FVA	67	69	75		

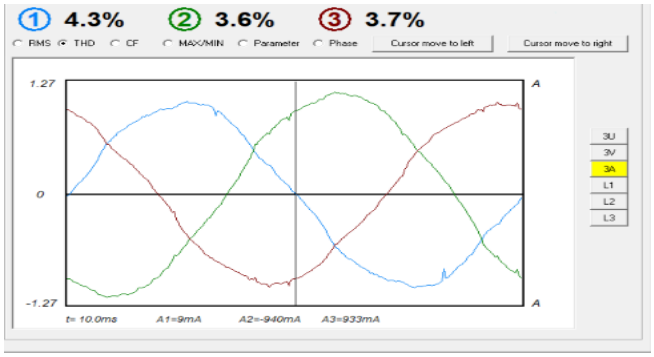
(**b**)

Figure 26. Motor current harmonics and consumed power at no load: (**a**) harmonic analysis, (**b**) consumed power.

The motor is later subjected to a fan load. The 31-level MLI supplied the current at about 0.75 A per phase to the motor to compensate for the applied load torque, as shown in Figure 27a. The THDs are still low, averaging about 3.8%, as shown in Figure 27b. The power consumed by the motor at load is shown in Figure 27c.



(**a**)



(**b**)

Consume energy Generate energy

	L1	L2	L3	?	avg
W	35.12	36.05	18.34	89.22	
Wh	6.433	6.572	3.381	16.387	
VAR	inductive 82.32	inductive 96.66	inductive 83.49	inductive 262.5	
VARh	inductive 15.169	inductive 17.848	inductive 15.479	inductive 48.496	
	capacitive 0.000	capacitive 0.000	capacitive 0.000	capacitive 0.000	
VA	89.38	103.2	85.48	278.0	
VAh	16.477	19.019	15.844	51.341	
PF	0.389	0.349	0.214		0.317
cosF	0.392	0.351	0.216		0.319
tanF	2.363	2.681	4.551		3.198
FVA	67	69	78		

Calculate start time: 1/2/2024 5:31:29 PM Calculate stop time:

(**c**)

Figure 27. Motor current, THDs, and consumed power at load: (**a**) motor currents, (**b**) motor THDs, (**c**) consumed power.

Using the MATLAB software, a three-phase motor was chosen with the following specifications: squirrel cage (5.4 HP (4 KW), 400 V, 50 Hz, 1430 RPM). To obtain an output voltage from the inverter of 400 volts, the value of the continuous source Vdc must be

equal to 24 volts in the Simulink model. On the practical side, a three-phase delta induction motor was connected to a voltage of 210 volts, which requires a Vdc voltage of 12 volts. Here, the difference in the value of the inverter output voltage between the simulation and the practical results appeared.

5. Conclusions

A three-phase, 31-level MLI is designed, modeled, and experimentally tested, as described in this paper. The genetic algorithm and grey wolf optimization algorithm are used to solve the trigonometric equations resulting from a Fourier analysis of the inverter voltages, in order to find the ideal angles to cancel most of the triple harmonics. The optimal angles are then chosen from the ideal angles, between the two algorithms, through curve fitting. The inverter is loaded with a resistive load and a three-phase induction motor. The THD values are not in excess of 5% for all the operating conditions, for the phase and line voltages or for the load currents. The frequency analysis shows that most of the triple harmonics are eliminated. The simulation of the three-phase MLI system is investigated using the MATLAB Simulink model, and the simulation results are in good agreement with the practical results. In all the operating conditions for the different resistive loads, as well as when the induction motor is loaded, the inverter works smoothly with a stable THD value, which indicates high efficiency of the practical model. The proposed 31-level MLI system can potentially become an efficient and reliable three-phase inverter for various static and dynamic loads. Table 6 summarizes the inverter's output regarding the phase voltage, line voltage, and current resulting from the resistive load and the induction motor. The amount of THD did not exceed 5%, on average; noting that the value of the THD is lower in regard to the inductive load compared to the resistive load, due to filtering characteristic of the inductive load.

Table 6. Summary of the inverter output voltage and current.

	Phase Voltage			**Line Voltage**			**Current**	
	RMS (V)	**THD %**	**Phase Shift Unbalance%**	**RMS (V)**	**THD %**	**Phase Shift Unbalance%**	**RMS (mA)**	**THD %**
No load	119	3.8	0.4	207	3.1	0.4	—	—
Resistance	119	4.6	0.4	207	4.0	0.4	245	4.7
Motor/No load	121	4.6	0.4	210	4.0	0.4	235	4.0
Motor/Load	121	4.6	0.4	210	4.0	0.4	831	3.6

6. Future Suggestions

The THD value has a fundamental impact on the efficiency and utility of an inverter. Two main factors significantly reduce the amount of FAD. First, optimal values should be used in regard to the operating angles of the power switches. This is achieved through choosing the best angles from a larger group of algorithms, which represents more algorithms than those considered in this research. Second, the number of switches used should be reduced by devising a topology that ensures smooth current pathways while, at the same time, obtaining a larger number of inverter levels and contributing to reducing the number of DC sources needed by the inverter.

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Conflicts of Interest: The authors declare no conflicts of interest.

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