

Article

Optimized Circulating Current Control and Enhanced AC Fault Ride-through Capability Using Model Predictive Control for MMC-HVDC Applications

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Abstract: This paper presents a novel model predictive control (MPC) approach for suppressing circulating currents in MMC-based HVDC systems. The proposed MPC eliminates the need for PI-regulators and pulse width modulators, resulting in improved dynamic response and controllability. The methodology demonstrates exceptional efficacy in controlling output current and addressing voltage ripple concerns associated with sub module (SM) capacitors. An innovative, communication-free fault ride-through (FRT) method is also introduced, eliminating the need for a DC chopper and ensuring rapid recovery following faults. To overcome the computational challenges associated with the traditional MPC algorithm, an aggregate model of the MMC is proposed, significantly reducing predicted states, hardware requirements, and calculations. Simulations validate the robustness of the proposed MPC control algorithm in tracking AC side current, suppressing circulating current, and regulating capacitor voltages under various scenarios. Future research will explore system expansion, integration with renewable energy sources, and hardware-in-loop setup testing for further validation.

Keywords: HVDC; fault ride-through (FRT); modular multilevel converter (MMC); circulating current control; model predictive control (MPC); capacitor voltage ripple (CVR)



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1. Introduction

HVDC is preferred over HVAC due to its higher efficiency, lower transmission losses, and ability to transmit power over long distances with lower costs. HVDC allows for asynchronous interconnections between grids with different frequencies and has a smaller footprint and lower electromagnetic interference compared to HVAC [1,2]. Additionally, HVDC technology is becoming increasingly advanced and cost-effective, making it a more attractive option for large-scale power transmission projects [3,4].

In HVDC projects, two converter topologies are commonly used: line-commutated converter (LCC) and voltage-source converter (VSC). While LCC converters have been widely used in HVDC projects for many years, VSC converters have gained popularity due to their superior performance and flexibility [5,6]. VSC converters are capable of reactive power control, which allows better system stability and control, and they are able to operate with a wider range of power flow directions. Within the VSC topology, the MMC, as shown in Figure 1, is considered a robust topology due to its ability to operate even with a high number of faulty components, making it ideal for high-voltage applications. Additionally, MMCs offer high power quality and low harmonic distortion, making them suitable for sensitive loads such as hospitals and data centers [7].

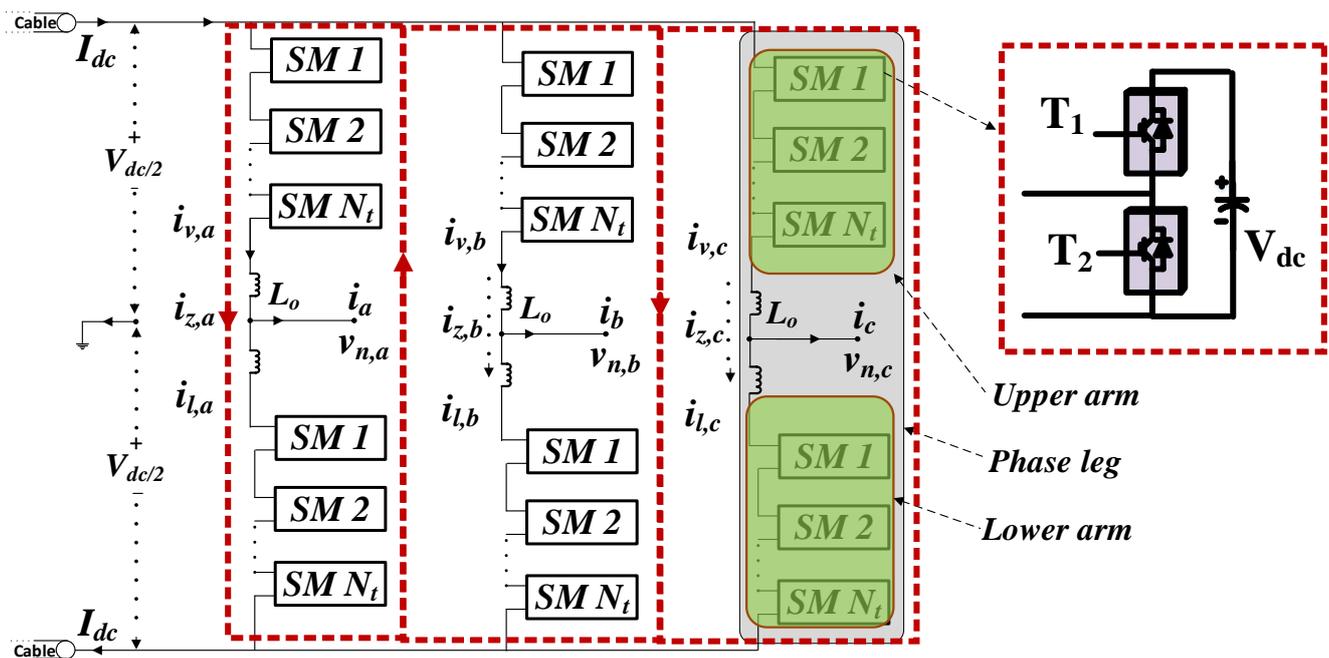


Figure 1. Three-phase equivalent structure of an MMC.

AC fault, such as voltage dip on the grid side in MMC-HVDC, can result in DC link fluctuation issues which stem from power imbalances between the sending-end converter (SEC) and receiving-end converter (REC) [8,9]. These imbalances jeopardize the performance of the MMC-HVDC system. Current grid code requirements mandate that the load receives constant and desired power even during AC fault, such as voltage dip [10]. Consequently, it is crucial to develop a communication-free, robust AC FRT technique that ensures smooth and ripple-free DC link voltages and can be validated through testing under AC fault, such as voltage dip.

Unmanageable circulating currents within MMCs can result in a range of adverse consequences, such as increased power losses, overheating of components, voltage instability, harmonic distortion, and diminished system reliability [11–15]. A review of the literature indicates a need for integrated control strategies that not only suppress circulating currents but also tackle the issue of capacitor voltage ripple (CVR).

In this research work, we introduce a comprehensive control strategy for the MMC-HVDC system that is characterized by its robustness, demonstrated through its AC FRT capability and internal dynamics control. Our approach effectively minimizes circulating current and addresses the problem of capacitor voltage ripple. Furthermore, we propose a communication-free improved FRT method, eliminating the need for a DC chopper.

2. Comparison with Previous Research

Various circulating current suppression and capacitor voltage balancing approaches have been extensively investigated for MMCs. In [16], an arm-level control scheme using the vector current control principle and a proportional resonant (PR) controller was proposed. The scheme's validity was demonstrated by comparing it with leg-level control based on a PR controller. In [17], an integral backstepping controller (IBS) outperformed the PR controller in suppressing circulating current and reducing CVR. In [18], an adaptive proportional integral (API) controller was shown to be more effective than the PR controller in suppressing circulating current. In [19], sliding mode control (SMC) was used to control output and circulating current, and its effectiveness was compared with the traditional PR controller. While these methods have been implemented at the unit level, their integration into HVDC systems and resilience in different fault scenarios have not been explored [16–19].

SM CVR and circulating current reduction in MMCs are challenging during AC fault (voltage dip). Exceeding safe limits can lead to converter tripping and stability issues. Strategies addressing MMC SM CVR and circulating current under AC fault, such as voltage dip conditions, are reported in the literature [20,21]. The goal is to ensure that CVR and circulating current operate within safe limits. However, studies focused on internal dynamic control (circulating current and CVR) without addressing outer loop implementation. Research was limited to unit-level MMC control and excluded transient analysis under different AC and DC faults [20,21].

Extensive research has been conducted on AC faults within HVDC. For HVDC systems, safeguarding against DC side faults has consistently been a primary research interest [22]. Various scholars have put forth diverse control and protection approaches to enhance the AC FRT capabilities of HVDC systems, as seen in references [23–27]. The stringent need for FRT in ensuring the grid's secure functioning during transients with minimal power disruptions serves as the motivation for these challenges [28]. Nonetheless, the risks associated with this requirement can be substantial during faults, such as power imbalances and increased DC bus voltage, potentially leading to damage to the DC cable in the event of symmetrical and asymmetrical faults. Under such circumstances, swift control measures can help rectify imbalances in DC voltage and power. Moreover, a HVDC system necessitates a high-quality power supply with a reduced THD when inverters are used to power passive loads from DC buses. Voltage dips, whether single or three-phase, can result in considerable damage to electrical equipment [29].

Certain suggested FRT systems, which concentrate on linking two AC grids, rely on a communication channel. For example, the study presented in [30] discovered that the point of common coupling (PCC) voltages observed on both ends of the DC link dictate the active power set point for the slave terminal. Consequently, the active power reference is automatically reduced if a voltage dip occurs on either side of the DC link. While employing a communication link generally leads to improved DC voltage performance, it also incurs additional costs and carries the risk of communication failure.

Furthermore, minimal efforts have been made to address voltage dip issues for passive loads in HVDC systems. The proposed remedies typically involve drawing a higher current from the grid during faults to keep the DC bus voltage stable. This approach necessitates the design of an oversized converter, which is not a cost-effective solution. A control method aimed at diminishing temporary voltage dips (AC FRT) for HVDC systems utilizing MMC was introduced in [31]. The goal was to employ the internal energy retained in MMC to deliver consistent power to passive loads during grid voltage dips. Nevertheless, the circulating current and CVR issues were not the primary focuses of these studies.

To overcome the issues mentioned above, in this research paper, MPC has been proposed for suppressing circulating currents in MMC-HVDC systems using the MATLAB/SIMULINK environment. The principal contributions of this research work include:

- The proposed MPC has no need for PI-regulators and pulse width modulators, thereby significantly enhancing dynamic response and controllability.
- The proposed MPC shows remarkable effectiveness not only in regulating circulating currents but also in controlling output current and addressing the voltage ripple issues linked to SM capacitors.
- Proposal of a novel communication-free, improved FRT method, eliminating the need for a DC chopper.
- The advanced FRT method guarantees quick recovery post-fault occurrence while effectively keeping DC link and capacitor voltages within safe boundaries.

The conventional MPC algorithm necessitates the evaluation of all potential switching states during each control period [32,33], making it a laborious and time-consuming process. For instance, with $n = 10$ SMs, the number of combinations can be calculated using the binomial coefficient $3C_{2N}^N = 554,268$, where for each phase, there are $C_{2N}^N = 184,756$ combinations. Consequently, even with advanced microprocessors, traditional MPC remains impractical. However, this study presents a novel approach by proposing an aggregate

model of the MMC, which eliminates the need for voltage sorting of capacitors. This innovation significantly reduces the number of predicted states, hardware requirements for sorting, and computational complexity.

A high-level summary is presented in Table 1, providing a comparison between the proposed method and existing approaches.

Table 1. Comparison between proposed method and existing approaches.

Study Ref.	Control Method	Major Findings and Limitations
[16]	Vector current control with PR controller	Validated at arm level, performed better than leg-level control with PR controller. No HVDC integration or fault scenario resilience tested.
[17]	Integral backstepping controller (IBS)	Suppressed circulating current and reduced CVR more effectively than PR controller. No HVDC integration or fault scenario resilience tested.
[18]	Adaptive proportional integral (API) controller	More effective than PR controller in suppressing circulating current. No HVDC integration or fault scenario resilience tested.
[19]	Sliding mode control (SMC)	Controlled output and circulating current effectively compared to PR controller. No HVDC integration or fault scenario resilience tested.
[20,21]	Various MMC SM CVR and circulating current control under AC fault	Ensured safe operation limits during AC faults. No transient analysis under different AC and DC faults.
[22–27]	Various control and protection approaches for HVDC	Enhanced AC FRT capabilities, yet risks were present during faults, causing power imbalances and increased DC bus voltage.
[30]	FRT systems with communication link	Achieved improved DC voltage performance but at the cost of potential communication failure and additional costs.
[31]	Control method aimed at diminishing voltage dips for HVDC	Used internal energy of MMC to provide consistent power during voltage dips. Did not focus on circulating current and CVR issues.
This Study	Proposed model predictive control (MPC)	Effectively regulated circulating currents and controlled output current. Eliminated need for PI-regulators and pulse width modulators. Proposed a novel communication-free, improved FRT method.

3. Proposed MPC for MMC-HVDC System

Among the advanced control strategies, MPC is the one that has gained significant attention in HVDC MMC applications. Although it was impractical at first to apply the technique to applications that had greater switching frequencies due to extensive calculations that would take a long time to complete, the MPC approach is increasingly being utilized for controlling power converters, owing to advancements in processor speed and features like rapid response, the straightforward integration of nonlinearities, adaptability to various objectives, and the presence of uncomplicated modulation methods [34]. The main characteristic of MPC is the use of the system model to examine the future behavior of the controlled variables. Based on this information, the controller provides optimal gate drives for the switches of the MMC to operate at optimal conditions. Figure 2 illustrates the block diagram of the suggested MPC approach for MMC.

The objectives of the MPC are to track the AC current and restrict the circulating current. The algorithm achieves those objectives by performing the following tasks:

- Anticipating the performance of controlled variables across all potential switching states;
- Assessing the cost function corresponding to each prediction;
- Choosing the switching state that results in a minimized cost function.

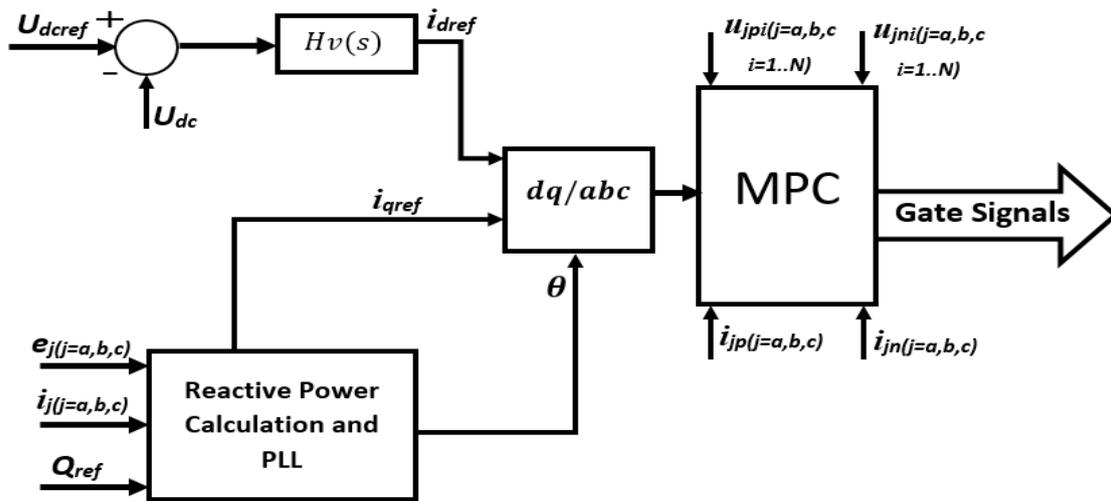


Figure 2. Block diagram of proposed MPC.

3.1. AC Current Tracking

The objective of the tracking of the AC current is to maintain the ac side current of MMC at a reference value. Figure 3 shows the single-phase equivalent diagram of three-phase MMC.

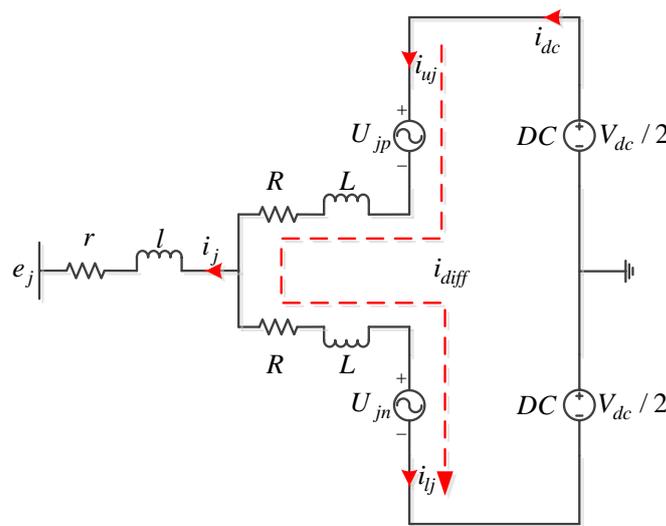


Figure 3. Single-phase equivalent of three-phase MMC.

Where i_{uj} and i_{lj} are the upper and lower arm currents, u_{jp} and u_{jn} are the upper and lower arm voltages, e_j is the grid side voltage, and i_{diffj} is the inner unbalanced current. Based on Figure 3, the equation for the voltage of the MMC can be written as Equation (2), where $L' = l + L/2$ and $R' = r + R/2$.

$$L' \frac{di_j(t)}{dt} = e_j(t) - \frac{u_{jn}(t) - u_{jp}(t)}{2} - R' i_j \tag{1}$$

Applying Euler approximation on (2), the ac side current can be written as Equation (3).

$$i_j(t + T_s) = \frac{T_s}{R' + L'} \left[e_j(t + T_s) - \frac{u_{jn}(t + T_s) - u_{jp}(t + T_s)}{2} \right] + \frac{L'}{T_s} i_j(t) \tag{2}$$

where T_s is the sampling time, $i_j(t + T_s)$ and $i_j(t)$ are the predicted and measured currents, respectively, and $e_j(t + T_s)$ is the grid side one step forward voltage. If T_s is assumed to be

a very small value, then $e_j(t + T_s)$ will become $e_j(t)$. Here, $u_{jp}(t + T_s)$ and $u_{jn}(t + T_s)$ are the one step forward predicted upper and lower arm capacitor voltages inserted in SMs. Thus, the cost function of the ac current tracking is defined as:

$$J_1 = \left| i_{jref}(t + T_s) - i_j(t + T_s) \right| \quad (3)$$

3.2. Restricting Circulating Current

The objective is to restrict the circulating current to the reference value so that the efficiency of the system is improved. The voltage and the inner unbalanced current equation are shown in Equations (5) and (6).

$$i_{jdiff} = \frac{i_{uj} + i_{lj}}{2} \quad (4)$$

$$L' \frac{di_{jdiff}(t)}{dt} = \frac{Vdc}{2} - \frac{u_{jn}(t) + u_{jp}}{2} \quad (5)$$

Applying Euler approximation on (6), the expression for the circulating current becomes:

$$i_{jdiff}(t + T_s) = \frac{T_s}{2L'} [Vdc - u_{jn}(t + T_s) - u_{jp}(t + T_s)] + i_{jdiff}(t) \quad (6)$$

where $i_{jdiff}(t)$ and $i_{jdiff}(t + T_s)$ are the measured and predicted circulating current and $i_{jdiff}(t)$ can be calculated from (5); $u_{jp}(t + T_s)$ and $u_{jn}(t + T_s)$ are the one step forward predicted upper and lower arm capacitor voltages inserted in submodules. Thus, the cost function of the circulating current is defined as:

$$J_2 = \left| i_{jdiff_ref}(t + T_s) - i_{jdiff}(t + T_s) \right| \quad (7)$$

3.3. Cost Function

The cost function assesses all the predicted states within each control period, selecting the optimal switching states that minimize the cost. It can comprise multiple subsets of cost functions, achieving diverse objectives simultaneously through the use of weighting factors [35]. The cost function might incorporate control objectives like lowering switching frequency, reducing common-mode voltage, decreasing reactive power, and minimizing current ripple to manage the MMC. The algorithm's cost function is formulated as depicted in Equation (1).

$$j_m = \lambda_1 J_1 + \lambda_2 J_2 \quad (8)$$

Generally, the MPC approach uses weighing factors to combine subsets of the cost function into a single cost function. The procedure to determine the weighting factors is based on the empirical method presented in [36].

Figure 4 is the flow diagram of MPC that demonstrates the implementation process of the algorithm. The subsets of the cost function J_1 and J_2 are calculated based on Equations (3) and (7) and then the algorithm evaluates the cost function J_m for all possible switching states and selects the one with the minimum value for J_m . These switching states are applied to the SMs and the algorithm eventually tracks the ac current and restricts the circulating current.

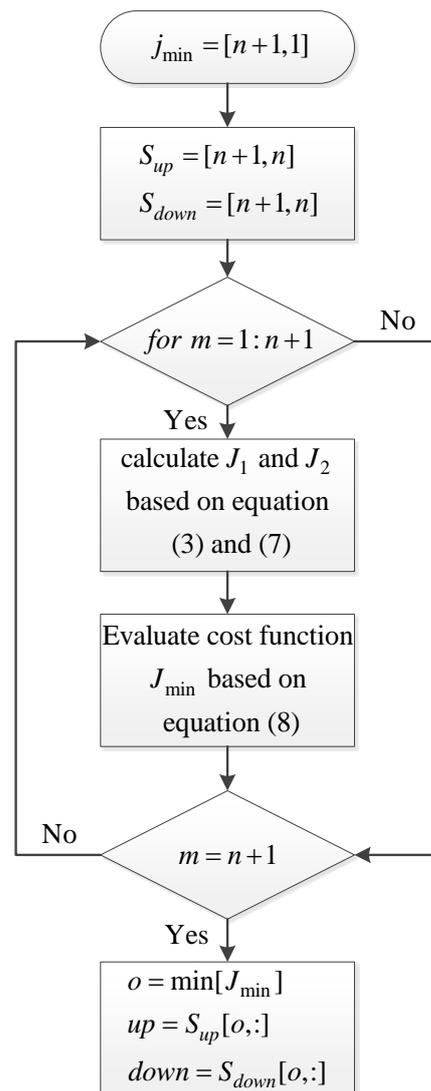


Figure 4. Flowchart of proposed MPC algorithm.

4. Proposed System Description

A 220MVA MMC-HVDC system is examined in the Matlab/Simulink environment. The simulated system has a DC bus voltage of 135 kV and is a 51-level MMC-HVDC system connected to a 66 kV grid. The load system consists of a 110 MW passive load. The performance of the simulation is improved by using an aggregate modelling method. The system is used in islanded mode, which means that the rectifier controls the DC bus voltage while the inverter primarily controls the AC voltage of the passive network. For the control of the system, the MPC algorithm is used, which has the primary functions of AC current tracking and suppressing the circulating current. The power electronic converters are very sensitive to an overcurrent that can last up to several cycles. To address this issue, a three-phase static thyristor AC breaker bypass system is implemented and synced with the grid. MMC and grid parameters are shown in Table 2 and load parameters are summarized in Table 3. The detailed MPC control system applied on MMC 1 and MMC 2 station on an MMC-HVDC system is shown in Figure 5.

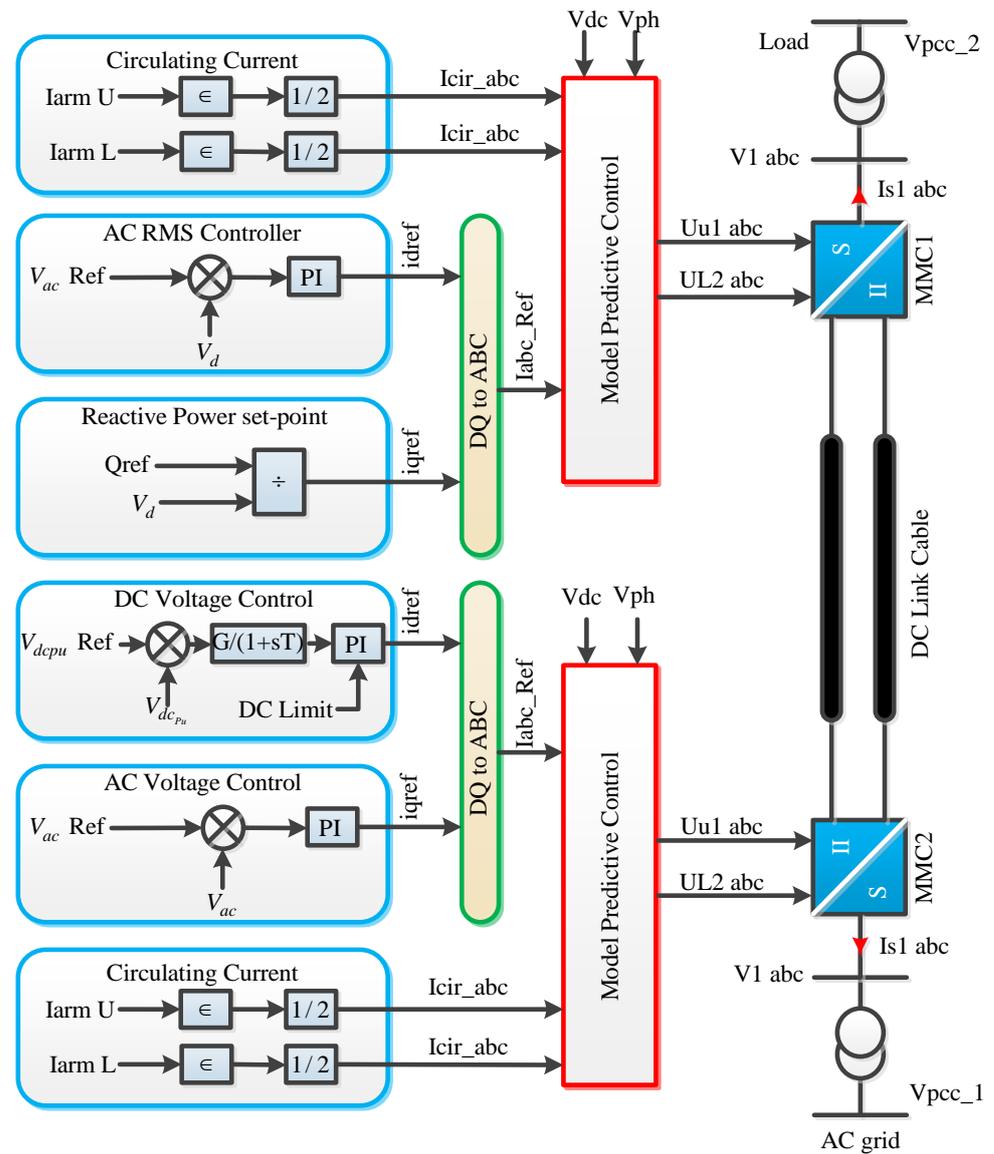


Figure 5. Detailed MPC control system applied on proposed system description.

Table 2. MMC and grid parameters.

Parameters	Symbols	Value	Unit
grid voltage (line–line)	v_s	66,000	V
grid frequency	F	50	Hz
dc-link voltage	V_{dc}	135,000	V
arm resistance	r_{arm}	0.5	Ω
arm inductance	l_{arm}	0.0207	mH
number of SM_s	n	50	
SM_s Capacitance	C_{SM}	15	mF

Table 3. Load parameters.

Parameters	Symbols	Value	Unit
nominal power for converters	P_{nom}	220	MW
nominal apparent power for converters	S_{nom}	220	MVA
nominal line current	I_{nom}	1.9	kA
startup resistance for inrush	r_{startup}	17	Ω
load active power nominal	P_{load}	110	MW
load reactive power nominal	Q_{load}	0	VAR
apparent load power	S_{load}	110	MVA

5. Result Discussions

5.1. Simulation Results for Proposed MPC-Based MMC-HVDC under Steady-State Operation

A crucial component of the converter's viability is determining its startup and steady-state operation. The startup charging current is controlled by inserting the charging resistors, providing the converter with initial energy. The circuit breaker is energized in 0.1 s, as can be observed in Figure 6a,b. The breaker and controllers can be systematically operated, and the converter can charge up the SMs capacitors and reach steady state in less than one second. The grid voltage is kept at its nominal value, which is 66 kV. Circulating current suppression and DC voltage regulation of the rectifier are turned on at 0.1 and 0.4 s, respectively, which are controlled using the MPC algorithm. They enhanced the power quality and reduced THD of MMC inverter voltage, and the inverter current adheres to IEEE guidelines, as demonstrated in the magnified sections of Figures 6c and 6d, respectively.

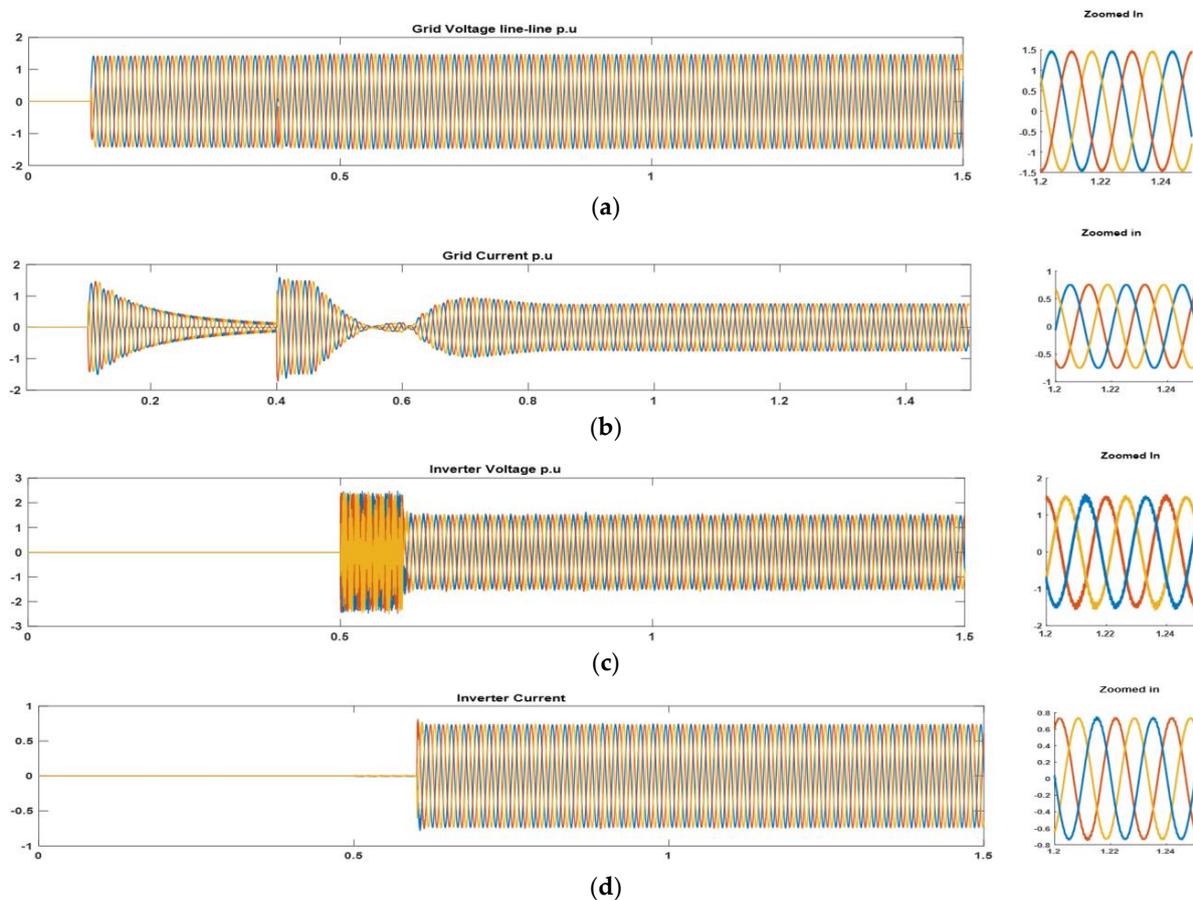
**Figure 6.** (a) Grid voltage to the rectifier station. (b) Grid current. (c) Inverter voltage. (d) Inverter current.

Figure 7a shows the power delivered from the inverter to the load. The nominal power of the system is 220 MW, while the load requirement is 110 MW. The MMC inverter provides constant power to the load at 0.5 p.u. The power drawn from the grid is also 0.5 p.u. as per the requirement of the load, which can be seen in Figure 7b. Figure 7c shows the DC bus power, and it can be observed that after reaching the steady state, the power has significantly lower deviations. Figure 7d presents the outcomes of simulations for DC link voltages. The suggested MPC-based circulating current suppression strategy has been implemented, resulting in more stable DC link voltages. By not requiring an extra controller, the proposed MPC-based circulating current regulation technique prevents the introduction of ripple components into the DC link voltages.

The suggested MMC-based HVDC system addresses circulating current and capacitor CVR challenges. The proposed MPC-based circulating current suppression strategy effectively reduces the circulating current for MMC rectifier and MMC inverter stations, as demonstrated in Figures 8a and 8b, respectively. The magnitude of circulating current for both MMC rectifier and inverter stations is 0.05 per unit (PU), which is below 10% of the nominal current in accordance with grid regulations. As depicted in Figure 9a,b, the MMCs' capacitor voltage for rectifier and inverter stations consistently operates within safe limits, preventing converter shutdown. Furthermore, the capacitor voltages remain balanced and exhibit decreased capacitor voltage fluctuations.

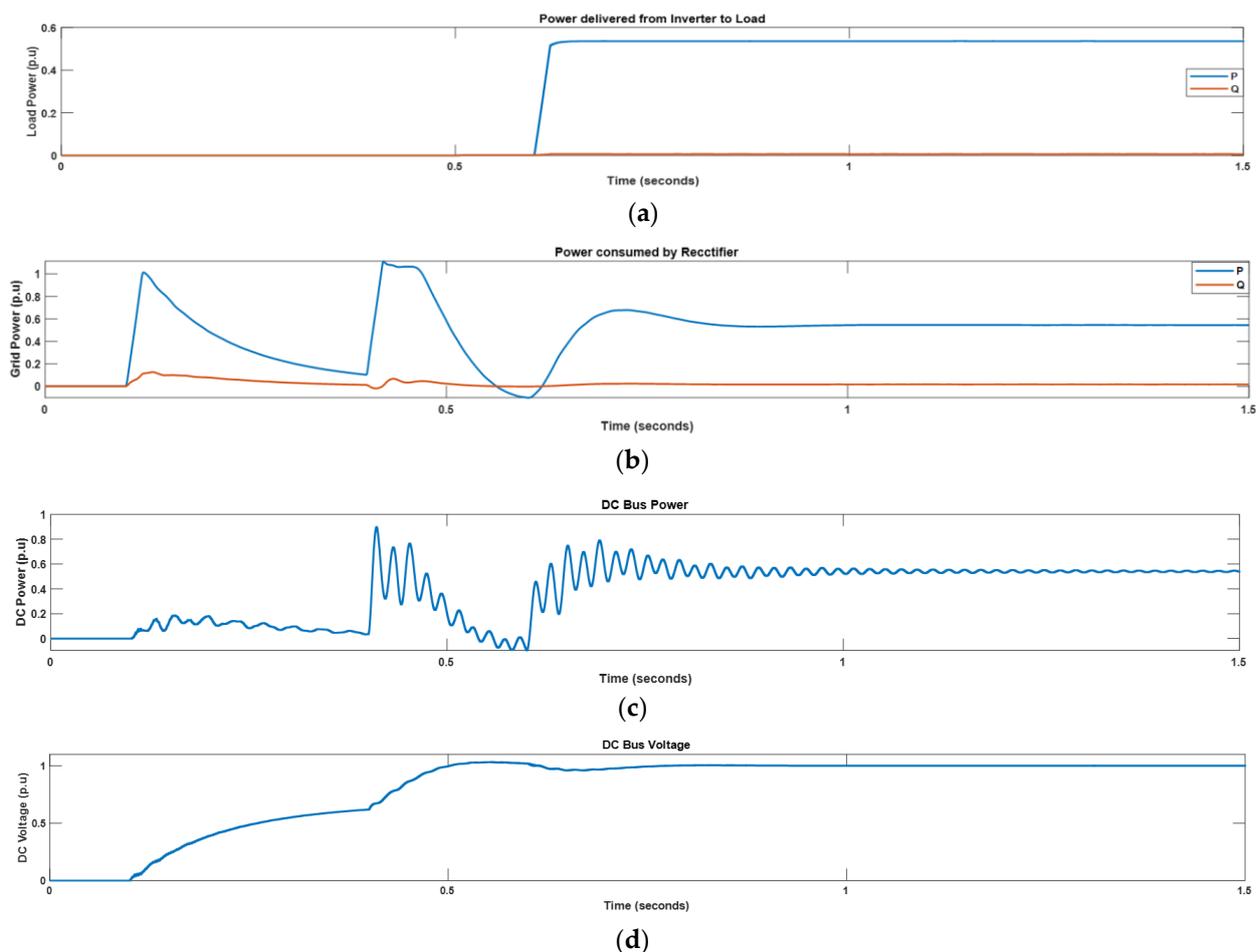


Figure 7. (a) Power delivered from inverter to load. (b) Power consumed by rectifier. (c) DC bus power and (d) DC bus voltage.

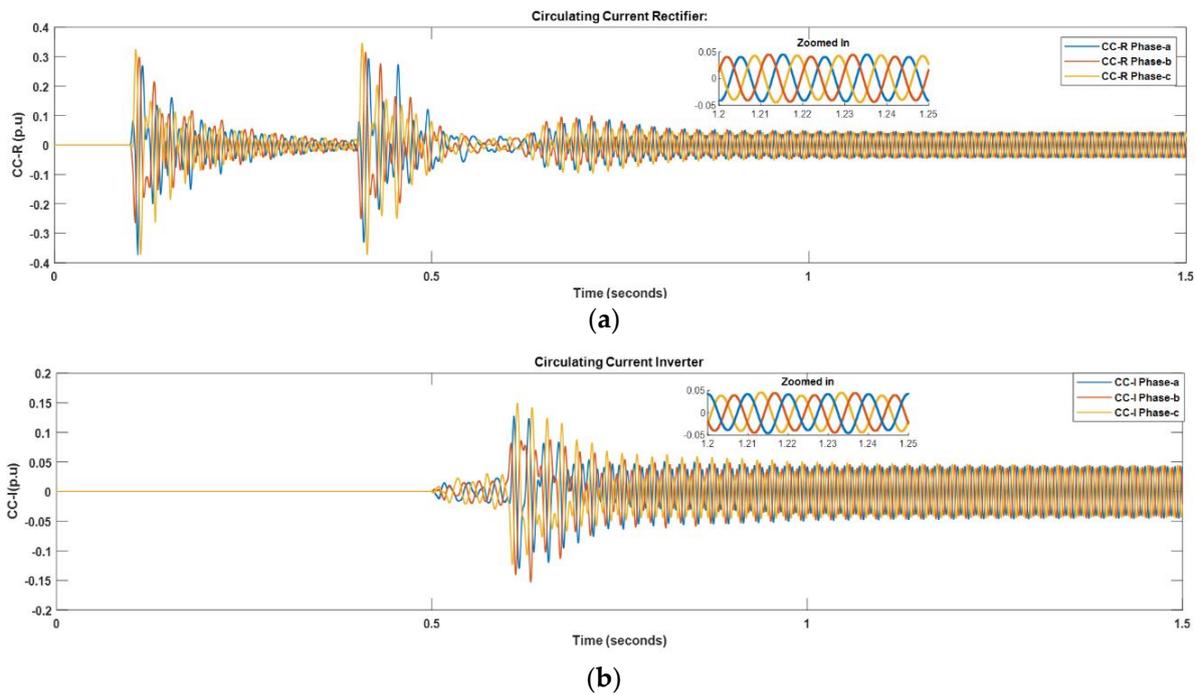


Figure 8. (a) Circulating current of MMC rectifier; (b) circulating current of MMC inverter.

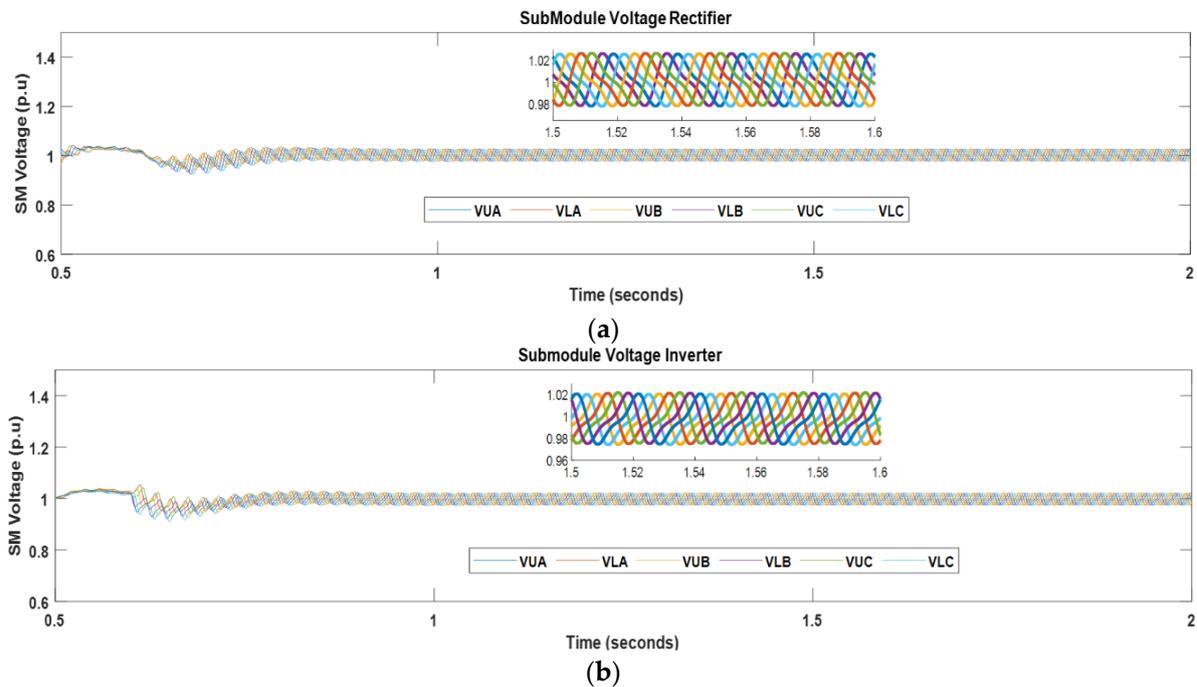


Figure 9. (a) SM capacitor voltage of MMC rectifier; (b) SM capacitor voltage of MMC inverter.

The proposed MPC-based control demonstrates strong performance in managing internal dynamics, effectively reducing circulating current and CVR issues. Consequently, the arm currents of the rectifier and inverter exhibit enhanced current quality and reduced harmonics, as illustrated in Figures 10a and 10b, respectively.

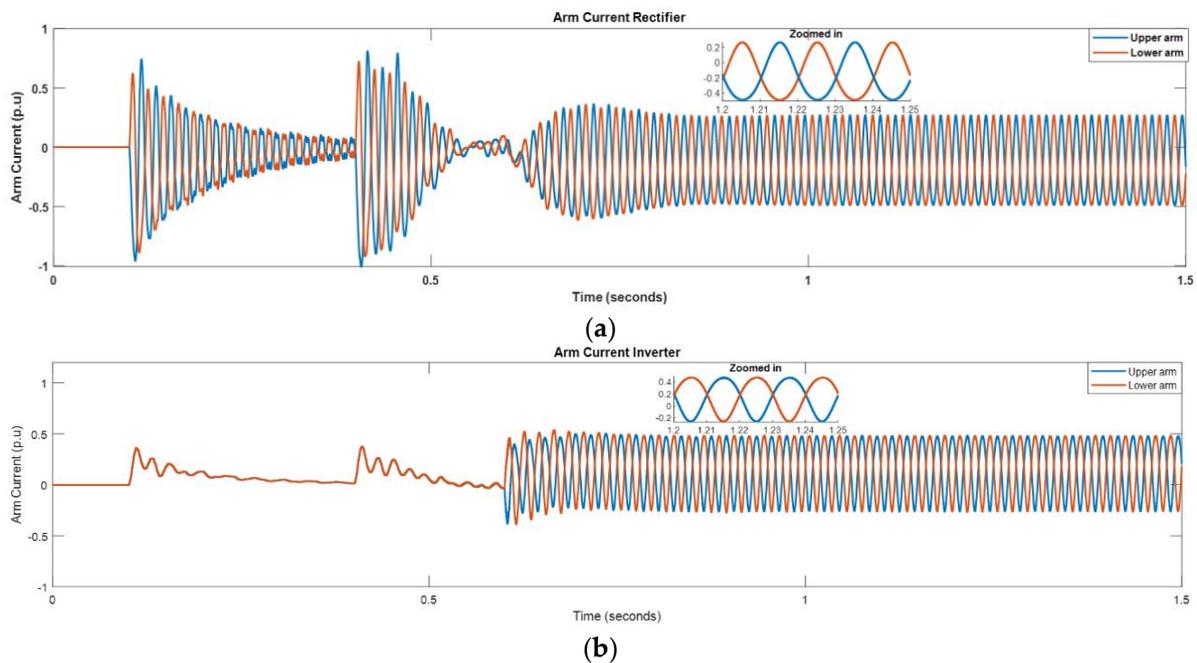


Figure 10. (a) MMC arm current rectifier; (b) MMC arm current inverter.

Besides improved control of internal dynamics, the proposed MPC algorithm demonstrates strong performance in tracking the AC current, as depicted in Figure 11. The measured current closely aligns with the reference, underscoring the effectiveness of the suggested MPC approach. Finally, Figure 12 demonstrates that the proposed MPC control maintains a standard modulation index value of 0.8 PU, which ensures the prevention of over-modulation and under-modulation problems during MMC operation.

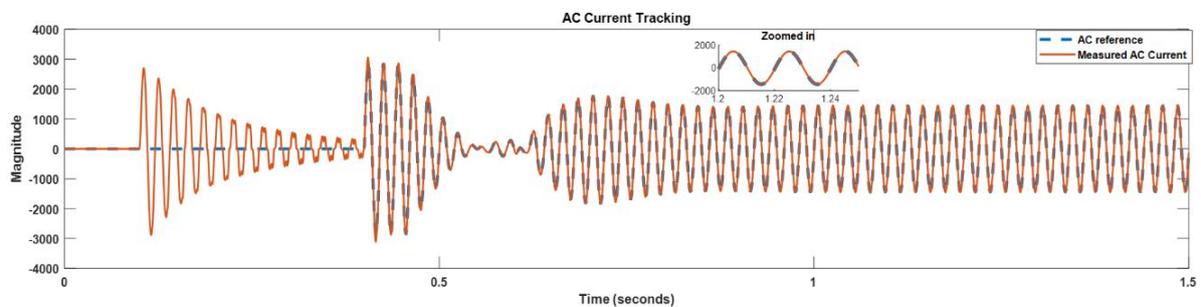


Figure 11. AC Current tracking by MPC algorithm.

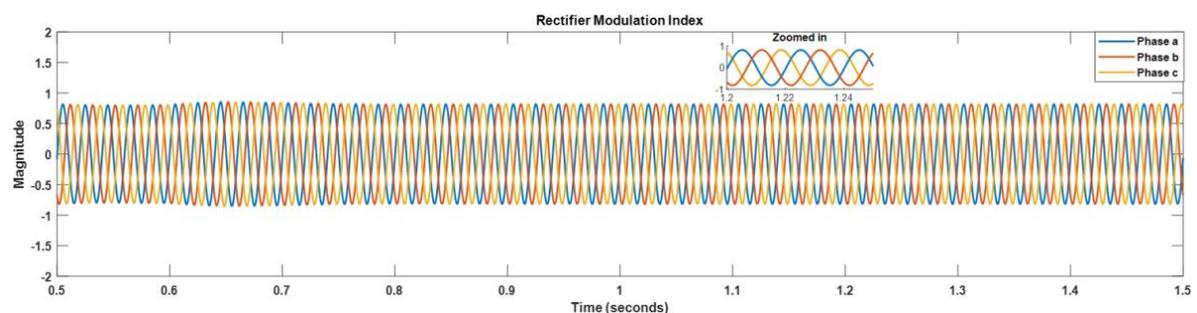


Figure 12. Modulation index of MMC rectifier.

5.2. Simulation Results for Proposed MPC-Based MMC-HVDC under AC Fault (Voltage Dip)

The resilience of the proposed system has been evaluated in the face of AC faults, such as voltage dips. One of the significant features of the MMC is its ability to mitigate

voltage dips occurring in the external grid. The voltage dip is modeled in the main source, which can be controlled to supply reduced voltage amplitude at any phase for a short duration. A voltage dip of 50% in magnitude for 75 milliseconds was introduced to assess the effectiveness of the proposed MPC algorithm, as shown in Figure 13a. It can be observed that only the grid-side voltage is affected, with a 50% decrease in magnitude, resulting in a slight increase in the grid-side current, as shown in Figure 13b. The converter station can readily accommodate this slight increase in the grid-side current. It should be noted that the MMC inverter voltage and inverter current (load side) remain unaffected by the AC fault (voltage dip), as shown in Figures 13c and 13d, respectively. Moreover, the MMC inverter voltage and inverter currents maintain an excellent sinusoidal waveform, following IEEE standards.

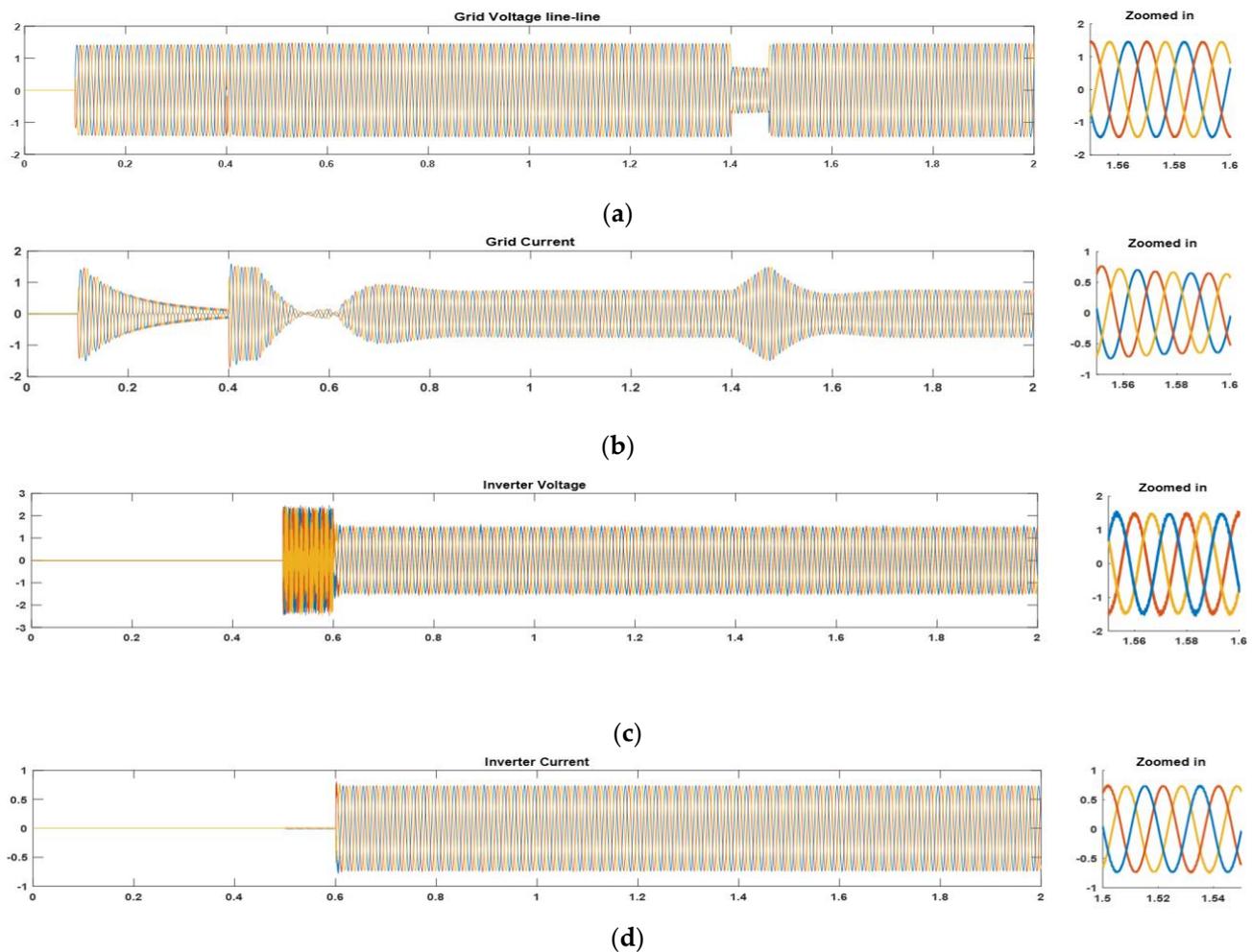


Figure 13. Results under AC fault (Voltage Dip): (a) grid voltage to the rectifier station; (b) grid current; (c) inverter voltage; (d) inverter current.

In the presence of an AC fault, such as a voltage dip, the DC bus voltage stays above 0.8 per unit, as depicted in Figure 14a. This demonstrates the suitable dimensioning of the converters and the resilience of the proposed MPC algorithm. Additionally, during the dip, the power drawn from the grid side diminishes, as illustrated in Figure 14c, while the load consistently receives constant power, as shown in Figure 14d, due to the robustness of the algorithm. The DC bus power returns to its steady-state value, ensuring FRT capability under voltage dip conditions, as displayed in Figure 14b.

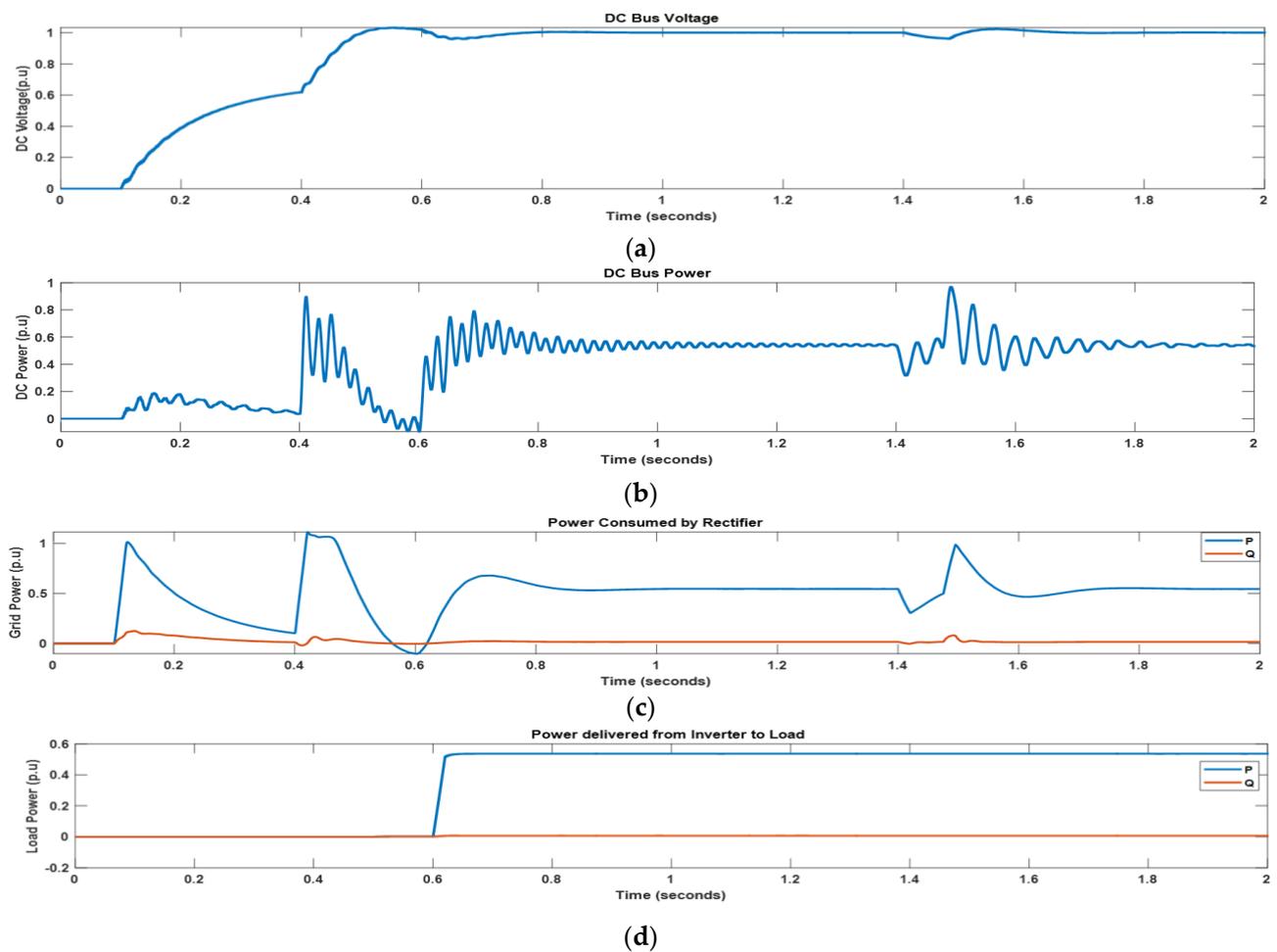


Figure 14. Results under AC fault (voltage dip): (a) DC bus voltage; (b) DC bus power; (c) power consumed by rectifier; (d) power delivered from inverter to load.

The circulating current of both MMCs under voltage dip is illustrated in Figure 15a,b. It becomes apparent that during the voltage dip, the circulating current of the rectifier experiences an increase due to the rise in grid-side current, whereas the inverter's circulating current exhibits minimal fluctuation since the inverter-side current remains constant throughout the voltage dip. The MPC algorithm stabilizes the circulating current back to its steady state once the voltage dip concludes. During the voltage dip, the submodule capacitor is expected to safely discharge its stored energy to offset the energy loss induced by the voltage sag, as demonstrated in Figure 16a,b. The capacitor voltages remain within secure boundaries both during and after the fault. Furthermore, the circulating current not only stays within the acceptable range during the fault but is also effectively suppressed.

The circulating current flowing into the arm is effectively suppressed by the MPC, resulting in purely sinusoidal arm currents, as illustrated in Figure 17a,b. Figure 18 presents the tracking of AC current by the MPC algorithm, demonstrating that the measured AC current accurately follows the reference, regardless of the voltage dip. The rectifier's modulation index, displayed in Figure 19, reveals a reduction by half during a voltage dip, which is attributed to the nominal current drawn by the MMC from the grid during the dip. Once the voltage dip ends, the modulation index returns to the standard value of 0.8. This observation confirms the efficacy of the proposed algorithm.

The comprehensive analysis presented above indicates that the developed system exhibits robust performance in both steady-state and voltage dip scenarios. It maintains the DC bus voltage at the standard level while ensuring consistent power delivery to the load, even during transient voltage dips. The proposed MPC algorithm effectively suppresses

the circulating current, controls the capacitor voltage, robustly tracks the AC current, and maintains the modulation index at its standard value.

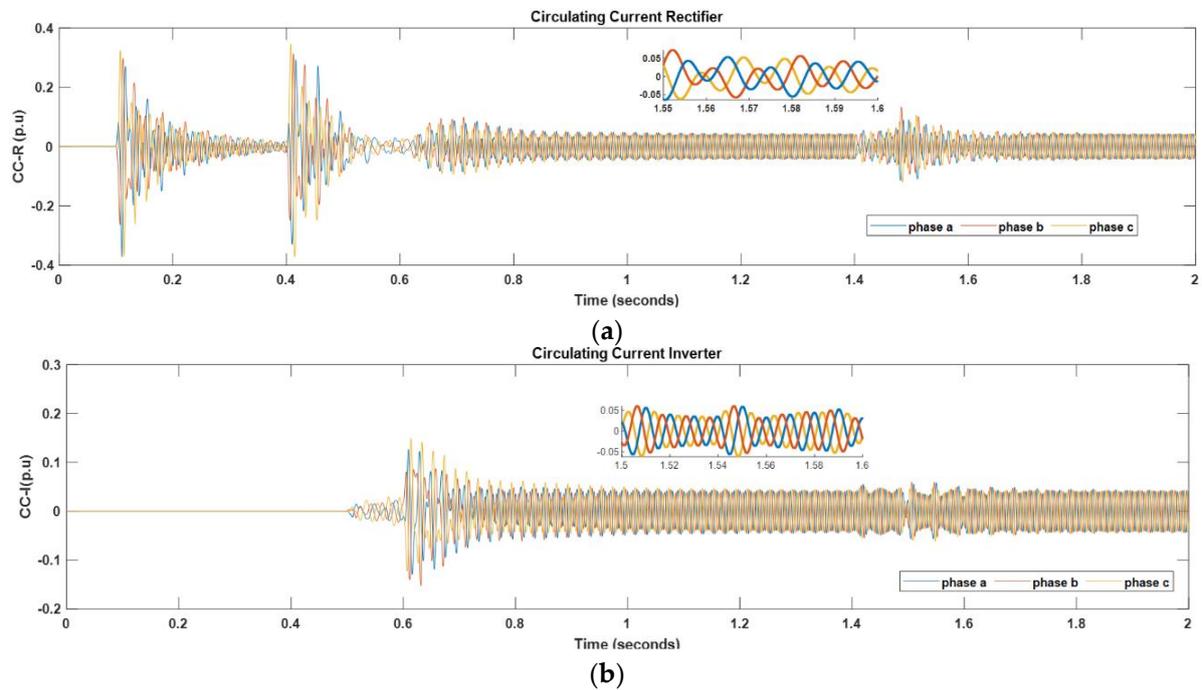


Figure 15. Results under AC fault (voltage dip): (a) circulating current of MMC rectifier; (b) circulating current of MMC inverter.

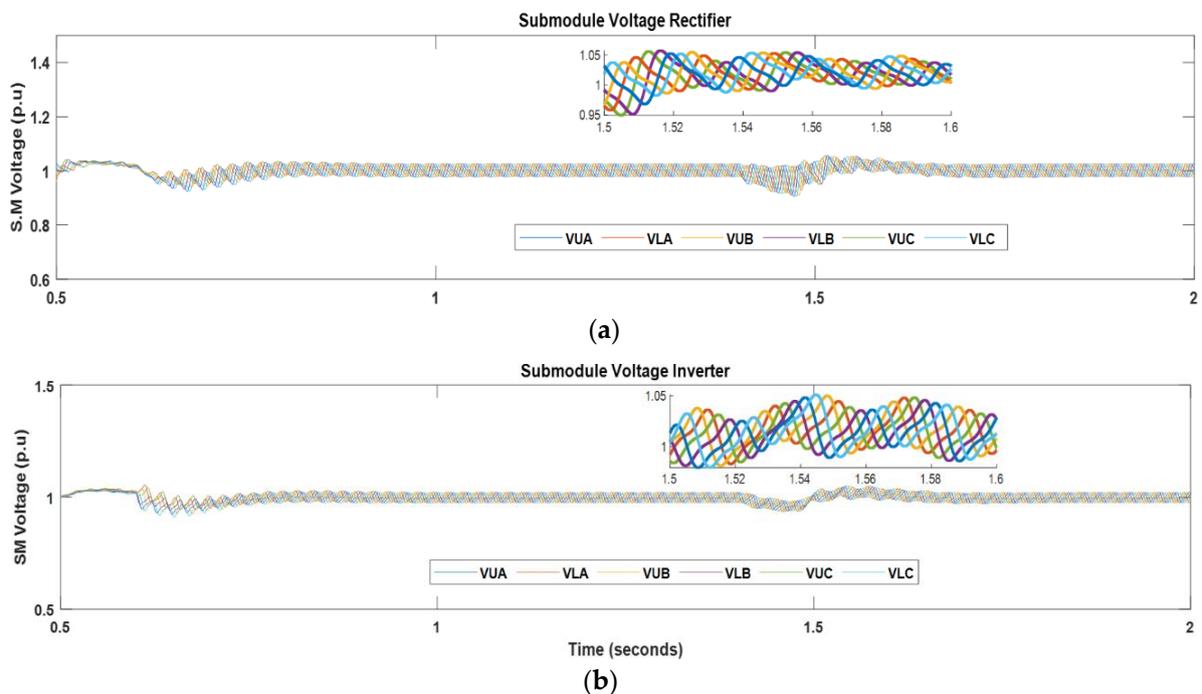


Figure 16. Results under AC fault (voltage dip): (a) SM capacitor voltage of MMC rectifier; (b) SM capacitor voltage of MMC inverter.

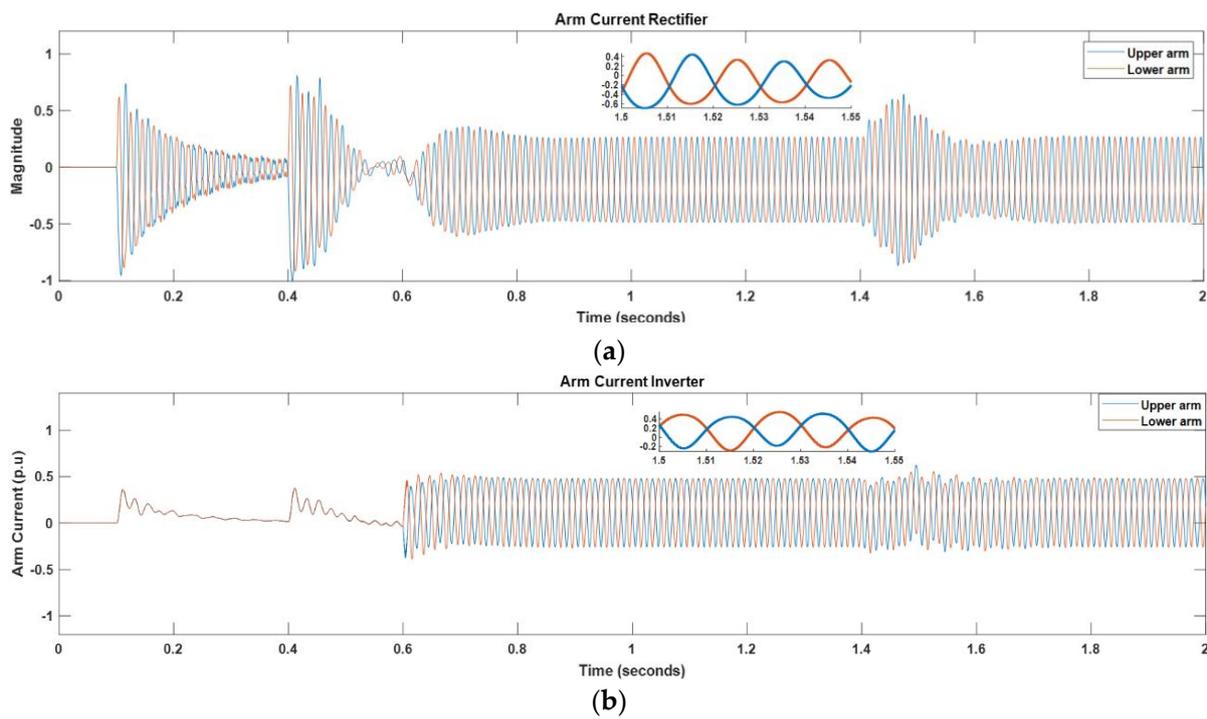


Figure 17. Results under AC fault (voltage dip): (a) MMC arm current rectifier; (b) MMC arm current inverter.

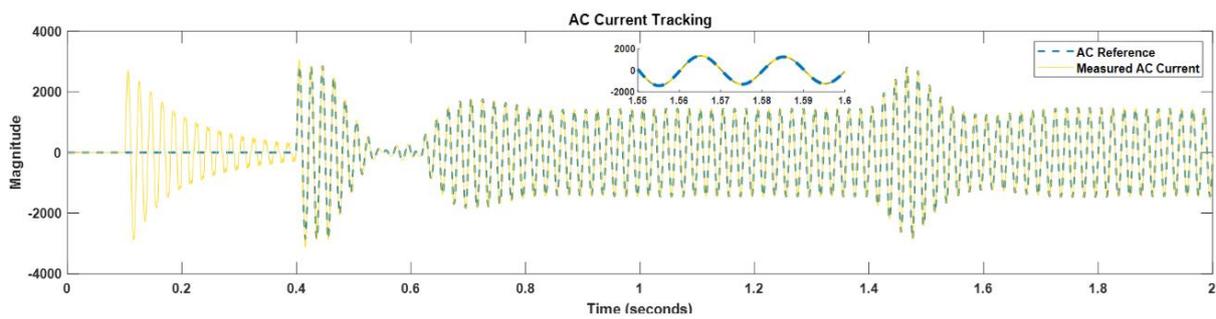


Figure 18. AC Current tracking by MPC algorithm under AC fault (voltage dip).

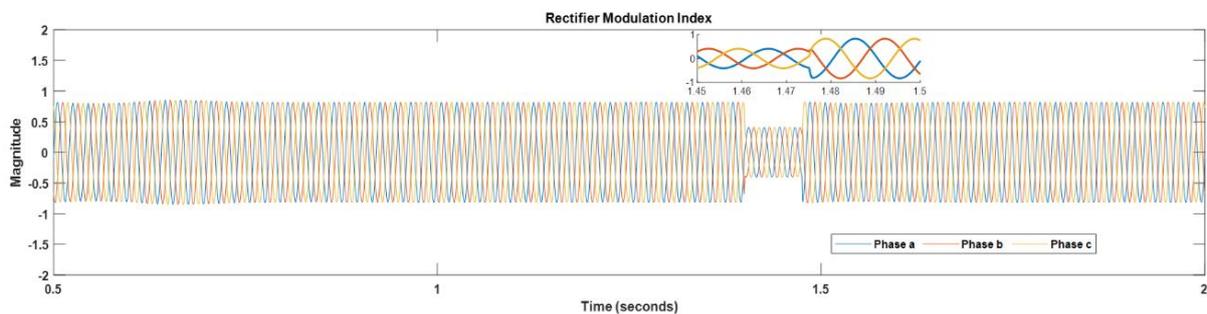


Figure 19. Modulation index of MMC rectifier under AC fault (voltage dip).

6. Conclusions

This paper presents the novel MPC algorithm to mitigate transient voltage dips for the MMC-HVDC system. The MPC algorithm is implemented and tested on various scenarios such as steady-state conditions and AC fault, such as three-phase voltage dips at the grid side. To develop the control algorithm, two cost functions are utilized: one for tracking the AC side current and another for suppressing the circulating current. The simulation results

demonstrate the robustness of the proposed MPC control algorithm, which effectively tracks the AC current and suppresses the circulating current and regulates capacitor voltages to comply with grid standards. Importantly, the developed MPC strategies efficiently manage the DC bus voltage, ensuring stable and desired power delivery to the connected load during AC faults. The proposed control strategies have demonstrated their effectiveness through validations on point-to-point HVDC systems. However, considering the global trend towards MTDC systems, it is essential to extend these tests to assess the suitability and performance of the strategies in MMC-based MTDC systems. This extension will address the emerging challenges and requirements in the evolving power transmission landscape. Although the current study provides a comprehensive analysis of AC FRT for MMC-HVDC systems, it does not cover DC FRT mechanisms. Therefore, future research should explore the development and implementation of effective DC FRT strategies to enhance the resilience and reliability of MMC-HVDC systems during DC-side faults. Additionally, expanding the system and testing it with the integration of renewable energy sources will be a focus for future research. The performance of the proposed control strategies will be analyzed in a hardware-in-the-loop (HIL) setup, further enhancing the scope of this study.

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