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A Family of Zero-Voltage-Transition Magnetic Coupling Bidirectional DC/DC Converters †

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Abstract: In this paper, a family of zero-voltage-transition (ZVT) magnetic coupling bidirectional DC/DC converters (BDCs) is proposed. The coupling inductor has two functions: to serve as a filter; and to provide the auxiliary current. In addition, the phase-shifting control method is used to reduce the conduction loss of the auxiliary circuit. The auxiliary switches are all working under zero-current-switching (ZCS) conditions; thus, all the switches have no switching loss. Furthermore, compared with the traditional ZVT implementation method based on the coupled inductor, this topology avoids the input source current notch and has a smaller ripple. Finally, a prototype of 800 W BDC is built to verify the feasibility of the proposed topology.

Keywords: zero-voltage-transition; zero-current-switching; buck/boost converter; coupled inductor

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1. Introduction

With the continuous growth of systems with energy storage devices, research on bidirectional DC–DC converters has been greatly promoted. Bidirectional DC–DC converters are widely used in photovoltaic and energy storage systems [1,2], electric/hybrid vehicles [3,4], uninterrupted power supply systems [5], fuel cell power systems [6,7], etc. In these applications, converters are required to have low current ripple requirements at the energy storage port. If electrical isolation is not required between the high-voltage port and low-voltage port, the BDC topology is usually chosen due to its low cost and simple structure. For BDC, switching loss is the main reason for limiting frequency increases. Therefore, in order to achieve a high-efficiency and high-frequency power conversion of BDC, it is necessary to introduce soft-switching technology.

One effective method to achieve the purpose of soft-switching is to make the BDC work in near-critical conduction modes [8–10]. However, the input current has a larger ripple, which leads to a high conduction loss and easy core saturation.

Quasi-resonant technology realizes the zero-voltage-switching (ZVS) of the main switch by using *LC* resonance to generate zero voltage when the main switch is turned on [11,12]. However, a large circulating current exists in the circuit, which leads to an increase in conduction loss. In addition, the switching frequency changes in a wide range when the load changes greatly, which will make the design of passive devices more difficult.

Active clamp ZVS technology also needs to add a resonant inductor in the main circuit to realize the ZVS of the main switch [13,14]. The circulating current of the auxiliary circuit is large, which increases the conduction loss. Moreover, the main switch has high voltage stress.

As the auxiliary circuit is removed from the main circuit and the auxiliary switch operates only during the period before and after the main switch is turned on, the conduction loss in the ZVT converter is reduced, while the voltage stress of the main switch is lower than that of the quasi-resonant converter and active clamp converter [15–18]. These ZVT converters all need additional inductors as resonant inductors, which are disadvantageous

to the improvement of power density because of the large volume and weight of magnetic components. Several soft-switching technologies based on coupled inductors have been proposed in [19–28].

In [19], a coupled winding is added to the same core of the main inductor to realize the soft switching of the main switch. In the ZVT BDC proposed in [20], a coupled inductor and two unidirectional auxiliary switches are used in the auxiliary circuit. A ZVT BDC is described in [21], while the auxiliary circuit consists of a coupled inductor and two auxiliary switches. A family of ZVS Buck, ZVS Boost, and ZVS BDC topologies is presented in [22], and the auxiliary circuit consists of a coupled inductor and a diode. In [23], a family of ZVS magnetic coupling BDC topologies is proposed. In those BDCs, the additional circuits contain two auxiliary switches. Two auxiliary voltage sources composed of passive components are used in the auxiliary circuit of the ZVS BDC in [24]. A ZVT BDC is proposed in [25], in which the auxiliary circuit consists of a coupled inductor, two unidirectional switches, and an auxiliary capacitor. In [26], a ZVT BDC is studied, in which all the switches implement ZVS or ZCS conditions. In [27], several ZVS DC–DC converters based on coupled inductors are proposed by changing the connection position of the coupling branch. A ZVS magnetic coupling BDC with no current notch at the low-voltage port is proposed in [28]. In [29], a ZVT PWM BDC based on coupled inductors is proposed. This topology needs two cores, increasing the complexity of the system. An overview of soft-switching technologies for BDC is given in [30].

As shown in Figure 1, there is an input current notch in the ZVS BDCs proposed in [20,21,23,24,26], which would hurt the life of storage equipment. In this paper, a family of ZVT magnetic coupling BDCs is proposed. The coupling inductor not only serves as a filter but also provides the auxiliary current. Compared with the traditional ZVS implementation method, this topology avoids the input source current notch and has a smaller ripple.

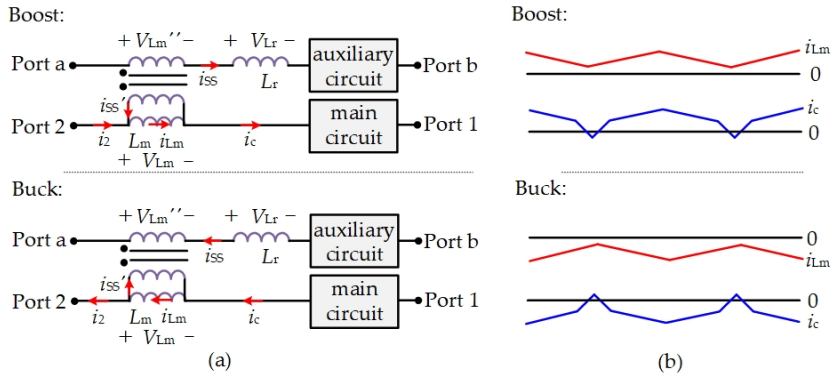

Figure 1. General circuit of ZVS BDCs with coupled filter inductors in [20,21,23,24,26]. (**a**) General circuit; (**b**) key waveforms of the input currents.

In Section 2, the topologies and operation process are demonstrated. In Section 3, the ZVT conditions of the main switches, the loss analysis, and the comparison between the proposed ZVT BDCs and the existing ZVT BDCs are given in detail. Moreover, the current frequency spectrum of the low-voltage port comparison between the proposed ZVT BDC and the traditional ZVT BDC is provided. In Section 4, the experimental results verify the validity of the topology. Finally, the conclusions are summarized.

2. Operation Process Analysis

2.1. Proposed ZVT BDCs

The ZVT magnetic coupling BDCs are shown in Figure 2. S_1 and S_2 are the switches of the main power circuit. S_{SS1} and S_{SS2} are the switches of the auxiliary circuit. C_{S1}, C_{S2}, and C_a are the three auxiliary capacitors. The coupled inductor is equivalent to an ideal transformer T, L_m (the excitation inductor), and L_r (the leakage inductor). C_1 and C_2 are

filter capacitors of Port 1 and Port 2. The difference between Topology 1 (as shown in Figure 2a) and Topology 2 (as shown in Figure 2b) is that the auxiliary circuit of Topology 1 is connected between Port 2 and the ground, and the auxiliary circuit of Topology 2 is connected between Port 1 and Port 2.

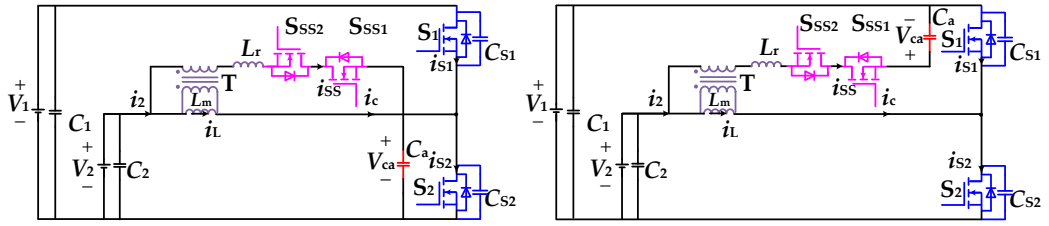

Figure 2. The proposed ZVS BDCs. (**a**) Topology 1; (**b**) Topology 2.

2.2. Operation Analysis of the Proposed ZVS BDCs

2.2.1. Operation Analysis of Topology 1

In Topology 1, as shown in Figure 2a, the switching process of each switch is shown in Figure 3. Taking the ZVS implementation of S_2 as an example, the switching process is analyzed, and the equivalent circuit of each stage is shown in Figure 4.

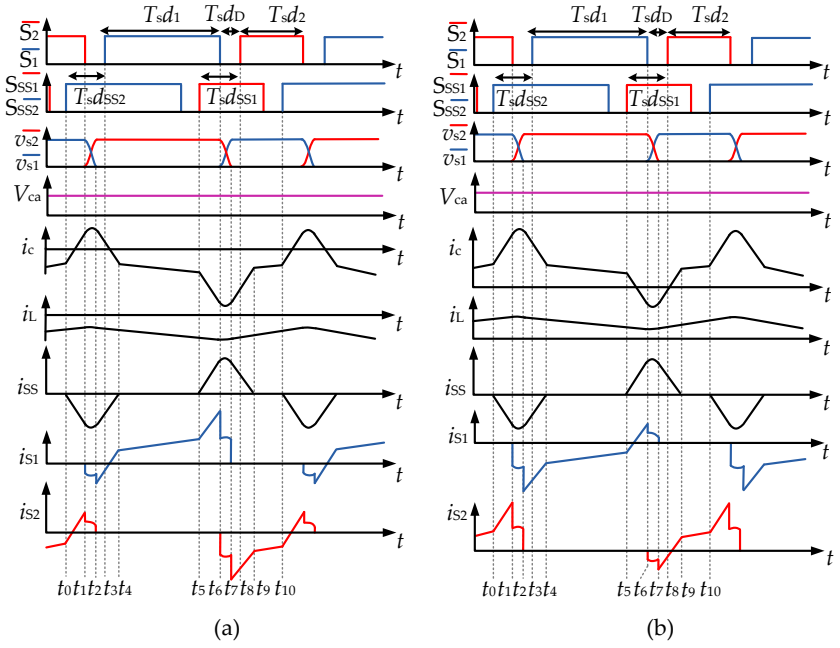

Figure 3. ZVS implementation of the main switch for topology 1. (**a**) ZVS implementation of S_1; (**b**) ZVS implementation of S_2.

Interval 1 [t_0–t_1]: At t_0, S_{SS2} is turned under the ZCS condition. The current i_{SS} increases because of the voltage clamp action of C_a, and the equivalent circuit is shown in Figure 4a.

Interval 2 [t_1–t_2]: At t_1, S_2 is turned off under the ZVS condition because of C_{S1} and C_{S2}. During this interval, v_{S1} decreases, v_{S2} increases, C_{S1} discharges, C_{S2} charges, and the equivalent circuit is shown in Figure 4b. The current i_{SS} at the resonance stage is:

$$i_{SS} = i_L(t_1) + 2A_{11}C_S\omega_{11}\sin(\omega_{11}(t - t_1) + \theta_{11}) \quad (1)$$

$$\omega_{11} = \frac{1}{\sqrt{2L_rC_S}} \quad (2)$$

$$A_{11} = \sqrt{{V_{ca}}^2 + \left[\frac{i_{SS}(t_1) - i_L(t_1)}{2C_S\omega_{11}}\right]^2} \tag{3}$$

$$\theta_{11} = \arctan\frac{i_{SS}(t_1) - i_L(t_1)}{-2C_S\omega_{11}V_{ca}} + \pi \tag{4}$$

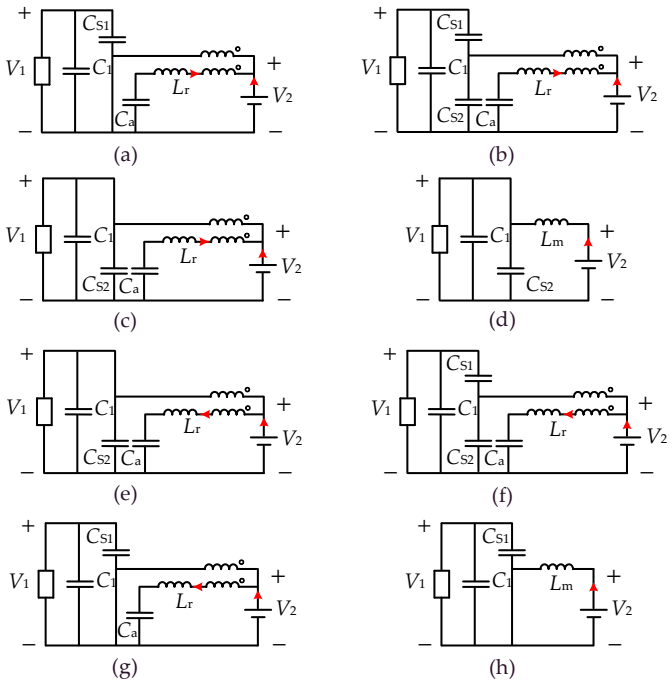

Figure 4. The equivalent circuit for each stage of Topology 1. (**a**) t_0–t_1; (**b**) t_1–t_2; (**c**) t_2–t_4; (**d**) t_4–t_5; (**e**) t_5–t_6; (**f**) t_6–t_7; (**g**) t_7–t_9; (**h**) t_9–t_{10}.

Interval 3 [t_2–t_3]: At t_2, v_{S1} decreases to 0, v_{S2} increases to V_1, and i_{S1} is a negative value, the equivalent circuit for this stage is shown in Figure 4c.

Interval 4 [t_3–t_4]: At t_3, S_1 is turned on under the ZVS condition.

Interval 5 [t_4–t_5]: The current i_{SS} is reduced to 0 at t_4, and the equivalent circuit for this stage is shown in Figure 4d.

Interval 6 [t_5–t_6]: S_{SS1} is turned on at t_5. The current i_{SS} increases because of the voltage clamp action of the capacitor C_a, and the equivalent circuit is shown in Figure 4e.

Interval 7 [t_6–t_7]: S_1 is turned off under ZVS condition at t_6 because of C_{S1} and C_{S2}. During this period, v_{S1} increases, v_{S2} decreases, C_{S1} charges, C_{S2} discharges, and the equivalent circuit is shown in Figure 4f. The auxiliary current i_{SS} at the resonance stage is:

$$i_{SS} = i_L(t_6) + 2A_{12}C_S\omega_{12}\sin(\omega_{12}(t - t_6) + \theta_{12}) \tag{5}$$

$$\omega_{12} = \frac{1}{\sqrt{2L_rC_S}} \tag{6}$$

$$A_{12} = \sqrt{(V_1 - V_{ca})^2 + \left[\frac{i_{SS}(t_6) - i_L(t_6)}{2C_S\omega_{12}}\right]^2} \tag{7}$$

$$\theta_{12} = \arctan\frac{i_{SS}(t_6) - i_L(t_6)}{2C_S\omega_{12}(V_1 - V_{ca})} \tag{8}$$

Interval 8 [t_7–t_8]: At t_7, v_{S1} increases to V_1, v_{S2} decreases to 0, and i_{S2} is a negative value. The equivalent circuit for this stage is shown in Figure 4g.

Interval 9 [t_8–t_9]: S_2 is turned on under the ZVS condition at t_8.

Interval 10 [t_9–t_{10}]: The current i_{SS} is reduced to 0 at t_9, and the equivalent circuit for this stage is shown in Figure 4h.

2.2.2. Operation Analysis of Topology 2

In Topology 2, as shown in Figure 2b, the switching process of each switch is shown in Figure 5. The switching process of S_1 is analyzed, and the equivalent circuit of each stage is shown in Figure 6.

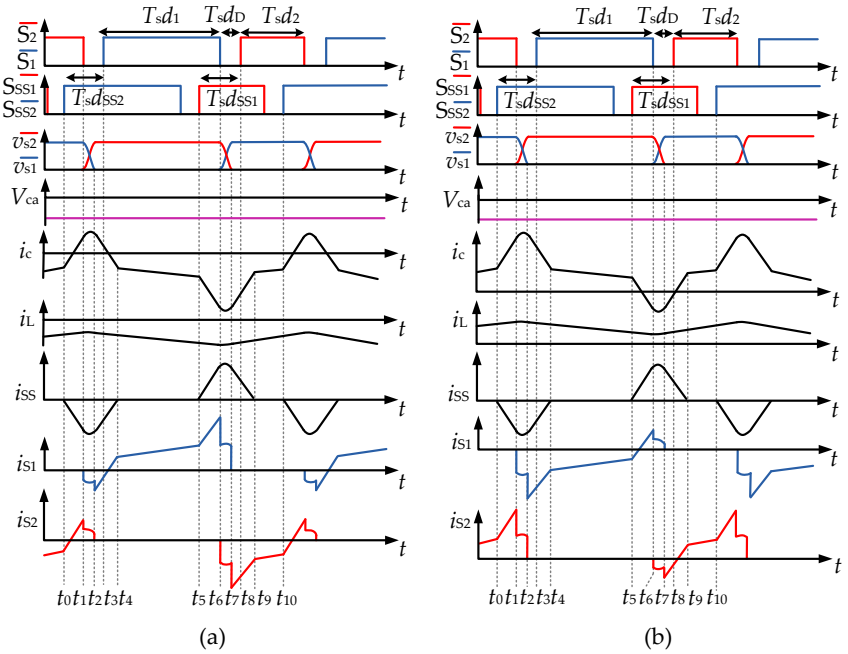

Figure 5. ZVS implementation of the main switch for Topology 2. (**a**) ZVS implementation of S_1; (**b**) ZVS implementation of S_2.

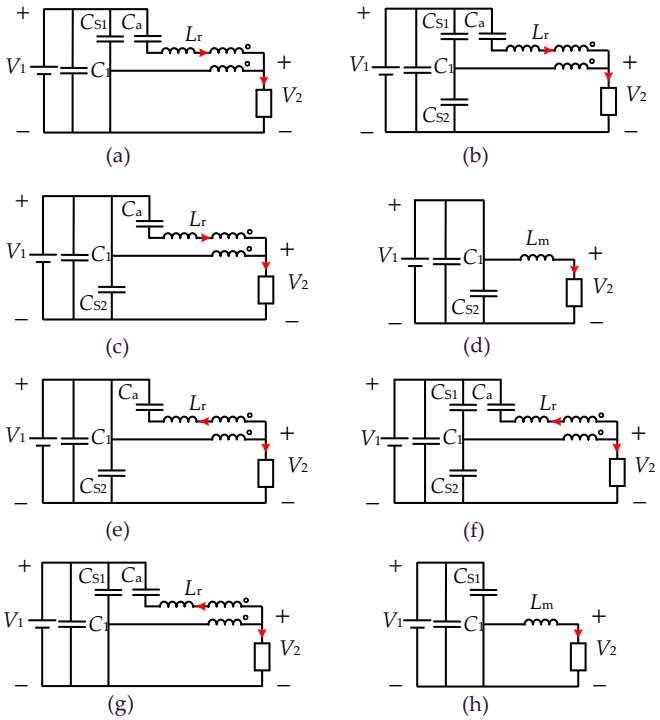

Figure 6. The equivalent circuit for each stage of Topology 2. (**a**) t_0–t_1; (**b**) t_1–t_2; (**c**) t_2–t_4; (**d**) t_4–t_5; (**e**) t_5–t_6; (**f**) t_6–t_7; (**g**) t_7–t_9; (**h**) t_9–t_{10}.

Interval 1 [t_0–t_1]: At t_0, S_{SS2} is turned on under the ZCS condition.

Interval 2 [t_1–t_2]: At t_1, S_2 is turned off under the ZVS condition. The current i_{SS} at the resonance stage is:

$$i_{SS} = i_L(t_1) + 2A_{21}C_S\omega_{21}\sin(\omega_{21}(t - t_1) + \theta_{21}) \tag{9}$$

$$\omega_{21} = \frac{1}{\sqrt{2L_rC_S}} \tag{10}$$

$$A_{21} = \sqrt{(V_1 + V_{ca})^2 + \left[\frac{i_{SS}(t_1) - i_L(t_1)}{2C_S\omega_{21}}\right]^2} \tag{11}$$

$$\theta_{21} = \arctan\frac{i_{SS}(t_1) - i_L(t_1)}{2C_S\omega_{21}(-V_1 - V_{ca})} + \pi \tag{12}$$

Interval 3 [t_2–t_3]: At t_2, v_{S1} decreases to 0, v_{S2} increases to V_1, and i_{S1} is a negative value.

Interval 4 [t_3–t_4]: At t_3, S_1 is turned on under the ZVS condition.

Interval 5 [t_4–t_5]: S_1 is on during this period.

Interval 6 [t_5–t_6]: S_{SS1} is turned on under the ZCS condition at t_5.

Interval 7 [t_6–t_7]: S_1 is turned off under the ZVS condition at t_6. The current i_{SS} at the resonance stage is:

$$i_{SS} = i_L(t_6) + 2A_{22}C_S\omega_{22}\sin(\omega_{22}(t - t_6) + \theta_{22}) \tag{13}$$

$$\omega_{22} = \frac{1}{\sqrt{2L_rC_S}} \tag{14}$$

$$A_{22} = \sqrt{{V_{ca}}^2 + \left[\frac{i_{SS}(t_6) - i_L(t_6)}{2C_S\omega_{22}}\right]^2} \tag{15}$$

$$\theta_{22} = \arctan\frac{i_{SS}(t_6) - i_L(t_6)}{-2C_S\omega_{22}V_{ca}} \tag{16}$$

Interval 8 [t_7–t_8]: At t_7, i_{S2} is a negative value.

Interval 9 [t_8–t_9]: S_2 is turned on under the ZVS condition at t_8.

Interval 10 [t_9–t_{10}]: S_2 is on during this period.

2.3. Other ZVT BDC Topologies

In addition to the topologies shown in Figure 2, other ZVT BDCs based on coupled inductor are shown in Figure 7.

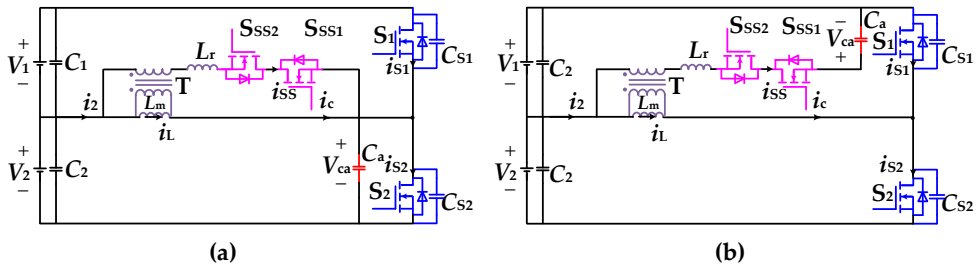

Figure 7. Other ZVT BDCs. (**a**) Topology 1; (**b**) Topology 2.

3. Performance Analysis

3.1. Analysis of Input Current Ripple

As shown in Figures 3 and 5, i_L is nearly constant during the resonance stage (t_1–t_2) and (t_6–t_7), and the ripple of i_L is:

$$\Delta I_L \approx \frac{V_2}{L_m} d_2 T_S \tag{17}$$

To further illustrate the advantages of the proposed ZVT BDCs, the harmonic comparison of i_L is compared between the ZVT BDC (shown in Figure 2a) and the traditional ZVS BDC (represented in [23]). Those two simulation models are built, with the simulation performed at the same voltage and power levels.

The simulation results are shown in Figures 8 and 9. Figure 8 shows the simulation results in Boost mode and Figure 9 in Buck mode. Figure 8a,b show the current i_2 and its harmonic analysis of ZVS BDC in [23], and when P_1 = 800 W, the harmonic amplitude of i_2 is 3.12 dBA (100 kHz). Figure 8c,d present the simulation results of the proposed ZVT BDC; the harmonic amplitude of i_2 is 0.63 dBA (100 kHz). As shown in Figure 9, when P_2 = 800 W, the proposed ZVT BDC has a 1.89 dBA (100 kHz) decrease in the harmonic amplitude of i_2 compared to ZVS BDC in [23].

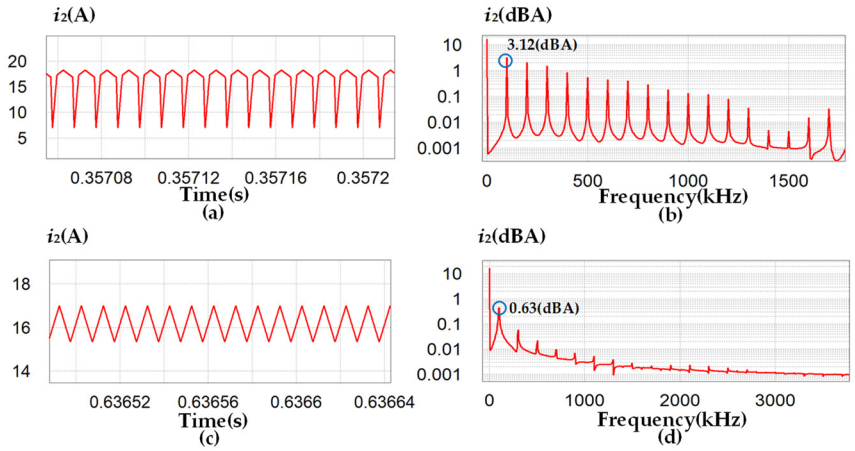

Figure 8. Harmonic comparison in Boost mode. (**a**) Input current of ZVS BDC in [23]; (**b**) harmonic analysis of input current of ZVS BDC in [23]; (**c**) input current of ZVT BDC (shown in Figure 2a); (**d**) harmonic analysis of input current of ZVT BDC (shown in Figure 2a).

3.2. Loss Analysis

In order to theoretically analyze the loss comparison between the traditional BDC and the proposed ZVT BDC, two simulation models are established. These work at 100 kHz and 500 kHz, respectively. The parameters are shown in Table 1, the proposed ZVT BDC is shown in Figure 2a, and the loss estimation is shown in Table 2.

Table 1. Detail parameters of 800 W ZVS Boost converter.

f_S = 100 kHz				f_S = 500 kHz			
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
V_2/V	50	V_1/V	100	V_2/V	50	V_1/V	100
P_{1max}/W	800	n	1	P_{1max}/W	800	n	1
L_c/μH	3.8	L_m/μH	130	L_c/μH	0.85	L_m/μH	160
C_1/μF	1000	C_2/μF	1000	C_1/μF	1000	C_2/μF	1000
C_S/nF	2.2	C_a/μF	200	C_S/nF	1	C_a/μF	80

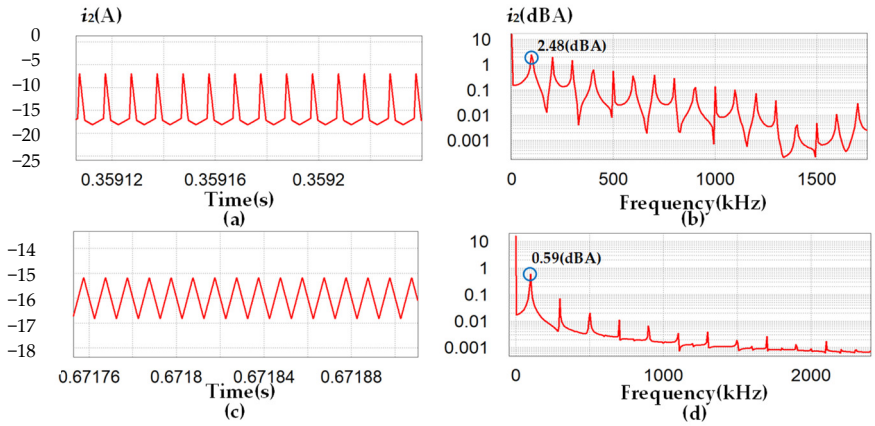

Figure 9. Harmonic comparison in Buck mode. (**a**) Output current of ZVS BDC in [23]; (**b**) harmonic analysis of output current of ZVS BDC in [23]; (**c**) output current of ZVT BDC (shown in Figure 2a); (**d**) harmonic analysis of output current of ZVT BDC (shown in Figure 2a).

Table 2. Loss comparison.

Loss Source	f_S = 100 kHz		f_S = 500 kHz	
	Traditional BDC	**Proposed BDC**	**Traditional BDC**	**Proposed BDC**
P_{c_S}	2.1 W	2.5 W	2.1 W	3.1 W
P_{c_SS}	---	5.4 W	---	10.4 W
P_{s_S}	19.1 W	---	95.5 W	---
P_{RR}	---	0.8 W	---	4.2 W
Core loss	1.9 W	2.1 W	0.3 W	0.4 W
Copper loss	2.7 W	3.3 W	2.9 W	4.3 W

For the proposed ZVT BDC, MOSFET IRFP4668 is applied as the main switch, and MOSFET SUP90142E is utilized as the auxiliary switch, respectively. The on-resistance of the main switch is 0.008 Ω, the on-resistance of the auxiliary switch is 0.017 Ω, and the diode forward voltage of the auxiliary switch is 0.85 V (the junction temperature (Tj) is 75°). The core of the coupled inductor is E220–18. In the traditional BDC model, the filter inductor adopts the magnetic core KS25060A, and the main switch adopts MOSFET IRFP4668.

For the traditional BDC, the main loss includes P_{c_S} (conduction loss of S_1 and S_2), P_{s_S} (switching loss of S_1 and S_2), core loss, and copper loss. For the proposed ZVS BDC, the main loss includes P_{c_S} (conduction loss of S_1 and S_2), P_{c_SS} (conduction loss of S_{SS1} and S_{SS2}), P_{RR} (Reverse recovery loss of S_{SS1} and S_{SS2}), core loss, and copper loss.

When the switching frequency of the converter is increased to more than 500 kHz, the switching loss of the conventional BDC will greatly reduce the efficiency of the converter; the introduction of soft-switching measures is especially necessary.

3.3. Topology Comparison

The ZVS conditions can be realized when the circuit is operating under Buck mode or Boost mode in the ZVS BDC in [19,22,27]. Table 3 shows the topology comparison between the ZVS BDC in the existing literature and the proposed ZVS BDC (as shown in Figure 2a).

Table 3. Topology comparison.

Topology	Number of Auxiliary Switches	Number of Auxiliary Diodes	Current Notch	Voltage Stress of Auxiliary Switches
ZVT BDC [17]	2	2	exist	$\max\{DV_1, (1-D)V_1\}$
ZVS BDC [18]	2	0	exist	Buck: V_2 Boost: $V_1 - V_2$
ZVT BDC [20]	2	2	exist	$(1+nD)V_2$
ZVT BDC [21]	2	0	exist	nDV_1
ZVS BDC [23]	2	0	exist	S_{a1}: $(n+1)V_2$ S_{a2}: $(n+1)(V_1 - V_2)$
ZVS BDC [24]	2	2	exist	Buck: $\max\{\lvert(n-1)(V_1-V_2)\rvert, V_2 + n(V_1-V_2)\}$ Boost: $\max\{\lvert(n-1)V_2\rvert, V_1 + (n-1)V_2\}$
ZVT BDC [25]	2	2	no	Buck: >0.5 V_2 Boost: >0.5 V_2
ZVT BDC [26]	2	0	exist	S_{a1}: $(n+1)(V_1 - V_2)$ S_{a2}: $(n+1)V_2$
ZVS BDC [28]	2	2	no	S_{SS1}: $\frac{2}{3}\left[\frac{L_1(V_1-V_2)}{L_1+L_c-2M} + V_2\right] - \frac{1}{3}V_1$ S_{SS2}: $-\frac{2}{3}\frac{(L_c-M)V_2}{L_1+L_c-2M} + \frac{1}{3}V_1$
Proposed ZVT BDCs	2	0	no	S_{SS1}: $V_1 - V_{ca}$ S_{SS2}: V_{ca}

The topologies in [17,18] construct auxiliary circuits by adding auxiliary inductors, and the topology in [24] constitutes an auxiliary circuit by adding an auxiliary inductor and introducing a coupling inductor. The topologies in [19–23,25–28] and this paper use coupling inductors to construct auxiliary branches, which reduce the number of inductors. In order to realize soft switching in both operating modes (Buck and Boost), two auxiliary switches are required. To reduce the loss of auxiliary circuits, the diodes in [20,25,28] need to have good reverse recovery characteristics and low–forward voltage drops, which will increase the cost. In the topologies in [17–24,26], to realize the ZVT of main switches, notches exist in the current at Port 2. When Port 2 is connected to a battery, the current notch can adversely affect the battery life. However, the proposed ZVT BDC can avoid this notch phenomenon. For the topologies with no current notch in [25,28] and the proposed ZVT BDC, the current stress of the auxiliary switch depends on the current and ripple at Port 2, and the current stress is similar when the power and voltage levels are the same. In terms of voltage stress, the topology of the proposed ZVT BDC is less than that of [25].

4. System Design

4.1. Design of Initial Value V_{ca}

4.1.1. Design of Initial Value V_{ca} in Topology 1

For Topology 1, shown in Figure 2a, in the switching process shown in Figure 3, the resonance process should be ignored to simplify the analysis. The voltage V_{ca} of the auxiliary capacitor C_a during the period (t_0–t_1) is:

$$V_{ca} = \frac{I_{SS} L_r}{t_1 - t_0} \tag{18}$$

During the period (t_5–t_6), the voltage V_{ca} of C_a is:

$$V_{ca} = V_1 - \frac{I_{SS} L_r}{t_6 - t_5} \tag{19}$$

When the period (t_0–t_1) and (t_5–t_6) are the same, the phase-shifting duty cycles of the auxiliary switch S_{SS1} and S_{SS2} are the same. According to (18) and (19), the initial value $V_{ca} = 0.5\ V_1$ can be obtained. Considering the resonant process in the dead time, the actual V_{ca} is different from $0.5\ V_1$.

4.1.2. Design of Initial Value V_{ca} in Topology 2

For Topology 2, shown in Figure 2b, the switching process is shown in Figure 5. During the period (t_0–t_1), V_{ca} is:

$$V_{ca} = -V_1 + \frac{I_{SS} L_r}{t_1 - t_2} \tag{20}$$

During the period (t_5–t_6), V_{ca} is:

$$V_{ca} = -\frac{I_{SS} L_r}{t_6 - t_5} \tag{21}$$

When the periods (t_0–t_1) and (t_5–t_6) are the same, the initial value $V_{ca} = -0.5\ V_1$ can be obtained according to (20) and (21). Considering the resonant process in the dead time, the actual V_{ca} is different from $-0.5\ V_1$.

4.2. Design of the Coupled Inductor

In the topology shown in Figure 2, the turn ratio of transformer T is n, the primary side is connected to the main circuit, the excitation inductor acts as a filter, and the secondary side is connected to the auxiliary circuit. i_L is the current flowing through the excitation inductor, i_{SS} is the current of the auxiliary circuit, i_{SS}' is the current converted to the primary side, and $i_{SS}' = i_{SS}/n$. The current of Port 2 is:

$$i_2 = i_{SS} + i_c \tag{22}$$

The current i_c is:

$$i_c = i_L - i_{SS}' \tag{23}$$

According to (22) and (23), the current of port 2 is $i_2 = i_{SS} + i_L - i_{SS}'$. Therefore, when $n = 1$, $i_2 = i_L$.

In the topology shown in Figure 2, L_m is the filter inductor for the BDC, duty cycle d_2 is $(1 - V_2/V_1)$, and the current ripple for i_L is:

$$\Delta i_L \approx \frac{V_2}{L_m} d_2 T_S \tag{24}$$

The ripple $\Delta i_2 = \Delta i_L$, taking $\Delta i_L = x_1 i_L$, x_1 is the ripple coefficient, and the value of L_m can be obtained according to the requirement of ripple.

4.2.1. Design of L_r in Topology 1

In Topology 1, the maximum value of auxiliary current i_{SS} is:

$$\Delta i_{SSmax\_1} = \frac{V_1 - V_{ca}}{L_r} T_S d_{SS1} \tag{25}$$

For Buck mode, the following condition should be met to realize the ZVS of S_1:

$$I_L + \frac{1}{2}\Delta i_L + \Delta i_{SSmax\_1} > 0 \tag{26}$$

For Boost mode, the following condition should be met:

$$I_L - \frac{1}{2}\Delta i_L - \Delta i_{SSmax\_1} < 0 \tag{27}$$

From (26) and (27), the value of L_r can be obtained.

4.2.2. Design of L_r in Topology 2

In topology 2, the maximum value of auxiliary current i_{SS} is:

$$\Delta i_{SSmax\_2} = \frac{-V_{ca}}{L_r} T_S d_{SS2} \tag{28}$$

To realize the ZVS of S_1 and S_2, the following conditions should be satisfied:

$$I_L + \frac{1}{2}\Delta i_L + \Delta i_{SSmax\_2} > 0 \tag{29}$$

$$I_L - \frac{1}{2}\Delta i_L - \Delta i_{SSmax\_2} < 0 \tag{30}$$

From (29) and (30), the value of L_r can be obtained.

4.3. Design of C_S

4.3.1. Design of C_S in Topology 1

For Topology 1, according to the ZVS implementation process as shown in Figure 3b, dead time needs to satisfy:

$$\Delta t_{12} = t_2 - t_1 = \frac{1}{\omega_{11}}(\arccos\frac{-V_{ca}}{A_{11}} - \arccos\frac{V_1 - V_{ca}}{A_{11}}) < t_D \tag{31}$$

$$\Delta t_{67} = t_7 - t_6 = \frac{1}{\omega_{12}}(\arccos\frac{-V_{ca}}{A_{12}} - \arccos\frac{V_1 - V_{ca}}{A_{12}}) < t_D \tag{32}$$

At time t_7, the values of i_c and i_{S2} are:

$$i_c(t_7) = -2A_{12}C_S\omega_{12}\sin(\omega_{12}(t_7 - t_6) + \theta_{12}) \tag{33}$$

$$i_{S2}(t_7) = -A_{12}C_S\omega_{12}\sin(\omega_{12}(t_7 - t_6) + \theta_{12}) \tag{34}$$

When S_2 is turned on, i_{S2} needs to meet:

$$i_{S2}(t_{S2\_on}) = i_{S2}(t_7) + \left(\frac{V_{ca}}{L_r} + \frac{V_2}{L_m}\right) \times (t_D - \Delta t_{67}) < 0 \tag{35}$$

According to (31)–(35),the value of C_S can be obtained.

4.3.2. Design of C_S in Topology 2

For Topology 2, according to the ZVS implementation process as shown in Figure 5a, in order to realize the ZVS of S_1, the following conditions should be met:

$$\Delta t_{12} = t_2 - t_1 = \frac{1}{\omega_{21}}(\arccos\frac{-V_1 - V_{ca}}{A_{21}} - \arccos\frac{-V_{ca}}{A_{21}}) < t_D \tag{36}$$

$$\Delta t_{67} = t_7 - t_6 = \frac{1}{\omega_{22}}(\arccos\frac{-V_1 - V_{ca}}{A_{22}} - \arccos\frac{-V_{ca}}{A_{22}}) < t_D \tag{37}$$

$$i_{S1}(t_{S1\_on}) = i_{S1}(t_2) + \left(\frac{-V_{ca}}{L_r} + \frac{V_1 - V_2}{L_m}\right) \times (t_D - \Delta t_{12}) < 0 \tag{38}$$

According to (36)–(38), the value of C_S can be obtained.

4.4. Design of C_a

4.4.1. Design of C_a in Topology 1

As the voltage source of the auxiliary circuit, the voltage V_{ca} of the auxiliary capacitor C_a can be determined according to the duration of (t_0–t_1) and (t_5–t_6), and the voltage ripple ΔV_{ca} is:

$$\Delta V_{ca} = \frac{1}{C_a}\int_{t_0}^{\frac{T_S}{2}} i_{SS}(t)dt \tag{39}$$

In order to simplify the analysis, ignoring the resonance process and according to (39) and Figure 3, ΔV_{ca} can be obtained:

$$\Delta V_{ca} \approx \frac{V_1 V_{ca} T_S^2 d_{SS2}^2}{2C_a L_r (V_1 - V_{ca})} \tag{40}$$

Taking $\Delta V_{ca} = x_2 V_{ca}$, x_2 is the voltage ripple coefficient, and the value of auxiliary capacitance C_a can be obtained according to the requirement of voltage ripple.

4.4.2. Design of C_a in Topology 2

According to (39), and Figure 5, ΔV_{ca} can be obtained:

$$\Delta V_{ca} \approx -\frac{V_1 (V_1 + V_{ca}) T_S^2 d_{SS2}^2}{2C_a L_r V_{ca}} \tag{41}$$

Similarly, according to the ripple requirements, the value of the auxiliary capacitor C_a can be obtained.

Taking the ZVT BDC (as shown in Figure 2a) design process as an example, a step-by-step design methodology working in Boost mode is given in Table 4. The other topologies and the design process in Buck mode are similar and will not be repeated.

4.5. Design of the Control Method

Figure 10 shows the implementation of the control method, which is divided into two cases (Buck mode and Boost mode). The PI regulator of the output voltage (V_2 under Buck, V_1 in Boost) generates the modulation signal v_{ctrl}, and the phase difference between the carrier signals v_{triS1} and v_{triS2} is 180°, generating the drive signals of S_1 and S_2 by comparators. To obtain the driving signals of S_{SS1} and S_{SS2}, firstly, judge the working mode of the system (Buck mode or Boost mode) according to the voltages and currents of Ports 1 and 2. The phase-shifting duty cycles d_{SS1} and d_{SS2} are calculated according to the working mode. In order to ensure that the auxiliary current is large enough, d_{SS1} and d_{SS2} require a certain amount of margin Δd. The phase-shifting controller shifts the carrier signals v_{triS1} and v_{triS2} according to d_{SS1} and d_{SS2}, and the carrier signals of S_{SS1} and S_{SS2}, v_{triSS1} and v_{triSS2}, are obtained. The driving signals of S_{SS1} and S_{SS2} are generated by comparators.

Table 4. Step-by-step design methodology.

Step 1	Determine the voltages (V_1 and V_2) and power level according to the system requirements.
Step 2	Ignore the resonance process and select initial value of V_{ca}, $V_{ca} = 0.5V_1$.
Step 3	Design L_m of T according to the requirements of current ripple, and $L_m \geq \frac{V_2 d_2 T_S}{x_1 I_L}$.
Step 4	Select $n = 1$.
Step 5	Design L_r of T according to $I_L - 0.5\Delta i_L - \Delta i_{SS} < 0$, in which $\Delta i_{SS} = \frac{V_1 - V_{ca}}{L_r} T_S d_{SS1}$.
Step 6	Determine value range of (C_S, t_d) according to $\begin{cases} t_{12} < t_d \\ t_{67} < t_d \\ i_{S2}(t_{S2\_on}) < 0 \end{cases}$, and select C_S and t_d.
Step 7	Design C_a according to the requirements of voltage ripple, and $C_a \geq \frac{1}{x_2 V_{ca}} \int_{t_0}^{\frac{T_s}{2}} i_{SS}(t)dt$.
Step 8	Simulation and experimental verification.

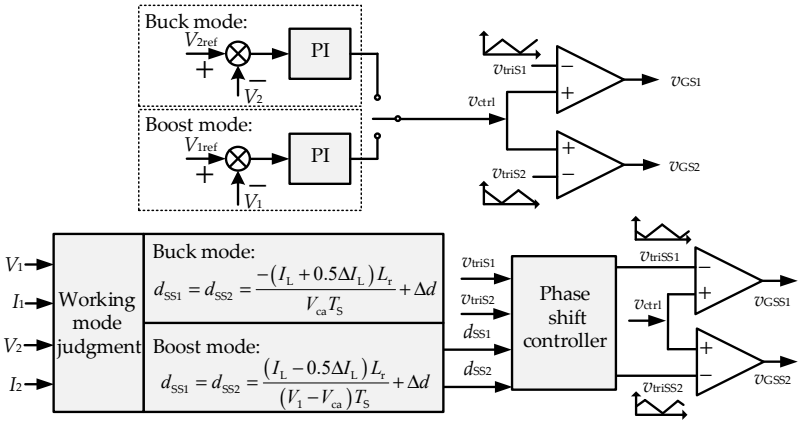

Figure 10. Control schematic diagram.

5. Experimental Verification

Using DSP TMS320F28377SPTPT as the controller, MOSFET IRFP4668 as the main switch, and MOSFET SUP90142E as the auxiliary switch, a BDC prototype is built, as shown in Figure 11. Detailed experimental parameters are shown in Table 5.

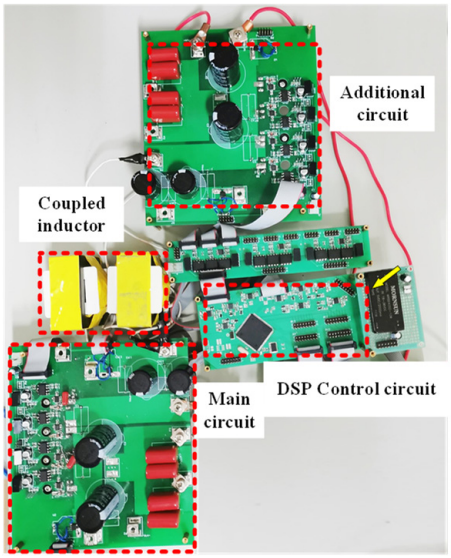

Figure 11. Experimental platform.

Table 5. Detail parameters of experimental platform.

Parameter	Value	Parameter	Value
V_2/V	40~60	V_1/V	100
f_S/kHz	100	n	1
L_c/μH	3.8	L_m/μH	130
C_1 and C_2/μF	1000	C_S/nF	2.2
P_{1max} and P_{2max}/W	800	C_a/μF	200

To verify the validity of the two ZVT BDCs shown in Figure 2, two sets of experiments were conducted, in each set of experiments; the power level is 800 W. The experimental waveforms of these two topologies operating in two modes (Buck and Boost) and two duty cycles (d_1 = 0.4 and d_1 = 0.6) are given. The control method utilized in the experiments is shown in Figure 10.

Figures 12–15 show the experimental waveforms of the topology shown in Figure 2a.

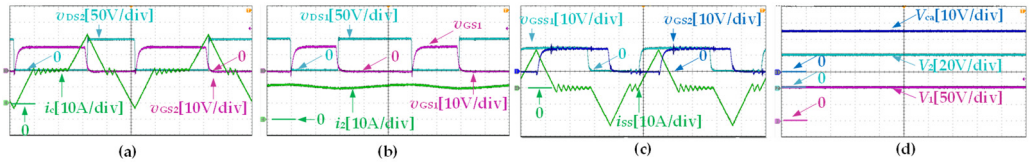

Figure 12. Experimental waveforms of BDC Topology 1 when P_1 = 800 W, V_1 = 100 V, d_1 = 0.4 (t − 2 µs/div). (**a**) v_{DS2}, v_{GS2}, and i_c; (**b**) v_{DS1}, v_{GS1}, and i_2; (**c**) v_{GSS1}, v_{GS2}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

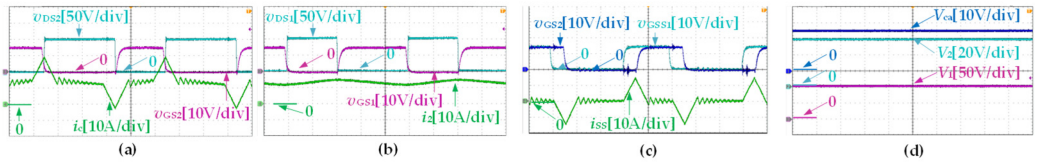

Figure 13. Experimental waveforms of BDC Topology 1 when P_1 = 800 W, V_1 = 100 V, d_1 = 0.6 (t − 2 µs/div). (**a**) v_{DS2}, v_{GS2}, and i_c; (**b**) v_{DS1}, v_{GS1}, and i_2; (**c**) v_{GSS1}, v_{GS2}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

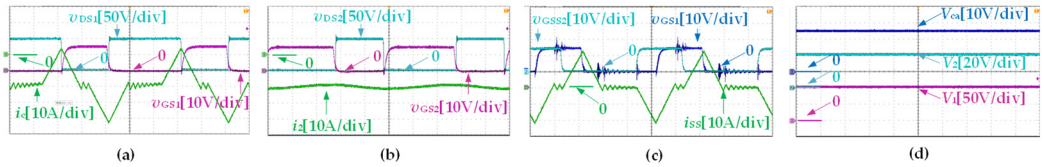

Figure 14. Experimental waveforms of BDC Topology 1 when P_2 = 800 W, V_1 = 100 V, d_1 = 0.4 (t − 2 µs/div). (**a**) v_{DS1}, v_{GS1}, and i_c; (**b**) v_{DS2}, v_{GS2}, and i_2; (**c**) v_{GSS2}, v_{GS1}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

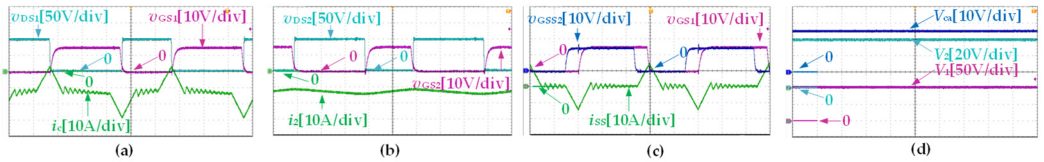

Figure 15. Experimental waveforms of BDC Topology 1 when P_2 = 800 W, V_1 = 100 V, d_1 = 0.6 (t − 2 µs/div). (**a**) v_{DS1}, v_{GS1}, and i_c; (**b**) v_{DS2}, v_{GS2}, and i_2; (**c**) v_{GSS2}, v_{GS1}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

When ZVS BDC operates in Boost mode, P_1 = 800 W, V_1 = 100 V, Figures 12 and 13 are the experimental waveforms under the condition of V_2 = 40 V and V_2 = 60 V, respectively. The main switches S_1 and S_2 are turned on and off under ZVS conditions, and the auxiliary switches S_{SS1} and S_{SS2} are turned on and off under ZCS conditions. When V_2 is 40 V and 60 V, in order to achieve the ZVS of S_2, the phase shift angles between the drive signals v_{GSS1} and v_{G2} can be 60° and 45°, respectively.

When ZVS BDC operates in Buck mode, P_2 = 800 W, V_1 = 100 V, Figures 14 and 15 are the experimental waveforms under the condition of V_2 = 40 V and V_2 = 60 V, respectively. The main switches S_1 and S_2, are turned on and off under ZVS conditions, and the auxiliary switches S_{SS1} and S_{SS2} are turned on and off under ZCS conditions. When V_2 is 40 V and 60 V, in order to achieve the ZVS of S_1, the phase shift angles between the drive signals v_{GSS2} and v_{G1} can be 60° and 45°, respectively.

Figures 16–19 show the experimental waveforms of the topology shown in Figure 2b.

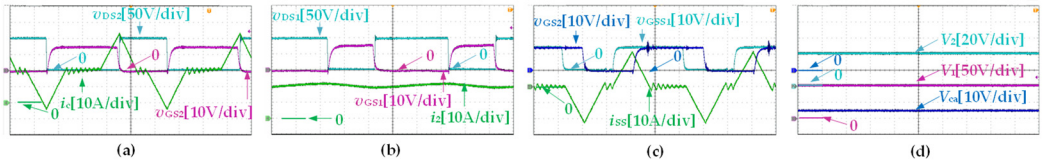

Figure 16. Experimental waveforms of BDC Topology 2 when P_1 = 800 W, V_1 = 100 V, d_1 = 0.4 (t – 2 µs/div). (**a**) v_{DS2}, v_{GS2}, and i_c; (**b**) v_{DS1}, v_{GS1}, and i_2; (**c**) v_{GSS1}, v_{GS2}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

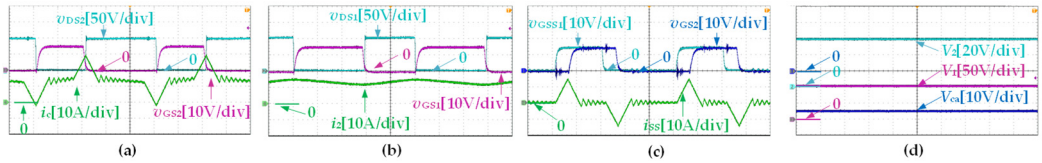

Figure 17. Experimental waveforms of BDC Topology 2 when P_1 = 800 W, V_1 = 100 V, d_1 = 0.6 (t – 2 µs/div). (**a**) v_{DS2}, v_{GS2}, and i_c; (**b**) v_{DS1}, v_{GS1}, and i_2; (**c**) v_{GSS1}, v_{GS2}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

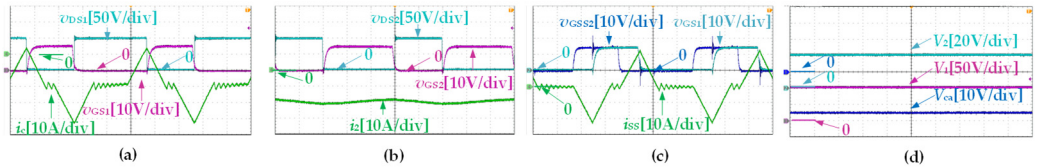

Figure 18. Experimental waveforms of BDC Topology 2 when P_2 = 800 W, V_1 = 100 V, d_1 = 0.4 (t – 2 µs/div). (**a**) v_{DS1}, v_{GS1}, and i_c; (**b**) v_{DS2}, v_{GS2}, and i_2; (**c**) v_{GSS2}, v_{GS1}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

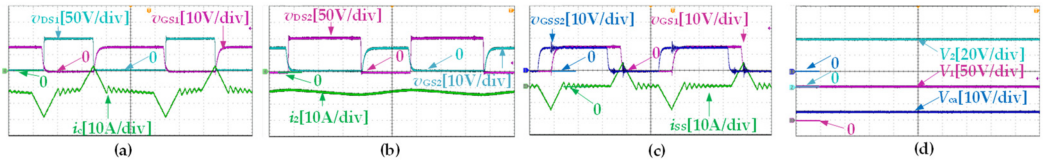

Figure 19. Experimental waveforms of BDC Topology 2 when P_2 = 800 W, V_1 = 100 V, d_1 = 0.6 (t – 2 µs/div). (**a**) v_{DS1}, v_{GS1}, and i_c; (**b**) v_{DS2}, v_{GS2}, and i_2; (**c**) v_{GSS2}, v_{GS1}, and i_{SS}; (**d**) V_1, V_2, and V_{ca}.

When ZVS BDC operates in Boost mode, P_1 = 800 W, V_1 = 100 V, Figures 16 and 17 are the experimental waveforms under the condition of V_2 = 40 V and V_2 = 60 V, respectively. The main switches S_1 and S_2 are turned on and off under ZVS conditions, and the auxiliary switches S_{SS1} and S_{SS2} are turned on and off under ZCS conditions. When V_2 is 40 V and 60 V, in order to achieve the ZVS of S_2, the phase shift angles between the drive signals v_{GSS1} and v_{G2} can be 60° and 45°, respectively.

When ZVS BDC operates in Buck mode, P_2 = 800 W, V_1 = 100 V, Figures 18 and 19 are the experimental waveforms under the condition of V_2 = 40 V and V_2 = 60 V, respectively. The main switches S_1 and S_2 are turned on and off under ZVS conditions, and the auxiliary switches S_{SS1} and S_{SS2} are turned on and off under ZCS conditions. When V_2 is 40 V and 60 V, in order to achieve the ZVS of S_1, the phase shift angles between the drive signals v_{GSS2} and v_{G1} can be 60° and 45°, respectively.

As shown in Figures 12–19, the current at Port 2 has no notch when these two proposed ZVT BDCs operate in both two modes (Buck and Boost). In Topology 1, $V_{ca} > 0$, and in Topology 2, $V_{ca} < 0$. When the power circuit operates in Buck mode, the current i_c flowing through the bridge arm (S_1 and S_2) changes from negative to positive before S_1 is turned on due to the auxiliary current. When the power circuit operates in Boost mode, i_c changes from positive to negative before S_2 is turned on, realizing ZVT conditions for S_1 and S_2.

When the average value of i_2 changes, the peak of i_{SS} has different requirements. Thus, d_{SS1} and d_{SS2} need to be adjusted. In addition, auxiliary switches are turned on and off under ZCS conditions.

As shown in Figure 20, the main loss sources of a traditional BDC include conduction loss of the main switch, switching loss of the main switch, copper loss and core loss of the inductor. The main loss sources of the proposed ZVS BDC include the conduction loss of the main switch, conduction loss of the auxiliary switch, RR loss of the auxiliary switch, copper loss, and core loss of inductor. For the traditional BDC topology, switching loss accounts for the largest proportion of the total loss, while for the proposed BDC, the largest source is conduction loss. As shown in Figure 21, compared to the traditional BDC, the maximum efficiency of the proposed BDC (shown in Figure 2a) can be improved by 1.2%.

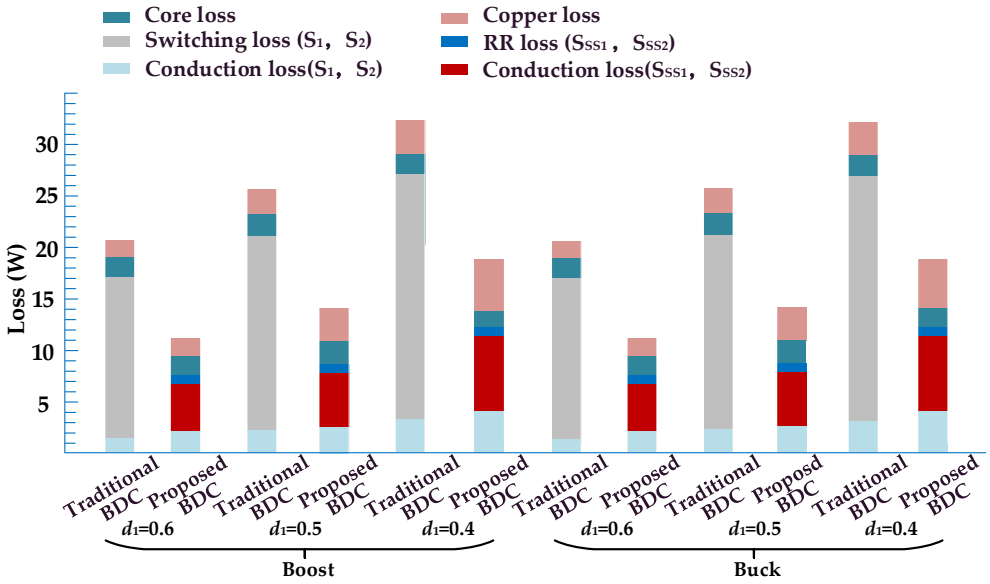

Figure 20. Loss analysis.

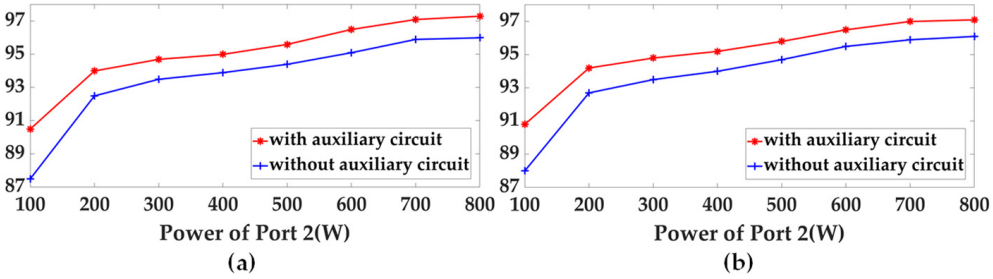

Figure 21. Efficiency curves with and without auxiliary circuit. (**a**) Boost; (**b**) Buck.

Through the theoretical analysis of the loss of traditional BDC, when the switching frequency is increased to more than 500 kHz, it is necessary to introduce the ZVT implementation measures. According to the efficiency curve of the existing topology, the loss analysis is carried out when the switching frequency is greater than 500 kHz, and the comparison of the theoretical efficiency values among different topologies under full load when the switching frequency $f_S \geq 500$ kHz is shown in Table 6.

Table 6. Efficiency comparison when the switching frequency $f_S \geq 500$ kHz.

Topology	Boost	Buck
ZVS BDC [17]	96.7%	95.2%
ZVS BDC [18]	97.2%	96.5%
ZVT BDC [20]	95.7%	95.6%
ZVT BDC [21]	97.7%	97.2%
ZVS BDC [23]	97.5%	97.5%
ZVS BDC [24]	96.3%	96.5%
ZVT BDC [25]	95.3%	95.4%
ZVT BDC [26]	92.2%	93.3%
ZVS BDC [28]	96.4%	96.2%
The proposed ZVT BDCs	96.7%	96.7%

6. Conclusions

In this paper, several ZVT magnetic coupling BDCs are proposed. In these topologies, the excitation inductor of the transformer acts as a filter, and the leakage inductor is used to generate auxiliary current. When the turn ratio is 1:1, the current of the original side and the secondary side is the same but in the opposite direction. Thus, the current notch at the low voltage port can be eliminated. The main switches can achieve ZVT conditions, and the auxiliary switches can achieve ZCS conditions. In order to verify the feasibility of these ZVT BDCs, 100-kHz and 800-W prototypes are built, and the experimental results of two working modes (Boost and Buck) are shown. Through detailed theoretical analysis and experimental verification, all switches of the converter realize soft switching, and no current notch exists at the low-voltage port. Compared with the traditional BDC, the maximum efficiency can be increased by 1.2%.

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