

## Article

# Design for a Four-Stage DC/DC High-Voltage Converter with High Precision and a Small Ripple

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**Abstract:** This paper presents a four-stage DC/DC converter with high precision and a small ripple utilized in an electronic power conditioner (EPC). The galvanically isolated four-stage topology contains four cascade connections: a buck circuit, a push–pull circuit, a power converter, and a voltage regulator. The push–pull switches, as well as the diodes in the output-side rectifier, operate in zero-voltage switching (ZVS) and zero-current switching (ZCS) modes at both switch off and switch on, which helps increase the efficiency. The maximum efficiency of the converter can reach 94.5%. The buck circuit and voltage regulator operate in a two-stage closed-loop condition and, thus, the precision is greater than 0.02%. Due to the voltage regulator, the ripple is less than 1 V when the output voltage reaches 7000 V.

**Keywords:** four-stage DC/DC; high-precision; small ripple

## 1. Introduction

Space traveling wave tubes amplifiers (STWTAs) [1], as the most important components of satellite systems, are mainly used to amplify the power of microwave signals [2]. An STWTA consists of a traveling wave tube (TWT) [3] and an electronic power conditioner (EPC) [4]. The TWT is a microwave vacuum electronic device [5]. The microwave signal can be amplified via energy exchange between electron injection and electromagnetic waves [6]. The main function of the EPC is to generate the high voltage required by the TWT via high-frequency and high-voltage power conversion technology [2,4,7].

The key performance indicators of the TWT, such as the phase shift, third-order intermodulation, and saturation gain, are directly affected by the voltage of the helix [1,8]. To ensure the working states and performance indicators of the STWTA, the high-voltage precision of the helix provided by the EPC should be greater than 0.05% [9]. Therefore, the high precision of high-voltage conversion becomes an important indicator of the EPC [10]. As the power supply of satellites come from solar energy conversion, whose efficiency is only approximately 28%, and the STWTA consumes 70% to 90% of DC energy, high efficiency also becomes a requirement of the EPC [2,5,11].

In recent years, EPC's main research has focused on topology studies, which is categorized into single-stage power conversion and multi-stage power conversion [12,13]. The single-stage converters include buck, boost non-isolated topologies, and forward, flyback, push–pull, half-bridge, full-bridge, and other topologies. The multi-stage converter consists of two or more of these topologies. The topology described in [14] is a boost-based, non-isolated transformation topology. Compared with non-isolated topology, the advantages of an isolated topology are as follows: isolation protects the system from high voltages and currents caused by line surges or ground loops. The ground potentials in parts of a satellite are not equal, so ground currents are generated between systems. Without isolation, this current can introduce noise into the system, reduce measurement accuracy, and even destroy system components. The authors of [15] describe the difference between buck and



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boost topologies in many aspects. For example, to achieve the same ripple of inductor current, the boost topology needs more inductance than the buck, but the rms current through the inductor is much less than that of the buck, with the buck topology requiring a large and expensive capacitor to smooth the discontinuous input current. The buck and boost topologies are shown in Figure 1, and if a short-circuit fault occurs in the power switch (the red one) of the buck circuit, it does not affect the power supply; however, if the same fault happens in the boost circuit, the power supply will be short-circuited. In addition, the comparison of isolated topology characteristics is shown in Table 1.

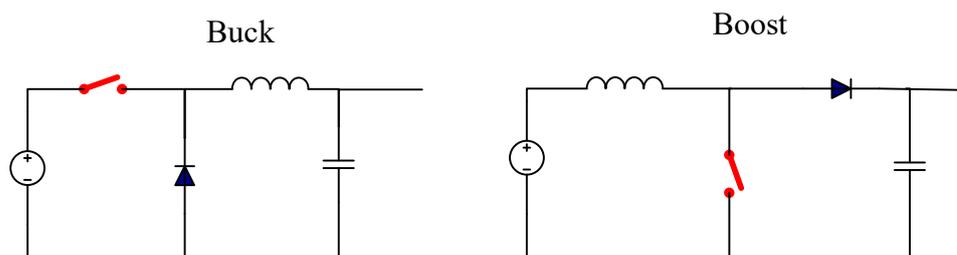


Figure 1. Buck and boost topologies.

Table 1. Comparison of isolated topology characteristics.

	Forward	Flyback	Push–Pull	Half-Bridge	Full-Bridge
Voltage stress	$2 V_{in}$	$2 V_{in}$	$2 V_{in}$	$V_{in}$	$V_{in}$
Current stress	$I_{in}$	$I_{in}$	$I_{in}$	$2 I_{in}$	$I_{in}$
Number of switches	1	1	2	2	4

To date, the major STWTA manufacturers in the world include the Tesat company in Germany [16–18], Thales company in France [19–21], and L-3 company [22,23] in the United States. The high-voltage precision of the EPC developed by L-3 is the best, reaching 0.03%. The ripple of the high voltage is approximately 1 V. The EPC developed by the Tesat company has a high efficiency that reaches 92.8%. Furthermore, in [24], an inductor-inductor-capacitor (LLC) resonant topology is proposed, with maximum efficiencies of 93.4% achieved at the output power of 5000 W, although the precision and the ripple of output voltage are not revealed. The authors of [25] describe the development of an 18 kV, 30 kW power supply for a pulsed current load whose output ripple is less than 0.01%, with the disadvantage of this design being the efficiency did not reach 90%.

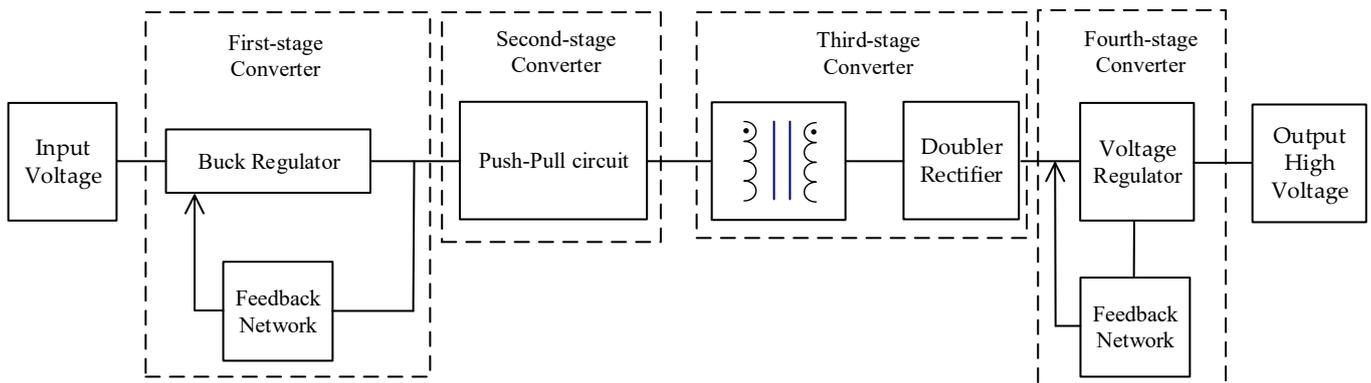
Motivated by the above analysis, the high precision, small ripple of the output high voltage and the high conversion efficiency are difficult to be realized at the same time. Thus, an isolated four-stage DC/DC high-voltage converter is presented in this paper. This four-stage DC/DC converter topology enjoys the following advantages:

1. The output high voltage can be controlled with a high accuracy of greater than 0.02%;
2. The ripple of the output high voltage is less than 1 V at voltages reaching 7000 V;
3. The efficiency of the converter can reach up to 94.5%.

The block diagram of this topology is shown in Figure 2.

As shown in Figure 2, the four-stage DC/DC high-voltage converter consists of a buck circuit, a push–pull circuit, a power converter, and a voltage regulator. The bus voltage in the satellite is transformed into a high voltage for the TWT through this four-stage converter.

The content of this paper starts with Section 2, which introduces the principle and the calculation of key parameters. Section 3 presents the experimental results of laboratory prototype. Section 4 describes the advantages and disadvantages of this topology, and the areas for improvement. Finally, conclusions are drawn in Section 5.

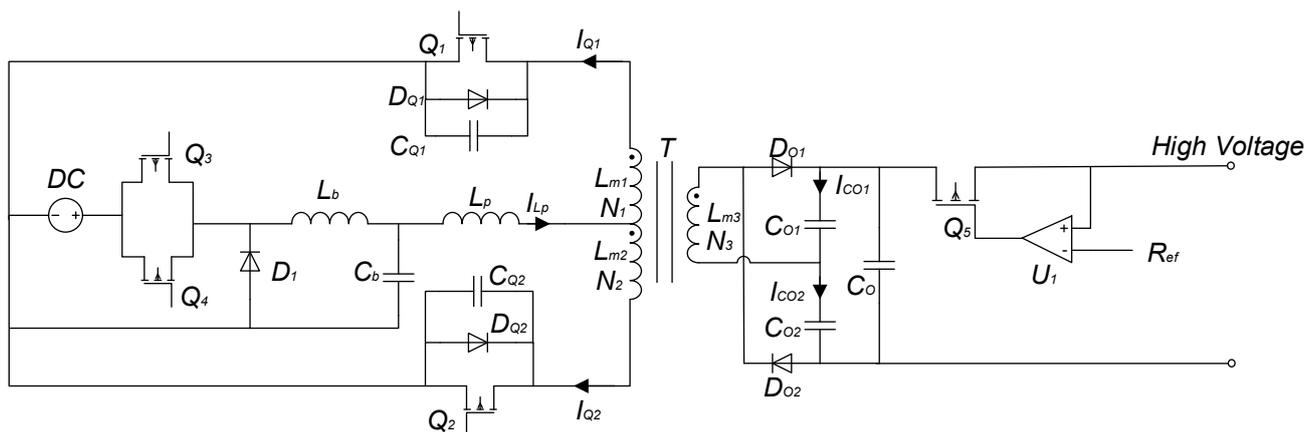


**Figure 2.** Block diagram of the four-stage DC/DC high-voltage converter.

## 2. Principle Introduction and Calculation of Key Parameters

### 2.1. Principle Introduction

A four-stage DC/DC high-voltage converter is proposed in this paper, with the topology of the schematic circuit depicted in Figure 3.



**Figure 3.** Topology of the four-stage DC/DC high-voltage converter.

In Figure 3,  $Q_3$ ,  $Q_4$ ,  $D_1$ ,  $L_b$ , and  $C_b$  form the first stage of transformation, an interleaved dual-driver buck circuit, where  $Q_3$  and  $Q_4$  are interleaved switches,  $D_1$  is the fly-wheel diode, and  $L_b$  and  $C_b$  are the inductance and capacitance, respectively, of the buck circuit. The switches  $Q_1$  and  $Q_2$  form the second stage of transformation: a push-pull circuit, where  $D_{Q1}$  and  $D_{Q2}$  are the body diodes of  $Q_1$  and  $Q_2$ , respectively, and  $C_{Q1}$  and  $C_{Q2}$  are the parasitic output capacitance. The power transformer  $T$  and the doubler rectifier circuit form the third stage of conversion, where  $L_p$  is the equivalent primary leakage inductance,  $D_{O1}$ ,  $D_{O2}$ ,  $C_{O1}$ , and  $C_{O2}$  are the voltage-doubling rectifier diodes and capacitances, and  $C_o$  is the filter capacitor. Switch  $Q_5$  and high-precision operational amplifier  $U_1$  form the fourth stage of transformation, i.e., a low-dropout regulator (LDO).

When  $Q_1$  and  $Q_2$  are both turned off, the equivalent circuit diagram is shown in Figure 4. On the primary side, part of the energy in  $L_b$  charges the capacitor  $C_b$ , while the other part flows through  $L_p$ ,  $L_m$ ,  $C_{Q1}$ ,  $C_{Q2}$ , and  $D_1$  sequentially, and then returns to  $L_b$ . On the secondary side, the current flows through  $Q_5$ ,  $R_o$ ,  $C_{O1}$ , and  $C_{O2}$  to form a loop. There is no energy exchange between the primary side and the secondary side. In Figure 4, the green, blue, and purple arrows indicate the direction of current flow on the primary side, the red arrows indicate the direction of current flow on the secondary side.

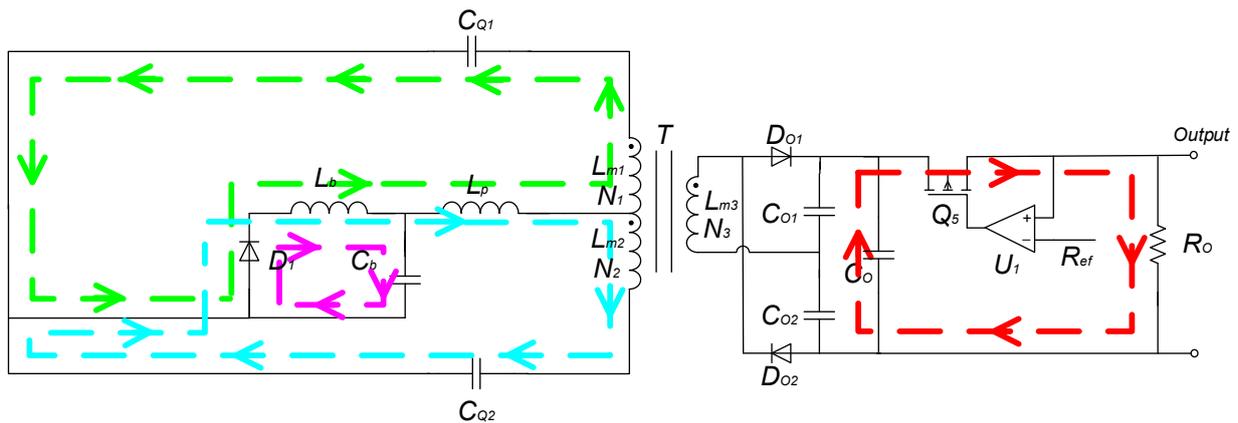


Figure 4. The equivalent circuit diagram when  $Q_1$  and  $Q_2$  are both turned off.

Since there is no energy exchange between the primary side and the secondary side, the voltage across  $C_b$  can be considered constant, with the equivalent circuit of Figure 4 depicted in Figure 5.

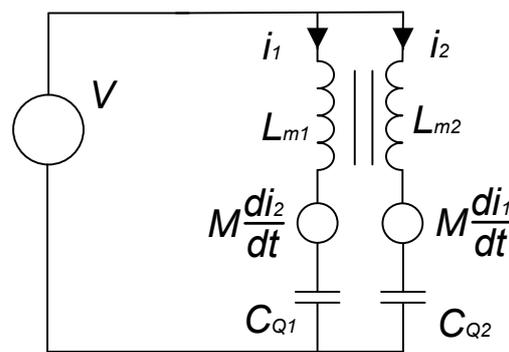


Figure 5. Approximated equivalent circuit of Figure 4.

Therefore:

$$\begin{cases} V - L_{m1} \frac{di_1}{dt} + M \frac{di_2}{dt} - \frac{1}{C_{Q1}} \int i_1 dt = 0 \\ V - L_{m2} \frac{di_2}{dt} - M \frac{di_1}{dt} - \frac{1}{C_{Q2}} \int i_2 dt = 0 \end{cases} \quad (1)$$

As  $L_{m1} = L_{m2} = L_m$  and  $C_{Q1} = C_{Q2} = C_Q$ , then, neglecting the effect of the leakage inductance, it is  $M = L_m$ , so that yields:

$$i_1 = -i_2 \quad (2)$$

Combining (1) and (2):

$$V - 2L_m \frac{di_1}{dt} - \frac{1}{C_Q} \int i_1 dt = 0 \quad (3)$$

The solution of (3) is:

$$i_1 t = \frac{I_m}{\sqrt{2} \cos \psi} \cos(\omega t + \psi) \omega = \frac{1}{\sqrt{2} L_m C_Q} I_m = \frac{1}{2} \frac{V}{L_m} T_{ON} \quad (4)$$

When  $Q_1$  is turned on, energy transfers from the primary side to the secondary side, with the equivalent circuit diagram shown in Figure 6. In Figure 6, the green and blue arrows indicate the direction of current flow on the primary side, the red arrows indicate the direction of current flow on the secondary side.

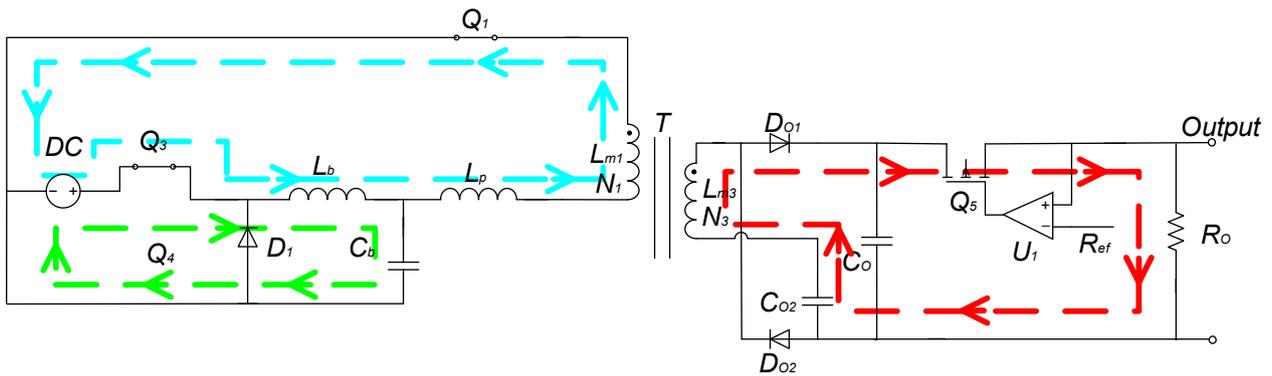


Figure 6. The equivalent circuit diagram when  $Q_1$  is turned on.

According to KCL,

$$I_{Lb} = I_{Cb} + I_{Lp} \tag{5}$$

Hence,

$$\frac{I_{Lb}}{C_b} = \frac{I_{Lp}}{C_b} + L_p \frac{d^2 I_{Lp}}{dt^2} \tag{6}$$

whose solution is:

$$I_{Lp}t = I_{Lb} - I_{Lb0} \cos(\omega t + \varphi) \tag{7}$$

$$\omega = \frac{1}{\sqrt{L_p C_b}}$$

The equivalent circuit diagram when  $Q_2$  is turned on is depicted in Figure 7. In Figure 7, the green and blue arrows indicate the direction of current flow on the primary side, the red arrows indicate the direction of current flow on the secondary side.

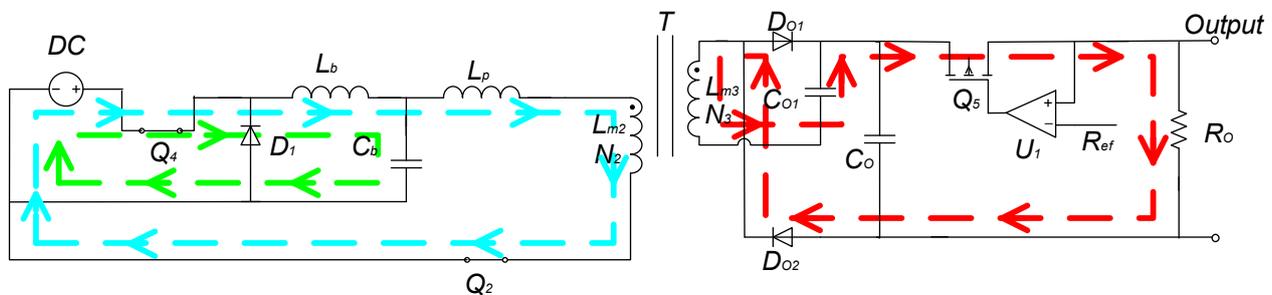


Figure 7. The equivalent circuit diagram when  $Q_2$  is turned on.

When the transformation enters the steady state, the ratio of input and output voltage is:

$$V_o = \frac{4DV_{in}N_s}{N_p} - V_{Q5\_DS} \tag{8}$$

where

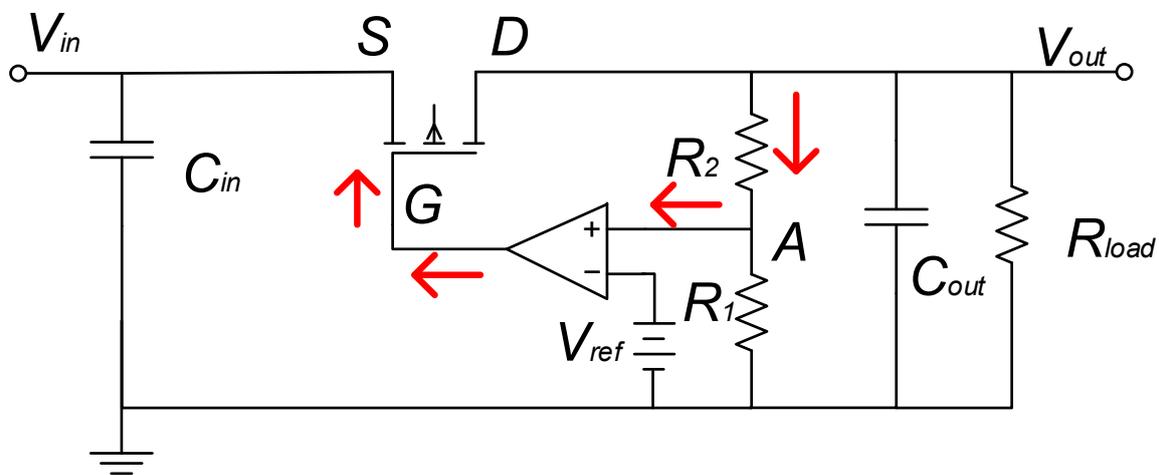
- $D$  is the duty cycle of interleaved switches;
- $N_s$  is the number of turns on the secondary side of the transformer;
- $N_p$  is the number of turns on the primary side of the transformer;
- $V_{Q5\_DS}$  is the pressure drop setting value of the MOSFET in the LDO module.

In the high-voltage conversion process, the loss of the switch tubes accounts for a large part. To achieve high efficiency, the switch tubes of the second-stage converter (push-pull circuit), which are connected to the third-stage converter (main power converter), should implement a soft switching process, namely, zero-voltage switching (ZVS) and zero-current

switching (ZCS), at both switch off and switch on, and the rectifier diode in the voltage-doubling rectifier circuit should achieve ZCS to reduce the loss in the switching process.

In this design, the buck circuit and push–pull circuit use the components themselves to generate resonances to achieve soft switching without the need for additional resonant components. The capacitance in the buck circuit  $C_b$  and the leakage inductance of the main power transformer  $L_p$  are fully utilized to form a resonant cavity.

After the first three levels of transformation, the output voltage is actually a high DC voltage with an AC component, and the peak value of the AC component is approximately 10 V. The existence of this AC component will seriously affect the phase shift, third-order intermodulation, saturation gain, and other performance indicators of the TWT, so this high voltage cannot be directly used to power the TWT. The LDO module is used to reduce the AC component so that the high voltage becomes a purer DC voltage. The principle of the fourth-stage converter LDO is shown in Figure 8. In Figure 8, red arrows indicate feedback paths of LDO.



**Figure 8.** Principle of the fourth-stage converter LDO.

When  $V_{out}$  drops due to load changes or other reasons, the voltage across the series divider resistor  $R_2$  will also drop, and then the voltage at point A drops. The voltage at point A is compared with  $V_{ref}$ , and the error amplifier will reduce the output so that the voltage at G decreases, the voltage  $V_s$  does not change, and the voltage difference  $|V_{gs}|$  then increases. The output current  $I_{out}$  increases, and this increase will make  $V_{out}$  rise, completing feedback control so that  $V_{out}$  returns to the normal voltage. By selecting and screening high-precision resistors to precisely control the divider ratio of two series resistors  $R_1$  and  $R_2$ , the output voltage can be accurately controlled. In this design, the  $V_{ref}$  is fixed, but if it changes, the divider ratio of  $R_1$  and  $R_2$  can be adjusted to change the noninverting input of the operational amplifier to keep the output of the operational amplifier constant, while the MOS tube operates in the linear region to ensure that the output voltage does not change.

## 2.2. Calculation of Key Parameters

According to the actual conditions in EPC applications, the input voltage  $V_{in} = 30$  V DC, the output voltage  $V_o = 7000$  V DC, the load power  $P_o = 130$  W, and the switching frequency  $f = 100$  kHz. The calculation of key parameters is as follows.

A resonant cavity is formed between  $C_b$  and  $L_p$ , and the resonant frequency is the switching frequency.

$$f = \frac{1}{2\pi\sqrt{L_p C_b}} = 100 \text{ kHz} \quad (9)$$

Depending on how the transformer is wound,  $L_p$  may differ, and adjusting  $C_b$  can achieve the switching frequency requirements. The lamination winding method is adopted for the main power transformer in this case, and the test result of the leakage inductance  $L_p$  is 0.6  $\mu\text{H}$ .

Therefore, the buck capacitance can be calculated as:

$$C_b = \frac{1}{f^2} \frac{1}{4\pi^2 L_p} = 4.2 \mu\text{F} \quad (10)$$

The inductance of the buck circuit can be calculated as:

$$L_b = \frac{V_b(1-D)}{K_{ind} I_b f} = 78.6 \mu\text{F} \quad (11)$$

where  $V_b$  is the output voltage of the buck circuit, with  $V_b = 22 \text{ V}$ ;  
 $D$  is the duty cycle of interleaved switches;

$$D = \frac{1}{2} \frac{V_b}{V_{in}} = 36.67\% \quad (12)$$

$K_{ind}$  is the ripple current rate, with  $K_{ind} = 0.3$  generally; and  $I_b$  is the root mean square (RMS) current of the buck output,

$$I_b = \frac{P_o}{V_b} = 5.91 \text{ A} \quad (13)$$

The number of turns on the primary side of the transformer can be calculated as:

$$N_p = \frac{V_{in}}{K_f f B_w A_e} \quad (14)$$

where

$K_f$  is the waveform factor of the square wave, with  $K_f = 4.0$ ;

$f$  is the switching frequency, with  $f = 100 \text{ kHz}$ ;

$B_w$  is the magnetic flux density, in which the TPW33-UYF36 series is adopted as the type of magnetic core, with  $B_w = 150 \text{ mT}$ ;

and  $A_e$  is the effective cross-sectional areas of the core, with  $A_e = 130.98 \text{ mm}^2$ .

Therefore,  $N_p = 4.16$  and an integer value is taken, that is,  $N_1 = N_2 = 5$ .

The number of turns on the secondary side of the transformer is:

$$N_s = \frac{N_p V_o}{V_{in}} = 583.4 \quad (15)$$

Taking an integer value,  $N_3 = 584$ .

### 3. Experimental Validation

According to the above principle and the parameter calculation, a prototype of a four-stage converter is fabricated. The input voltage  $V_{in} = 30 \text{ V DC}$ , the output voltage  $V_o = 7000 \text{ V DC}$ , the load power  $P_o = 130 \text{ W}$ , and the switching frequency  $f = 100 \text{ kHz}$ .

A laboratory prototype of the four-stage converter was fabricated, as shown in Figure 9. There are four power switches in the converter, with two switches used as interleaved dual-driver in the buck circuit and the other two switches used in the push-pull circuit. The main uses of Schmitt triggers are waveform shaping, transformation, comparison, etc. All of the control signals are processed in CPLD.

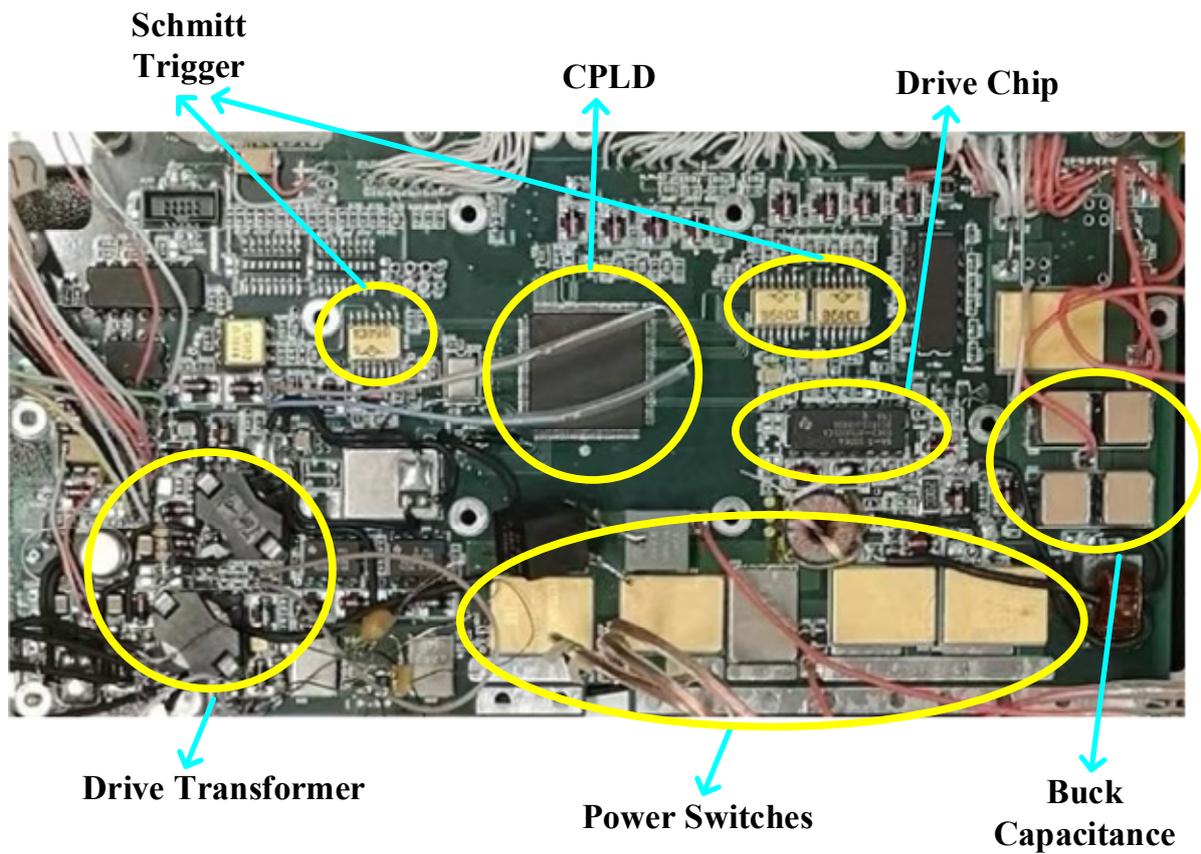


Figure 9. Experimental converter in the laboratory.

The voltage and current waveforms of the second-stage push–pull switches of the prototype are presented in Figure 10.

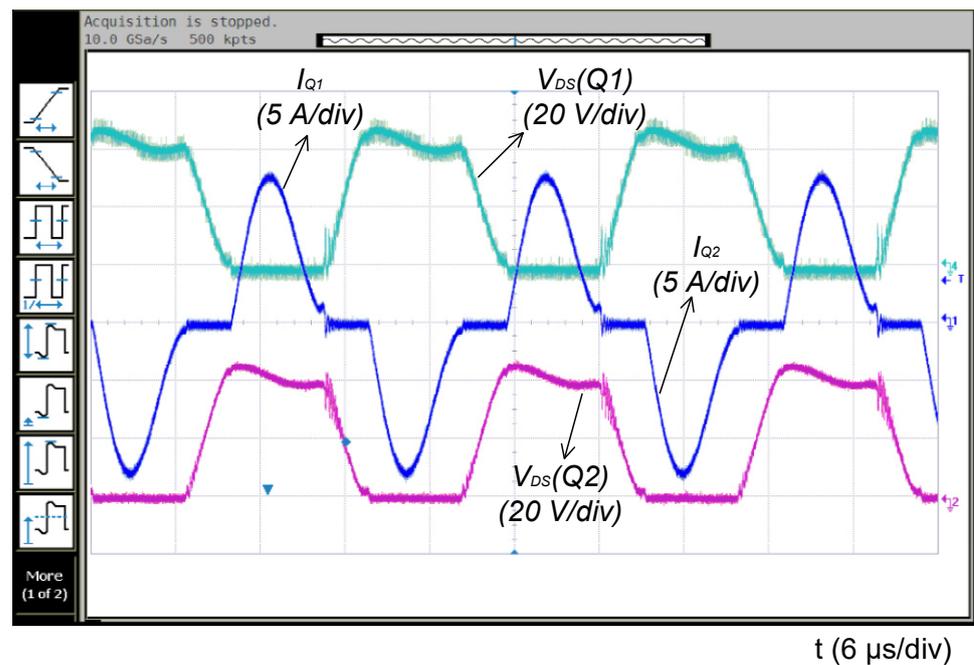


Figure 10. Voltage and current waveforms of the push–pull switches.

Figure 10 shows that the voltage waveform at the DS terminal of the push–pull switches  $Q_1$  and  $Q_2$  is approximately a trapezoidal wave, and the current waveform flowing through the switches is close to a sine wave, without obvious voltage spikes or current overshoots. ZCS and ZVS can be realized at both turning on and off. The voltage stress of the switches in the push–pull circuit is:

$$V_{p-p} = 2V_b = 46 \text{ V} \quad (16)$$

The peak current of the switches is:

$$I_{p-p} = \frac{P_o}{V_b} + \frac{P_o}{V_b} \cos^{-1} \cot \frac{(T_{off} - T_{on})^2 f^2 \pi}{2} = 12.6 \text{ A} \quad (17)$$

where  $f$  is the operating frequency of dual interleaved drivers,  $T_{off}$  is the off time of the switches, and  $T_{on}$  is the on time of the switches.

After the first three stages of conversion, the voltage flows into the fourth-stage converter LDO, as shown in Figure 11 ( $V_{MOS-D}$ ), and the ripple is approximately 10 V. With a 1000:1 high-voltage probe of oscilloscope (which the maximum measurement voltage can reach 15 kV), the test value of the output high voltage after passing through the LDO module obtained by an oscilloscope is also shown in Figure 11 ( $V_o$ ). According to the test result of  $V_o$  (inside the red dashed box), the output high voltage is 7000.4 V DC.

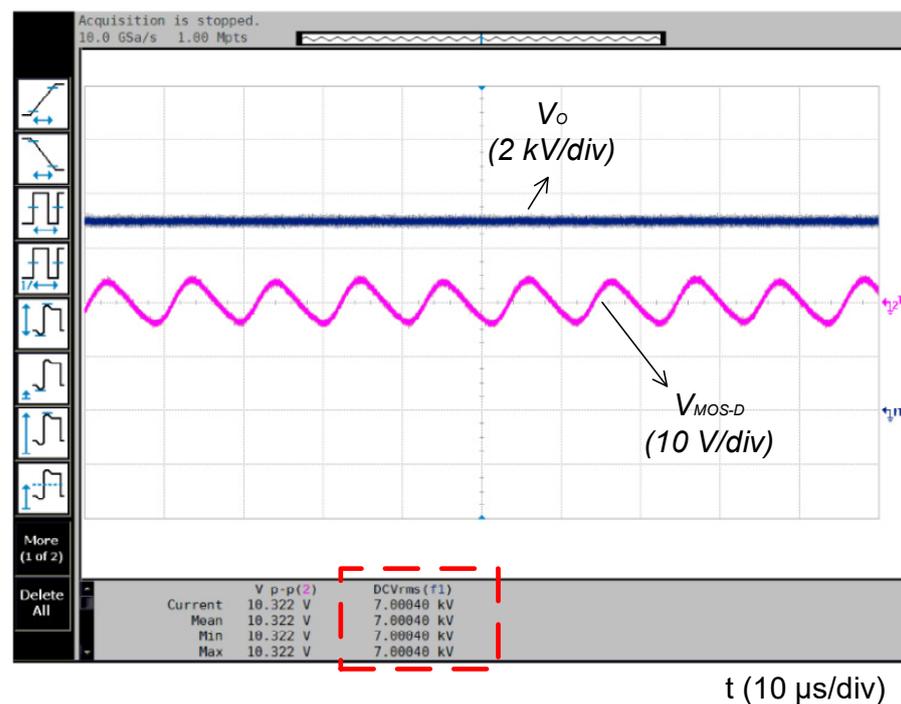


Figure 11. LDO input voltage ripple ( $V_{MOS-D}$ ) and test value of the output high voltage ( $V_o$ ).

The test value of the output high voltage obtained by a digital multimeter is shown in Figure 12. The digital multimeter performs measurements with a 1000:1 probe, so the test value is 7.00011 V DC.

The test values of both the oscilloscope and digital multimeter are 7000 V, indicating that the output voltage accuracy of this four-stage DC/DC converter is greater than 0.02%.

When the output high voltage is 7000 V, the high-voltage ripple is approximately 0.8 V, as shown in Figure 13, indicating that the voltage ripple is greatly reduced after the fourth-stage LDO conversion, with the ripple less than 1 V.

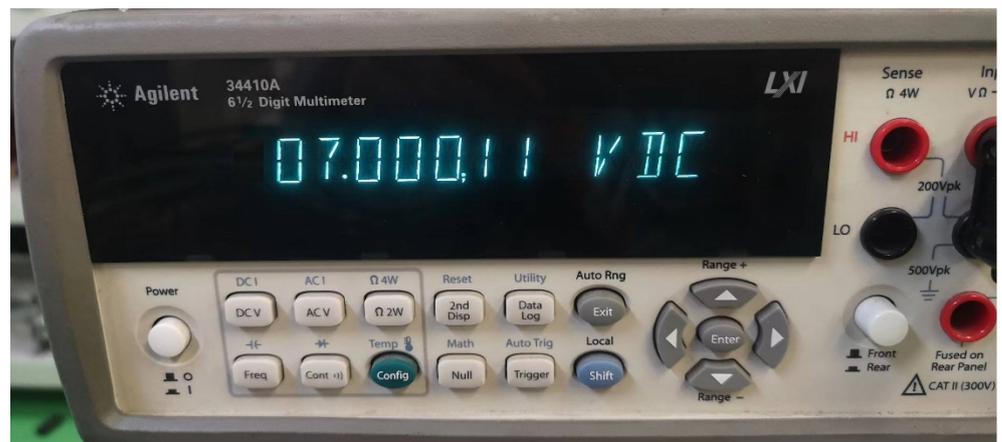


Figure 12. Test value of the output high voltage obtained by a digital multimeter.

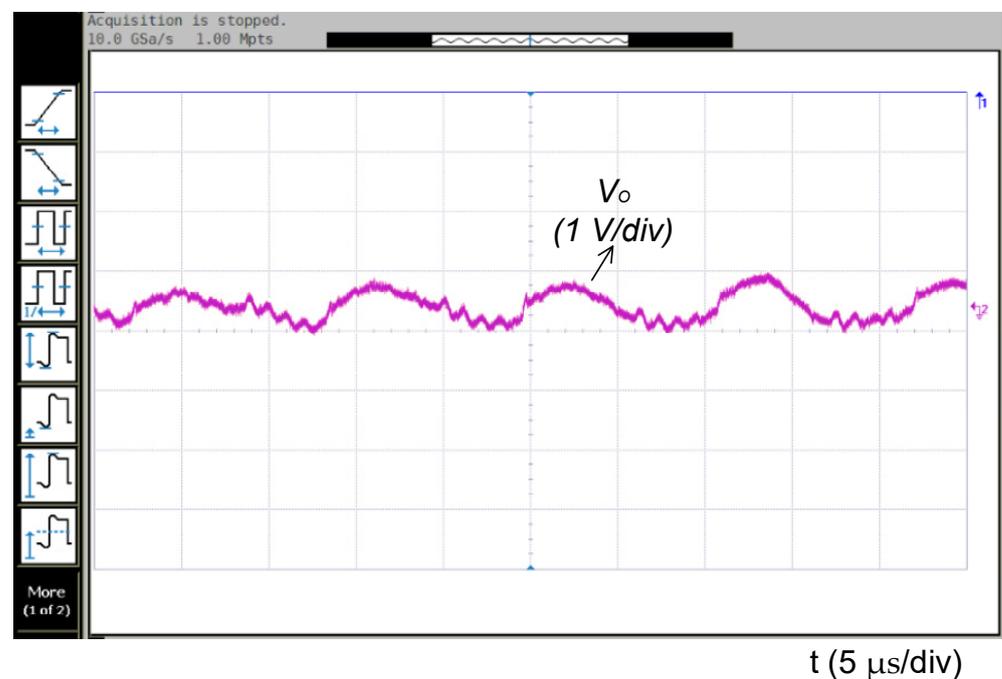


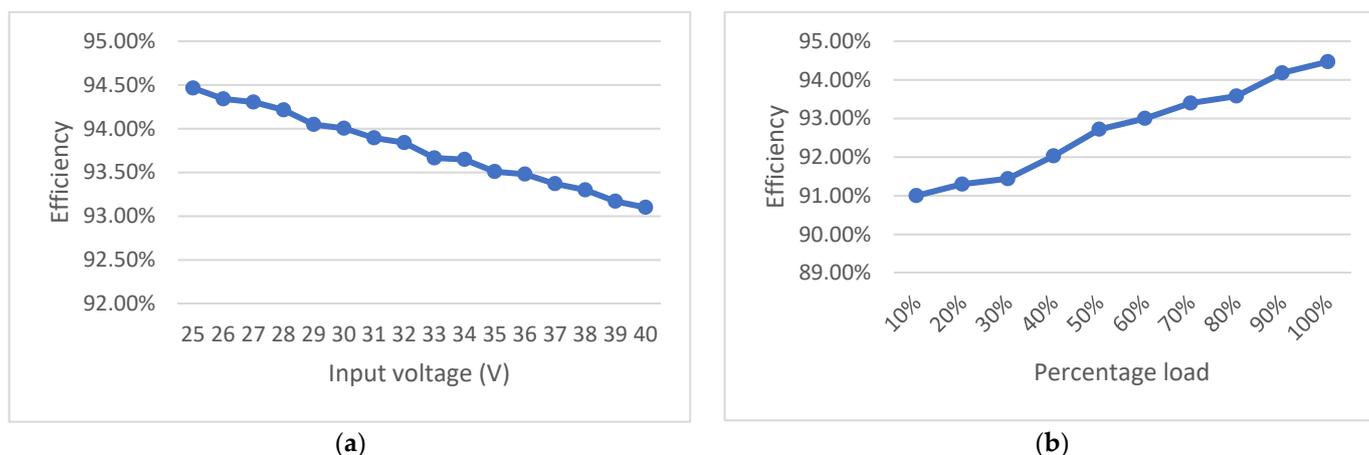
Figure 13. Ripple of the output high voltage.

Since the LDO module, the output high voltage does not change while the input voltage differs, with the efficiency calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \frac{7000 \times I_{out}}{V_{in} \times I_{in}} \quad (18)$$

where  $V_{in}$  and  $I_{in}$  can be read from the DC input power supply and  $I_{out}$  is measured by stringing into a multimeter.

Figure 14 shows the efficiency test of this four-stage converter. In Figure 14a, with a full load, the efficiency is tested at different bus input voltages, which indicates that the lower the bus input voltage is, the higher the potential efficiency. The bus voltage on a satellite is usually 25~40 V DC, and the efficiency of this four-stage converter can reach 94.5%. In addition, Figure 14b shows the efficiency results for different loads when the input voltage is 25 V, with the graph suggesting that the heavier the load, the higher the efficiency.



**Figure 14.** Efficiency test of the converter. (a) Efficiency test for different bus input voltages. (b) Efficiency test for different loads.

#### 4. Discussion

The four-stage DC/DC high-voltage converter is composed of a buck circuit, a push-pull circuit, a power converter, and an LDO regulator, with the first three stages of conversion being typical switching power conversion, which is characterized by high efficiency. However, the working principle of the LDO is to apply an excess voltage that is higher than the set value to the switch to form a DS voltage drop and to simultaneously make the switch work in the linear region to achieve the voltage regulation function; thus, the loss of the switch will increase and the efficiency will be relatively low. In subsequent work, an approach for improving the conversion efficiency of the LDO will be studied to further improve the efficiency of the EPC. Additionally, the switches of the first-stage converter operate in hard-switching mode, and a method for higher efficiency of the buck circuit will be researched.

#### 5. Conclusions

This paper investigated the research status of EPC and showed that it is difficult to meet high accuracy, small ripple, and high efficiency at the same time. Therefore, in order to achieve high accuracy, small ripple, and high efficiency, a four-stage DC/DC high-voltage converter topology is proposed in this paper, with the advantages of the converter verified through the experimental results of a prototype, which proves that this converter topology has the following characteristics:

1. The output high voltage can be controlled with a high accuracy of greater than 0.02%;
2. The ripple of the output high voltage is small, less than 1 V at voltages up to 7000 V;
3. The power switches in the push-pull circuit can realize ZVS and ZCS at both turning on and off, with the efficiency of the converter reaching 94.5%.

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