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A Single-Phase Transformerless Nine-Level Inverter and Its Control Strategy

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Abstract: To reduce the device number per unit level of the existing nine-level inverters, a topology of single-phase transformerless nine-level inverter was proposed. The proposed topology consists of only 10 switching devices and 4 capacitors. Firstly, the working principle of the proposed topology was analyzed in detail, and the comparison with conventional nine-level topologies in terms of device switching loss and conduction loss was presented. Then, combined with one-dimensional space vector modulation, a floating capacitor voltage estimation method was presented by the analysis of the operation mode before the arrival of redundant switching state. On this basis, a floating capacitor voltage sensorless control scheme was proposed, to achieve the balance of the floating capacitor voltages. Finally, simulations and experiments verified the effectiveness and correctness of the proposed topology and floating capacitor voltage sensorless control method.

Keywords: nine-level inverter; one-dimensional space vector modulation; floating capacitor voltage estimation; voltage balancing control

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1. Introduction

In recent years, high-order multi-level inverters have attracted the attention of many scholars in low-voltage applications such as new energy power generation, microgrids, and motor drives, due to their advantages of high output power quality, low current harmonics, and low voltage stress of switching devices [1–5]. At present, multi-level inverter circuits mainly include neutral-point-clamped (NPC), flying capacitors (FC), cascaded H-bridge (CHB), stacked multicell converter (SMC) and other topologies. A nine-level active NPC (ANPC) inverter topology is proposed to expand the inverter capacity while reducing the filter size by interleaving and paralleling two five-level ANPC inverters [6]. However, this topology requires 24 switching devices, and the circuit hardware cost is high. A new approach is developed in [7], which connects four flying capacitor H-bridges in series with one two-level half bridge, effectively reducing the number of switching devices in the nine-level topology to 18, but the flying capacitor voltage control of this topology is relatively complex. The nine-level inverter topology presented in [8] uses a switched capacitor circuit combined with an H-bridge. This circuit only needs one voltage source, and fewer switching devices. Although the voltage stress of switching devices is relatively small, the energy of this circuit can only be transmitted in one direction. The stacked multi-unit multi-level circuit is proposed in [9,10], which not only reduces the energy storage of the inverter, but also improves the voltage withstand capability of the circuit. The above-mentioned multi-level topology is not suitable for low-voltage application, due to the large number of devices and complex control. In order to solve the above problems, four nine-level topologies suitable for low-voltage application are proposed in the literature [11–13].

However, these topologies require more DC power sources in practical applications, which greatly increases the system cost.

The unbalance of floating capacitor voltages has always been one of the key problems to be solved in high-order multilevel inverters. Thus, several floating capacitor voltage balance control methods have been proposed. A capacitance voltage estimation method is proposed in [14]. By connecting a voltage sensor between two capacitor anodes and analyzing the current flow path, only half of the voltage sensors can estimate the overall capacitance voltage. The SVPWM modulation strategy is adopted in [15,16], and the balance between the dc-link capacitor voltages and the floating capacitor voltages is achieved by reasonably selecting the redundant vector. However, due to the large number of voltage vectors, the calculation is very complicated. Compared with the SVPWM method, the SPWM is simple and has been widely used in high-order multi-level topologies. A simple logic-form equation based PWM is designed in [17], which can make the floating capacitors voltage around its reference value. An inverter capacitor voltage balancing method based on optimal zero sequence voltage injection is proposed in [18]. This method is realized by hybrid carrier pulse width modulation, which can balance and adjust the voltage of DC link capacitor and floating capacitors in the topology. A new carrier-based modulation scheme was adopted in [19], which solves the problem of floating capacitors voltage balance by clamping the modulation reference safely to the pole voltage level conducive to floating capacitors voltage balance. A SPWM-based floating capacitor voltage control method is proposed in [20], which achieves the balance of the floating capacitor voltage by reasonably selecting redundant switch states during phase switching. By adjusting the duty cycle, the dwell time of the redundant switch state is changed, and then the floating capacitor voltages are controlled to be balanced [21]. A one-dimensional space vector modulation method is proposed in [22], which can achieve the voltage balance of the floating capacitors while reducing the switching loss and the control complexity. Compared with SPWM, the one-dimensional space vector can increase the control degree of freedom of the inverter, which is more conducive to the high-frequency output of the inverter.

However, the realization of the above-mentioned floating capacitor voltage balance methods requires the use of voltage sensor to obtain a voltage signal. Since the actual operating environment of the inverter is complex, humidity, vibration, noise, electromagnetic interference, etc. will affect the measurement accuracy of the sensor, and even lead to sensor failure. Therefore, how to realize sensorless control or less sensor control is the key to ensure the reliable operation of the inverter system. However, most of the existing sensorless control strategies are proposed to cancel the grid voltage or current sensors [23–25], while the floating capacitor voltage sensorless control is relatively rarely reported.

To tackle the above problems, this paper proposes a low-voltage single-phase non-isolated nine-level inverter topology with simple structure and few switching devices, and it presents a floating capacitor voltage sensorless control strategy based on one-dimensional space vector modulation. First, the working principle of the proposed nine-level inverter is analyzed in detail, and the comparison with the existing nine-level topologies is presented. Then, combined with the one-dimensional space vector modulation algorithm, a control strategy without floating capacitor voltage sensor is proposed, and the voltage balance is realized by estimating and predicting the floating capacitor voltages. Finally, simulation and experimental results have verified the validity and feasibility of the proposed topology and control algorithm.

2. The Proposed Nine-Level Inverter Topology and Its Working Principle

2.1. Topology

The proposed single-phase non-isolated nine-level inverter topology is shown in Figure 1. The circuit is mainly composed of 10 switching devices and 4 capacitors. S_2, S_3, and S_7 are composed of two switching devices, which are bidirectional blocking switches, and S_1, S_4, S_5 and S_6 are unidirectional blocking switches. Assuming that the total dc-link voltage V_{DC} is $8E$, the voltage of the dc-link capacitors C_1 and C_2 is $4E$, and the voltage of

the floating capacitors C_3 and C_4 is E. I_{DC} and I_O are the dc-link current and load current, respectively, while I_{C1}, I_{C2}, I_{C3} and I_{C4} are the currents flowing through the capacitors C_1, C_2, C_3 and C_4, respectively.

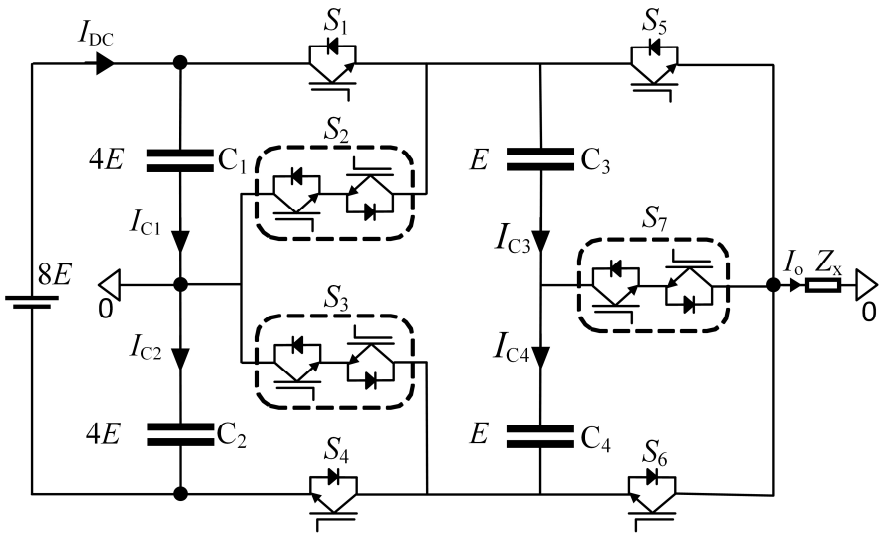


Figure 1. The topology of the proposed 9-level converter.

2.2. Working Modal Analysis

Figure 2 shows the 12 working states of the proposed topology. The solid arrows in the figure represent the reference positive direction of the current on each path, and the dashed arrows represent the actual flow direction of the current. The detailed switch status analysis is as follows:

(1) State P4 (Figure 2a): The switches S_1 and S_5 are turned on, the current flows from the positive terminal of the dc-link through the switches S_1, S_5 and the load, and then returns to the neutral point, the inverter output voltage $V_O = V_{DC}/2$. The current flowing through capacitors C_3 and C_4 is $I_{C3} = I_{C4} = 0$.

(2) State P3 (Figure 2b): The switches S_1 and S_7 are turned on, the current starts from the positive end of the dc-link and returns to the neutral point after passing through S_1, C_3, S_7 and the load, and the output voltage $V_O = 3V_{DC}/8$. The current through C_3 is I_O and the current through C_4 is 0.

(3) State P2P (Figure 2c): the switches S_1 and S_6 are turned on, the current starts from the positive terminal of the dc-link and returns to the neutral point through S_1, C_3, C_4, S_6 and the load. The output voltage $V_O = V_{DC}/4$, and the currents $I_{C3} = I_{C4} = I_O$.

(4) State P2N (Figure 2d): the switch S_3 and S_5 are turned on, the current starts from the neutral point and returns to the neutral point after passing through S_3, C_4, C_3, S_5 and the load. The output voltage $V_O = V_{DC}/4$, and the currents $I_{C3} = I_{C4} = -I_O$.

(5) State P1 (Figure 2e): the switches S_3 and S_7 are turned on, the current starts from the neutral point and returns to the neutral point after passing through S_3, C_4, S_7 and the load. The output voltage $V_O = V_{DC}/8$, while the currents $I_{C3} = 0$ and $I_{C4} = -I_O$.

(6) State OP (Figure 2f): The switches S_2 and S_5 are turned on, and the current starts from the neutral point and returns to the neutral point after passing through S_2, S_5 and the load. At this time, $V_O = 0$, $I_{C3} = I_{C4} = 0$.

(7) The state is ON (Figure 2g): the switches S_3 and S_6 are turned on, the current starts from the neutral point and then returns to the neutral point after passing through S_3, S_6 and the load, and the voltage $V_O = 0$, and the currents $I_{C3} = I_{C4} = 0$.

(8) State N1 (Figure 2h): The switches S_2 and S_7 are turned on, the current starts from the neutral point and returns to the neutral point after passing through S_2, C_3, S_7 and the load. The output voltage $V_O = -V_{DC}/8$, and the currents $I_{C3} = I_O$, $I_{C4} = 0$.

(9) State N2P (Figure 2i): The switch tubes S_2 and S_6 are turned on, the current starts from the neutral point and returns to the neutral point after passing through S_2, C_3, C_4, S_6 and the load. The voltage $V_O = -V_{DC}/4$, and the currents $I_{C3} = I_{C4} = I_O$.

(10) State N2N (Figure 2j): The switches S_4 and S_5 are turned on, and the current starts from the negative end of the dc-link and returns to the neutral point through S_4, C_4, C_3, S_5 and the load. The output voltage $V_O = -V_{DC}/4$, and the currents $I_{C3} = I_{C4} = -I_O$.

(11) State N3 (Figure 2k): the switches S_4 and S_7 are turned on, the current starts from the negative end of the dc-link and then returns to the negative end of the dc-link through S_4, C_4, S_7 and the load. The voltage $V_O = -3V_{DC}/8$, and the current $I_{C4} = -I_O$.

(12) State N4 (Figure 2l): The switches S_4 and S_6 are turned on, the current starts from the negative end of the dc-link and returns to the neutral point after passing through S_4, S_6 and the load. The voltage $V_O = -V_{DC}/2$, and the currents $I_{C3} = I_{C4} = 0$.

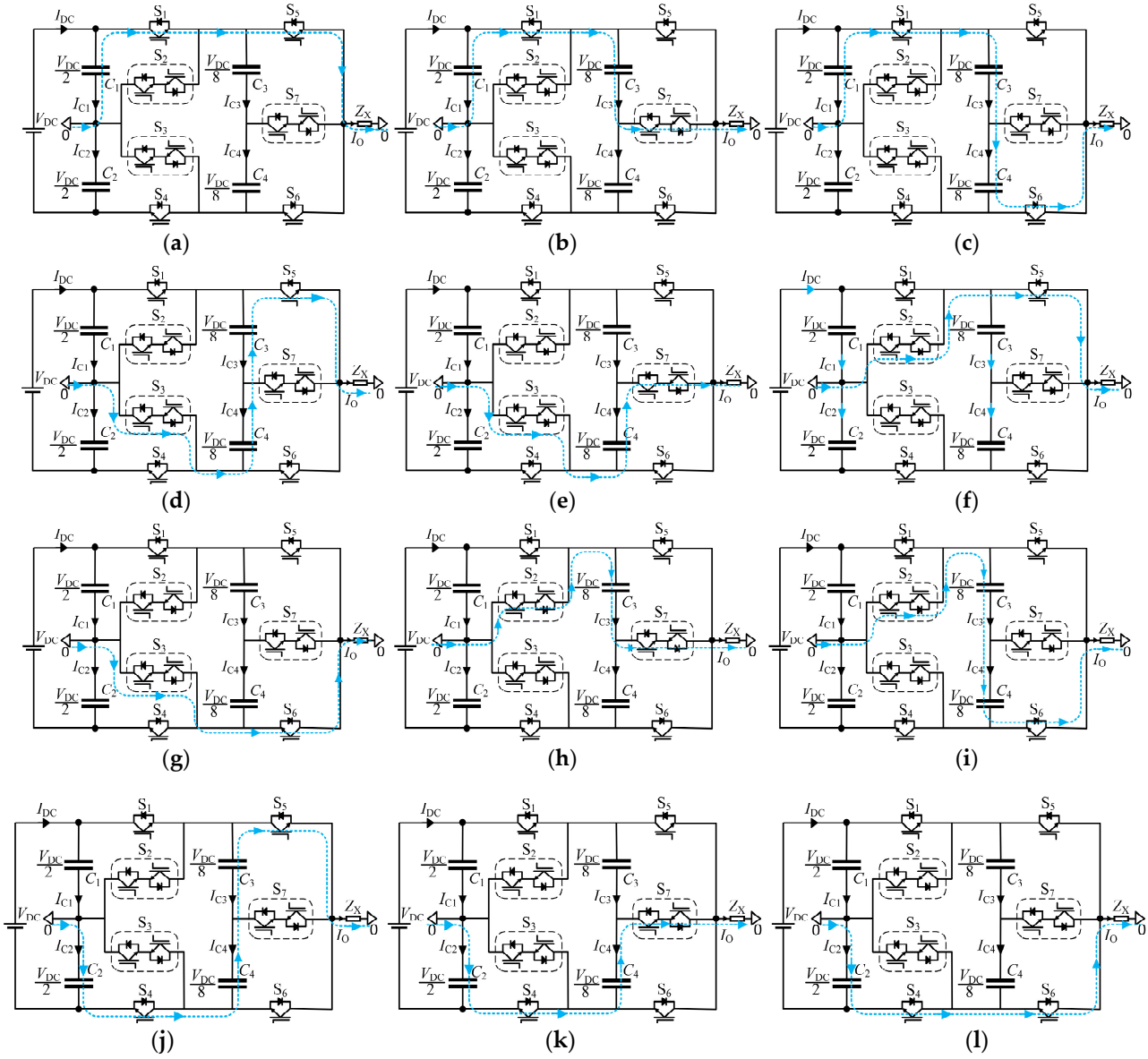


Figure 2. Operating states of the proposed 9-level topology. (**a**) $V_O = 4E$; (**b**) $V_O = 3E$; (**c**) $V_O = 2E$; (**d**) $V_O = 2E$; (**e**) $V_O = E$; (**f**) $V_O = 0$; (**g**) $V_O = 0$; (**h**) $V_O = -E$; (**i**) $V_O = -2E$; (**j**) $V_O = -2E$; (**k**) $V_O = -3E$; (**l**) $V_O = -4E$.

It can be seen from Figure 2 that the proposed nine-level topology has a total of 12 switching states, as shown in Table 1.

Table 1. Switching states of the proposed 9-level converter.

S_1–S_7	States	V_{C3}		V_{C4}		V_O
		$I_O > 0$	$I_O < 0$	$I_O > 0$	$I_O < 0$	
1000100	P4	-	-	-	-	$4E$
1000001	P3	↑	↓	-	-	$3E$
1000010	P2P	↑	↓	↑	↓	$2E$
0010100	P2N	↓	↑	↓	↑	$2E$
0010001	P1	-	-	↓	↑	E
0100100	OP	-	-	-	-	0
0010010	ON	-	-	-	-	0
0100001	N1	↑	↓	-	-	E
0100010	N2P	↑	↓	↑	↓	$-2E$
0001100	N2N	↓	↑	↓	↑	$-2E$
0001001	N3	-	-		↑	$-3E$
0001010	N4	-	-	-	-	$-4E$

Note: '↑' means capacitor charging; '↓' means capacitor discharge.

2.3. Comparison with Existing Nine-Level Inverter Topologies

In order to explain the advantages of the proposed topology more intuitively, this paper selects the traditional ANPC and SMC nine-level topology as the comparison objects. Figure 3 shows the above circuit topologies.

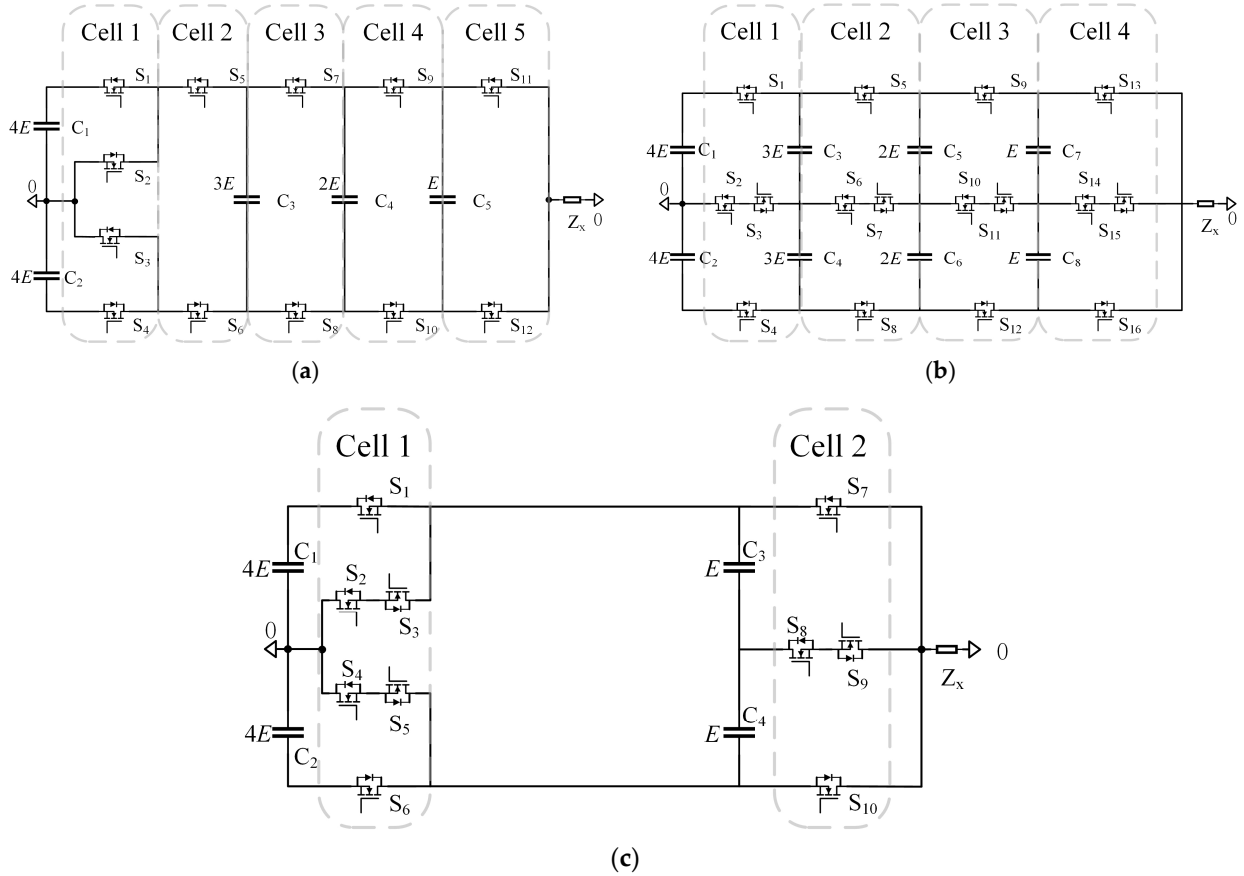


Figure 3. The topology of the three nine-level converters. (**a**) ANPC-9L; (**b**) SMC-9L; (**c**) The proposed topology.

Table 2 presents the main circuit parameter comparison between the proposed topology and two typical nine-level topologies. In terms of the number of switching devices, the number of switching devices in the proposed topology is 5/8 than that of the SMC-9L topology and 5/6 than that of the ANPC-9L topology. The proposed topology can effectively

reduce the difficulty of circuit design, reduce the system cost, and improve the reliability of the inverter. Compared with ANPC-9L, the number of floating capacitors in the proposed topology is reduced by 1, and 4 less than that of SMC-9L, and the withstand voltage is lower, which can reduce the volume of floating capacitors. In addition, the number of sensors of the proposed topology is also less than other topologies.

Table 2. Parameters comparison of the main circuit.

Parameters	ANPC-9L	SMC-9L	Proposed Topology
number of switching devices	12	16	10
switching devices withstand voltage	$4E \times 4 + E \times 8$	$E \times 16$	$4E \times 6 + E \times 4$
capacitive voltage sensing number of devices	5	8	4
number of floating capacitors	3	6	2
suspension capacitance withstand voltage	$3E \times 1 + 2E \times 1 + E \times 1$	$3E \times 2 + 2E \times 2 + E \times 2$	$E \times 2$

In order to compare the switching losses of the above three topologies, the ANPC-9L is divided into 5 units, the SMC-9L is divided into 4 units, and the proposed topology is divided into 2 units, as shown in Figure 3. It can be seen that the ANPC-9L unit 1 has the same structure as the unit 1 of the proposed topology, and the voltages of the devices are both $4E$. Therefore, under the same switching frequency, the switching losses of the devices in the two topological units 1 are the same. The devices of ANPC-9L units 2, 3, 4, and 5 and the devices in the proposed topology unit 2 are both subjected to voltage E, but the proposed topology unit 2 has only 4 switching devices, while the ANPC-9L units 2, 2, There are a total of 8 switching devices in 3, 4 and 5. Obviously, at the same switching frequency, the proposed topology has smaller switching losses.

Compared with the SMC-9L, the proposed topology unit 2 and SMC-9L unit 4 have the same structure, and the voltages of the devices are both E. Under the same switching frequency, the switching loss of the proposed topology unit 2 and SMC-9L unit 4 is the same. There are 6 switching devices in the proposed topology unit 1, the withstand voltage is $4E$, the number of switching devices in SMC-9L units 1, 2, and 3 is 12, and the device withstand voltage is E; thus, under the same switching frequency, the device switching loss of the unit 1 in proposed topology is slightly larger than that of the sum of the units 1, 2, 3 in SMC-9L.

Table 3 shows the comparison results of the total number of devices in the current path when the three nine-level topologies output different voltage levels. It can be seen that when the proposed topology outputs each level, the number of devices through which the current flows is the smallest, so the conduction loss is also the smallest. Generally, the switching frequency of a multilevel inverter is low, and the conduction loss accounts for the main part of the device loss. Therefore, the topology proposed in this paper has the lowest total device loss.

Table 3. Comparison of the total number of devices in the current path.

V_O	Total Number of Devices in the Current Path		
	ANPC-9L	SMC-9L	Proposed Topology
$4E$	5	4	2
$3E$	5	5	3
$2E$	5	6	2
E	5	7	4
0	5	8	3
$-E$	5	7	4
$-2E$	5	6	2
$-3E$	5	5	3
$-4E$	5	4	2

3. Control Strategy of Voltage Sensor without Floating Capacitance

The control objectives of the proposed nine-level inverter are: output voltage V_O, dc-link capacitor voltages V_{C1}, V_{C2}, and flying capacitor voltages V_{C3}, V_{C4}. Since the one-dimensional space vector modulation algorithm has the advantages of high degree of freedom and can control multiple targets at the same time [26,27], the one-dimensional space vector modulation algorithm is adopted in this paper. On this basis, by analyzing the circuit state before the redundant switch state arrives, the estimation method of the floating capacitor voltage is given, and then the appropriate value is selected according to the difference between the estimated value of the floating capacitor voltage and the reference value and the positive and negative current of the current. Redundant switching state, a voltage sensor control algorithm without floating capacitance is proposed.

3.1. One-Dimensional Space Vector Modulation Algorithm

Let the output voltage vector of the single-phase nine-level inverter be $\boldsymbol{V}_O$, and the reference voltage vector be the modulating wave vector $\boldsymbol{u}_r$. Figure 4 shows the one-dimensional space vector diagram of the single-phase nine-level inverter.

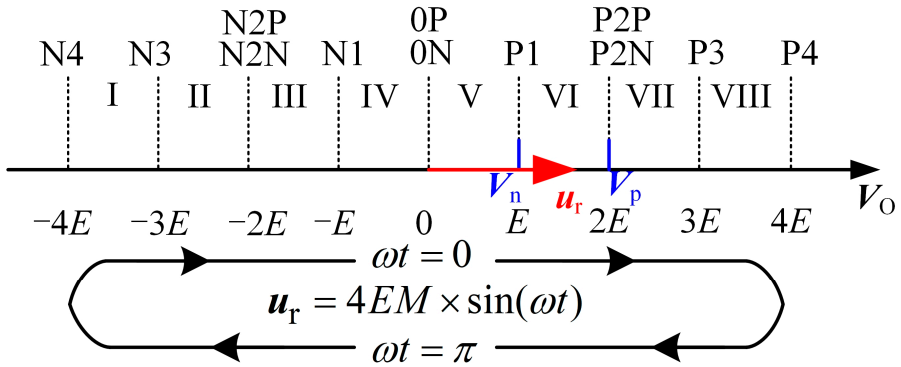


Figure 4. One-dimensional SVM of the proposed 9-level converter.

The expression of the modulation signal $\boldsymbol{u}_r$ is defined as

$$\boldsymbol{u}_r = \frac{1}{2} M V_{DC} \sin(\omega t), \tag{1}$$

where M is the modulation degree, and $0 \leq M \leq 1$. In the one-dimensional vector space, select the most recent two voltage vectors to synthesize the reference voltage $\boldsymbol{u}_r$. Let the vector with the larger modulus value be V_p, and the vector with the smaller modulus value be V_n. It can be noticed that the interval where $\boldsymbol{u}_r$ is located can be determined according to the sign and modulus value of $\boldsymbol{u}_r$. If $\boldsymbol{u}_r$ is in the interval VI, the vector $2E$ and E are used for synthesis.

According to volt-second balance principle, the dwell time of the vectors V_p and V_n satisfies Equation (2), where T_s is the switching period.

$$\begin{cases} \boldsymbol{u}_r T_s = \boldsymbol{V}_p T_p + \boldsymbol{V}_n T_n \\ T_s = T_p + T_n \end{cases}, \tag{2}$$

3.2. Control Strategy of Voltage Sensor without Floating Capacitance

From Table 1, the redundant switch states P2P, P2N, N2P and N2N can affect the floating capacitors C_3 and C_4 at the same time. Therefore, the floating capacitor voltage can be adjusted by reasonably selecting the redundant switch states corresponding to the $\pm 2E$ level. In order to cancel the floating capacitor voltage sensor, it is necessary to accurately estimate the floating capacitor voltage before outputting the $\pm 2E$ level.

Figure 5 shows the switch sequence diagram in which the output levels $2E$ and $-2E$ participate. Before the output voltage reaches the $2E$ level, there are two level states, $3E$

and E. Therefore, it is necessary to perform voltage estimation in these two states. Taking Figure 5a as an example, the floating capacitor voltage value is estimated when the $3E$ level is output, and the redundant switch state selection is performed when the $2E$ level is output. Before the output voltage reaches the $-2E$ level, there are two level states, $-3E$ and $-E$, and the voltage needs to be estimated in these two states. In Figure 5c, when the output voltage is at the $-E$ level, the floating capacitor voltage value is estimated, and the redundant switch state selection is performed when the output $-2E$ level.

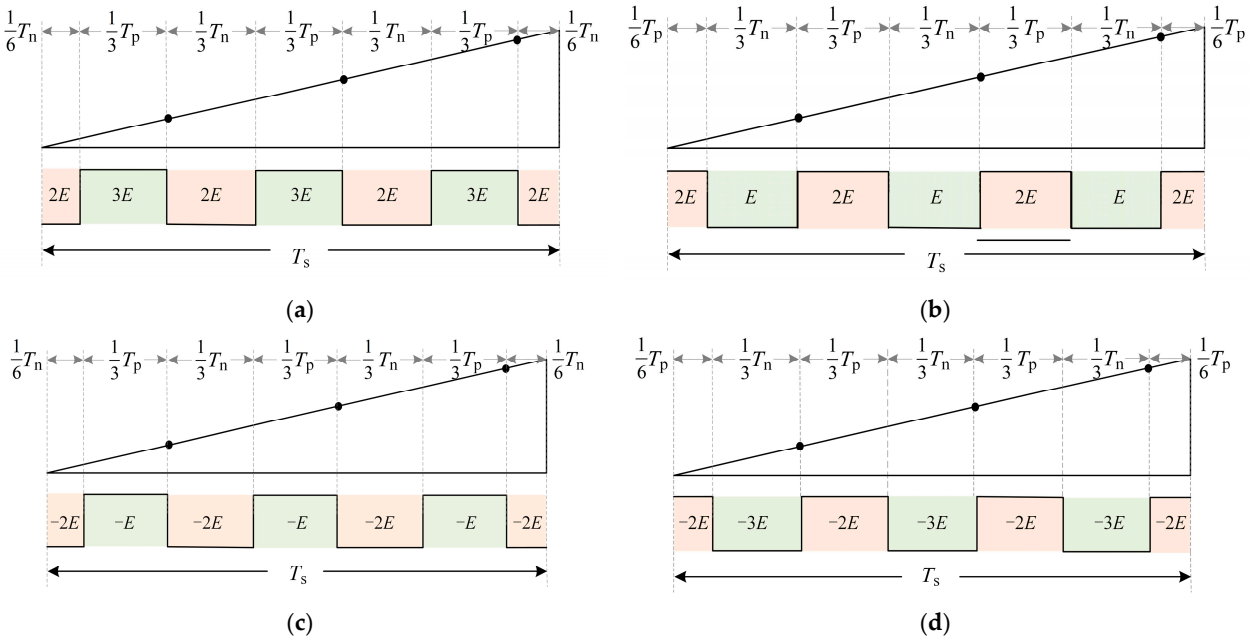


Figure 5. The switching sequences that contain the $2E$, $-2E$ voltage vector. (**a**) $N = 3$; (**b**) $N = 1$; (**c**) $N = -1$; (**d**) $N = -3$.

In order to distinguish the four level states of $3E$, E, $-E$, and $-3E$, define the inverter output voltage to round up the level N:

$$N = \text{ceil}(\frac{V_O}{E}), \tag{3}$$

where ceil(x) is the round-up function.

As can be seen from Figure 5, there are 3 sampling data reading points in one switching sequence cycle, and the values of V_{C1}, V_{C2}, V_O, and I_O can be read at the sampling points. In Figure 2b, when the level state is $3E$, the current flows through C_1, C_3 and the load and returns to the neutral point. According to Kirchhoff's voltage law, the floating capacitor voltage V_{C3} can be expressed as $V_{C1} - V_O$. In Figure 2h, when the level state is $-E$, the current flows through C_3 and the load and returns to the neutral point, and the floating capacitor voltage V_{C3} can be expressed as $-V_O$. Therefore, when the switch states are P3 and N1, the voltage of C_3 can be estimated. In Figure 2e, when the level state is E, the current flows through C_4 and the load and returns to the neutral point, and the floating capacitor voltage V_{C4} can be expressed as V_O. When the flat state is $-3E$, the current flows through C_2, C_4 and the load and returns to the neutral point, and the floating capacitor voltage V_{C4} can be expressed as $V_O + V_{C2}$. Therefore, when the switching states are P1

and N3, the voltage of C_4 can be estimated. Therefore, the voltage estimation formula of capacitors C_3 and C_4 can be expressed as:

$$V_{\mathrm{FC\_est}} = \begin{cases} V_{\mathrm{C1}} - V_{\mathrm{O}}, & V_{\mathrm{O}} = 3E \\ V_{\mathrm{O}}, & V_{\mathrm{O}} = E \\ -V_{\mathrm{O}}, & V_{\mathrm{O}} = -E \\ V_{\mathrm{O}} + V_{\mathrm{C2}}, & V_{\mathrm{O}} = -3E \end{cases}, \tag{4}$$

However, when voltage estimation is performed, there will be cases where the estimated value changes abruptly as the switch state changes. Therefore, it is necessary to deal with this sudden change in the control algorithm: use the estimated value at the previous moment to select the redundant switch state, so as to avoid the sudden change in the estimated value causing the estimated voltages of C_3 and C_4 to be unbalanced.

Since the proposed topology and modulation signal $\boldsymbol{u}_{\mathrm{r}}$ are both symmetrical, in theory, the charge and discharge capacities of capacitors C_3 and C_4 are not much different, and the redundant switch states at $2E$ and $-2E$ levels have the same effect on the charge and discharge of C_3 and C_4. Therefore, it is not necessary to set the priority of voltage regulation of C_3 and C_4 in the proposed control algorithm, and unified tracking regulation can be performed according to the estimated floating capacitor voltage value corresponding to the moment before the arrival of the output level $\pm 2E$. Let ΔV_{CF} be the voltage offset state between the estimated value of C_3 or C_4 and the reference value, the polarity of the voltage offset of C_3 and C_4 can be expressed as:

$$D_{\mathrm{C}} = \begin{cases} 1, \ \Delta V_{\mathrm{CF}} > 0 \\ 0, \ \Delta V_{\mathrm{CF}} \leq 0 \end{cases}, \tag{5}$$

Let the direction of the current flowing out of the inverter be the positive direction, and the current direction is represented by D_{I}:

$$D_{\mathrm{I}} = \begin{cases} 1, \ i_{\mathrm{O}} > 0 \\ 0, \ i_{\mathrm{O}} \leq 0 \end{cases}, \tag{6}$$

It can be seen from the literature [28] that the selection of the reference value of the floating capacitor voltage determines the storage and transmission of capacitive energy in the topology, and the transfer relationship of the capacitive energy is:

$$\Delta Q_{\mathrm{C1}} + \Delta Q_{\mathrm{FC\_P}} = \Delta Q_{\mathrm{C2}} + \Delta Q_{\mathrm{FC\_N}}, \tag{7}$$

In the formula, ΔQ_{C1} and ΔQ_{C2} are the energy transferred from C_1 and C_2 to the load in one modulating wave cycle, respectively; $\Delta Q_{\mathrm{FC\_P}}$ and $\Delta Q_{\mathrm{FC\_N}}$ are the energy transferred from C_3 and C_4 to the load in the positive and negative half cycles. Therefore, the voltage reference value of the positive and negative half-cycle floating capacitors can be set as:

$$V^{*}_{\mathrm{FC\_P}} = E + K(2E - \frac{V_{\mathrm{C2}}}{2}), \tag{8}$$

$$V^{*}_{\mathrm{FC\_N}} = E + K(2E - \frac{V_{\mathrm{C1}}}{2}), \tag{9}$$

In the formula, K is the voltage correction coefficient, and the value of K affects the balance degree of V_{C1} and V_{C2}.

When the estimated voltage of the floating capacitor C_3 or C_4 is greater than or less than the reference voltages $V_{\mathrm{FC\_P}^{*}}$ and $V_{\mathrm{FC\_N}^{*}}$, it needs to be discharged or charged, and then the switch state at the next moment is selected according to the direction of the output current I_{O} at this time. When the inverter outputs $2E$ and $-2E$ levels, the switching state selection principle for balancing the voltage of the floating capacitor is as follows:

$$S_{\mathrm{P2}} = [D_{\mathrm{C}} \odot D_{\mathrm{I}}] * \mathrm{P2P} + [D_{\mathrm{C}} \oplus D_{\mathrm{I}}] * \mathrm{P2N}, \tag{10}$$

$$S_{N2} = [D_C \odot D_I] * \text{N2P} + [D_C \oplus D_I] * \text{N2N}. \quad (11)$$

3.3. Implementation of the Proposed Algorithm

The implementation process of the floating capacitor voltage estimation is shown in Figure 6. By judging the size of the output voltage rounding up the level N, the estimation formula of the floating capacitor voltage is selected.

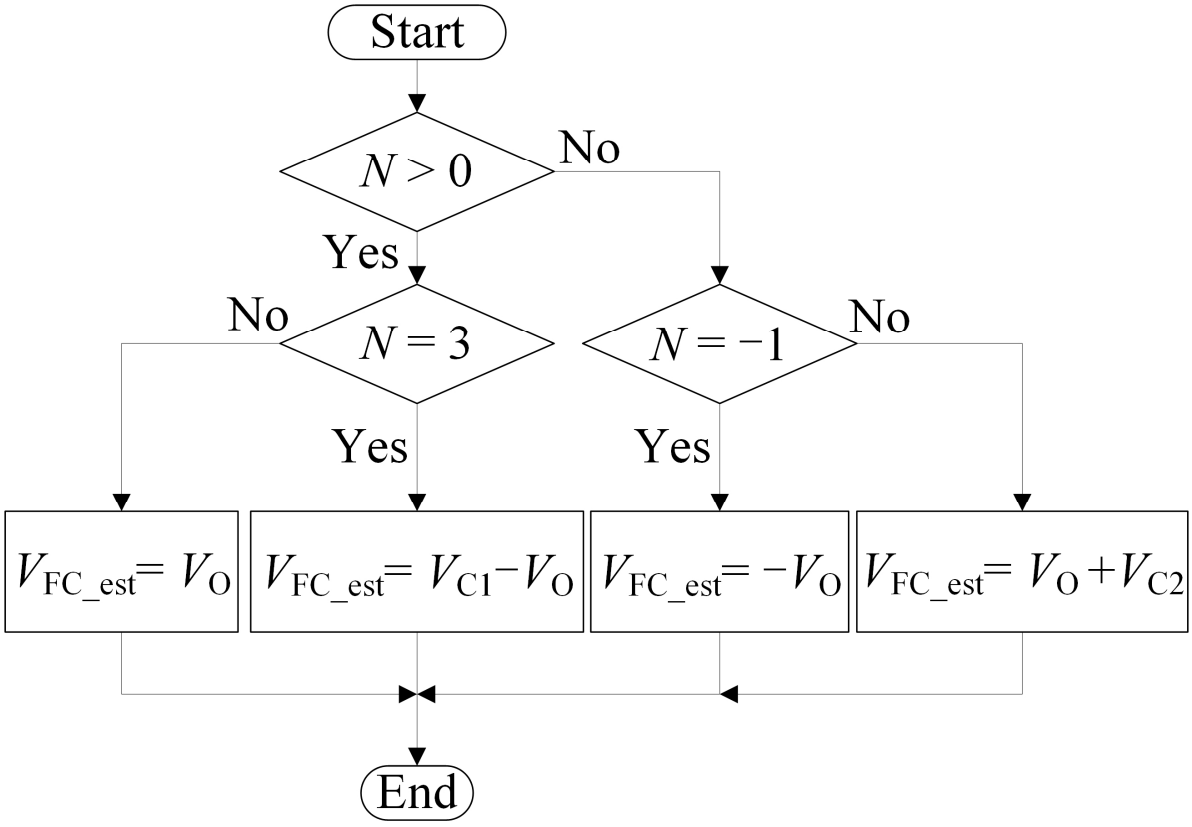


Figure 6. The flow chart of floating capacitor voltage estimation.

The flowchart of redundant switch state selection is shown in Figure 7. Combined with Table 1, if the sampled output current $I_O > 0$ and the output voltage V_O is positive, when the estimated value of the floating capacitor voltage is greater than the reference value, select the P2N switch state to discharge; when the estimated value of the floating capacitor voltage is less than the reference value, select the P2P switching state for charging, so that the voltage of the floating capacitor returns to a balanced state. Similarly, other redundant switch states can be selected according to Figure 7.

The block diagram of the proposed control strategy is shown in Figure 8. The nine-level inverter adopts one-dimensional space vector modulation, obtains the real-time operating parameters V_{C1}, V_{C2}, V_O, I_O of the inverter through sampling, selects the calculation formula of the floating capacitor voltages according to the redundant switch state, judges the positive and negative output current. Then, calculate the difference between the estimated value of the floating capacitor voltage and the reference value, and select the redundant switch state according to the charging and discharging requirements of the floating capacitor, and finally output the driving pulse of the switch tube S_k (k = 1, 2, ... 7).

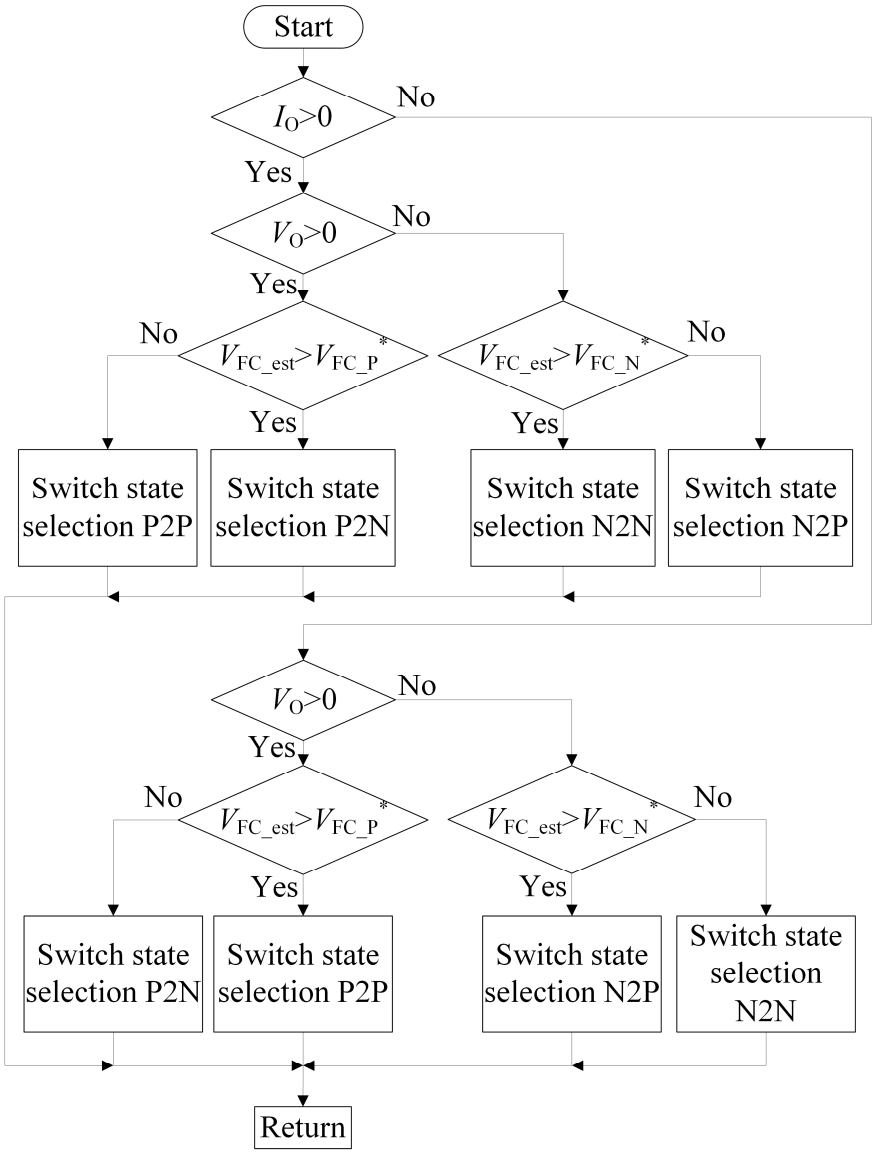


Figure 7. The flow chart of redundant switching states selection.

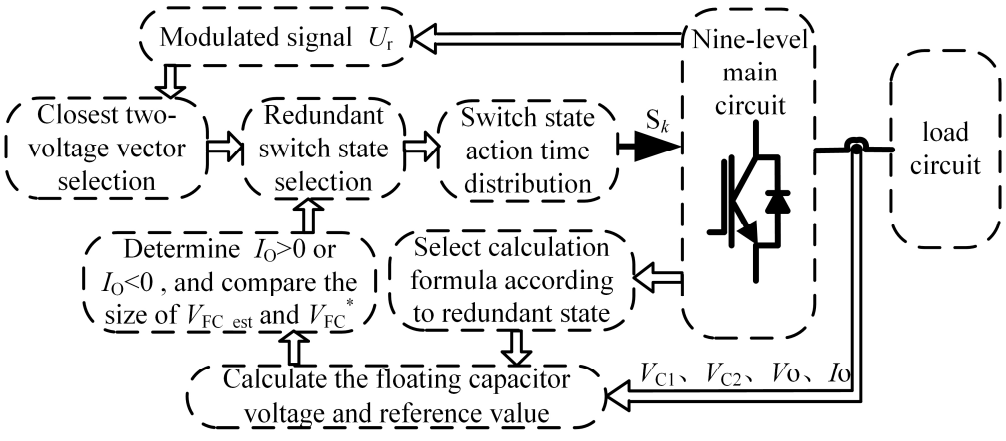


Figure 8. The block diagram of the proposed floating capacitor voltage sensorless control scheme.

4. Simulation and Experimental Analysis

4.1. Simulation Analysis

In order to verify the validity of the proposed topology and the feasibility of the control strategy, a single-phase nine-level inverter simulation model was built in Matlab/Simulink. The simulation parameters are listed as follows: dc-link voltage reference value is 400 V, bus capacitor $C_1 = C_2 = 6720$ uF, flying capacitor $C_3 = C_4 = 6$ mF, output voltage fundamental frequency is 50 Hz, load $L_f = 30$ mH, $R_f = 10$ Ω. The voltage correction coefficient K in Equations (8) and (9) is tuned as 0.1.

Figure 9 shows the steady-state simulation waveforms of the proposed topology. It can be seen from Figure 9a,b that the output voltage of the proposed topology is a nine-level staircase wave, the output current has a high sine degree, and the current THD is 0.28%. In Figure 9c, the bus capacitor voltage is stable around 200 V, with a fluctuation range of ±3.8 V, and the floating capacitor voltage is stable around 50 V, with an up and down fluctuation range of ±2.2 V.

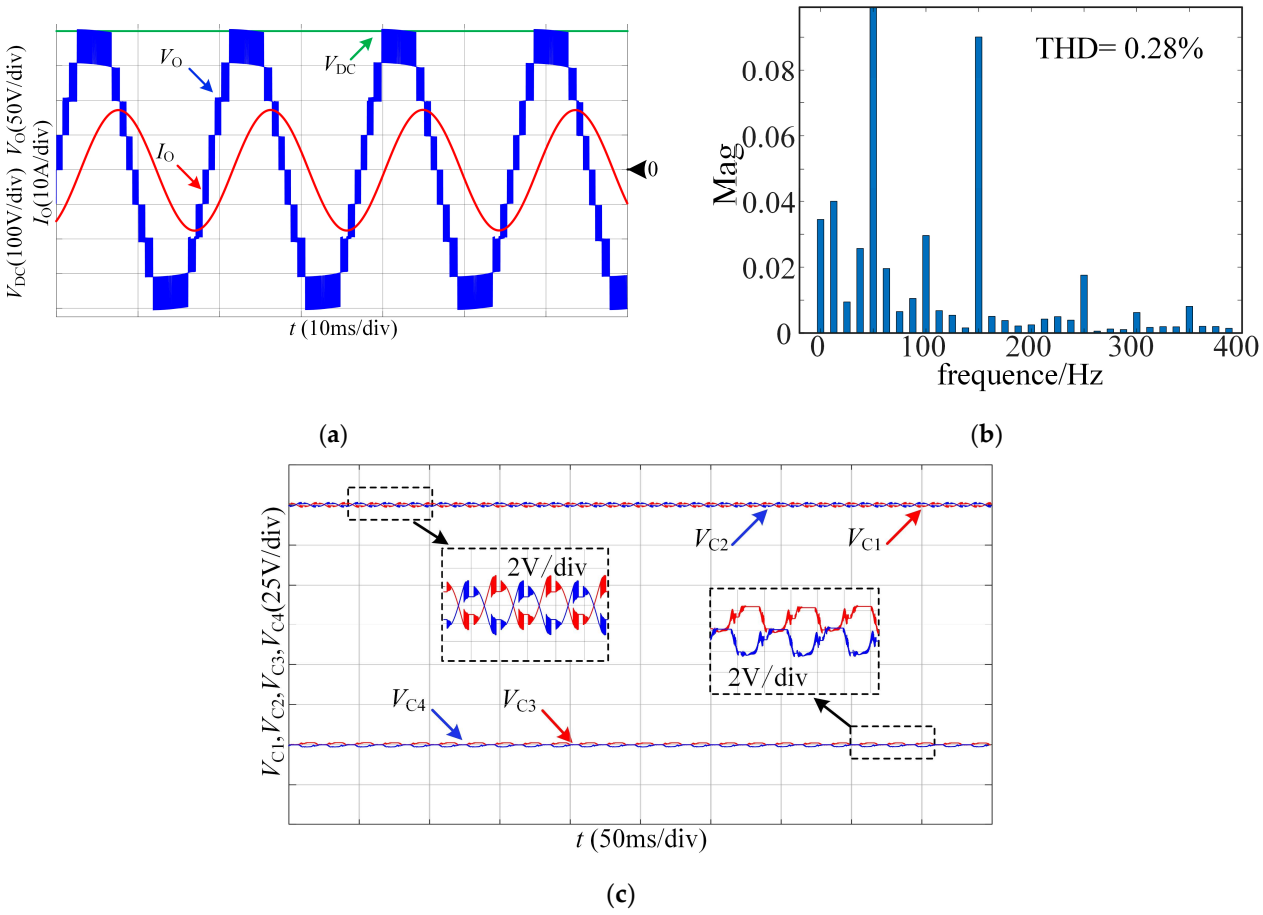


Figure 9. Simulation waveforms of the proposed topology in the steady-state. (**a**) Bus voltage output voltage and output current simulation waveform; (**b**) Output current FFT analysis results; (**c**) Simulation Waveforms of dc-link Capacitor Voltage and Suspended Capacitor Voltage.

Figure 10 shows the simulation waveforms of the dc-link voltage, bus capacitor voltage, floating capacitor voltage, output voltage and output current when the modulation factor $M = 0.7$, $M = 0.85$ and $M = 1$. THD_V and THD_I are the THD values of the output voltage and output current, respectively. It can be seen from Figure 10 that when the modulation degree is small, the output voltage presents a seven-level staircase wave. When the modulation degree changes, the output voltage can achieve a smooth transition. Under different modulations, both the bus capacitor voltage and the floating capacitor voltage are stable

near their reference values, where the bus capacitor voltage ripple is 7 V, and the floating capacitor voltage ripple is 5 V.

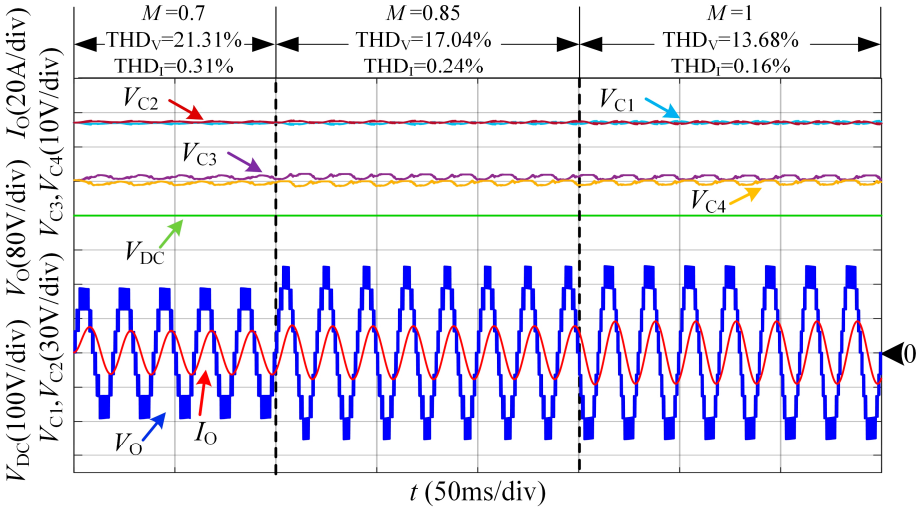
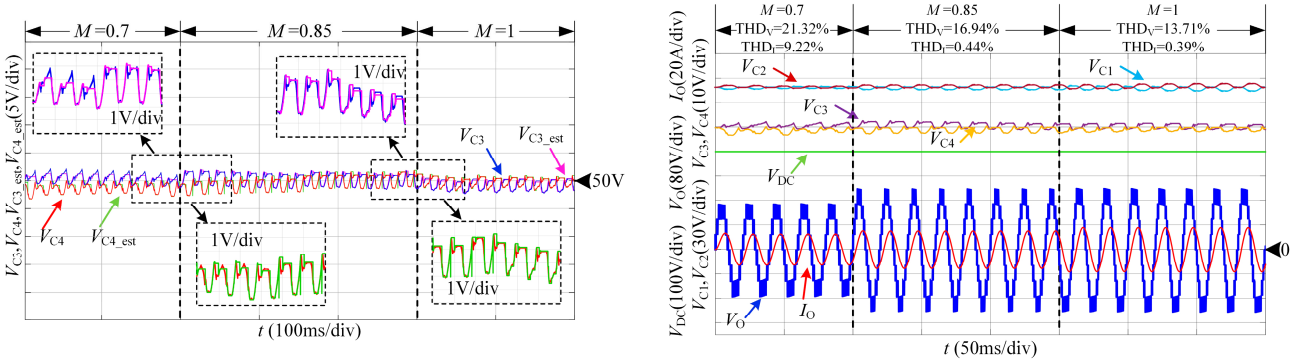


Figure 10. Simulation results under different modulation degree *M*.

Figure 11 shows the simulation waveforms of the proposed voltage sensorless control strategy. It can be seen from Figure 11a that the proposed control method can track the voltage of the floating capacitor quickly and accurately under different modulation degrees, and the error rate is less than 2%. Comparing Figures 10 and 11b, the proposed method has the same output performance as the traditional sensor measurement method, but its capacitor voltage ripple is larger than that of the sensor measurement, the bus capacitor voltage ripple is 13 V, and the floating capacitor voltage ripple is 7 V. Because the floating capacitor voltage estimation method is affected by the sampling time and the system calculation time, a slight delay leads to a larger estimation error.



(**a**) (**b**)

Figure 11. Simulation waveforms of the proposed floating capacitor voltage sensorless control scheme. (**a**) Simulation waveform of actual and estimated value of floating capacitor voltage; (**b**) Capacitor voltage, output voltage and output current simulation waveforms.

4.2. Experimental Analysis

To further verify the effect of the circuit topology and control method proposed in this paper, an experimental platform is built, as shown in Figure 12. The experimental parameters are as follows: dc-link voltage reference value is 400 V, dc-link capacitor $C_1 = C_2 = 6720$ uF, floating capacitor $C_3 = C_4 = 6$ mF, output voltage fundamental frequency $f_g = 50$ Hz, load $L_f = 30$ mH, $R_f = 6\ \Omega$, and system switch Frequency $f_s = 2$ kHz. The switch device model used in this platform is IPW60R070C6, and its driver is QC962-8A.

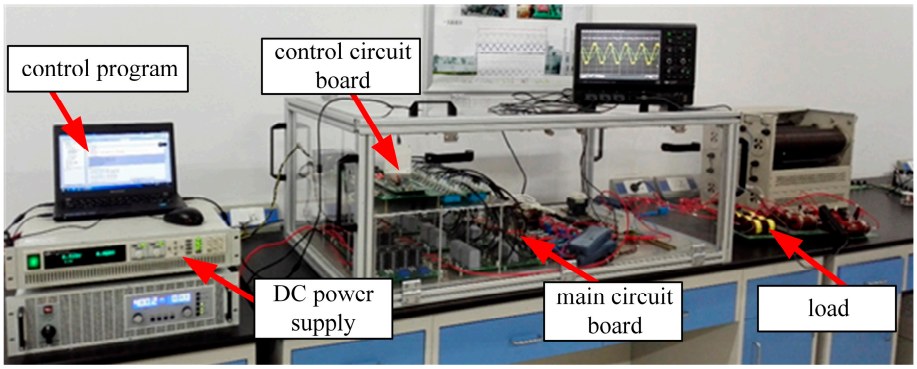


Figure 12. Scaled-down experimental platform of the proposed single-phase nine-level inverter.

Figure 13 shows the experimental waveforms of the proposed topology at different modulation degrees. In Figure 13a, the experimental waveform is basically consistent with the simulation result, the output voltage is a nine-level staircase wave, and the output current has a high sine degree. Due to the influence of the load inductance L_f, the current lags the voltage. It can be seen that the nine-level topology has good output performance. It can be seen from Figure 13b that V_{C1} and V_{C2} are both stable at about 200 V, and the voltage fluctuation range is ±12 V. It can be seen from Figure 13c that V_{C3} and V_{C4} are both stable at about 50 V, and the voltage fluctuation range is ±4 V.

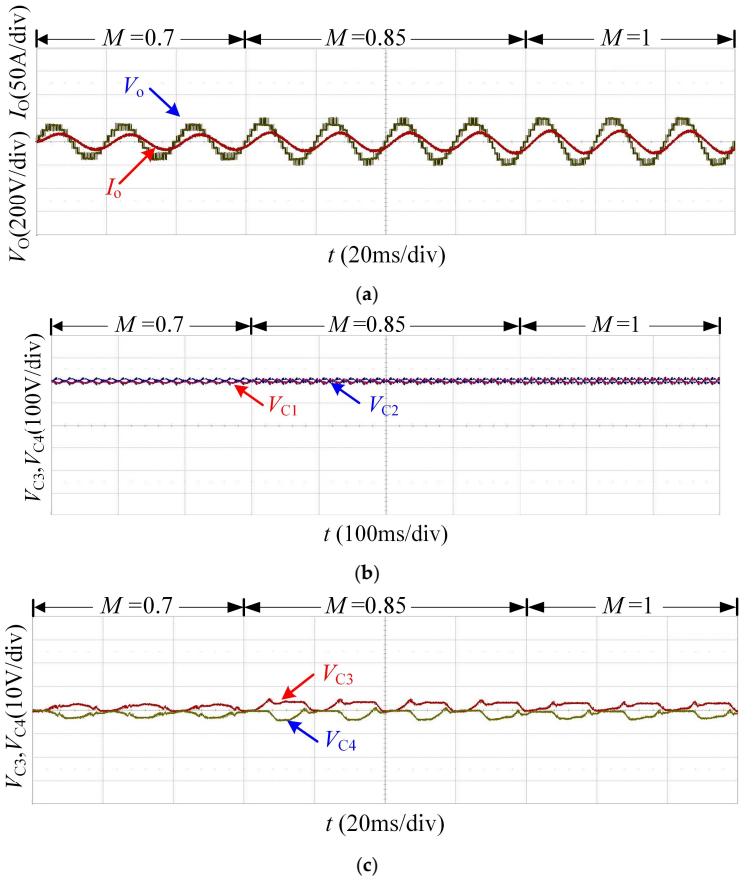


Figure 13. Experimental results of the proposed inverter with different *M*. (**a**) Output voltage V_O and output current I_O waveform; (**b**) dc-link capacitor voltage V_{C1}, V_{C2} waveform; (**c**) Suspension capacitor voltage V_{C3}, V_{C4} waveform.

Figure 14 shows the experimental waveforms of the proposed voltage sensorless control strategy. It can be seen from Figure 14a that under different modulation degrees, the proposed method has the same effect as using the floating capacitor voltage sensor, and both can achieve stable output of the inverter. In Figure 14b, V_{C1} and V_{C2} have the smallest ripple when M = 0.85, and the voltage ripple range is ±14 V. From Figure 14c, it can be noticed that the voltage fluctuation range of V_{C3} and V_{C4} is ±8 V, which is slightly larger than that of the method with floating capacitor voltage sensor. It is because the voltage ripple is affected by factors such as the control frequency of the system, the correction coefficient K, and the number of estimated sampling points. Although the voltage ripple is large, the proposed sensorless control strategy can reduce the hardware cost of the system, since there is no need to design the sampling circuit of the floating capacitor voltages.

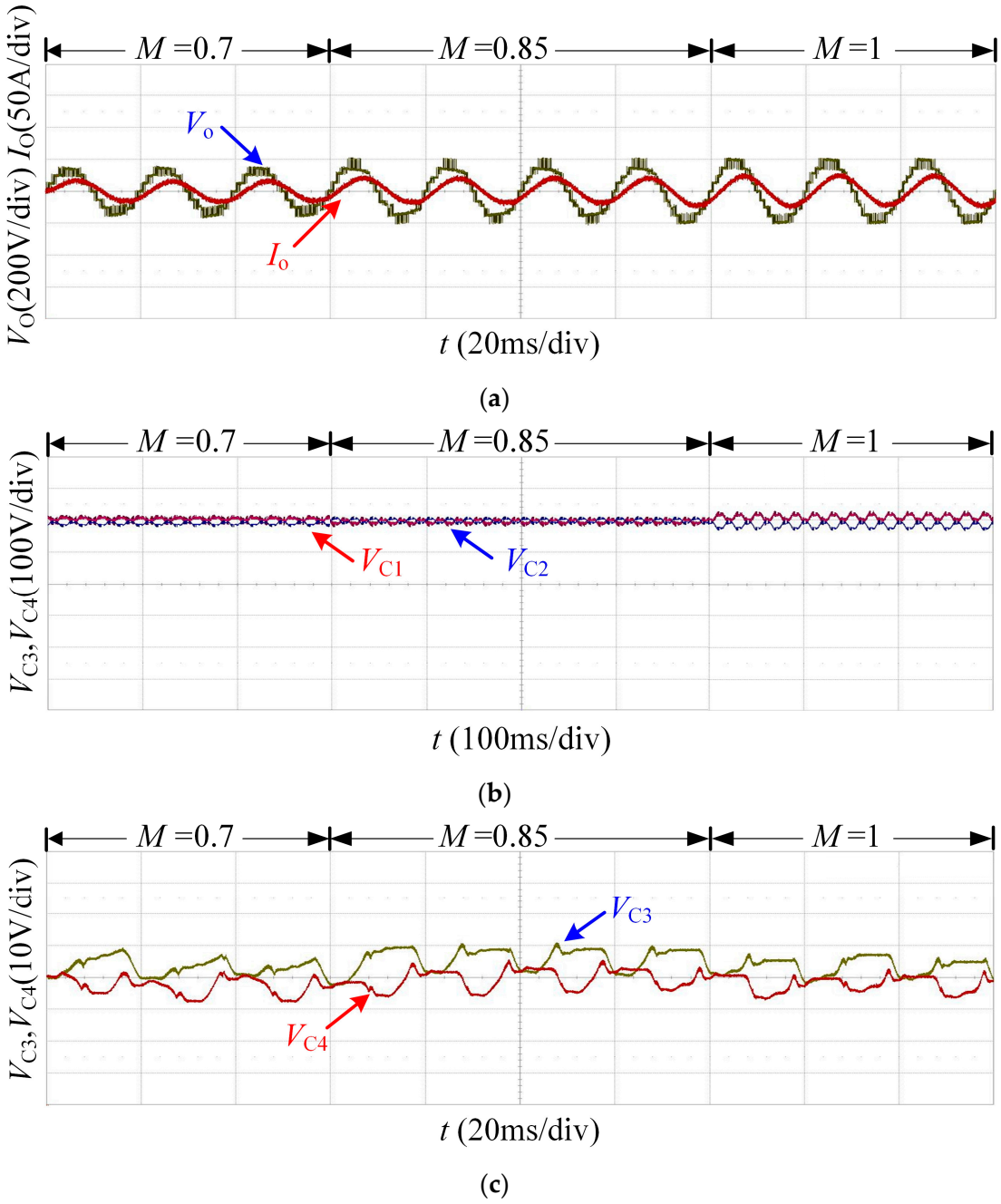


Figure 14. Experimental results of the floating capacitor voltage sensorless control scheme. (**a**) Waveforms of the output voltage V_O and output current I_O; (**b**) Waveforms of the dc-link capacitor voltages V_{C1}, V_{C2}; (**c**) Waveforms of the capacitor voltage V_{C3}, V_{C4}.

5. Conclusions

This paper proposes a single-phase non-isolated nine-level inverter topology. Compared with the traditional topology, this topology has the advantages of fewer switching devices and fewer floating capacitors. Additionally, a floating capacitor voltage sensorless control algorithm is presented. The algorithm realizes the estimation of the floating capacitor voltages by sampling the output voltage and the bus capacitor voltage, and it achieves the balance of the floating capacitor voltages combined with the one-dimensional space vector modulation method. Finally, the proposed algorithm is verified by computer simulation and experiments. Theoretical analysis and simulation experimental results show that the proposed topology and control method have the following advantages:

(1) Compared with the traditional nine level inverter topology, the proposed nine level inverter has obvious advantages in the number of switching devices and the number of flying capacitors. The most prominent is that the number of switching devices through which the current flows is the least, which reduces the device switching loss in the inverter.
(2) The proposed method reduces 50% capacitor voltage sampling circuit, which can greatly reduce the cost of the system, and it can realize the accurate estimation of the floating capacitor voltage and its balance control at a specific moment.

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