

## Article

# A Model of DC-DC Converter with Switched-Capacitor Structure for Electric Vehicle Applications

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**Abstract:** In this paper, a DC-DC converter with an innovative topology for automotive applications is proposed. The goal of the presented power converter is the electrical storage system management of an electric vehicle (EV). The presented converter is specifically compliant with a 400 V battery, which represents the high-voltage primary source of the system. This topology is also able to act as a bidirectional power converter, so that in this case, the output section is an active stage, which is able to provide power as, for example, in the case of a low-voltage battery or a supercapacitor. The proposed topology can behave either in step-down or in step-up mode, presenting in both cases a high gain between the input and output voltage. Simulation results concerning the proposed converter, demonstrating the early feasibility of the system, were obtained in a PowerSIM environment and are described in this paper.

**Keywords:** DC-DC converter; automotive converter; high-gain converter; electric mobility



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## 1. Introduction

The idea of a sustainable society represents a goal for all the major drivers of technological progress in several fields. Mobility plays a key role in this, since it has long been a primary need of human beings; it has therefore stimulated notable interest from industries and researchers as far as the use of sustainable energy sources is concerned. Therefore, the idea of eco-sustainable mobility is increasingly strong; in particular, there is an increasing focus on electric mobility. Nevertheless, to be truly ecologically sustainable, electric mobility must use energy arising from renewable sources. In order to use power at any time, storage systems are fundamental to compensate the typically intermittent nature of the power generated by means of renewable sources. In the general scenario of sustainable electric mobility, made of renewable sources, electric storage systems and electrical drives, power electronics assumes a fundamental role, consisting in the interconnection between all these components in order to produce smart and efficient energy conversion.

Technical-economic issues for the use of renewable sources and control strategies for the proper exploitation of the power arising from them are fundamental [1–3], as well as the efficient power management of hybrid electrical storage systems made, for example, of batteries and ultracapacitors, in order to take advantage of the inherent benefits given by each storage element in terms of power density, energy density, reliability, and durability [4,5]. Among the innovative approaches to truly eco-sustainable mobility, the use of fuel-cells represents a notably valid solution, provided that green hydrogen is used [6]. The use of power electronics is also the basis for innovative electric vehicle (EV) charging methods, such as inductive power transfer (IPT), which makes it possible to wirelessly charge the storage system [7]. By means of reversible power electronics stages, the energy can also flow from the EV storage system to the grid, according to the vehicle-to-grid (V2G) concept. The V2G idea is strongly related to the current concept of active demand: in a smart electrical network, the consumer can also be a producer of energy. In the case of

surplus of energy stored in some devices of the grid, the power can flow towards other devices requiring energy. The V2G idea is flexible and strongly related to other similar approaches, such as vehicle-to-vehicle and vehicle-to-home [8,9].

The target of this paper consists of a crucial stage in the production of an electric vehicle (EV), that is, the on-board power conversion system. Specifically, the main focus of this work is the DC-DC converter, which interconnects a high-voltage primary source and a low-voltage section. The considered case is a (400–48) V DC-DC bidirectional converter, where 400 V represents the higher voltage primary source, typically a battery, whereas 48 V represents the lower voltage section, which is either a DC voltage bus or another storage system. The investigated converter must therefore guarantee a high gain both in the step-down operation, i.e., from 400 V to 48 V, and in the step-up operation, i.e., from 48 V to 400 V. In addition to this, it must be able to present low current ripple at the input and output sections, in order to minimize the electromagnetic interference inside the vehicle. For the gain maximization of DC-DC converters, different isolated topologies have been presented in scientific research. Some examples are given in [10–15], presenting a high conversion ratio but needing expensive filtering and snubber networks, in addition to the high costs due to the transformer stage. Generally, in spite of the advantages offered by electrical insulation in terms of safety and grounding issues, isolated converters are heavy, bulky, and expensive.

This paper focuses on non-isolated topologies of DC-DC converters aiming at high output-to-input voltage ratios. Simple topologies are generally preferred to complex ones, so that design and control can be made easier; therefore, if the basic unidirectional version is considered, one-switch topologies are better than two-switch topologies. In [16], different topologies with multiple inductors and capacitors are presented. Although superbuck and superboost converters, based on two-inductor and one-switch switching cells, are excellent in terms of the low current ripple at their terminal sections, they present the same gain as conventional buck and boost converters, respectively [17,18]. The interleaved converter described in [19] guarantees a higher gain with respect to the conventional buck or boost converter and gives low current ripple as well, but it is quite complex, presenting two active switches and four diodes. Other DC-DC converters reach high gain but with high complexity and high current ripple. In [20], the proposed boost converter reaches a notable gain with one controlled switch, but at the cost of a high number of components, consisting of eight diodes, four inductances, and one capacitance, as well as a pulsating output current. In [21], a high-conversion-ratio bidirectional DC-DC converter with coupled inductors is presented, but at the cost of a notably complex circuit, also based on five active switches and three capacitors, as well as a pulsating output current, which implies the addition of heavy and bulky filters to the already expensive coupled inductors. Similarly, in [22], in spite of the high complexity of the proposed converter, notable filters are required at the output section in order to smooth the pulsating current.

Among the different solutions of DC-DC converters proposed in scientific research in order to obtain high conversion ratios, the topologies based on switched capacitors are particularly effective and promising. Nevertheless, different issues in terms of cost and complexity are generally present in these converters. In [23], a high-voltage gain-switched capacitor boost converter is proposed, presenting seven switches, three capacitors, and one inductor, at the cost of a highly pulsating current at the output section, thus requiring heavy filtering networks in addition to its several components. In [24], the proposed converter presents both a high number of components and a pulsating output current. The switched capacitor/switched inductor topology proposed in [25], in spite of a high gain, presents a pulsating output current and a notable amount of components, that is, two controlled switches, two inductors, three capacitors, and six diodes. Despite featuring fewer components, the converter proposed in [26] presents a high pulsating output current. In the converter presented in [27], in which only two capacitors and one inductor are present as reactive components, high gain and efficiency are obtained at the cost of seven controlled switches, which increase the system's complexity. The topology of the converter presented

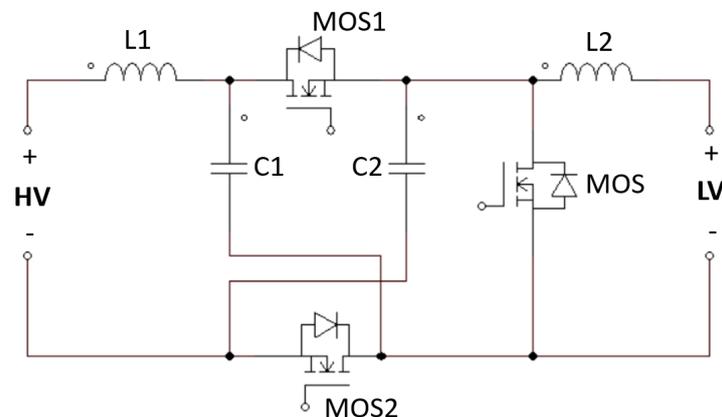
in [28] offers continuous current waveforms at the terminal sections, with relatively low complexity, but it is unidirectional. Complex topologies and analytical methods regarding switched-capacitor converters are presented in [29–33].

In this paper, a non-isolated bidirectional DC-DC converter with low complexity, low input, and output current ripple with high gain is proposed. The proposed topology is based on a switched-capacitor structure, meaning that the electrical connection between two capacitors changes whenever a commutation occurs. This converter was designed and simulated in order to investigate its operation and feasibility between 400 V and 48 V, compliant with electric vehicle applications, particularly concerning storage system management.

This paper is organized as follows: Section 2 provides a description of the proposed power converter and analyzes both the step-down and step-up operation; Section 3 focuses on the parasitic effects on the converter gain, especially in the step-up operation; Section 4 discusses the obtained simulation results; in Section 5, conclusions are given.

## 2. Analysis of the Proposed Switched-Capacitor Converter

A schematic of the proposed DC-DC converter is shown in Figure 1. It consists of three switching devices (MOS1–MOS2–MOS), two inductors (L1–L2), and two capacitors (C1–C2). The presented DC-DC converter is able to work according to a buck-boost operation, meaning that, according to the energy flow direction, it can work in either in step-down (buck) or in step-up (boost) operation: in the buck operation, the high voltage (HV) is the source and the low voltage (LV) is the load, whereas in the step-up operation, the energy flows in the opposite direction.



**Figure 1.** Schematic of the proposed switched-capacitor converter.

In Table 1, the main intended specifications are given in terms of the HV and LV voltages  $V_{HV}$  and  $V_{LV}$ , target power level  $P$ , maximum current ripple on HV and LV sides ( $\Delta I_{L1,max}$  and  $\Delta I_{L2,max}$  respectively), power density, and maximum desired power losses.

**Table 1.** The converter specifications.

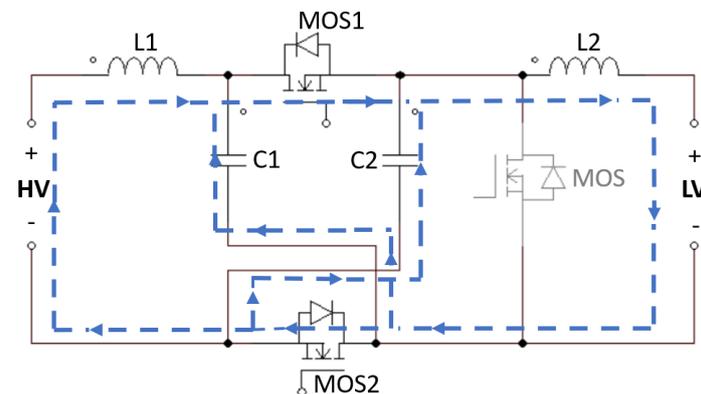
Parameter	Value
$V_{HV}$	400 V
$V_{LV}$	48 V
$P$	30 kW
$\Delta I_{L1,max} = \Delta I_{L2,max}$	10 A
Power Density	2 kW/kg
Max Power Losses	10%

Based on pulse-width modulation (PWM) control, the power flow amount and direction can be regulated according to the duration of the on and off states of the MOSFETs:

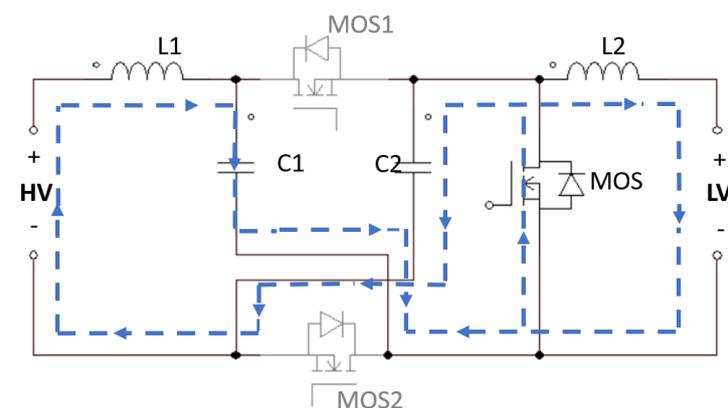
when MOS1 and MOS2 are on (during  $T_{on}$ ), MOS is off, and vice versa (during  $T_{off}$ ). This topology is quite simple if the corresponding unidirectional configuration is considered, where the active switches MOS1 and MOS2 are replaced by two diodes and the only active switch is MOS. Furthermore, due to the use of bidirectional switches, the direction of the current on the inductors can also be reversed, so that the converter is in continuous conduction mode (CCM) in any condition. As for the current ripple at the input and output sections, this is inherently low in the proposed converter since this topology is based on two inductances at both the terminal sections, leading to a current that does not pulsate. This implies the need of external filtering networks that are not bulky, limited electromagnetic emissions, and a reduction in the ripple of the input and output voltages.

### 2.1. Step-Down Operation

In Figures 2 and 3, the proposed converter is shown in its two operating modes regarding the step-down configuration, corresponding to the periods  $T_{on}$  and  $T_{off}$ , respectively, and referenced as Mode 1 and Mode 2. Inside the switching  $T_s$  period,  $T_{on}$  and  $T_{off}$  are the subperiods when MOS1 and MOS2 are on and off, respectively. Notably, according to the switched-capacitor structure, the connection between C1 and C2 changes from parallel in Mode 1 to series in Mode 2.



**Figure 2.** The proposed converter in step-down operation: Mode 1.



**Figure 3.** The proposed converter in step-down operation: Mode 2.

By assuming that  $V_{C1} = V_{C2}$  in both operating modes, since C1 and C2 are considered identical, and according to the Kirchhoff laws, as known from circuits theory, the following equations arise:

During Mode 1:

$$V_{L1} = V_{HV} - V_{C1} \quad (1)$$

$$V_{L2} = V_{C1} - V_{LV} \quad (2)$$

During Mode 2:

$$V_{L1} = V_{HV} - 2V_{C1} \quad (3)$$

$$V_{L2} = -V_{LV} \quad (4)$$

According to the energy balance regarding inductors  $L1$  and  $L2$  in a steady-state condition and according to the previous equations, the following expressions are obtained:

$$(V_{HV} - V_{C1}) \cdot T_{on} = -(V_{HV} - 2V_{C1}) \cdot T_{off} \quad (5)$$

$$(V_{C1} - V_{LV}) \cdot T_{on} = V_{LV} \cdot T_{off} \quad (6)$$

According to (6), the following equation regarding capacitor voltage arises:

$$V_{C1} = (V_{LV} \cdot T_{off} + V_{LV} \cdot T_{on}) / T_{on} \quad (7)$$

The duty cycle  $D$  is defined as follows:

$$D = \frac{T_{on}}{T_{on} + T_{off}} \quad (8)$$

The switching period can be defined as:

$$T_S = T_{on} + T_{off} \quad (9)$$

Therefore, according to (7)–(9):

$$V_{C1} = \frac{V_{LV}}{D} \quad (10)$$

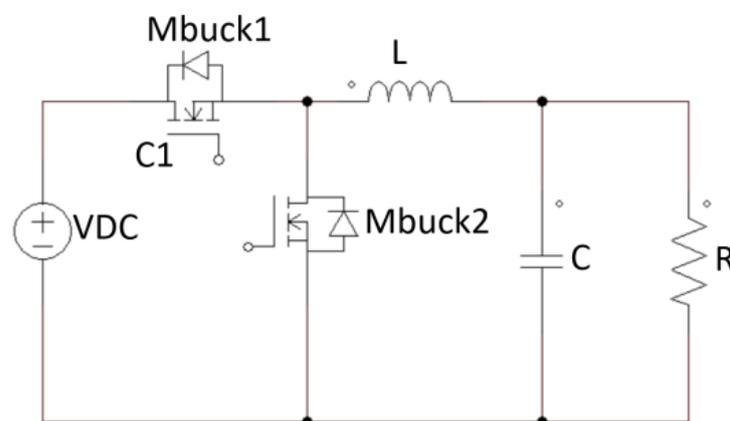
By substituting (10) into (5), the following equation is obtained:

$$V_{HV} \cdot T_S = \frac{V_{LV}}{D} T_{on} + 2 \frac{V_{LV}}{D} T_{off} \quad (11)$$

Finally, the load-to-source voltage gain can be derived as:

$$\frac{V_{LV}}{V_{HV}} = \frac{D}{2 - D} \quad (12)$$

In Figure 4, a schematic of a conventional buck converter is shown.



**Figure 4.** Schematic of the conventional buck converter.

Assuming that in this switching converter,  $T_{on}$  and  $T_{off}$  refer to the switch  $M_{buck1}$ , the following load-to-source gain is derived, as is well known:

$$\frac{V_R^{buck}}{V_{DC}^{buck}} = D^{buck} \quad (13)$$

According to (12) and (13), in Figure 5, the ideal conversion ratio of the output voltage to the input voltage for the proposed converter in step-down mode is shown as a function of the duty cycle, and compared to the conventional buck converter gain.

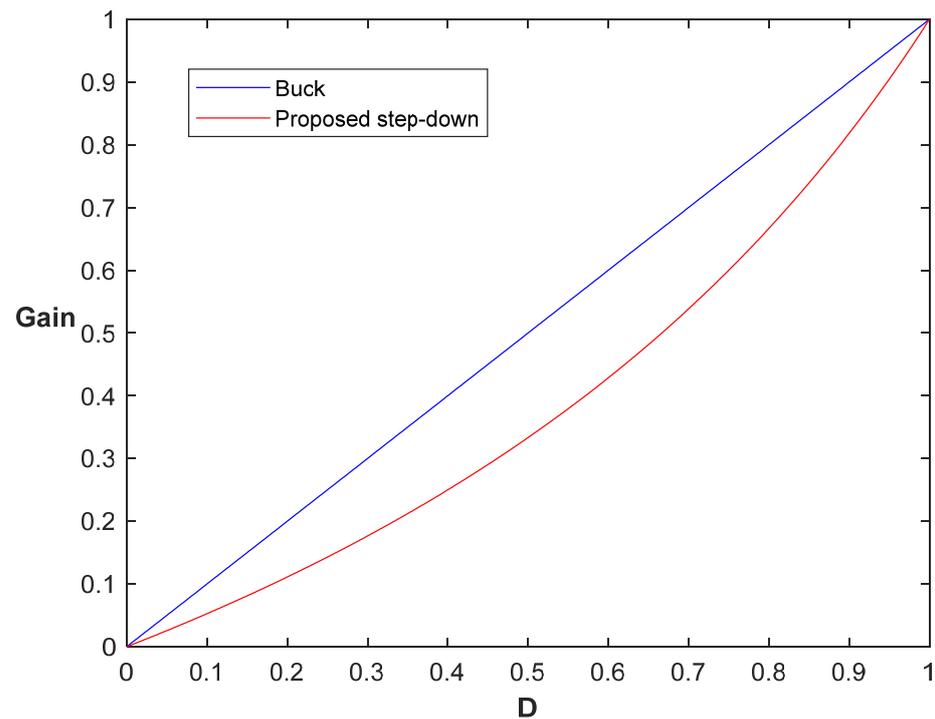


Figure 5. Gain vs. duty cycle for conventional and proposed step-down converter.

## 2.2. Step-Up Operation

In Figures 6 and 7, the proposed converter is shown in its two operating modes regarding the step-up configuration.

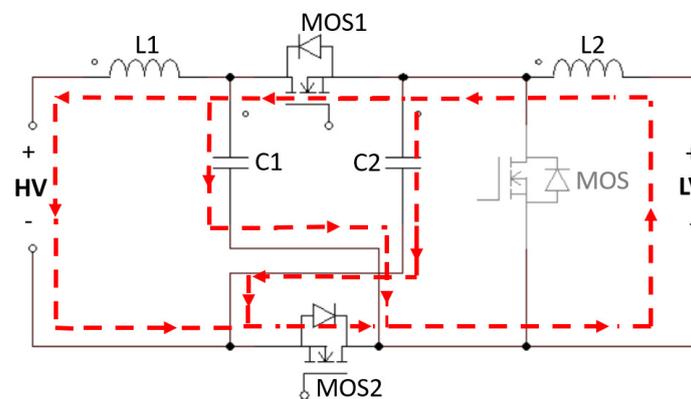


Figure 6. The proposed converter in step-up operation: Mode 1.

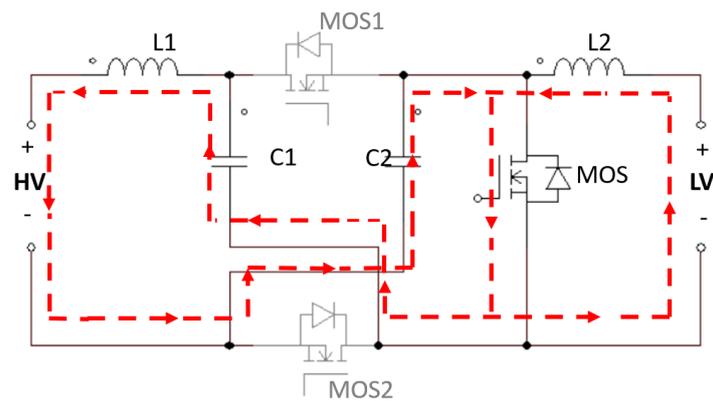


Figure 7. The proposed converter in step-up operation: Mode 2.

In the same way as in the step-down case, a system of proper equations can also be gained for the step-up operation, thus obtaining the ideal conversion ratio, as in the following:

$$\frac{V_{HV}}{V_{LV}} = \frac{2 - D}{D} \tag{14}$$

In Figure 8, a schematic of a conventional boost converter is shown.

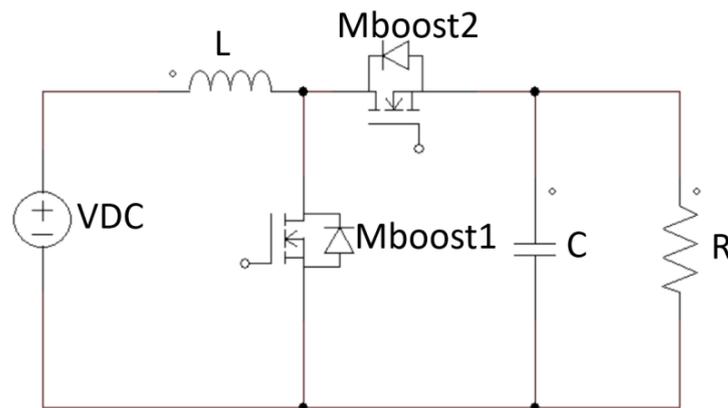
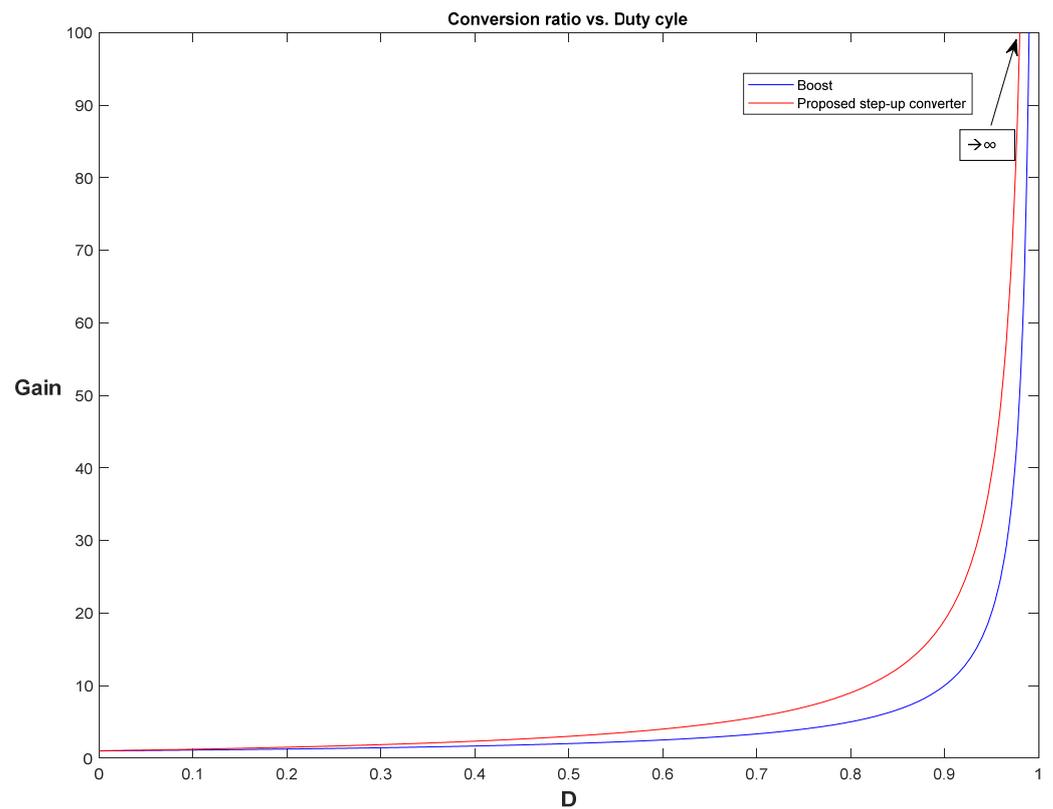


Figure 8. Schematic of the conventional boost converter.

Assuming that in this switching converter,  $T_{on}$  and  $T_{off}$  refer to the switch  $Mboost1$ , the following load-to-source is derived, as is well known:

$$\frac{V_R^{boost}}{V_{DC}^{boost}} = \frac{1}{1 - D^{boost}} \tag{15}$$

According to (14) and (15), in Figure 9, the ideal conversion ratio of the output voltage to the input voltage for the proposed converter in step-up mode is shown as a function of the duty cycle, and compared to the conventional boost converter gain. In this case, the duty cycle of the proposed converter has been referred to the switch  $MOS$  in order to obtain a gain increase along with the duty cycle increase.



**Figure 9.** Gain vs. duty cycle for conventional and proposed step-up converter.

### 2.3. Steady-State Current Analysis and Voltage Stress across the Components

Regarding the current waveforms, the following equations arise, both in step-down and step-up operations:

During Mode 1:

$$I_{L1} = I_{C1} + I_{MOS1} \quad (16)$$

$$I_{L2} = I_{MOS1} - I_{C2} \quad (17)$$

Therefore:

$$I_{L1} - I_{L2} = I_{C1} + I_{C2} \quad (18)$$

During Mode 2:

$$I_{L1} = I_{C1} = I_{C2} = -I_{MOS} - I_{L2} \quad (19)$$

A proper investigation into the voltage stress across the single components should be performed in order to choose them correctly. According to Equations (1)–(4), the maximum voltage stress on each inductor can be obtained. Based on (1), (3), and (10), the voltage across  $L1$  during Mode 1 and Mode 2 is:

During Mode 1:

$$V_{L1} = V_{HV} - \frac{V_{LV}}{D} \quad (20)$$

During Mode 2:

$$V_{L1} = V_{HV} - 2\frac{V_{LV}}{D} \quad (21)$$

According to (12), from (13) and (14) the following arise:

During Mode 1:

$$V_{L1} = V_{HV} - \frac{V_{HV} \frac{D}{2-D}}{D} = V_{HV} \left( \frac{1-D}{2-D} \right) \quad (22)$$

During Mode 2:

$$V_{L1} = V_{HV} - 2 \frac{V_{HV} \frac{D}{2-D}}{D} = -V_{HV} \left( \frac{D}{2-D} \right) \quad (23)$$

Based on (2), (4), and (10), the voltage across L2 during Mode 1 and Mode 2 is:

During Mode 1:

$$V_{L2} = V_{LV} \left( \frac{1-D}{D} \right) \quad (24)$$

During Mode 2:

$$V_{L2} = -V_{LV} \quad (25)$$

According to (12), from (17) and (18) the following arise:

During Mode 1:

$$V_{L2} = V_{HV} \left( \frac{D}{2-D} \right) \left( \frac{1-D}{D} \right) = V_{HV} \left( \frac{1-D}{2-D} \right) \quad (26)$$

During Mode 2:

$$V_{L2} = -V_{HV} \left( \frac{D}{2-D} \right) \quad (27)$$

Considering the results of Equations (15), (16), (19) and (20), the voltage across the inductors is the same:

$$V_{L1} = V_{L2} \quad (28)$$

Therefore, according to (19)–(21), the maximum voltage stress on each inductor is equal to  $V_{HV}$ . Regarding the voltage across the switches, the maximum voltage stress occurs when in interdiction; therefore, during Mode 1 for MOS and during Mode 2 for MOS1 and MOS2:

During Mode 1:

$$V_{MOS} = V_{C2} = \frac{V_{LV}}{D} \quad (29)$$

During Mode 2:

$$V_{MOS1} = V_{C1} = \frac{V_{LV}}{D} \quad (30)$$

$$V_{MOS2} = V_{C2} = \frac{V_{LV}}{D} \quad (31)$$

Therefore, the maximum voltage stress on the switches arises:

$$V_{MOS1,max} = V_{MOS1,max} = V_{MOS,max} = \frac{V_{LV}}{D} \quad (32)$$

### 3. Design of the Proposed Switched-Capacitor Converter

In Figures 10 and 11, the main waveforms of the proposed converter are highlighted in order to show its behavior.

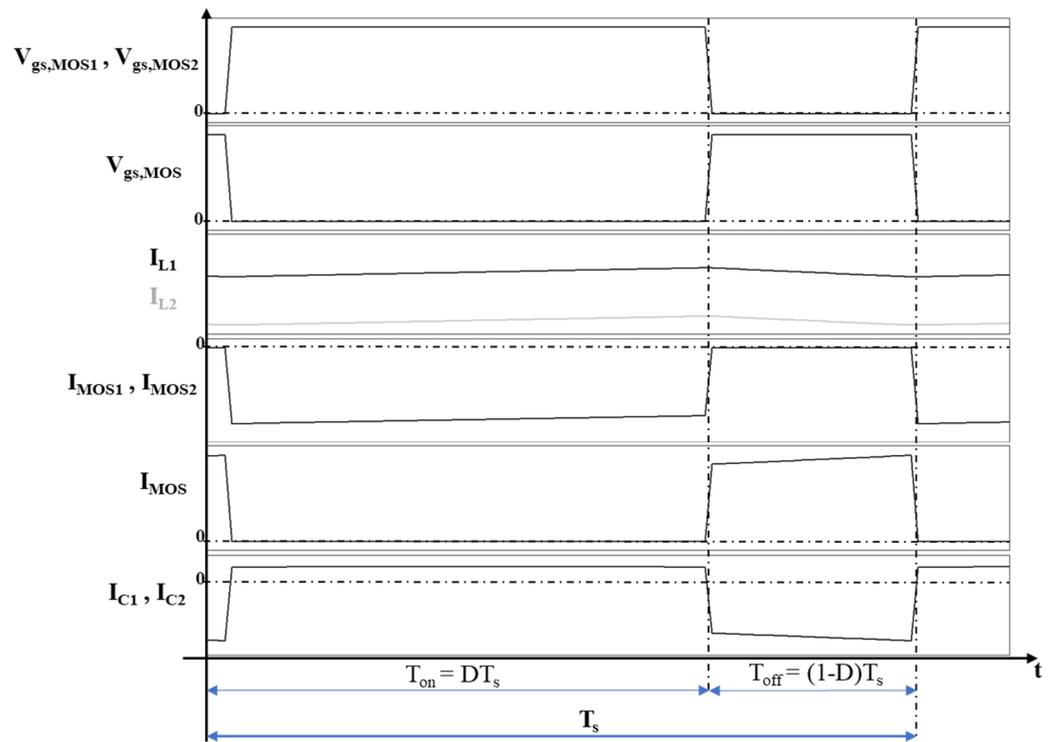


Figure 10. The main current waveforms of the proposed converter during the switching period  $T_s$ .

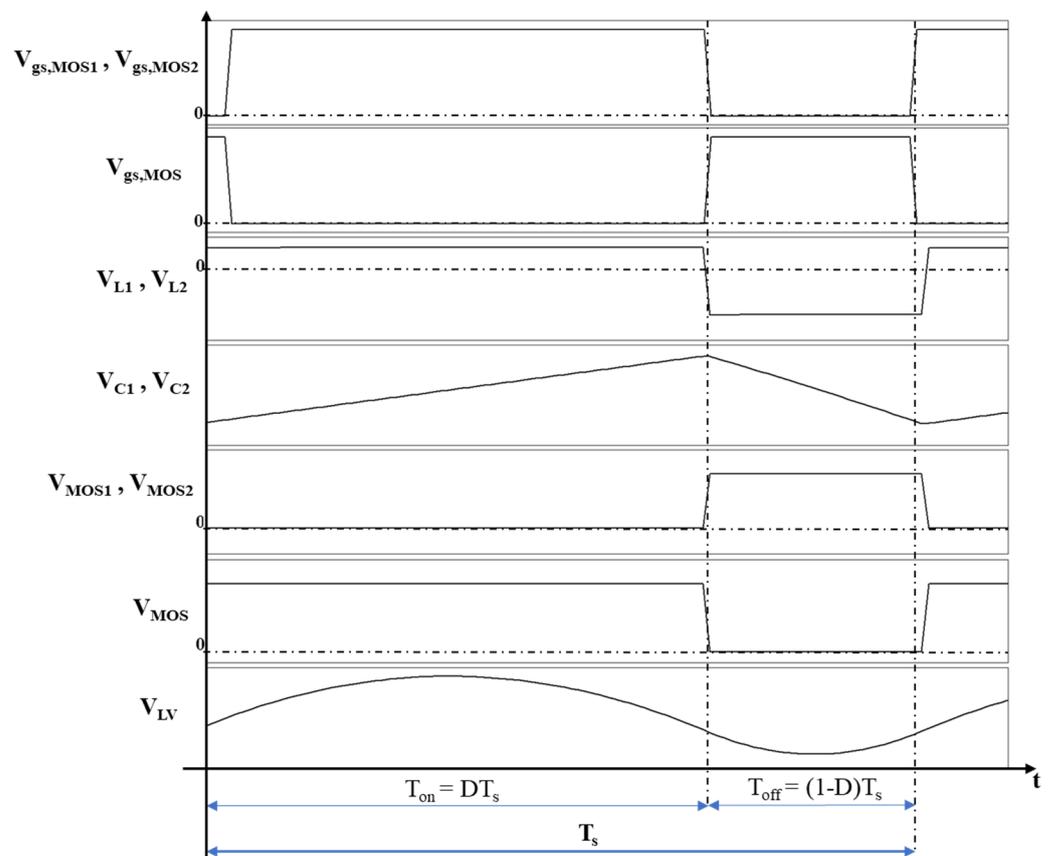


Figure 11. The main voltage waveforms of the proposed converter during the switching period  $T_s$ .

The maximum current ripple and maximum voltage ripple were considered as the design criteria to size the inductances and capacitances, respectively. The ripples of current  $\Delta I_{L1}$  and  $\Delta I_{L2}$  can be obtained by considering either the  $T_{on}$  (Mode 1) or the  $T_{off}$  (Mode 2). If Mode 1 is considered, then:

$$L_1 \frac{\Delta I_{L1}}{T_{on}} = |V_{HV} - V_{C1} - V_{MOS2}| = V_{HV} \left( \frac{D}{2-D} \right) \quad (33)$$

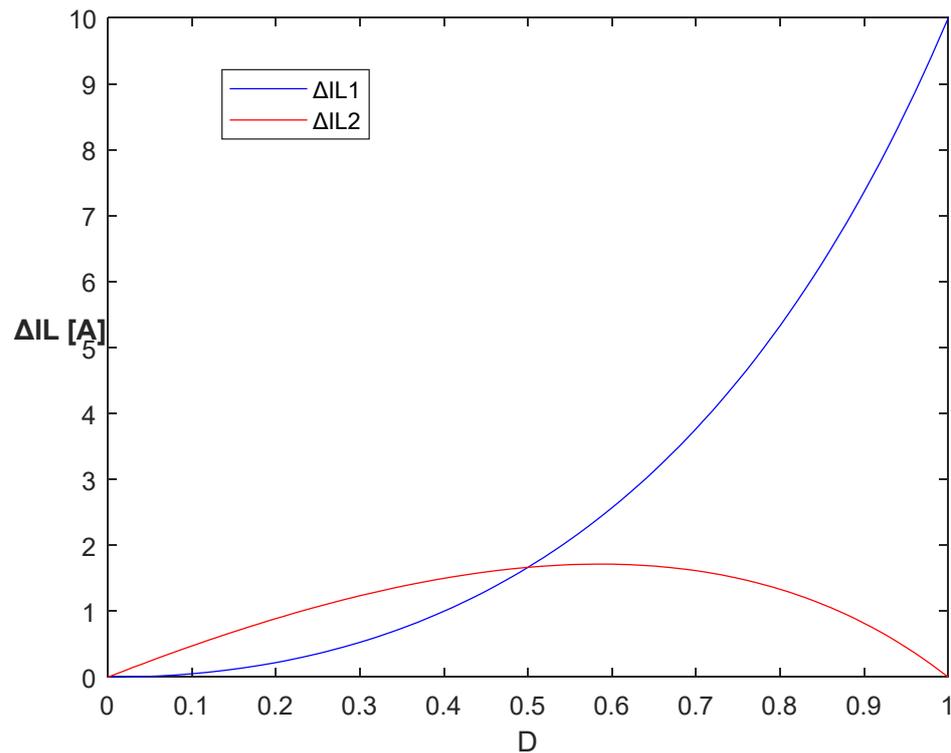
$$L_2 \frac{\Delta I_{L2}}{T_{on}} = V_{MOS} - V_{LV} = V_{HV} \left( \frac{1-D}{2-D} \right) \quad (34)$$

Therefore:

$$\Delta I_{L1} = \frac{D}{L_1} T_s V_{HV} \left( \frac{D}{2-D} \right) = \frac{D^2 V_{HV}}{f_s L_1 (2-D)} \quad (35)$$

$$\Delta I_{L2} = \frac{D}{L_2} T_s V_{HV} \left( \frac{1-D}{2-D} \right) = \frac{D(1-D) V_{HV}}{f_s L_2 (2-D)} \quad (36)$$

The maximum desired current ripple can be considered as a design criterion in order to size inductances. If a maximum 10 A value is defined for the current ripple, considering a case of a switching frequency  $f_s$  equal to 400 kHz,  $L_1$  and  $L_2$  are sized equal to 100  $\mu$ H. The corresponding values of the current ripple are reported in Figure 12.



**Figure 12.** Current ripple on  $L_1$  and  $L_2$  as function of the duty cycle  $D$ .

The ripples of voltage  $\Delta V_{C1}$  and  $\Delta V_{C2}$  can be obtained by considering either the  $T_{on}$  (Mode 1) or the  $T_{off}$  (Mode 2). If Mode 2 is considered, then:

$$I_{C1} = I_{C2} = C_1 \frac{\Delta V_{C1}}{T_{off}} = C_1 \frac{\Delta V_{C2}}{T_{off}} = I_{L1} \quad (37)$$

Therefore:

$$\Delta V_{C1} = \Delta V_{C2} = I_{L1} \frac{T_{off}}{C_1} = I_{L1} \frac{(1-D)}{C_1 f_s} \quad (38)$$

The maximum desired voltage ripple can be considered as a design criterion in order to size the capacitances. If a maximum 2.5 V value is defined for voltage ripple, considering a case of a switching frequency  $f_s$  equal to 400 kHz and a pessimistic case of  $L_1$  average current equal to 1000 A,  $C_1$  and  $C_2$  are sized equal to 1000  $\mu\text{F}$ . Correspondingly, the voltage ripples follow a decreasing linear trend with respect to the duty cycle, starting from the maximum ripple of 2.5 V at  $D = 0$ .

The capacitance  $C$  is implemented through an electrolytic capacitor, whereas the capacitances  $C_1$  and  $C_2$  are realized by means of metallized polypropylene film capacitors. A more detailed description of possible components that can be accordingly used is given in the following paragraphs. The switching frequency value of 400 kHz was chosen as an example, supposing that at high frequency and high voltage levels, SiC switching devices are used.

The parameter values of the proposed converter are accordingly reported in Table 2.

**Table 2.** The chosen parameters.

$C_1 = C_2 = C$	$L_1 = L_2$	$f_s$
1000 $\mu\text{F}$	100 $\mu\text{H}$	400 kHz

#### 4. Parasitic Effects on the Converter Gain

The convenience of the proposed configuration is highlighted by Figures 5 and 9, since the input-to-output gain in the step-down operation and the output-to-input gain in the step-up operation are higher for any duty cycle.

Nevertheless, a proper comparison must also consider the parasitic elements of the real components, due to their power losses. In order to estimate the influence of the parasitic components on the steady-state behavior of the proposed converter, only the equivalent series resistances of the employed components were considered as parasitic elements. This is especially evident in the step-up configurations, for which the real gain declines as the duty cycle approaches zero.

Indeed, both in the conventional boost converter and in the proposed step-up configuration, no energy can supply the load if the duty cycle is zero. Therefore, a peak in the gain vs. duty cycle curve is present for an intermediate value of  $D$ .

Simulations in the PowerSIM environment of the proposed converter, according to the parameters reported in Table 2, were carried out in order to evaluate the feasibility of the production of a future prototype and to estimate the influence of the parasitic effects on the voltage gain. In the simulation, a simple model for MOSFETs was considered, consisting mainly in the conductive losses, due to the need to understand the general behavior of the proposed converter, without investigating in detail, in a preliminary phase of study, the switching transients.

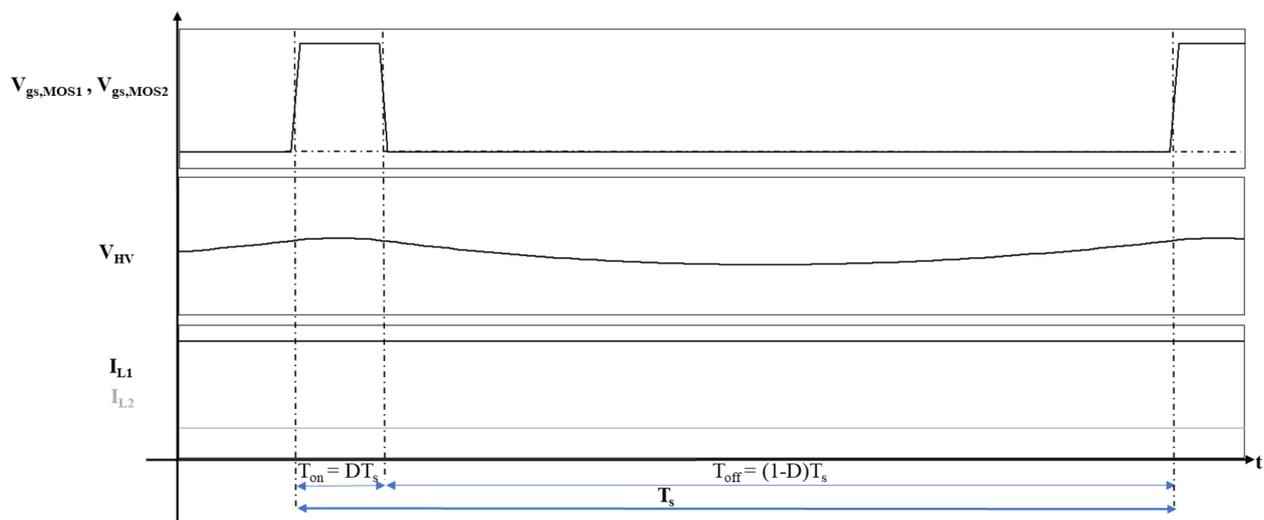
Most of the power losses are concentrated in the series elements, which are the switches, the capacitors, and the inductors. Therefore, for each of these components, an equivalent resistance  $R_s$  was considered and, for the sake of simplicity, the  $R_s$  value was chosen to be identical for each of them. Furthermore, as reported in Table 3 two different cases of parasitic effects were investigated, corresponding to two different values of per-unit-resistance  $R^*$ , defined as the ratio of  $R_s$  to the load resistance  $R$ : case (a) refers to an  $R^*$  of 0.001; case (b) refers to an  $R^*$  of 0.01. The conventional boost (conv. step-up) and the proposed converter in step-up operation (prop. step-up) were compared, considering open-loop simulations according to the values reported in Table 2, to a DC source voltage of 48 V and to a load resistance  $R$  of 10  $\Omega$ .

In Figures 13–16, the main waveforms in terms of gate signals, output voltage, and inductor currents regarding the proposed step-up and the conventional boost converter

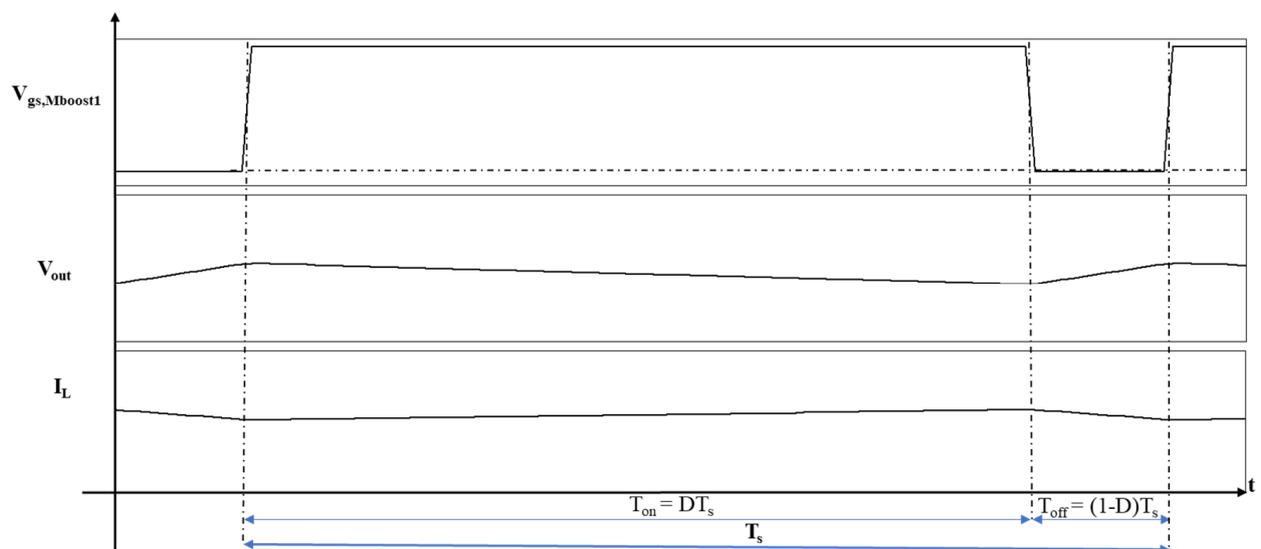
are provided with respect to both the considered cases of parasitic effects. The provided simulation plots refer to the maximum achieved gains. In more detail, Figures 13 and 14 concern case (a), whereas Figures 15 and 16 concern case (b), respectively.

**Table 3.** Considered cases of parasitic effects.

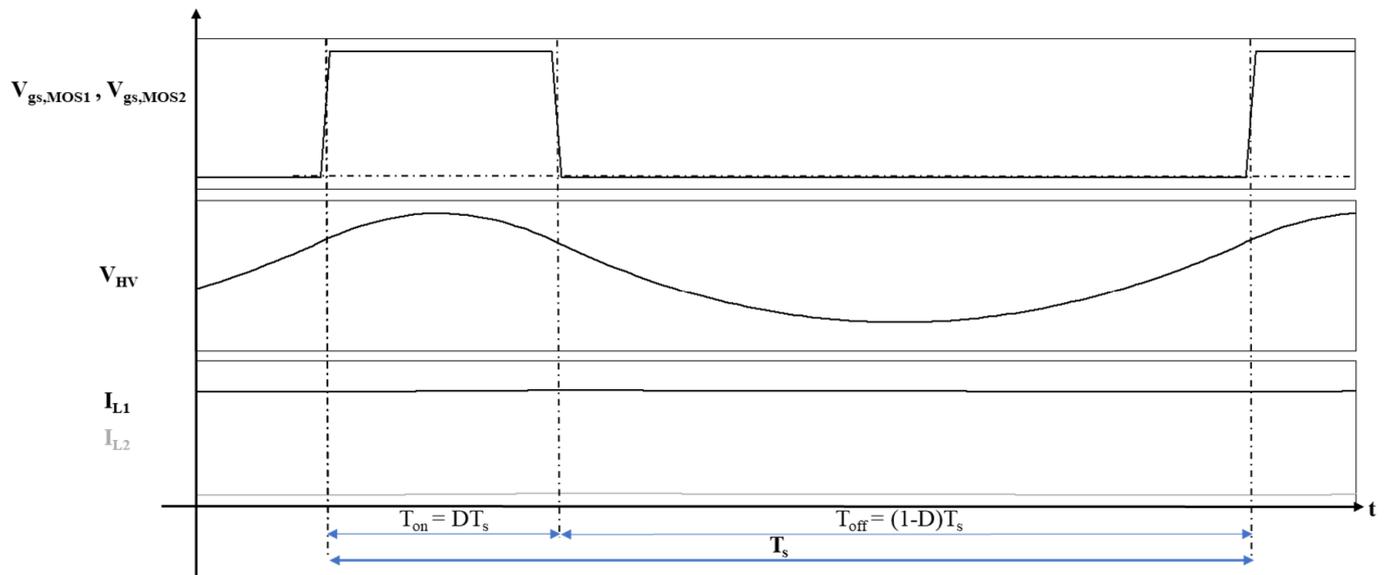
Case	Conv. Step-Up	Prop. Step-Up
	$R_s = R_{on,MOS1} = R_{on,MOS2} = R_L$	$R_s = R_{on,MOS1} = R_{on,MOS2} = R_{on,MOS} = R_{L1} = R_{L2} = R_{C1} = R_{C2}$
(a)	$R^* = R_s/R = 0.001$	$R^* = R_s/R = 0.001$
(b)	$R^* = R_s/R = 0.01$	$R^* = R_s/R = 0.01$



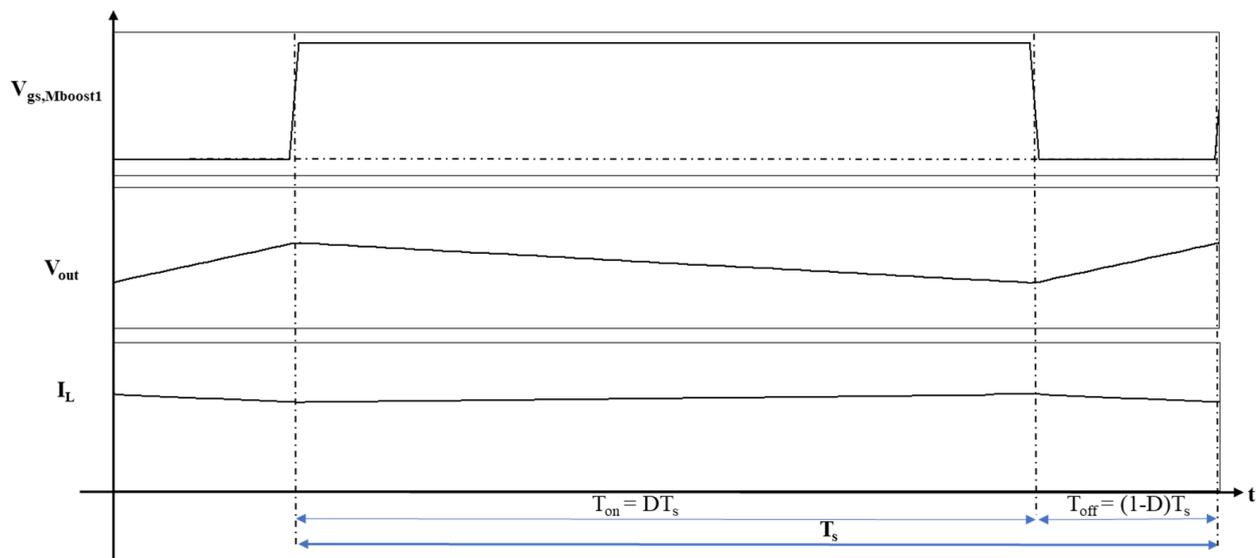
**Figure 13.** Gate signals, output voltage, and inductor current waveforms of the proposed converter for case (a) at maximum achieved gain:  $V_{LV} = 48$  V;  $V_{HV} = 528$  V;  $D = 0.1$ .



**Figure 14.** Gate signal, output voltage, and inductor current waveforms of the conventional boost converter for case (a) at maximum achieved gain:  $V_{in} = 48$  V;  $V_{out} = 297$  V;  $D = 0.85$ .



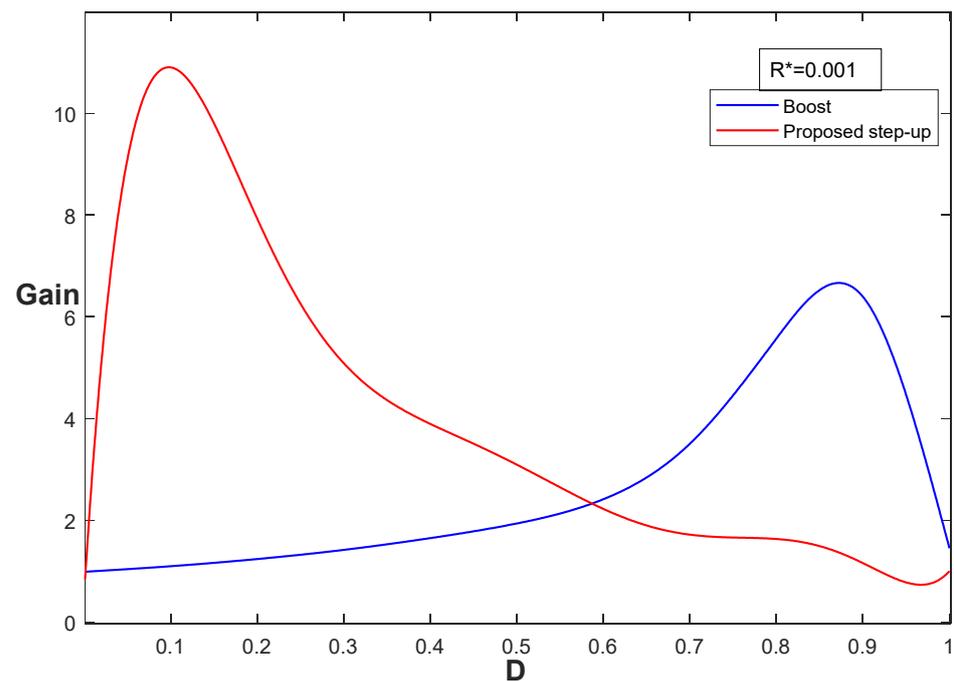
**Figure 15.** Gate signals, output voltage, and inductor current waveforms of the proposed converter for case (b) at maximum achieved gain:  $V_{LV} = 48$  V;  $V_{HV} = 170$  V;  $D = 0.25$ .



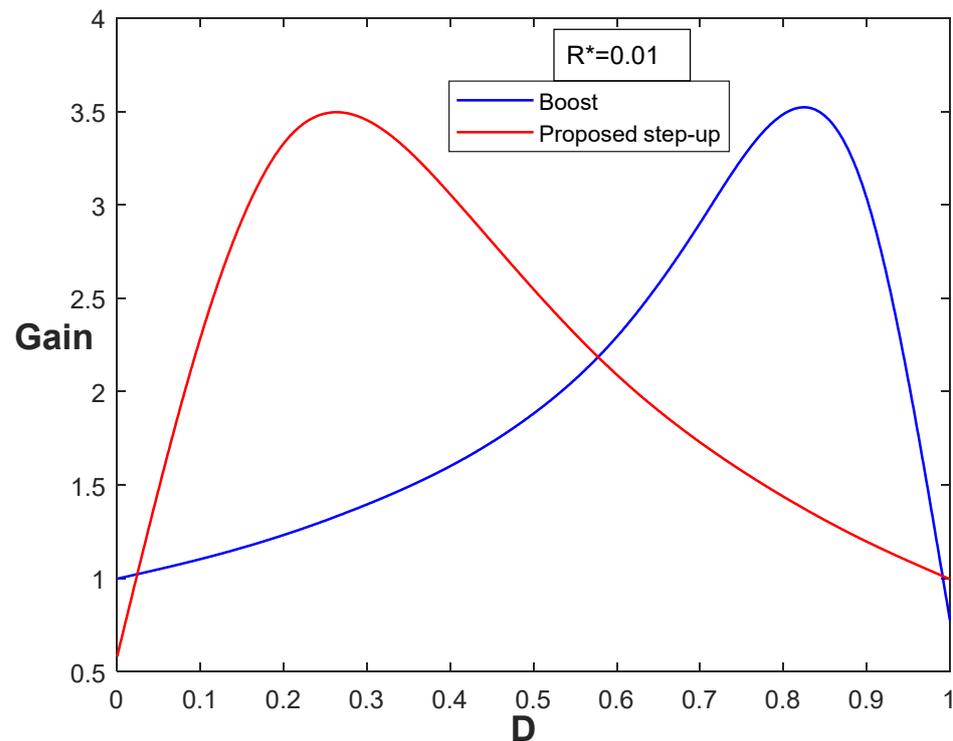
**Figure 16.** Gate signal, output voltage, and inductor current waveforms of the conventional boost converter for case (b) at maximum achieved gain:  $V_{in} = 48$  V;  $V_{out} = 165$  V;  $D = 0.8$ .

By post-processing these simulation results, the curves highlighted in Figures 17 and 18 were determined.

Methods for modelling the influence of switching losses on converter gain are described in [34,35].



**Figure 17.** Gain vs. duty cycle for conventional and proposed step-up converter for parasitic effects (a).



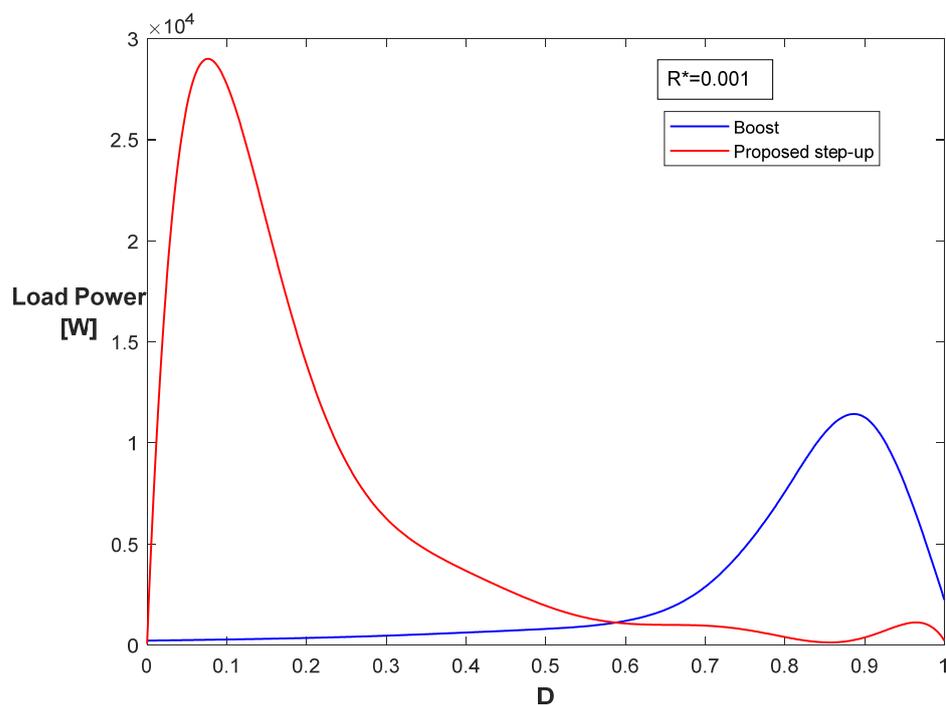
**Figure 18.** Gain vs. duty cycle for conventional and proposed step-up converter for parasitic effects (b).

## 5. Discussion

Based on the results reported above, the convenience of the proposed converter with respect to the conventional boost topology arises if the components are designed and produced to minimize power losses.

Therefore, it is crucial to select the devices and design the power converter so that the equivalent series resistances are minimized. Regarding this issue, case (a) in Table 3, which is the most challenging case in terms of power losses, is compliant with the equivalent series resistance (ESR) of some emerging switch and capacitor technologies. Silicon carbide (SiC) power MOSFETs [36] and metallized polypropylene film capacitors [37] compliant with the capacitance value in Table 2 guarantee very low ESRs at 600 V, equal to 12 m $\Omega$  and 1.7 m $\Omega$ , respectively. Attention should be paid to single electrolytic capacitors, since the higher the voltage rating, the higher the equivalent series resistance (ESR). Nevertheless, the higher the capacitance value, the lower the ESR; therefore, it is convenient to select a high-value electrolytic capacitor in order to minimize parasitic effects. For instance, given the capacitance value reported in Table 2, a maximum ESR of 143 m $\Omega$  was reported by a typical datasheet for a 400 V voltage [38], but if the value is decreased to 3600  $\mu$ F, a maximum ESR of 43 m $\Omega$  is reported. Solutions based on the device's parallel connection are particularly advantageous, offering a minimization of the equivalent series resistance even for the highest power levels. Indeed, a maximum voltage gain of more than 10 can be obtained from the proposed topology in case (a), which is more than compliant with the (400–48) V specification for the DC-DC converter.

From the comparison between the given results, the proposed converter is able to supply a maximum power of almost 30 kW for a load resistor  $R$  of 10  $\Omega$ , whereas the maximum power supplied by the conventional topology is half of this, as highlighted in Figure 19. These data were obtained via simulation results post-processing, considering the open-loop step-up configuration with a source voltage of 48 V. For a duty cycle of about 0.1, the maximum power load was obtained, corresponding to a load voltage of about 547 V.



**Figure 19.** Transferred power vs. duty cycle for conventional and proposed step-up converter for parasitic effects (a).

In automotive environments, the results achieved by the proposed converter represent a great advantage due to the need for high voltage ratios, e.g., between DC storage systems or between low-voltage battery packs and high-voltage electric motors, and for low electromagnetic disturbances without bulky and expensive filtering networks. Indeed, the presence of the series inductor inside the converter topology guarantees low current ripples.

The power efficiency at the maximum load power is 57% for  $R^* = 0.001$ . This implies an input power of around 50 kW, equivalent to an average source current of 1000 A. Although this represents the worst case, it is required to parallelize devices in order to obtain a total maximum current rate of 1000 A. The power efficiency reaches at least 95% for load power values of less than 5 kW, since the lower the current, the lower the conduction losses. This is compliant with the specifications given in Table 1, reporting a 10% maximum value in terms of desired converter power losses.

The efficiency estimation was taken into account, in addition to the equivalent series resistances of the reactive components and the conduction losses of the switching devices. The switching losses were not considered because they are beyond the focus of this paper, even though a future efficiency analysis would be appropriate to better compare it to other topologies.

Table 4 reports the voltage rating of the devices according to (19)–(22) and (28)–(32), where a value of  $D$  equal to 0.1 was considered as the worst case, considering that under this value, the power load curve quickly reaches zero, as highlighted by Figure 19.

**Table 4.** Voltage rating of devices.

Voltage	Rated Value
$ V_{L1,max}  =  V_{L2,max}  = V_{HV}$	400 V
$V_{C1,max} = V_{C2,max} = V_{LV}/D$	480 V
$V_{MOS1,max} = V_{MOS2,max} = V_{MOS,max} = V_R/D$	480 V

Although power transfer efficiency is an issue beyond the focus of this paper, future developments of the proposed circuit involve improvements in order to guarantee high levels of efficiency, even for the highest voltage and power levels, as required by automotive applications. Capacitor soft-charging capability is possibly needed for this purpose, so that hard switching power losses generally occurring in switching capacitor-based converters can be properly smoothed.

As far as the transistor selection is concerned, a derating factor of half its rated maximum voltage is suggested as a design safety margin. Furthermore, snubber networks are recommended to smooth over voltages due to inductive parasitic elements.

An investigation of switching losses with respect to the switching frequency will be crucial to better evaluate the behavior in real applications, as well as considering emerging technologies in switching semiconductor devices.

## 6. Conclusions

In this paper, a bidirectional DC-DC converter for the management of a storage system is proposed. One of the most important fields in which electrical storage systems are applied is electric mobility.

In the context of an electric vehicle (EV), the on-board power system architecture can include a high-voltage primary source and a low-voltage section, represented by a DC voltage bus or a storage system.

The main goal of this study was to present an innovative bidirectional DC-DC converter interconnecting a 400 V battery and a 48 V DC section. The proposed converter features low electromagnetic emissions due to the series inductors at the input and output sections, thus minimizing current ripples, and low complexity with respect to other high-gain topologies.

Specifically, a non-isolated converter was selected and investigated, in order to avoid the bulky and expensive implications of using a transformer.

After a deep steady-state analysis of the converter, the main electrical waveforms were presented in order to depict the circuit behavior. Design considerations regarding the sizing of reactive components and the current and voltage rating of switching devices were also provided.

The presented simulation results, arising from the software tool PowerSIM, highlight the convenience of the proposed topology in terms of voltage gain with respect to the conventional buck-boost converter, as well as considering the influence of parasitic effects. The results prove the feasibility of an experimental realization, reaching a maximum power level of 30 kW, which is double that reached in the conventional topology.

Furthermore, with respect to other non-isolated converters with higher gain than conventional buck or boost converters, particularly the switched-capacitor converters to which it belongs, the proposed converter provides an optimal trade-off between complexity and electromagnetic emissions, as well as offering the possibility of bidirectional operation.

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