energies

MDPI

Article

Differential Power Processing Converter with an Integrated Transformer and Secondary Switch for Power Generation Optimization of Multiple Photovoltaic Submodules

Ji-Hoon Lim [1], Dong-In Lee [1], Ye-Ji Hyeon [1], Jae-Hyuk Choi [2] and Han-Shin Youn [1,*]

[1] Department of Electrical Engineering, Incheon National University, Incheon 22012, Korea; ljh95606@inu.ac.kr (J.-H.L.); apwn2955@inu.ac.kr (D.-I.L.); iwbffdiw766@inu.ac.kr (Y.-J.H.)
[2] Advanced Electrification Engineering Design Team, Hyundai Motor Company, Hwaseong 18280, Korea; reformjh@hyundai.com
* Correspondence: hsyoun@inu.ac.kr

Abstract: In recent years, to increase the fuel efficiency of environment-friendly vehicles, a large volume of research is ongoing regarding applying photovoltaic (PV) systems. However, in PV systems, a power imbalance between submodules is common due to shading or pollution, and this degrades the power generation efficiency of the system. To solve this problem, various differential power processing (DPP) converters have been developed. In order to adopt the DPP converter to environment-friendly vehicles, the DPP converter must have a small volume, high efficiency, and high price competitiveness. In this regard, we propose a DPP converter with a single multi-winding transformer by integrating multiple transformers and secondary sides of the conventional flyback DPP converter. Since the proposed DPP converter can be applied to battery balancing circuits as well as photovoltaic systems, the proposed circuit is a valuable converter. In the PV system, the maximum output power of each submodule is 60 W, and the total PV system is 240 W by connecting four submodules in series. To verify the validity of the proposed DPP converter, a prototype with 8 V input and 60 W/30 V output specification was built and tested, and the effectiveness of the proposed converter is supported by the experimental results.

Keywords: differential power processing (DPP); flyback converter; integrated transformer; multi-winding; photovoltaic (PV); submodule

Citation: Lim, J.-H.; Lee, D.-I.; Hyeon, Y.-J.; Choi, J.-H.; Youn, H.-S. Differential Power Processing Converter with an Integrated Transformer and Secondary Switch for Power Generation Optimization of Multiple Photovoltaic Submodules. *Energies* **2022**, *15*, 1210. https://doi.org/10.3390/en15031210

Academic Editors: Pedro Roncero-Sanchez, Trung Van Nguyen, João Paulo Carvalho Lustosa da Costa, Caiping Zhang, Kaamran Raahemifar and Roberto Villafafila-Robles

Received: 13 January 2022
Accepted: 3 February 2022
Published: 7 February 2022

1. Introduction

Owing to their ability to improve fuel-efficiency, photovoltaic (PV) systems have been extensively applied in a wide range of environment-friendly vehicles, from Hybrid Electric Vehicles (HEVs) and Electric Vehicles (EVs) to mass-produced ones [1]. In addition, large-capacity PV systems have also been installed on the roofs of electric buses and trucks. In these PV systems, the PV submodules are connected in both series and parallel to generate high voltage and sufficient power. However, due to partial shading and contamination of the PV submodules, variations in power and current occur in the submodules, which, in turn, results in limited output power and small current in submodules. The power generation efficiency, thus, becomes considerably degraded [2]. In the PV system, excessive power dissipation, known as hot spotting, occurs due to cell reverse biasing [3].

To overcome the drawbacks of the PV system, various converters, such as DC optimizer [4,5] and cascaded converters [6,7], have been introduced, which can improve the power generation efficiency and solve the hot spot problem of the PV system. However, since these converters have to handle the rated power of each submodule or total system, other problems, such as bulky volume of the converter and the loss of the entire system creep in [8]. For small volume and low loss of converters, a differential power processing (DPP) converter that can only handle power differences between the submodules was

proposed [9]. These DPP converters have a variety of architectures, such as PV–Bus [10–13], PV–PV [14–16], and PV–isolated port (IP) [17,18]. For the PV–PV converter topology, the bidirectional buck-boost converter is commonly used, and for the PV–IP and PV–Bus converter topology, the bidirectional flyback converter is widely applied as the DPP converter.

The DPP converters with the PV–IP architecture are installed between the PV submodules and the IP to achieve maximum power out of the total system via distributing the excessive power to the low-power submodules and thereby mitigating any current differences between submodules [19]. Figure 1a shows the PV–IP architecture, and Figure 1b shows the circuit diagram when the bidirectional flyback DPP converters are utilized with the PV–IP architecture. Assuming that the number of submodules in the conventional DPP converters are N, then N transformers, N primary and secondary side switches, and 2 N driving circuits are required, and due to these several components, the volume of magnetics and switches also increases.

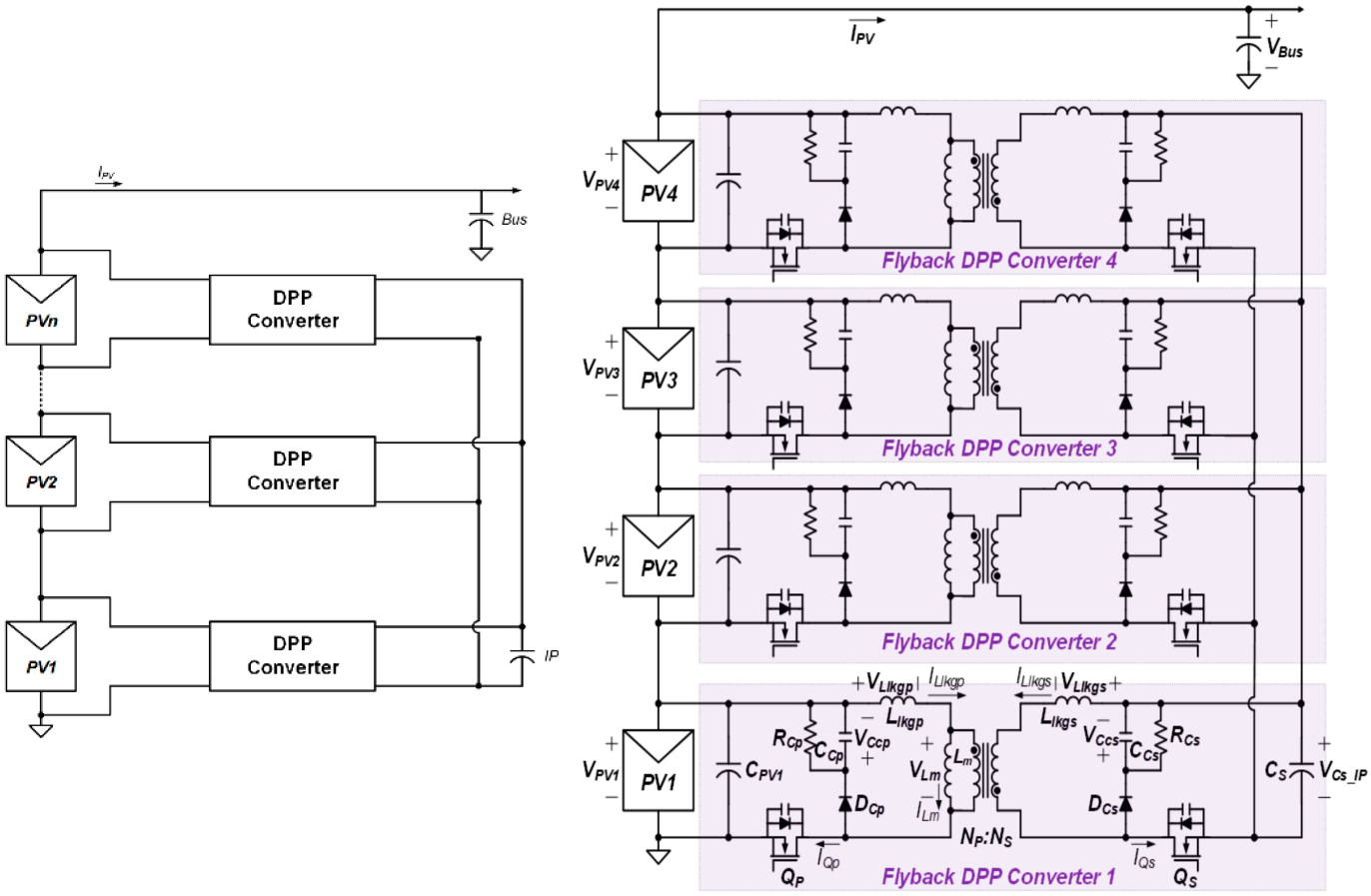

Figure 1. A conventional flyback Differential Power Processing converter (**a**) architecture and (**b**) circuit diagram.

Moreover, assuming that there is an imbalance in the power and energy of submodules in the PV system, since a transformer of the conventional flyback DPP converter stores and transmits imbalanced energy, the magnetizing current of the transformer has an offset that causes a large volume. Thus, conventional DPP converters are difficult to use in applications that require small volume and high price competitiveness, such as environmentally friendly vehicles. To address this issue, the current research aimed to introduce a new DPP converter with a single integrated transformer with PV–IP architecture.

The proposed DPP converter achieved high power density by integrating the transformer and secondary side switches. Thus, the proposed converter can improve the price

competitiveness by reducing components. Moreover, it also improved efficiency by reducing conduction loss and switching loss. In addition, the compensation of power generation imbalance among PV submodules is possible since the imbalanced power is transferred and delivered through the transformer when all primary switches are turned on at the same time. Moreover, the proposed DPP converter can be used as the battery cell balancing circuit because it can equalize the power difference [20].

This paper is organized as follows. In Section 2, the characteristics and operation principle of the proposed DPP converter are explained, and the design method of the proposed DPP converter is presented via Section 3. The effectiveness of the proposed converter is supported by the experimental results with a 8 V input, 60 W and 30 V output prototype.

2. The Proposed DPP Converter

2.1. Characeristics of the Proposed DPP Converter

As shown in Figure 1, a conventional flyback DPP converter has several transformers. However, our proposed DPP converter has a single multi-winding transformer and is illustrated in Figure 2. The proposed DPP converter has the disadvantage of causing breakdown in all converters if a secondary circuit is at fault. However, since components of the proposed converter are considerably reduced compared with the conventional flyback DPP converters, high power density and high price competitiveness can be achieved in the former.

In the proposed DPP converter, the excessive energy induced by high power submodule is stored in the leakage inductor of the integrated transformer, and this energy is transferred to the other submodules through the primary winding and switches. Accordingly, the magnetizing inductor does not store energy but only serves in power transfer. Therefore, the integrated transformer can be designed with zero offset magnetizing current so that the volume of the transformer can be reduced.

Moreover, since all switches are capable of zero voltage switching (ZVS), it is possible to reduce the switching losses too. As a result, the proposed DPP converter not only has a small volume and thus low price but also has high efficiency. Hence, the proposed DPP converter is very suitable for environment-friendly vehicle systems that require high power density for limited space and high price competitiveness for mass production.

2.2. Operation Principle of the Proposed DPP Converter

Figures 3 and 4 illustrate the key waveforms and operational principle of the proposed converter. Furthermore, two PV submodules were configured and the analysis of the proposed DPP converter was performed with respect to six modes.

In addition, the following assumptions are made:

1. Power generation of the *PV1* submodule is greater than that of the *PV2* submodule due to shading and failure of the *PV2* submodule ($P_{PV1} > P_{PV2}$).
2. All leakage inductances of the integrated transformer are equal ($L_{lkg1} = L_{lkg2} = L_{lkgs}$).
3. The capacitance of the secondary side IP port is large enough, and it is assumed to be a voltage source.
4. All transformer windings have the same number of turns (N_{P1}:N_{P2}:N_S = 1:1:1).

As can be seen in Figures 3 and 4, the primary side switches Q_{P1} and Q_{P2} are turned on and off at the same time, and switch Q_S operates opposite to Q_{P1} and Q_{P2}. The operating waveforms in Figure 3 represent leakage inductor voltage $v_{Llkg1}(t)$, $v_{Llkg2}(t)$, magnetizing inductor voltage $v_{Lm}(t)$, leakage inductor current $i_{Llkg1}(t)$, $i_{Llkg2}(t)$, magnetizing inductor current $i_{Lm}(t)$, primary side the switch voltages $v_{QP1}(t)$, $v_{QP2}(t)$, the secondary side switch current $i_{QS}(t)$, and the secondary side switch voltage $v_{QS}(t)$ are shown, and the circuit in Figure 4 consists of the input and output capacitors C_{PV1}, C_{PV2}, and C_S; leakage inductors L_{lkg1}, L_{lkg2}, and L_{lkgs}; snubber resistors R_{C1}, R_{C2}, and R_{CS}; snubber capacitors C_{C1}, C_{C2}, and C_{Cs}; snubber diodes D_{C1}, D_{C2}, and D_{CS}; magnetizing inductor L_m, and 1:1:1 transformers.

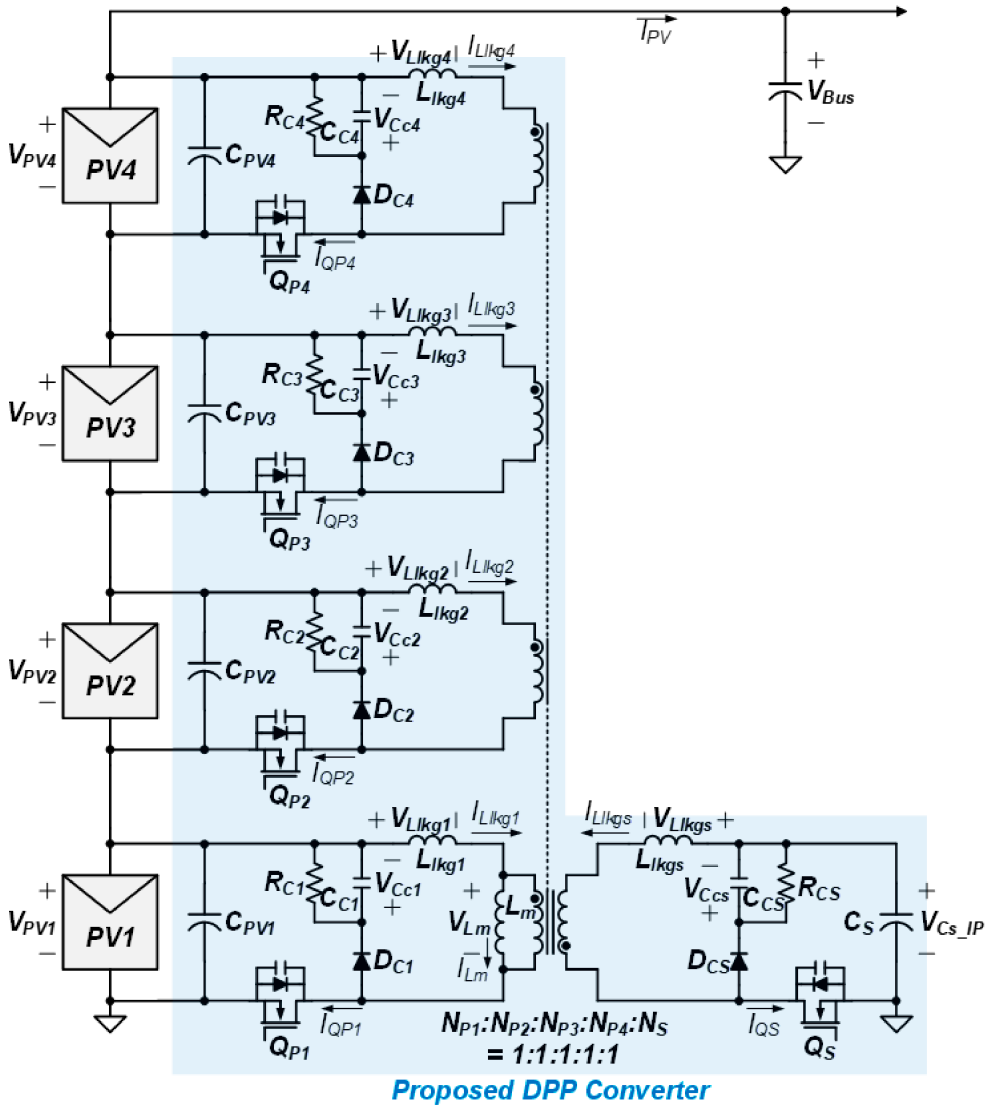

Figure 2. Circuit configuration of the proposed Differential Power Processing converter.

Mode 1 (t_0–t_1): Both Q_{P1} and Q_{P2} remain turned on, and the PV1 voltage ($v_{PV1}(t)$) is greater than the PV2 voltage ($v_{PV2}(t)$) as mentioned in the above assumptions. Therefore, the voltage applied to the L_m ($v_{Lm}(t)$) has a value between $v_{PV1}(t)$ and $v_{PV2}(t)$. As a result, the voltages of L_{lkg1} and L_{lkg2} are as shown below.

$$v_{Llkg1}(t) = v_{PV1}(t) - v_{Lm}(t), \tag{1}$$

$$v_{Llkg2}(t) = v_{PV2}(t) - v_{Lm}(t), \tag{2}$$

From (1) and (2), $i_{Llkg1}(t)$ increases and $i_{Llkg2}(t)$ decreases. For $i_{Llkg2}(t)$, since the transformer windings N_{P1} and N_{P2} are the same, it can be expressed as (3). Therefore, it can be seen that the current of the PV1 submodule flows to the PV2 submodule and $v_{Lm}(t)$ can be obtained using (1)–(3) and represented as (4)

$$i_{Llkg2}(t) = i_{Lm}(t) - i_{Llkg1}(t), \tag{3}$$

$$v_{Lm}(t) = \frac{(v_{PV1}(t) + v_{PV2}(t)) \cdot L_m}{L_{lkg} + 2L_m}, \tag{4}$$

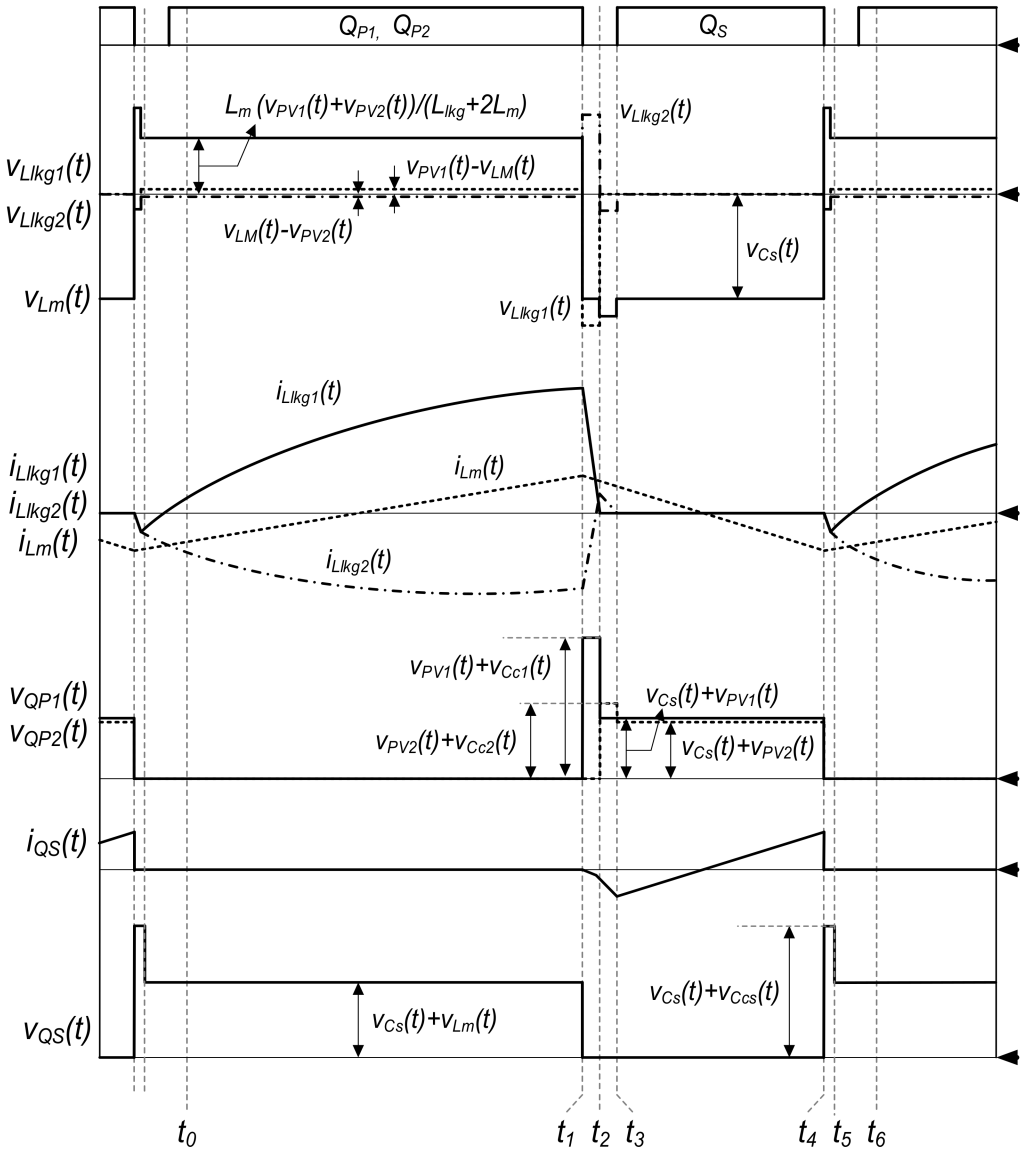

Figure 3. Operational key waveforms of the DPP.

Mode 2 (t_1–t_2): Both Q_{P1} and Q_{P2} are turned off, and the body diodes of Q_{P2} and Q_S conduct. The magnetizing current $i_{Lm}(t)$ decreases when an output voltage $-V_{Cs\_IP}\cdot N_{P1}/N_S$ is applied at the primary side. The energy stored in the leakage inductor L_{lkg1} is consumed through an RCD snubber.

Mode 3 (t_2–t_3): In Mode 2, both Q_{P1} and Q_{P2} maintain a turn-off state, while the primary and secondary sides of the PV2 submodule are commutated to reduce the current flowing through the primary side and increase the current flowing through the secondary. In addition, since the Q_S switch is turned off, the current flowing through the secondary side continues to flow through the body diode. At this time, the energy stored in L_{lkg2} is consumed by the RCD snubber. Since the voltage of the magnetizing inductor is $-V_{Cs\_IP}\cdot N_{P1}/N_S - V_{Llkgs}(t)$, $i_{Lm}(t)$ continues to decrease. Furthermore, the voltage, L_{lkg1} becomes zero, and therefore, i_{Llkg1} also remains zero.

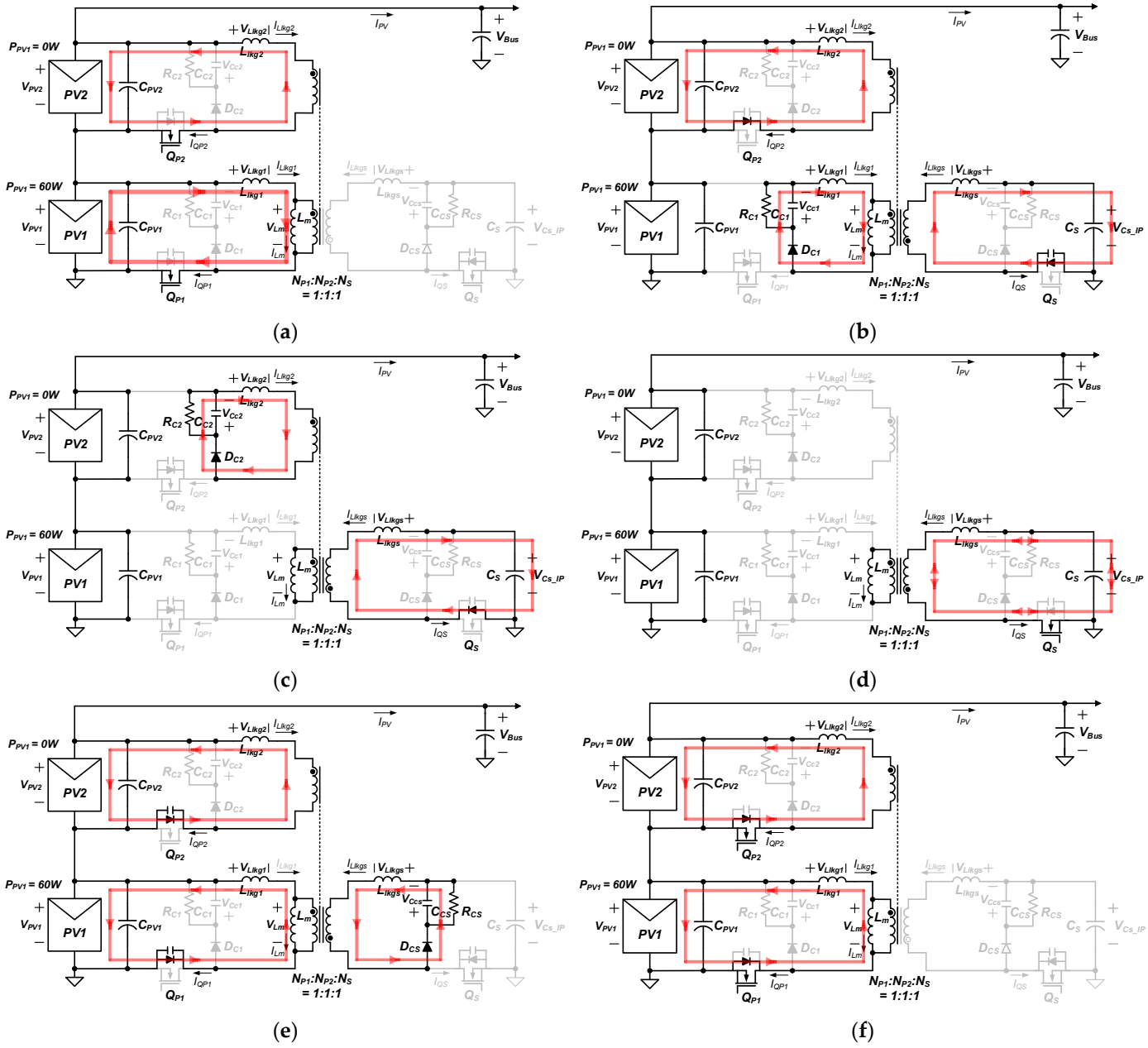

Figure 4. Operational mode of the DPP. (**a**) Mode 1 (t_0–t_1). (**b**) Mode 2 (t_1–t_2). (**c**) Mode 3 (t_2–t_3). (**d**) Mode 4 (t_3–t_4). (**e**) Mode 5 (t_4–t_5). (**f**) Mode 6 (t_5–t_6).

Mode 4 (t_3–t_4): In Mode 2 and Mode 3, ZVS is possible because the secondary side body diode conducted current. For L_m, since $-V_{Cs\_IP} \cdot N_{P1}/N_S$ is reflected, the magnetizing current $i_{Lm}(t)$ decreases from a positive value to a negative value, as shown in Figure 3. At the same time, at the secondary side, both charge and discharge occur, which, in turn, resets the transformer. As a result, the average value of the secondary side current becomes zero, and thus the magnetizing current offset becomes zero.

Mode 5 (t_4–t_5): The Q_S switch is turned off, and the energy stored in the leakage inductance L_{lkgs} is consumed by the RCD snubber resistance. At this time, the leakage inductor current is reflected to the primary side, resulting in commutation on the primary and secondary sides.

Mode 6 (t_5–t_6): It starts when the primary and secondary sides commutation is finished. Since the voltages reflected to L_{lkg1} and L_{lkg2} are the same as (1) and (2), $i_{Llkg1}(t)$ increases

and $i_{Llkg2}(t)$ decreases. In addition, since $i_{Llkg1}(t)$ and $i_{Llkg2}(t)$ are conducting through the switch body diode, ZVS turn-on is performed when both Q_{P1} and Q_{P2} are turned on.

3. Proposed DPP Converter Design Method

3.1. Bus Voltage and IP Port Voltage

The bus voltage of the proposed DPP converter is shown in Figure 2, and the PV submodules are connected in series, so the bus voltage can be represented by (5). The IP port voltage can be expressed as (6) because it is same as the input–output.

$$V_{Bus} \approx 4 \cdot V_{PV,module}, \tag{5}$$

$$V_{Cs\_IP} \approx \frac{n\mathrm{D}}{1-\mathrm{D}} V_{PV,module}, \tag{6}$$

where $n = \mathrm{Ns}/\mathrm{N_P}$ is the turn ratio.

3.2. Primary Side Current of the Proposed DPP Converter

Since the primary side current is same as the switch current, it is proportional to the switch turn-off loss and the RCD snubber loss. Figure 5 shows the equivalent circuit of the primary switch turned-on state when two PV submodules are connected in series. In this equivalent circuit the magnetizing inductor was ignored because the magnetizing inductance is much larger than the leakage inductance. In addition, since the leakage inductance is very small, it is simply shown in Figure 5 considering the wire resistance (R_{wire}) and the switch-on resistance ($R_{ds(on)}$). The PV1 input capacitor voltage $v_{CPV1}(t)$ can be obtained through the equivalent circuit in Figure 5, and it can be expressed by (7) using a Laplace transformation. The voltage $v_{CPV1}(t)$ of the input capacitor can be obtained by the inverse Laplace transform of (7), and this is shown in (8).

$$V_{CPV1}(S) = \frac{V_{CPV1(0)}}{S} + \frac{\frac{1}{SC_{PV1}}}{R_{eq} + SL_{eq} + \frac{1}{SC_{eq}}} \times \left(\frac{V_{CPV2(0)}}{S} - \frac{V_{CPV1(0)}}{S} + L_{lkg2} I_{Llkg2(0)} - I_{Llkg1(0)} \right), \tag{7}$$

$$\begin{aligned} v_{CPV1}(t) = \; & V_{CPV1(0)} + \frac{C_{eq}}{C_{PV1}} \times \left[\left(V_{CPV1(0)} - V_{CPV2(0)} \right) \cdot \left(\frac{e^{-\frac{\omega}{2Q}t} \sin(\omega\beta t + \theta)}{\beta} - 1 \right) \right. \\ & \left. + \left(L_{lkg2} I_{Llkg2(0)} - L_{lkg1} I_{Llkg1(0)} \right) \cdot \left(\frac{\omega}{\beta} e^{-\frac{\omega}{2Q}t} \sin(\omega\beta t) \right) \right], \end{aligned} \tag{8}$$

where R_{eq} is the equivalent resistance of R_{wire} and $R_{ds(on)}$, L_{eq} is the equivalent leakage inductance of L_{lkg1} and L_{lkg2}, and C_{eq} is the equivalent capacitance of C_{PV1} and C_{PV2}, $\omega = 1/\sqrt{L_{eq}C_{eq}}$, $\mathrm{Q} = \sqrt{L_{eq}}/\left(R_{eq}\sqrt{C_{eq}}\right)$, $\beta = \sqrt{1 - 1/(4\mathrm{Q}^2)}$, $\theta = \cos^{-1}(1/(2\mathrm{Q}))$, and $v_{CPV1(0)}$, $v_{CPV2(0)}$, $i_{Llkg1(0)}$, and $i_{Llkg2(0)}$ are the initial values. $i_{Llkg1}(t)$ can be obtained by (9)

$$i_{Llkg1}(t) = -C_{PV1}\frac{dV_{CPV1}(t)}{dt} + I_{PV1,in}, \tag{9}$$

where $I_{PV1,in}$ signifies the input current induced by the PV submodule. It can be seen that, in (9), the leakage inductor current is affected by a small variation in the input capacitor voltage. In addition, since a small voltage is applied to the leakage inductor because of the voltage of the equivalent resistor, the leakage inductor current performs a Quasi-resonance operation. Therefore, due to the Quasi-resonant leakage current, a low leakage current at switch turn-off can be achieved resulting in a low snubber loss and switch turn-off loss.

3.3. Switch Loss and RCD Snubber Loss of Proposed DPP Converter

The root-mean-square (RMS) currents at the primary and secondary sides of the DPP converter are shown in Table 1. The losses of the conventional flyback DPP converter and the proposed DPP converter are shown in Figure 6.

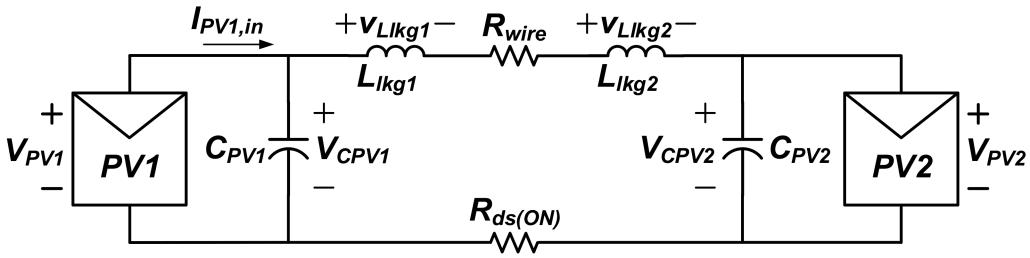

Figure 5. Equivalent circuit for the primary side turned-on state.

Table 1. RMS current of primary and secondary side of DPP converter.

Parameter	Conventional Flyback DPP Converter
I_{P,rms_PV1}	7.78 A
$I_{P,rms\_PV2–4}$	2.73 A
I_{S,rms_PV1}	5.51 A
$I_{S,rms\_PV2–4}$	1.93 A
Parameter	**Proposed DPP Converter**
I_{P,rms_PV1}	8.49 A
$I_{P,rms\_PV2–4}$	2.7 A
$I_{S,rms}$	1.03 A

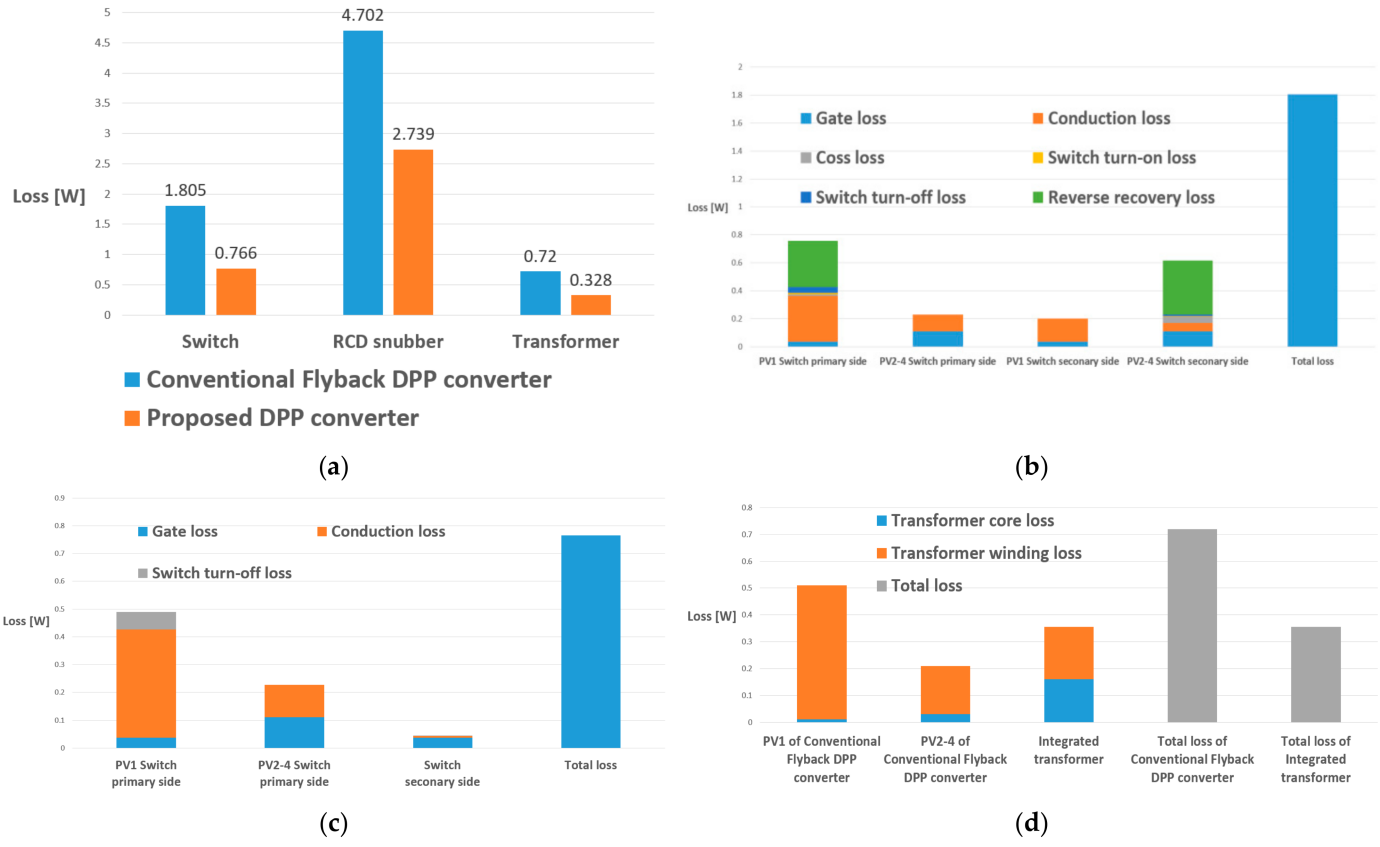

Figure 6. Loss analysis and comparison. (**a**) Switch, RCD snubber and transformer. (**b**) Conventional flyback DPP converter. (**c**) Proposed DPP converter. (**d**) Transformer.

The RCD snubber design should set the RCD snubber capacitor voltage V_{Cc} in consideration of the switch voltage. In the case of the RCD snubber resistance, it can be obtained by (10)

$$\frac{1}{2}L_{lkg} \times i_{Llkg}^2 \times f_s = \frac{V_{Cc}^2}{R_C} \tag{10}$$

As the frequency increaes, V_{Cc} increases, and the switch voltage rating should increase. That is, when desinging an RCD snubber, appropriate frequency selection is required. The proposed DPP converter can be obtained using the equivalent circuit of Figure 5.

The proposed DPP converter reduces the number of switches by integrating the secondary side. In addition, since the entire switch performs a ZVS turn on, as shown in Figures 4 and 7, the switching loss of the proposed DPP converter is decreased. Figure 6 presents a loss analysis diagram and shows that the switching loss of the proposed DPP converter is smaller than that of the conventional flyback DPP converter. The switch loss can be obtained as [21,22]:

$$P_{Q(on)} = 0.5V_{DS} \cdot I_{DS(min)} \cdot t_{on} \cdot f_S + V_{DS} \cdot f_S \times \left(I_{DS(min)} \cdot t_{rr} + Q_{rr} \right), \tag{11}$$

$$P_{Q(off)} = 0.5V_{DS} \cdot I_{DS(max)} \cdot t_{off} \cdot f_S, \tag{12}$$

$$P_{Q,coss} = 0.5C_{OSS} \cdot V_{DS}^2 \cdot f_S, \tag{13}$$

$$P_{Q,cond} = R_{ds(on)} \cdot I_{rms}^2, \tag{14}$$

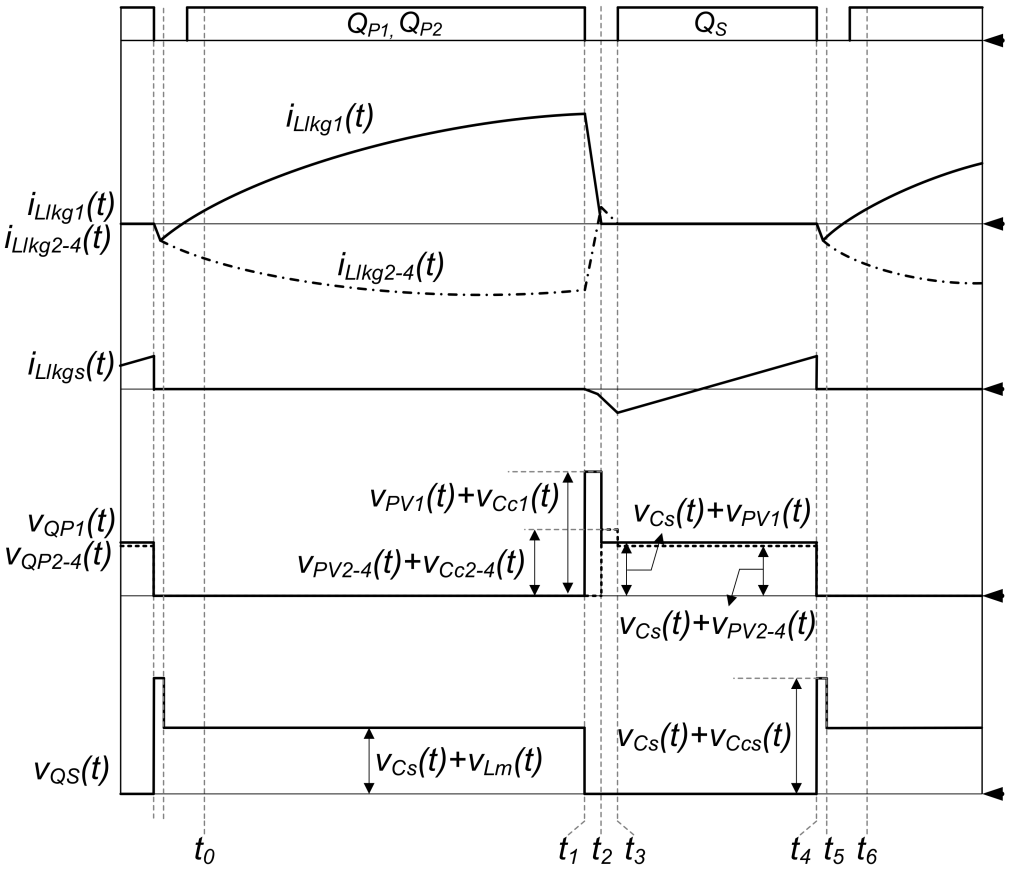

Figure 7. Leakage inductor current and switch voltage waveforms.

For the conventional flyback DPP converter, the leakage inductance is larger than the proposed DPP converter because the number of windings is large. In addition, the RCD snubber loss increases due to large leakage inductance and large number of RCD snubbers.

The RCD snubber loss of the proposed DPP converter is relatively low compared with that of the conventional converter. This is because a low leakage inductance is induced by a low turn-number of the integrated transformer, and a quasi-resonant leakage inductor current induces a small amount of energy in the leakage inductor at the switch turn-off instant.

3.4. Transformer Design and Loss

Table 2 shows the transformer area product (A_P) values of the conventional flyback DPP converter and the proposed DPP converter. Since the transformer in a conventional DPP converter stores energy, a magnetizing current offset occurs. Therefore, the transformer should be designed with high number of transformer windings. As a result, not only would the volume of the transformer be large but also multiple transformers are required. This makes the size of the conventional DPP converter considerably large.

Table 2. Transformer A_P.

Parameter	**Conventional Flyback DPP Converter**
A_P	13,736 mm^4
Total A_P	54,944 mm^4
Parameter	**Proposed DPP Converter**
A_P	24,085.6 mm^4

On the other hand, the proposed DPP converter stores and transmits energy through the leakage inductor. Thus, it is possible to reduce the number of windings by removing the magnetizing current offset and increasing flux variation of the transformer. As a result, despite the multi-winding structure of the integrated transformer, the proposed integrated transformer has a reduced volume of up to 44% of the multiple transformers in the conventional flyback DPP converter. The transformer A_P of the proposed DPP converter can be expressed by (14) considering the number of multi-windings (N_{mw}) on the primary side in the transformer core window area (A_w).

$$A_P = A_e \cdot A_w = \frac{L_m I_{Lm,peak}}{N_P B_m} \cdot \left(\frac{N_{mw} \cdot I_{p,rms} N_P + I_{s,rms} N_s}{K_u J} \right). \quad (15)$$

A conventional flyback DPP converter uses four transformer cores, and even if core loss is small due to low peak-to-peak flux density (ΔB), the number of windings is large; thus, the conduction loss increases. By contrast, the proposed DPP converter comprises only one transformer, and even if the core loss increases due to the high ΔB, the conduction loss decreases, and therefore the transformer loss is lower than that of the conventional flyback DPP converter as shown in Figure 6.

Figure 8 shows the relationship between duty and loss when the magnetizing current is constant. As the duty increases, the conduction loss decreases and core loss increases. In addition, the total loss, which is the sum of the conduction loss and the core loss, becomes the smallest around 0.5 duty. Accordingly, the proposed DPP converter was designed to operate at about 0.5 duty.

In the proposed DPP converter, the volume of the transformer was reduced by removing the magnetizing current offset of the transformer despite the integration of multiple transformers. The number of components and volume of the transformer were also decreased by integrating the secondary side switches. Moreover, since all the switches perform ZVS turn on, the efficiency is improved by reducing the switching loss. Therefore, the proposed DPP converter is a promising converter in regard to its wide range of application, such as a battery cell balancing circuit and PV.

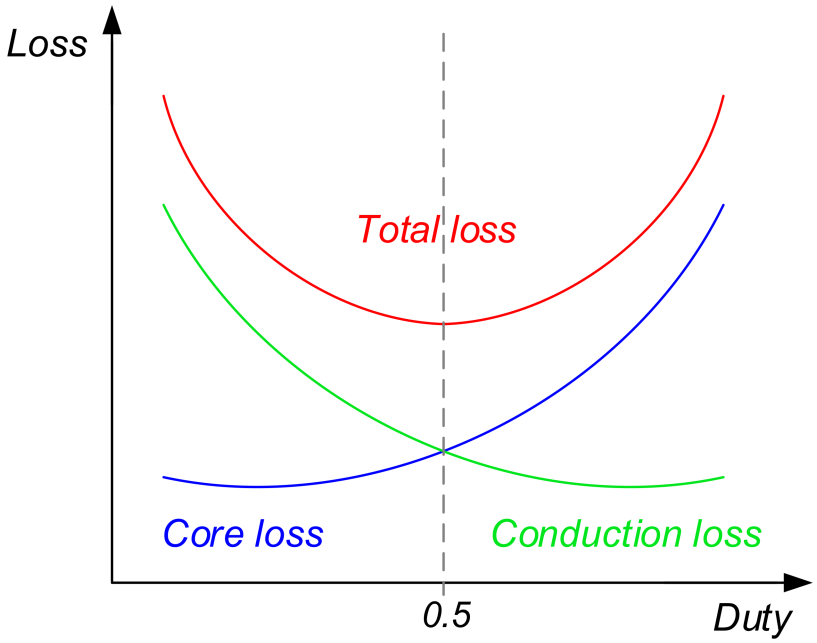

Figure 8. Variation of Loss with duty.

4. Experimental Results

The prototype was tested using power analyzer (WT5000), DC power supply (DSP1500WS), oscilloscope (WaveRunner 8058HD), and electronic load (PRODIGIT 34105A) and used the PV Simulator function of DC power supply.

Figure 9 illustrates a prototype of the proposed DPP converter, and it was built to solve the power imbalance when PV submodules are connected in series. The design specifications of the proposed and conventional flyback DPP converters are represented in Tables 3 and 4. Table 4 represents conventional flyback specification, and since the switching frequency is larger than the proposed DPP converter, the transformer core volume may be designed to be smaller.

The proposed DPP converter was designed at 45 kHz, which further reduced the transformer volume. However, the snubber voltage and snubber loss are proportional to the frequency, and thus the switching frequency must be limited. The proposed converter as designed at 30 kHz to reduce snubber loss. Even if the switching frequency is designed to be 30 kHz, the transformer is small, and thus efficiency and power density can be simultaneously improved.

To verify the performance of the proposed converter, various experiments were conducted considering the worst-case condition as shown in Figure 10. The worst-case condition means that the PV1 submodule generates 60 W power while the other submodules generate 0 W. As a result, the DPP converter absorbs the 45 W surplus power from the PV1 submodule and supplies 15 W power to each submodule to mitigate the power imbalance among submodules.

Figure 11 shoes experimental waveforms of the proposed converter with respect to load variation. As shown in Figure 11, through the proposed DPP converter, the surplus current of the PV1 submodule is injected to other submodules to reduce the power difference. Meanwhile, as presented in Figures 7 and 11, the deviation of the leakage inductor currents of submodules occur.

This is because the leakage inductor of the proposed DPP converter is too small; the small voltage variation in the leakage inductor, resulting from the input capacitor voltage ripple, leads to a large current variation similar to quasi-resonant current. Due to this quasi-resonant current, the switch turn-off current of the proposed converter can be reduced,

which leads to small switching loss and snubber loss. Consequently, the proposed converter is able to provide high efficiency compared with the conventional DPP converter.

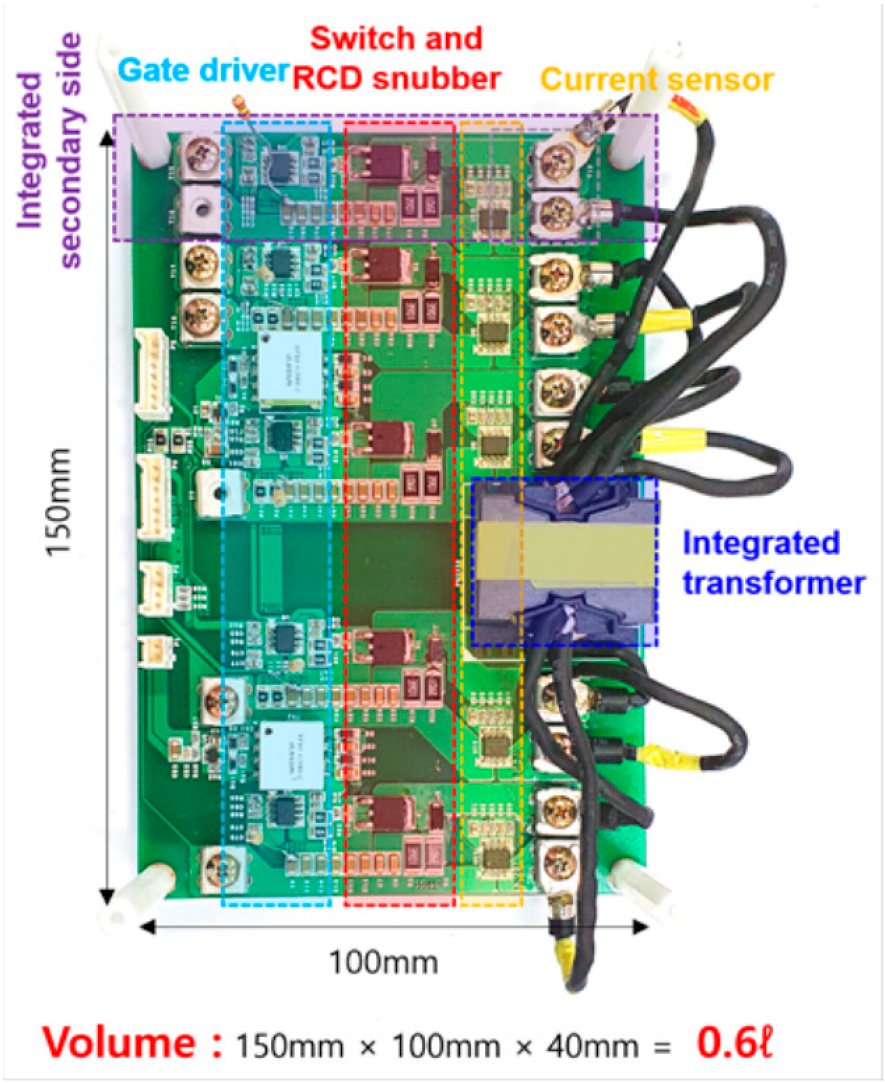

Figure 9. The experimental prototype.

Table 3. Proposed DPP converter parameters.

Parameter	Value
Input voltage	8 V
Output voltage	30 V, 45 W
Switching frequency f_s	30 kHz
Transformer Core	PQ3230
Turn ratio $N_P : N_{Pn} : N_s$	4:4:4
Magnetizing inductance L_m	30 uH
Pri leakage inductance L_{lkgp}	0.42 uH
Sec leakage inductance L_{lkgs}	0.3 uH
Primary winding	0.1 Φ/200 strands
Secondary winding	0.5 Φ
RCD snubber resistance R_C	2 kΩ
RCD snubber Diode	NRVTSA3100ET3G
Switch Q	IPD054N08
Hall Sensor	ACS730KLCLU-30AB-T

Table 4. Conventional flyback DPP converter parameters.

Parameter	Value
Input voltage	8 V
Output voltage	12 V, 45 W
Switching frequency f_s	45 kHz
Transformer Core	PQ3220
Turn ratio $N_P : N_{Pn} : N_s$	6:8
Magnetizing inductance L_m	22.2 uH
Pri leakage inductance L_{lkgp}	0.378 uH
Sec leakage inductance L_{lkgs}	0.669 uH
Primary winding	0.1 Φ/160 strands
Secondary winding	0.1 Φ/120 strands
RCD snubber resistance R_C	1.1 kΩ
Switch Q	IPP057N08N3G

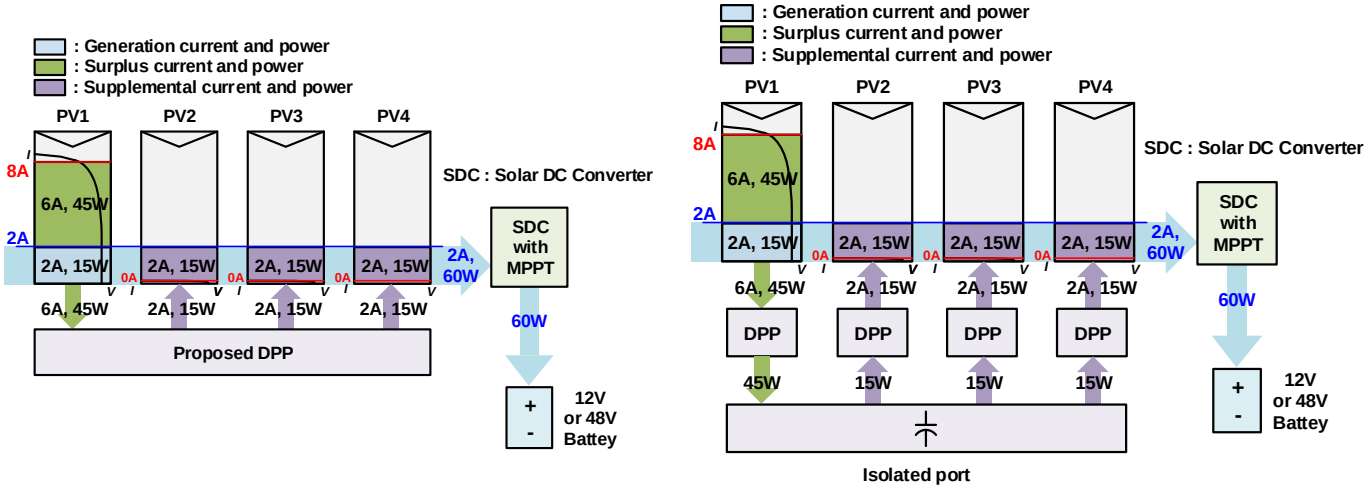

Figure 10. (**a**) Power flowchart of the proposed DPP converter. (**b**) Power flowchart of a conventional flyback DPP converter.

Figure 12 shows the magnetizing current waveform of integrated transformer. As shown in Figure 12, the magnetizing current shows zero offset current due to the current second balance of IP port capacitor, which signifies zero DC bias of the transformer.

Moreover, it is possible to design the integrated transformer with relatively large flux variation inducing low turn numbers compared with the conventional flyback DPP converter. Thus, in spite of primary multi-windings, the integrated transformer significantly reduces the volume of the magnetic components.

Figure 13 presents the ZVS characteristics of the proposed DPP converter under the worst-case conditions. Since the ripple of the magnetizing current is constant and the magnetizing current shows a zero offset, the conduction period of the body diode of the switch reduces as the load increases. Therefore, the 100% load condition is the worst-case condition for the ZVS operation. As represented in Figure 13, we confirmed that the ZVS performed well under full-load conditions, i.e., the worst-case conditions.

Figure 14 presents the voltages of the PV submodules before and after the DPP converter is used. Prior to the operation of the DPP converter, the input voltage was applied only to PV1. However, after complete operation of the DPP converter, the voltages of the PV submodules became balanced since the power difference between the submodules was mitigated.

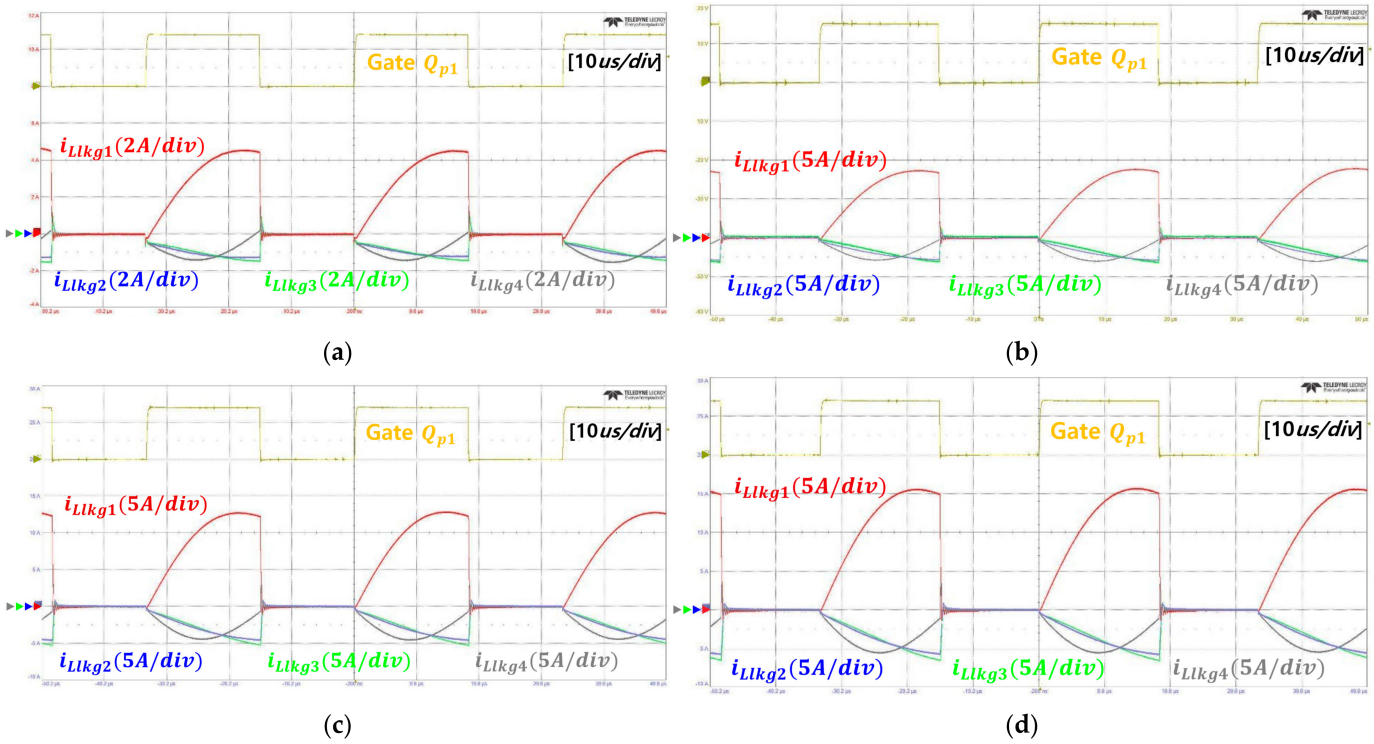

Figure 11. Experimental key waveform at 8 V input, 30 V output. (**a**) 20% load. (**b**) 50% load. (**c**) 80% load. (**d**) 100% load conditions.

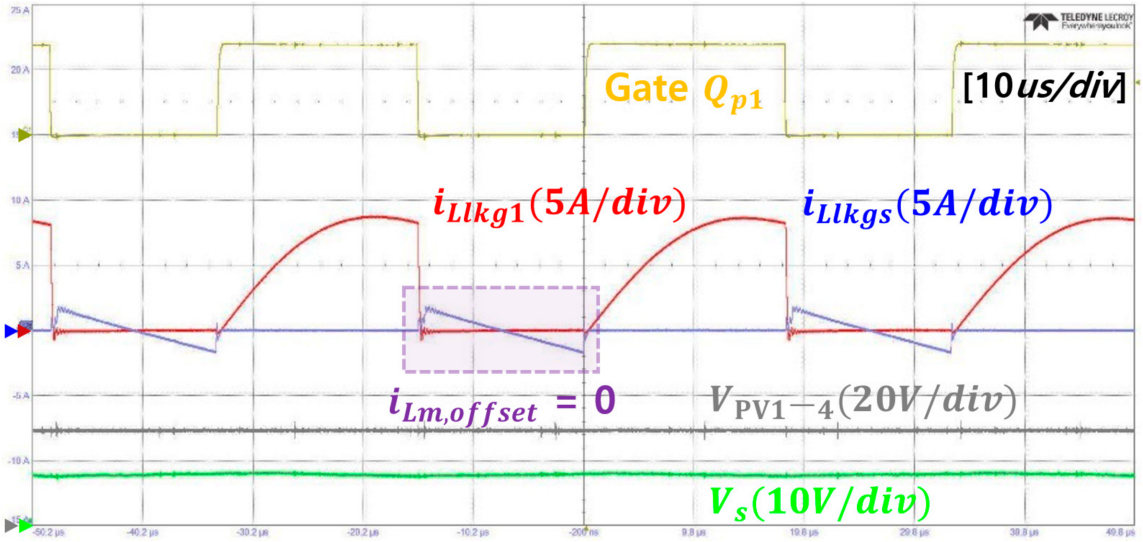

Figure 12. Experimental key waveform of the magnetizing current of an integrated transformer.

Figure 15 shows the key waveform at the soft start-up region that can start the converter without excessive inrush current. It can be seen that the output voltage is charged compared with the proposed DPP converter through soft start up. As a result, it is possible to operate stably.

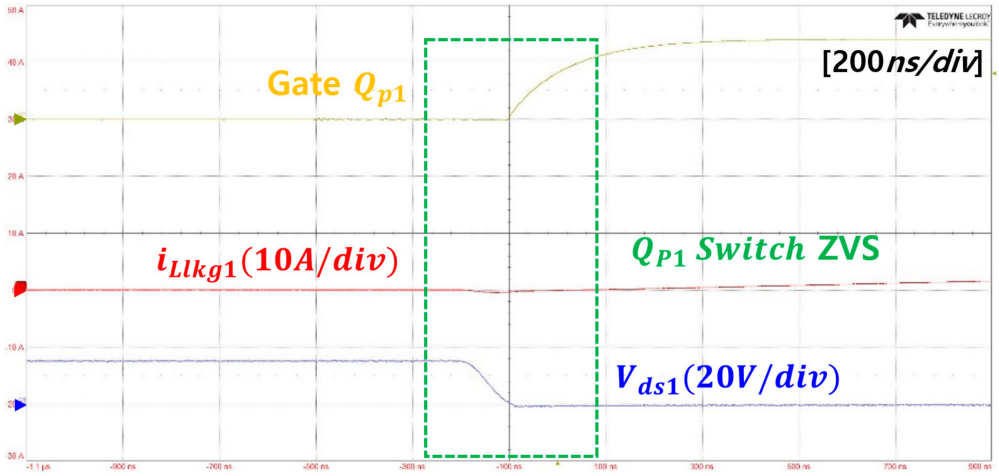

Figure 13. ZVS waveform under 100% load conditions.

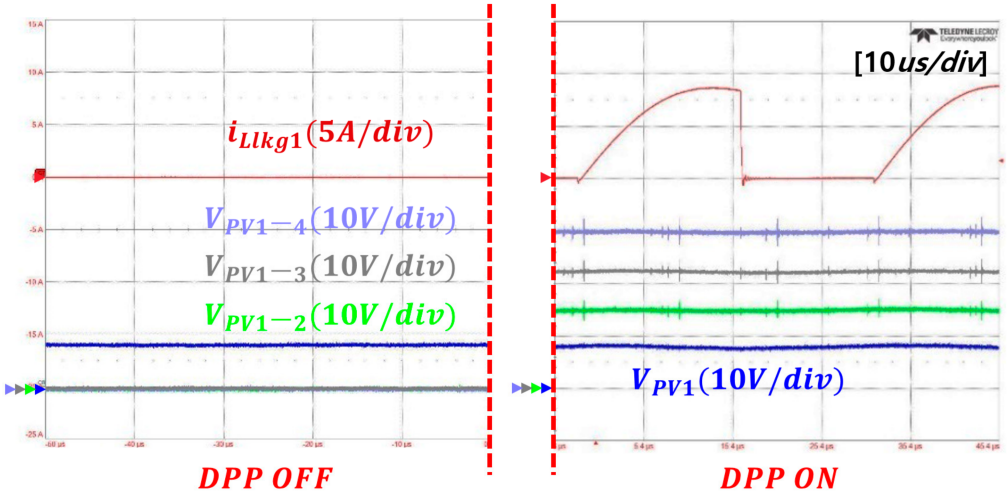

Figure 14. Experimental key waveform of submodule voltage with respect to the DPP operation.

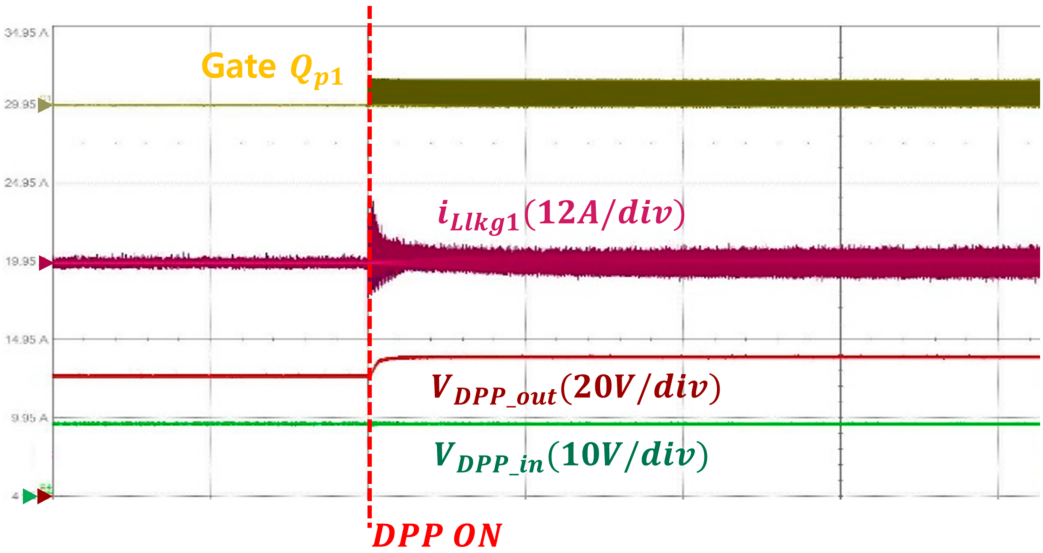

Figure 15. Experimental key waveform of the DPP converter at the soft-start-up region.

Figure 16 shows the load transient waveform. When partial shading occurs in the PV module, the dynamic of proposed converter can be checked.

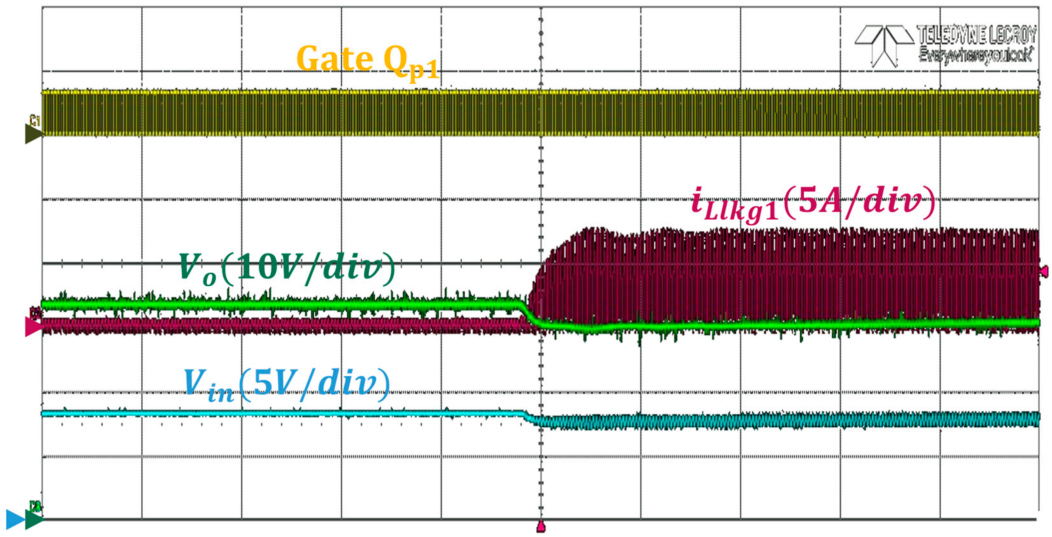

Figure 16. Experimental key waveform of the DPP converter at the load transition.

Figure 17 shows the efficiencies of the proposed DPP converter and the conventional flyback DDP converter. It can be seen that the efficiency of the proposed DPP converter is about 5% higher than that of the conventional converter under entire load conditions. For the proposed DPP converter, more than 93% efficiency under 20–50% load and maximum 93.475% efficiency about 40% load were achieved. Since the proposed DPP converter provides high power density and efficiency, the DPP converter can be applied to various applications with power imbalance, such as a battery equalizer.

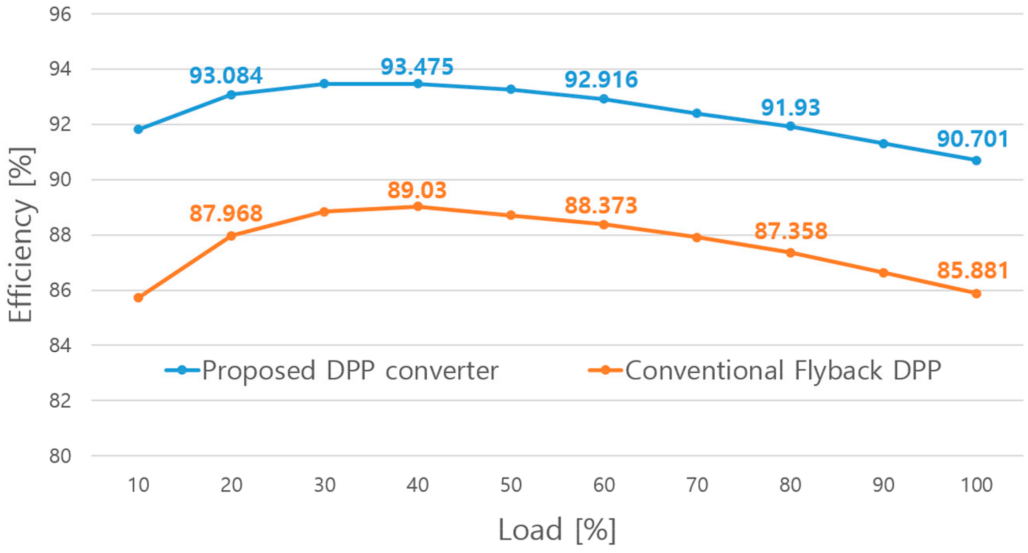

Figure 17. Variation of measured efficiency with a load for 8 V input and 30 V output.

5. Conclusions

The current research developed a DPP converter with single multi-winding transformer by integrating multiple transformers and secondary sides of the conventional flyback DPP converter. The integrated transformer has a reduced volume and can maximize the power density because the magnetizing current offset is removed. Therefore, the proposed DPP converter can decrease both the conduction loss and core loss because of the zero magnetizing current offset and integrated transformer.

In addition, since ZVS is possible, the efficiency can be maximized. Moreover, since the gate signal of the primary side switch is driven by a single PWM signal, the control and driving circuits can be simplified. Therefore, the proposed converter is suiFigure for a DPP converter and can be applicable to battery balancing circuits. In the future, we plan to conduct research that further optimizes the power density eliminating the secondary side and using a planar transformer instead of a PQ core.

Author Contributions: Conceptualization, J.-H.L. and H.-S.Y.; Data curation, J.-H.L., D.-I.L., Y.-J.H. and H.-S.Y.; Formal analysis, J.-H.L., D.-I.L., Y.-J.H. and H.-S.Y.; Project administration, J.-H.C.; Supervision, J.-H.C. and H.-S.Y.; Writin—original draft, J.-H.L. and H.-S.Y.; Writing—review & editing, J.-H.L. and H.-S.Y. All authors have read and agreed to the published version of the manuscript.

Funding: Research Assistance Program (2021) of Incheon National University. National Research Foundation of Korea: NRF-2020R1C1C1010268.

Acknowledgments: This work was supported by Research Assistance Program (2021) of Incheon National University. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (NRF-2020R1C1C1010268).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chmielewski, A.; Szulim, P.; Gregorczyk, M.; Gumiński, R.; Mydłowski, T.; Mączak, J. Model of an electric vehicle powered by a PV cell—A case study. In Proceedings of the 2017 22nd International Conference on Methods and Models in Automation and Robotics (MMAR), Miedzyzdrije, Poland, 28–31 August 2017; pp. 1009–1014.
2. Mäki, A.; Valkealahti, S. Power Losses in Long String and Parallel-Connected Short Strings of Series-Connected Silicon-Based Photovoltaic Modules Due to Partial Shading Conditions. *IEEE Trans. Energy Convers.* **2012**, *27*, 173–183. [CrossRef]
3. Winston, D.P. Efficient Output Power Enhancement and Protection Technique for Hot Spotted Solar Photovoltaic Modules. *IEEE Trans. Device Mater. Rel.* **2019**, *19*, 664–670. [CrossRef]
4. Chen, S.M.; Liang, T.J.; Hu, K.R. Design, analysis, and implementation of solar power optimizer for DC distribution system. *IEEE Trans. Power Electron.* **2013**, *28*, 1764–1772. [CrossRef]
5. Kim, N.; Parkhideh, B. PV-battery series inverter architecture: A solar inverter for seamless battery integration with partial power dc-dc optimizer. *IEEE Trans. Energy Convers.* **2018**, *34*, 478–485. [CrossRef]
6. Walker, G.R.; Sernia, P.C. Cascaded dc-dc converter connection of photovoltaic modules. *Proc. IEEE Power Electron. Spec. Conf.* **2022**, *1*, 24–29.
7. Kashani, M.G.; Mobarrez, M.; Bhattacharya, S. Variable interleaving technique for photovoltaic cascaded DC–DC converters. In Proceedings of the 40th Annu. Conf. IEEE Ind. Electron. Soc. (IECON), Dallas, TX, USA, 29 October–1 November 2014; pp. 5612–5617.
8. Khan, O.; Xiao, W. Review and qualitative analysis of submodule-level distributed power electronic solutions in PV power systems. *Renew. Sustain. Energy Rev.* **2017**, *76*, 516–528. [CrossRef]
9. Olalla, C.; Hasan, M.N.; Deline, C.; Maksimovic, D. Mitigation of hot-spots in photovoltaic systems using distributed power electronics. *Energies* **2018**, *11*, 726. [CrossRef]
10. Kim, K.A.; Shenoy, P.S.; Krein, P.T. Converter Rating Analysis for Photovoltaic Differential Power Processing Systems. *IEEE Trans. Power Electron.* **2015**, *30*, 1987–1997. [CrossRef]
11. Jeong, H.; Cho, H.-T.; Kim, T.; Liu, Y.-C.; Kim, K.A. A scalable unit differential power processing system design for photovoltaic applications. In Proceedings of the IEEE Workshop Control Model Power Electron., Padova, Italy, 25–28 June 2018; pp. 1–8.
12. Sun, K.; Qiu, Z.; Wu, H.; Xing, Y. Evaluation on High-Efficiency Thermoelectric Generation Systems Based on Differential Power Processing. *IEEE Trans. Ind. Electron.* **2018**, *65*, 699–708. [CrossRef]
13. Jeon, Y.-T.; Park, J.-H. Unit-minimum least power point tracking for the optimization of photovoltaic differential power processing systems. *IEEE Trans. Power Electron.* **2019**, *34*, 311–324. [CrossRef]
14. Ye, Z.; Wen, H.; Chu, G.; Li, X. Minimum-power-tracking for PV-PV differential power processing systems. In Proceedings of the 2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA), San Diego, CA, USA, 5–8 November 2017; pp. 696–700.
15. Shenoy, P.S.; Kim, K.A.; Johnson, B.B.; Krein, P.T. Differential power processing for increased energy production and reliability of photovoltaic systems. *IEEE Trans. Power Electron.* **2013**, *28*, 2968–2979. [CrossRef]
16. Qin, S.; Cady, S.T.; Dominguez-Garcia, A.D.; Podgurski, R.C.N.P. A distributed approach to maximum power point tracking for photovoltaic submodule differential power processing. *IEEE Trans. Power Electron.* **2015**, *30*, 2024–2040. [CrossRef]
17. Chu, G.; Wen, H. Design and Optimization of PV-Isolated-Port Photovoltaic Differential Power Porcessing System. In Proceedings of the 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 18–21 December 2018; pp. 1–6.

18. Olalla, C.; Deline, C.; Clement, D.; Levron, Y.; Rodriguez, M.; Maksimovic, D. Performance of power-limited differential power processing architectures in mismatched PV systems. *IEEE Trans. Power Electron.* **2015**, *30*, 618–631. [CrossRef]
19. Jeong, H.; Lee, H.; Liu, Y.C.; Kim, K.A. Review of differential power processing converters techniques for photovoltaic applications. *IEEE Trans. Energy Convers.* **2019**, *34*, 351–360. [CrossRef]
20. Jeon, Y.; Park, J.; Park, J. Differential Power Processing converter with cell balancing operation of multiple photovoltaic module systems. In Proceedings of the 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, 22–26 May 2016; pp. 736–740.
21. Improving Efficiency of Synchronous Rectification by Analysis of the MOSFET Power Loss Mechanism. Available online: https://www.infineon.com/dgdl/Infineon-MOSFET_OptiMOS_improving_efficiency_of_synchronous_rectification_by_analysis_of_the_MOSFET_power_loss_mechanism-AN-v03_00-EN.pdf?fileId=db3a304320d39d590121a671f2d90c38 (accessed on 10 January 2022).
22. Simple Design Techniques for Optimizing Efficiency and Efficiency and Overvoltage Spike of Synchronous Rectification in DC to DC Converters. Available online: https://www.infineon.com/dgdl/Infineon-MOSFET_OptiMOS_simple_design_techniques_for_optimizing_synchronous_rectification-AN-v01_00-EN.pdf?fileId=db3a304328c6bd5c0128da4cf0102cfe (accessed on 10 January 2022).