energies

MDPI

Article

Design and Simulation of a Highly Reliable Modular High-Power Current Source

Qing Zhou [1], Yuelei Xu [1,*], Xin Qi [2] and Zhaoxiang Zhang [1]

[1] Unmanned System Research Institute, Northwestern Polytechnical University, Xi'an 710072, China
[2] The Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China
* Correspondence: xuyuelei@nwpu.edu.cn

Abstract: Currently, modularization, low complexity, and high performance are the three directions that high-power power supplies are gradually moving toward. Under the premise of determining the objective conditions such as operating environment and material technology, a significant task in power supply reliability design is to optimize the power supply's structure, topology, and mode of operation. In this paper, we analyze the reliability design of parallel module redundancy in detail and design the overall structure of the power supply. To further improve the reliability of the power supply, methods for power reliability design at the leg level and component level are proposed. This paper verifies the correctness of the design through simulation and develops a $N + 1$ modular redundant power supply according to the design scheme. The simulation experiment verifies the consistency of the design scheme and parameters.

Keywords: reliability; $N + 1$ modular power supply; redundancy; phase-shifted full bridge

Citation: Zhou, Q.; Xu, Y.; Qi, X.; Zhang, Z. Design and Simulation of a Highly Reliable Modular High-Power Current Source. *Energies* **2022**, *15*, 8593. https://doi.org/10.3390/en15228593

Academic Editors: Ričardas Krikštolaitis and Linas Martišauskas

Received: 16 September 2022
Accepted: 3 November 2022
Published: 16 November 2022

1. Introduction

The concept of reliability originated in the aviation field. In the 1950s, reliability engineering emerged and developed in the US military. People began to develop a series of military standards for reliability. In the 1960s, the results of reliability research began to be applied to the civilian industry. Based on this, reliability knowledge gradually formed a somewhat complete theoretical system. Reliability theory can directly affect the quality and cost of products, and indirectly influence the service quality delivered through those products [1–3].

Highly reliable power supplies play an increasingly important role in applications such as telecommunication power supplies [4], electric aircraft [5–7], large-scale scientific facilities, high-tier data centers, hospitals, etc. [8–10]. In these applications, the continuity of power supply is critical [11]. However, field experience showed that power devices, such as insulated-gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs), are vulnerable to failure [12,13].

One of the most significant approaches to boosting system reliability is fault-tolerant techniques. To increase the continuity of the power supply, many fault-tolerant methods have been introduced [14–16]. The fault-tolerant solutions usually employ hardware redundancy [17,18]. Reference [13] presents a comprehensive review of fault tolerance methods for power electronic converters when power devices fail. The authors summarize four types of fault-tolerant solutions of hardware redundancy and classify them as system level, module level, leg level, and switch level. First, system-level redundancy at least doubles the system cost, while the cost of paralleled power modules operating in $N + 1$ mode only increases by $1/(N + 1)$. The leg level and switch level generally have two types of faults: open circuit failure (OC) and short circuit failure (SC). Refs. [16,19] introduced a topology that configures the full-bridge structure into a half-bridge structure. Nevertheless, it is required that the fault type of the switches is SC fault and other switches on the same

bridge must keep open. Ref. [20] proposed a fault-tolerant direct current (DC)-DC converter derived from a resonant converter. The switch's failure type is also an SC fault. However, the probability of an OC is fault not less than that of an SC fault, so both faults should be considered, which adds complexity to the hardware solution and operation mode, and is not conducive to the reliability of the power supply. Once the power module fails (whether it is an OC or an SC of components), the module or system generally ends up as an OC because of the protection mechanism. In summary, the module level has more advantages in redundancy and fault tolerance.

At the leg level and switch/component level (we use component level in this article), we can focus on the optimization of design and component selection rather than fault tolerance due to the above analysis. Circuit failures are mostly caused by damaged components. The reliability of components is related to the component's temperature, voltage (power stress), quality and environmental conditions, etc. It is difficult to improve the reliability of the components by improving the manufacturing technology or environmental conditions for technically mature and quality-qualified components. Temperature is relatively easy to reduce through pertinency design. For electronic components, reliability is a function of temperature, and they are positively correlated. The reliability and lifetime of a transistor directly depend on its operation temperature [21,22]. Wang proposed in [23] that the transistors have the highest failure rate in power electronic converters due to temperature fluctuations. They found that during the operation of the IGBT, the heat generated by the semiconductor power loss will be transmitted to the heat sink to produce junction temperature fluctuations, causing the bond wire to generate shear stress at its welding point, and the changing stress produces cracks that cause the bond wires to fall off. In the design process of the power module, special attention should be paid to devices with high power and high heat. Devices with low reliability are often high-power devices, such as transistors, inductors, capacitors, and sampling resistors. Because the transistor is the core device of current conversion and the structure is complex, it not only has high power but also low reliability. To reduce the heat of the transistors, the buck circuit of the SLAC National Accelerator Laboratory power system is designed with two bridge arms that work alternately to reduce the switching frequency by half, and MOSFETs are used to replace the freewheeling diode to obtain a smaller resistance [24,25]. Therefore, at the leg level and component level, we can reduce the operating temperature of the power supply through methods such as topology design, derating design, and operation strategy [26].

At the module level, the redundant structure of $N + 1$ modules can significantly improve the reliability of the power supply [27], while it is also important to improve the reliability of each parallel module. The design and operation strategy at the leg level and component level are important factors [28].

In this article, we have conducted a comprehensive analysis of the reliability design of high-power current sources. We propose a set of methods for power reliability design at the module level, leg level, and component level. The new approaches in this paper are as follows:

(1) At the module level, we proposed the most favorable form and the operation strategy of module redundancy for power supply reliability, and provided an analysis method to determine the optimal number of parallel modules;
(2) At the leg level, we reduced the power consumption and temperature of the transistors by utilizing the zero voltage switching (ZVS) characteristics of the PSFB topology;
(3) At the component level, we reduce the power consumption and temperature of the components through derating design. We calculated the design parameters of the components and set aside margins when selecting the components.

In Section 2.1, we analyze and compare three forms of power redundancy, and choose the optimal form and the optimal number of modules. Then we show the of design the overall structure of the power supply and the topology of each module. In Sections 2.2 and 2.3, we propose reliability design methods at the leg level and component level of the power supply respectively. In Section 2.4, we point out the effectiveness of the

power supply reliability design and some reliability weaknesses through the analysis of the power consumption of key components of the power supply. In Section 3, we simulate the power redundancy strategy and the design of key parts, and we also verify the correctness of the design parameters. The conclusions of this paper are summarized in Section 4.

2. Design of the Highly Reliable Current Source

2.1. Selection of Redundancy Forms and Design of Fault Tolerance Mechanisms at the Module Level

2.1.1. Selection of Redundancy Forms

Module redundancy can significantly improve the reliability of the power supply. The first thing we need to determine is the form of redundancy. Redundancy can be designed in three forms: series redundancy, parallel redundancy, and hot spare [29], as shown in Figure 1. We will analyze the reliability advantages of the form of redundancy we chose and the fault-tolerant approach we designed.

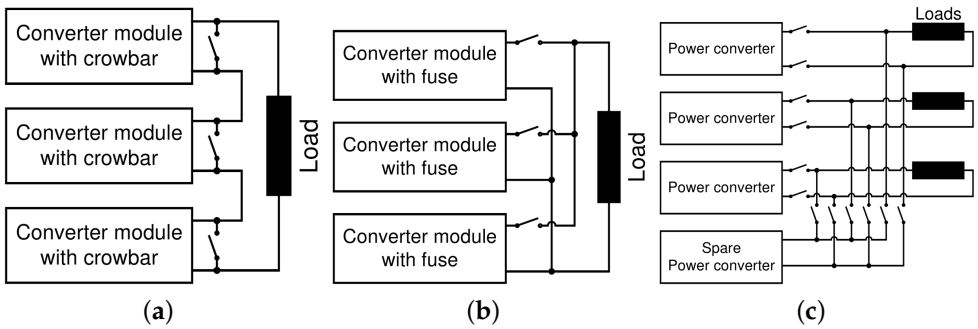


Figure 1. Redundant structure of the power supply. (**a**) Series redundancy diagram. (**b**) Parallel redundancy diagram. (**c**) Hot spare diagram.

We know that the power module in Figure 1a is a voltage source and the power module in Figure 1b is a current source because voltage sources are not allowed in parallel and current sources are not allowed in series. Additionally, the failure of the module is almost always OC as described earlier. When a module in Figure 1a fails, the crowbar must be used to short-circuit the module, while in Figure 1b, when a module fails, there is no need to deal with the module (in the case of an SC, the fuse is burned, and the module is still OC). The crowbar structure in Figure 1a will introduce additional risks to the reliable operation of the power supply. Moreover, each module in Figure 1a outputs 1/3 the voltage, and each module in Figure 1b outputs 1/3 the current. The transistors usually have a far greater ability to bear voltage than to bear current, so it is more reasonable for all modules to share the current in the design of high-power power supplies. For Figure 1c, which is called hot spare, when a module fails, the switching control of the backup module is difficult. Additionally, the backup module needs to be connected to every power supply module, so the circuit is complicated. When designing for power availability, we should simplify the circuit rather than increase the complexity. Moreover, when the backup module is switched, the output voltage or output current of the power supply fluctuates greatly, which also affects the reliability of the power supply. Therefore, Figure 1b's redundant structure has more advantages in reliability. The operation mode is that each module runs below the rated current. When one module fails (OC), the remaining modules increase the current, work at the rated power, and the total output returns to the state before the failure. Each module operates with derating, resulting in lower power consumption, lower temperature, and higher reliability.

2.1.2. Determination of the Number of Modules

The choice of how many modules to connect in parallel is based first on the needs of the actual situation. We analyze the optimal number of modules from three factors, reliability of power modules, current fluctuations after failure, and cost. Mean time between

failures (MTBF) was chosen as the evaluation parameter for reliability. The formula for calculating the reliability of the $N + 1$ system is as follows [30].

$$MTBF_{N+1} = \frac{t}{1 - [(N+1)e^{-\frac{N^2}{N+1}\lambda_r t} - Ne^{-N\lambda_r t}]} \quad (1)$$

where N is the number of modules and λ_r is the failure rate of each power module working at rated power. The equation shows that the $MTBF$ of the $N + 1$ system is a decreasing value over time, unlike most products which are constant. Additionally, since the power supply system is repairable, we assume that the reliability of the power supply is approximately restored to its highest level after each repair, so the $MTBF$ of the $N + 1$ system decreases periodically. We assume that the power supply system is repaired in the 12th month of each year, then the $MTBF$ of the power supply system reaches the minimum value at the end of the 11th month, and we take this value, so t = 8016 h. We have surveyed the products of our partner power supply manufacturers and found that the $MTBF$ of power supply modules is mostly between 1 year and 10 years. To simplify the calculation, we set $MTBF_{\text{mod}} = 10^4$ h and $MTBF_{\text{mod}} = 10^5$ h to approximately represent the number of hours of 1 year and 10 years, respectively. The corresponding module failure rates $\lambda_r = 1/MTBF$ are 10^{-4} h and 10^{-5} h, respectively. We get the Table 1.

From Table 1, we know that when $MTBF_{\text{mod}} = 10^4$ h, the lowest $MTBF$ of the 4 + 1 power supply is higher than the $MTBF$ of a single module; when $MTBF_{\text{mod}} = 10^5$ h, the lowest $MTBF$ of the 6 + 1 power supply is higher than the $MTBF$ of a single module. and the higher the $MTBF$ of a single module, the more obvious the reliability advantage of the $N + 1$ power supply. For the current fluctuation after the fault, if the power supply is in the form of a hot spare, the delay time for the standby module to replace the faulty module is long, so the current usually fluctuates around $1/N + 1$ [31]. If the redundant form of Figure 1b is used, due to the freewheeling capability of the inductor in the power supply, the current fluctuation range after a module fault will not exceed $I/(N + 1)$ (where I is the rated current), which is also an advantage of this structure. The current fluctuation is usually in the range of (0.2 0.6)$I/(N + 1)$ [15,32,33]. In this paper, we choose $0.4I/(N + 1)$. Regarding the cost, in order to simplify the calculation, we set the cost of the power supply without redundancy as C, and the cost of $N + 1$ power supply increases by at least C/N. To display the curves of the three variables in the same coordinate, we normalized the variables, as shown in Figure 2.

We hope that the current fluctuation and the proportion of additional costs are small and the MTBF is large. In Figure 2, when the number of power modules is 2 + 1, 3 + 1, and 4 + 1, the curvature of the three curves is large. That is to say, the power supply obtains the best cost performance in this interval. Therefore, the 3 + 1 or 4 + 1 form is more reasonable. In this paper, we choose four power modules, that is, the 3 + 1 form.

We use a backplane to connect four identical power modules in parallel. The power control circuit is arranged in the control box, and the control box uses a metal layer to shield the signal interference of the power module. The block diagram of the power supply design is shown in Figure 3.

Table 1. Derating design parameters of key components.

$N + 1$	Module	1 + 1	2 + 1	3 + 1	4 + 1	5 + 1	6 + 1	7 + 1	8 + 1	9 + 1	10 + 1
$MTBF$	10^4	7.4×10^4	2.1×10^4	1.3×10^4	1.0×10^4	9.1×10^3	8.6×10^3	8.3×10^3	8.2×10^3	8.1×10^3	8.1×10^3
(h)	10^5	5.2×10^6	1.0×10^6	4.2×10^5	2.4×10^5	1.5×10^5	1.1×10^5	8.2×10^4	6.4×10^4	5.3×10^4	4.5×10^4

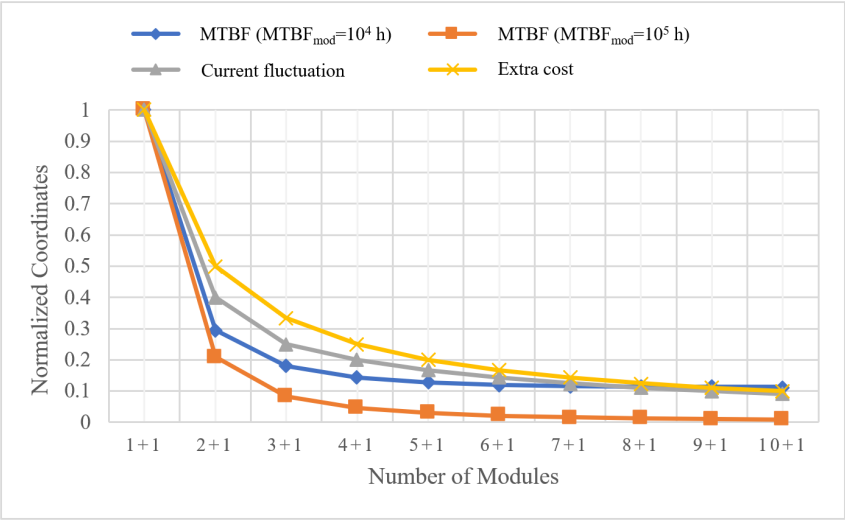


Figure 2. Trend curves of MTBF, current fluctuation, and extra cost with an increasing number of power modules.

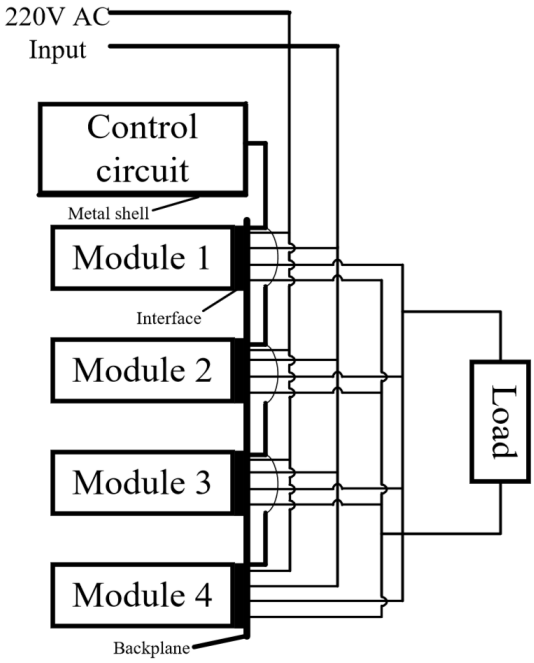


Figure 3. Power supply block diagram.

2.1.3. Main Parameters and Topology of the Module

After we determine the form of redundancy, we need to design the topology of each module of the current source. We added a power factor correction (PFC) structure to the front part of the power supply, not only to improve the power factor of the power supply but also to reduce the pollution of the power supply to the grid. The object of our research is high-power current sources, so we tried our best to make the power of the prototype as high as possible, each module was designed to 1000 W. At the output side, we use a transformer to achieve step-down and isolation to get a low-voltage, high-current output, which is very important for the safety of the experimenters. On the main side of the transformer, we need to design an H-bridge to change DC to alternating current (AC) so that the power can be transferred through the transformer. This also prepares the ground for the realization of ZVS. The main system parameters of the module are shown in Table 2.

Table 2. The main system parameters of the module.

Power	Input Voltage	Output Voltage	Output Current	DC Bus Voltage
1000 W	220 V AC	50 V	20 A	390 V DC

The topology of the power module is shown in Figure 4.

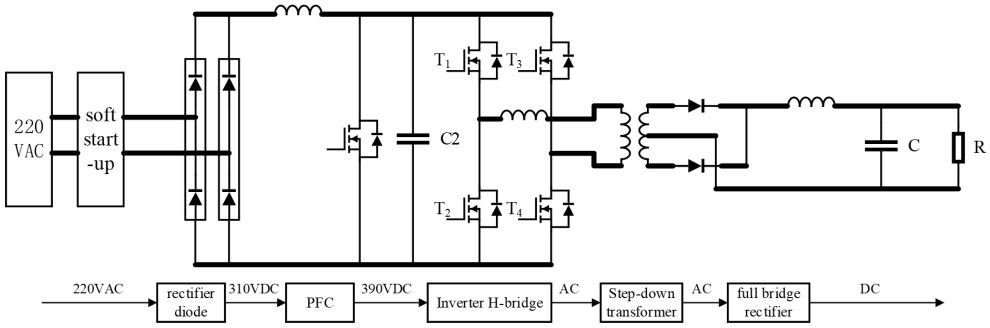


Figure 4. The topology of the power module.

The power supply mainly includes two parts: power factor correction (PFC) and DC/DC. A PFC circuit is added before the converter. The power factor and power of the power supply can be improved. First, 220 V AC is rectified and filtered into about 310 V DC voltage, and then boosted to about 390 V by PFC BOOST. The DC/DC section contains inversion and rectification. The 390 V voltage is inverted by the H-bridge. After inversion, the transformer is used to step down and boost the current. The transformer also plays the role of isolating the high voltage to ensure the safety of the operator. Finally, full-wave rectification is performed to output 50 V/20 A DC power. The module power is designed to be 1000 W.

2.2. Design of PSFB Topology at the Leg Level

The reliability model of each power module is a series model (that is, if any one device is damaged, the power supply will fail). As mentioned above, when objective conditions such as environment and manufacturing process are determined, temperature is the factor that most affects the reliability of electronic devices. The reliability of electronic devices is a function of temperature, and the two are inversely related. Usually, high-frequency devices consume more power, such as transistors, sampling resistors, diodes, high-frequency inductors, and capacitors. The heat generated by power consumption will cause the temperature of the device to rise, and the failure rate of electronic components such as switches and inductors will be greatly increased at high temperatures. Among all the components, the transistors have the highest manufacturing complexity and the lowest reliability. Therefore, besides cooling, it is necessary to reduce the loss of the transistors as much as possible. In this paper, we use PSFB to realize ZVS [34], which can greatly reduce the temperature of transistors operation. The circuit is shown in Figure 5a. Q1–Q4 are transistors, C1–C4 are capacitors, Lr is the resonant inductor (including the leakage inductance of the high-frequency transformer), the capacitor Cd is the blocking capacitor, and T is the high-frequency transformer. Using the junction capacitance of the power components and the leakage inductance of the transformer as the resonant element, the resonance is realized in the dead time, so that the four transistors of the H-bridge are turned on and closed at zero voltage in turn to achieve ZVS. The ZVS of the leading leg is affected by output filter inductance and transformer leakage, while the lagging leg is affected by leakage inductance. There are 12 operating modes of PSFB during a complete operating cycle, as shown in Figure 5b. The positive and negative half-cycles are symmetrical to each other, and each has six operating modes, including two freewheeling processes and four resonance processes. U_{ab} is the voltage difference at the midpoint of the two legs, i_p is the

current at the primary side of the transformer, and U_{rect} is the voltage at the cathode of the rectifier diodes.

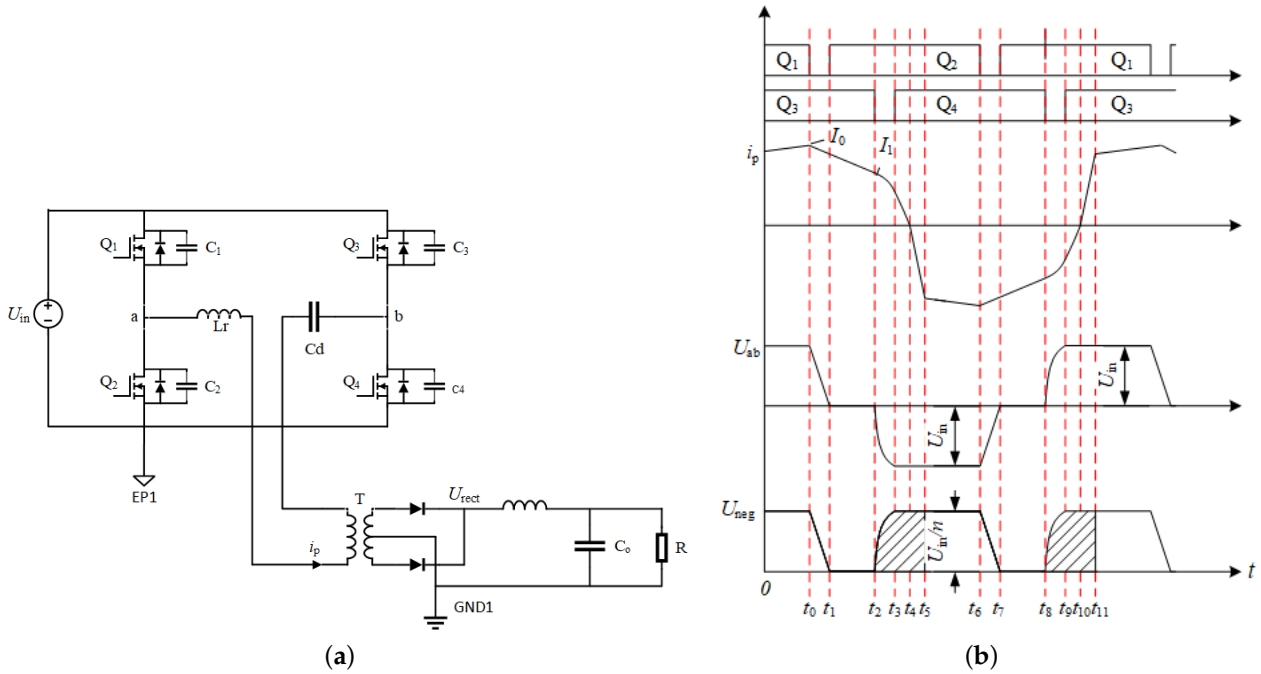


Figure 5. Circuit of the phase-shifted full bridge. (**a**) Circuit of PSFB; (**b**) the 12 operating modes of PSFB.

The output terminals A/B and C/D can drive the two legs of Q1/Q2 and Q3/Q4, respectively, and the two legs can independently set the dead time. All pulse width modulation (PWM) duty cycles are close to 50%. When the Q1 and Q4 transistors are turned on at the same time, the current is positive; when the Q2 and Q3 transistors are turned on at the same time, the current is negative. A freely adjustable dead time is set before each output stage. When the Q1 and Q4 transistors cannot be turned on at the same time, the forward current is cut off. Before turning on Q3, due to the dead time setting, the leakage inductance current will continue to flow in the direction of Q2→Q3, which is also the process of C2 and C3 discharging, so that the voltage of Q2 and Q3 transistors sequentially drops to 0, creating conditions for ZVS. The waveform of the control signal of PSFB is shown in Figure 6.

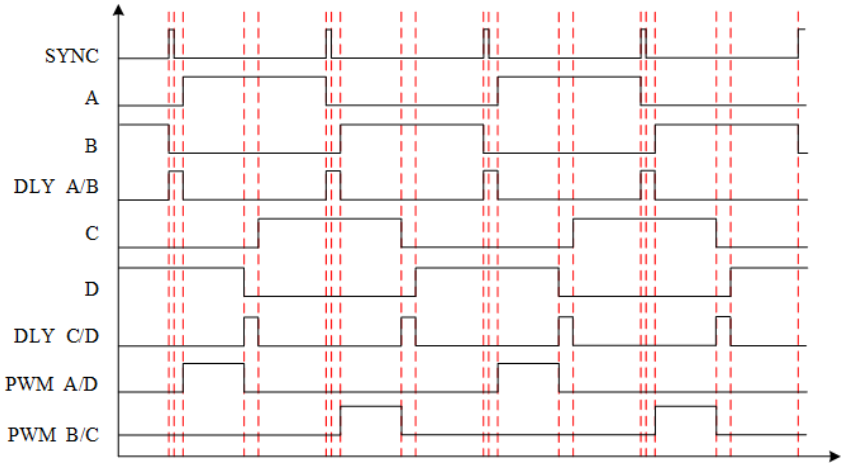


Figure 6. Waveform of the control signal of PSFB.

Correct setting of dead time is a necessary condition for the transistor to achieve zero voltage turn-on. The ZVS of the leading leg is determined by the output filter capacitor and transformer leakage inductance, while the lagging leg is determined only by the leakage inductance. The leakage inductance energy is usually small. If its energy is not enough to help the output capacitor of the lagging leg discharge completely, and the primary current reverses in advance, a hard switching phenomenon will occur, and an auxiliary circuit design is required for this. The delay time is

$$T_{delay1} = \frac{2C_{lead}U_{dc}}{I_P(t_0)} \approx \frac{2C_{lead}U_{dc}}{I_{Pm}} = \frac{2C_{lead}U_{dc}}{\sqrt{2}\frac{P}{U_{dc}}} = \frac{2 \times 470 \times 10^{-12} \times 390}{\sqrt{2} \times \frac{100}{390}} = 0.10\ \mu s \quad (2)$$

where $I_P(t_0)$ is the current value of the first working mode. Dead time is set by adjusting the resistance value of R_{delay} connected to Pin 15 and Pin 7. In this circuit, take R_{elay} = 5.1 KΩ, then

$$T_{delay} = \frac{62.5 \times 10^{-12}}{I_{delay}} = \frac{62.5 \times 10^{-12} \cdot R_{delay}}{V_{delay}} \approx 0.12\ \mu s \approx 0.10\ \mu s \quad (3)$$

This value meets the design requirements. The selected MOSFETS is IRFP460, the turn-off time is 45 ns, and the dead time can ensure the reliable turn-off of MOSFETS. In this paper, L1 = 22 μH is set by simulation.

2.3. Derating Design at the Component Level

At the component level, we mainly achieve reliability improvement through derating design. The 3 + 1 power supply works at 3/4 of the rated power. When one of the modules fails, the other three modules automatically work at the rated power. In the design process of the power module, special attention should be paid to the components with high power and high heat generation, and the derating design should be carried out for the components with low reliability. Usually, these components are transistors, high-frequency inductors, capacitors, sampling resistors, etc.

(1) Transistor parameters

Assuming that the PFC output voltage fluctuates by 5%, the maximum reverse voltage that the power semiconductor switch can withstand is 390 × 1.05 = 409.5 V. Its peak current is:

$$I_{peak(\max)} = \frac{\sqrt{2}P}{U_{dc(\min)}} = \frac{\sqrt{2} \times 1000}{390 \times (1 - 0.05)} = 3.86\ \text{A} \quad (4)$$

(2) High frequency transformer parameters

The power capacity of the 1000 W, 50 kHz switching power supply is designed as

$$Ap = \frac{P_T \times 10^4}{4fB_mJK_0} = \frac{P\left(\frac{1}{\eta} + \sqrt{2}\right) \times 10^4}{4fB_mJK_0} = \frac{1000 \times (\frac{1}{0.95} + \sqrt{2}) \times 10^4}{4 \times 50\,\text{kHz} \times 0.12 \times 350 \times 0.4} = 7.34\,(\text{cm})^4 \quad (5)$$

where P_T is the apparent power of the transformer, for a full-wave structure transformer, there is $P_T = P(1 + 1/\eta)$ (P is the input power of the transformer, η is the working efficiency of the transformer, take 0.95); f is the switching frequency; B_m is magnetic induction, to prevent core saturation, the value should be lower than 1/3 of the maximum value of the hysteresis loop. Take 0.12 T here. J is the current density on the wire, generally not more than 600 A/cm^2. Take 350 A/cm^2 here. K_0 is the window usage coefficient, which is related to the wire diameter and the number of windings, and the typical value is 0.4.

We choose ferrite core EE65, the cross-sectional area of its central column is A_e = 5 cm^2, the window area is A_Q = 4.83 cm^2, and its capacity is $A_e \times A_Q$ = 24.15 > 7.34, which is sufficient.

Table 3 lists key component derating design parameters.

Table 3. Derating design parameters of key components.

Component	Maximum Value	Design Value
Transistor	204.75 V/3.86 A	500 V/20 A IRFP460
High-frequency transformer capacity	7.34 cm^4	24.15 cm^4 EE65
Input rectifier bridge	342 V/10 A	700 V/35 A KBPC2510
PFC BOOST	439.39 μF	600 μH
PFC output capacitor	300 V/644.12 μF	450 V/660 μF
Output rectifier diode	134 V/24 A	420 V/30 A HER3006

2.4. Power Consumption Assessment of Key Components

Semiconductor transistors, power diodes, high-frequency transformers, and filter inductors generate significant heat and they are the weak links in power reliability. The power consumption of the input rectifier bridge, PFC transistor, H bridge, and output rectifier diode are estimated separately below. Grid fluctuations are not considered.

(1) Rectifier bridge

The effective value of the rectifier bridge current is

$$I_{in\_rms} = \frac{P}{\eta U_{in}} = \frac{1000}{0.94 \times 220} = 4.84 \text{ A} \tag{6}$$

where η is the efficiency of the PFC. The average current value of the rectifier bridge is

$$I_{in\_avg} = \frac{2 \times \sqrt{2} I_{in\_rms}}{\pi} = \frac{2 \times \sqrt{2} \times 4.84}{\pi} = 4.36 \text{ A} \tag{7}$$

Then the power of the rectifier bridge is

$$P_{bridge} = V_{forward} \cdot I_{in\_avg} = 1.2 \times 4.36 = 5.232 \text{ W} \tag{8}$$

where $V_{forward}$ is the forward voltage drop of the diode.

(2) PFC transistor

The PFC switch tube is SPW35N60CFD, and its conduction loss is [35]

$$P_{pcond} = I_{ds}^2 \cdot R_{ds(on)} = \left(\frac{P}{U_{in\_peak}} \sqrt{2 - \frac{16 U_{in\_peak)}}{3\pi U_{dc}}} \right)^2 \cdot R_{ds(on)} = 0.744 \text{ W} \tag{9}$$

Through manual query, the PFC switch tube rise time t_r = 25 ns, fall time t_f = 12 ns, and output capacitance C_oss = 1400 PF. Then the switching loss is

$$P_{psw} = f_{sw}[0.5 U_{dc} U_{inpeak}(t_r + t_f) + 0.5 C_{oss} U_{dc}^2] = 10.57 \text{ W} \tag{10}$$

Therefore, the total power consumption of the PFC switch is

$$P_{ptotal} = p_{pcond} + p_{psw} = 11.32 \text{ W} \tag{11}$$

(3) H bridge

Since the circuit works in the ZVS state, the switching loss is very small and can be ignored. The conduction loss of the H-bridge is proportional to the duty cycle, and its maximum conduction loss is

$$P_{hcond(max)} = 4I^2 \cdot R_{ds(on)} \cdot D_{(max)} = 4 \times 2.56^2 \times 0.27 \times 0.5 = 3.54 \text{ W} \quad (12)$$

(4) Output rectifier diode

Diode losses mainly include conduction loss P_{con}, reverse loss P_r, and reverse recovery loss P_{rr}. When outputting 50 V/20A DC in the rated working state, then

$$P_{con} = 2{I_{out}}^2 R_{on} D_{diode} = 2 \times 20^2 \times 1.85 \times 0.5 = 740 \text{ W} \quad (13)$$

$$P_r = 2V_r I_r D_{diode} = 2 \times 50 \times 10 \times 10^{-6} \times 0.5 = 5 \times 10^{-4} \text{ W} \quad (14)$$

$$P_{rr} = 2 \times \frac{1}{2} V_r I_r t_r f_s = 2.25 \times 10^{-5} \text{ W} \quad (15)$$

where D_{diode} is the duty cycle of the diode, which is taken as 0.5, and V_r is the reverse voltage of the diode.

It can be seen that the power consumption of the H bridge is low due to the realization of ZVS. The high power consumption of PFC transistors is one of the obstacles to their application in high-power power supplies. The diode has the highest power dissipation of all components due to its large on resistance (1.85 Ω).

3. Simulation of the Highly Reliable Current Source

The purpose of the simulation is to analyze and verify the feasibility of the design method, parameters, and operation scheme of the power supply. For the simulation software, we choose Saber and Simulink Editor, which is a visual simulation tool in MATLAB. Saber simulation is more accurate and suitable for detailed simulation, so it is selected for the simulation of the phase-shifted full bridge; while Simulink Editor is more suitable for system simulations such as principle and operation schemes.

3.1. Simulation of Fault Tolerance Mechanism of the 3 + 1 Parallel Redundant Current Source

As mentioned above, each module of the power supply operates below the rated current, once a module fails, the remaining modules increase the current and work at the rated power, and the total output returns to the state before the failure. We simulated this operation mode by using Simulink, as shown in Figure 7. We use a timing switch to disconnect the output of the first module at 1 s.

The result is shown in Figure 8. In the figure, the abscissa stands for the simulation time and the vertical coordinate stands for the current value. CH1_Cur, CH2_Cur, CH3_Cur, and CH4_Cur indicate the current of module 1, module 2, module 3, and module 4, respectively. The figure shows that when the first module fails, the other three modules automatically increase the power due to the closed-loop feedback, and the total output current remains unchanged. Due to the inductance in the circuit, the fluctuation of the total current is less than 1/4, which is approximately equal to 0.4I/(3 + 1), which is consistent with the analysis in Section 2.1.

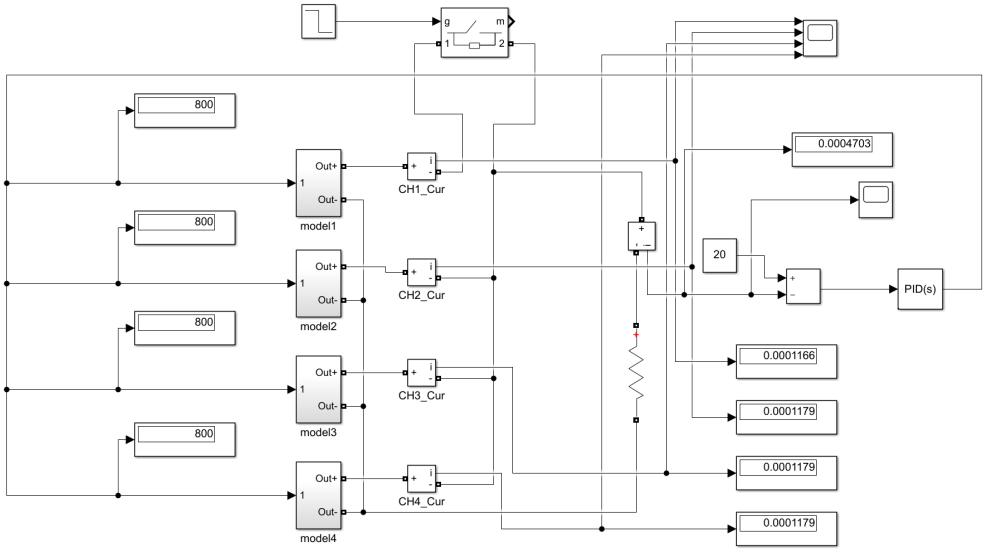


Figure 7. Simulink model of the 3 + 1 parallel redundant current source.

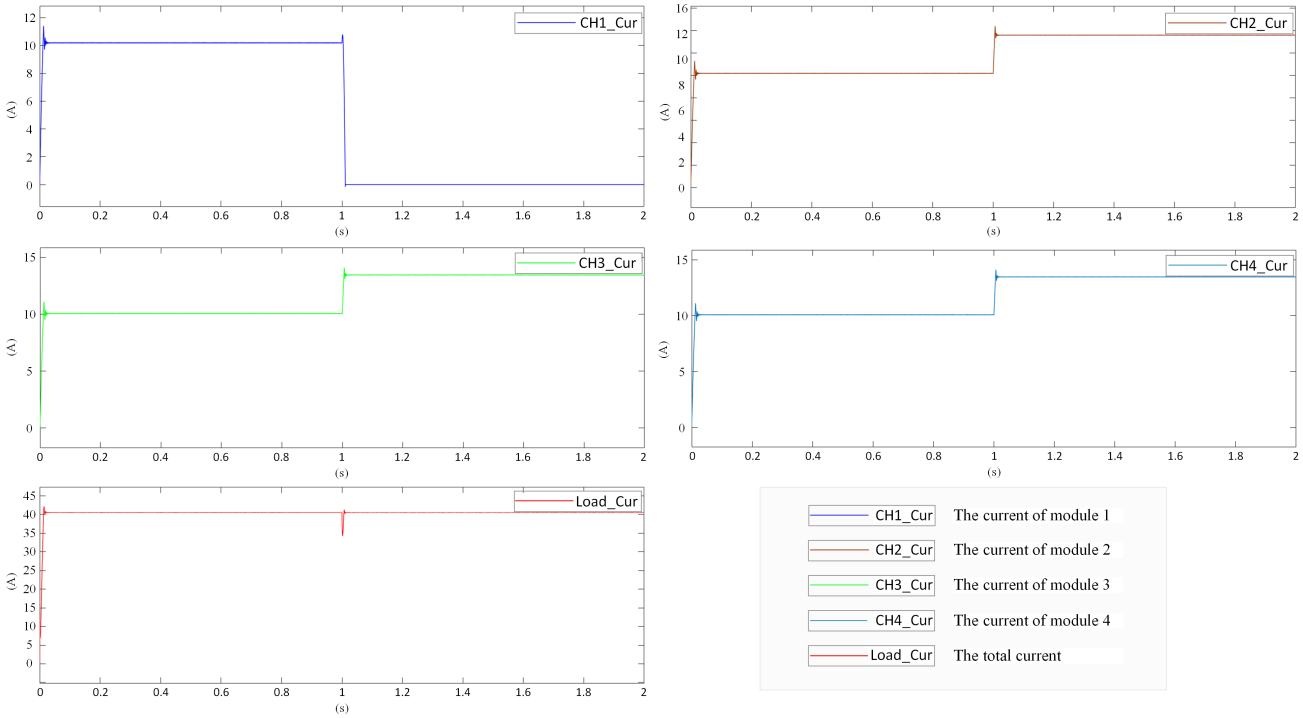


Figure 8. Simulation result of the 3 + 1 parallel redundant current source.

3.2. The Simulation of PFC

Figure 9 shows the simulation model of PFC. Two closed loops are designed, the outer loop ensures a stable DC voltage output, and the inner loop ensures the phase synchronization of current and voltage [36]. The MOSFET in the figure is a PFC transistor. In order to achieve stable control, the adjustment speed of the inner loop needs to be much faster than the outer loop. The outer loop samples the voltage of the DC bus, and this value is compared with a given voltage of 390 V to increase the DC bus voltage to 390 V. The inner loop samples the current of the DC bus, and the value is compared with the bus voltage after processing to achieve the purpose of forcing the current phase to be consistent with the voltage phase. To control the response of the outer loop, a PID regulator is added. The modulation wave (feedback value) is compared with the carrier wave (triangular wave) to generate PWM to control the MOSFET.

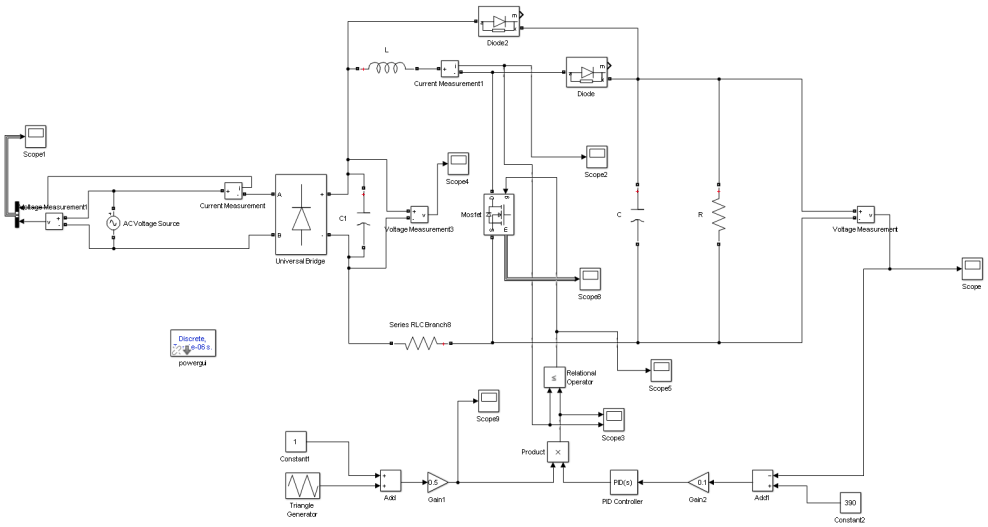
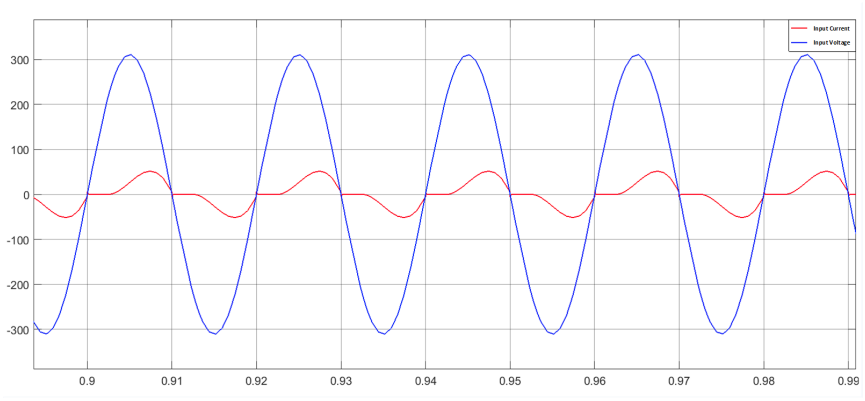


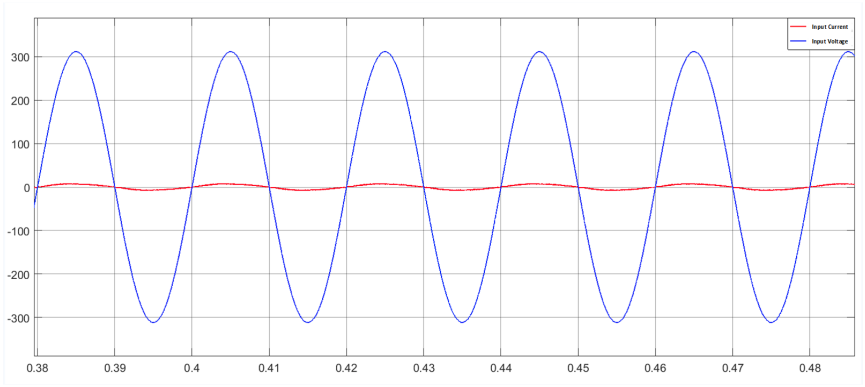
Figure 9. The simulation model of PFC.

The simulation results of the input voltage and current are shown in Figure 10.

It can be seen from Figure 10a that the impedance angle φ (phase difference between the input voltage and current) is large and the power factor cosφ is small; Figure 10b shows that the input voltage and current phase are consistent and the power factor can reach more than 99%.



(**a**)



(**b**)

Figure 10. The simulation result of PFC. (**a**) Waveform without PFC. (**b**) Waveform without PFC.

The PFC output voltage fluctuates around 390 V, as shown in Figure 11.

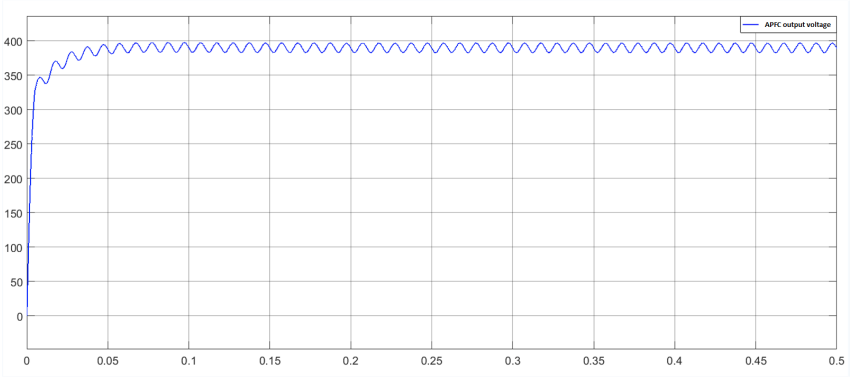


Figure 11. The PFC output voltage.

3.3. Simulation of the Phase-Shifted Full Bridge

The main purpose of the phase-shifted full bridge of this power module is to realize ZVS. Saber provides a suitable control chip model, which brings great convenience to the simulation. The power supply outputs a stable voltage value, as shown in Figure 12, indicating that the simulation model is working normally. The four-phase PWM drive waveforms of A, B, C, and D are shown in Figure 13. It can be seen that the order in which the transistors are turned on is A→C→B→D, which is the correct working mode. Figure 14 shows the dead time of phases A and B, which is about 0.12 µs, which is consistent with the calculation in Section 2.2. Figure 15 shows the voltage between the midpoints of the two legs of the H-bridge and the current waveform of the resonant inductor, and the current amplitude is I = 2.56 A, so I_peak = 2.56 × 1.414 = 3.62 A, which is approximately consistent with the calculation result of the Formula (5). Figure 16 shows the voltage of the DC-blocking capacitor. We design the voltage to be 1% of the bus voltage, which is about 3.9 V, which is roughly consistent with the simulation. Figure 17 shows the drain-source voltage and driving voltage of the transistor Q1. It can be seen that after the drain-source voltage drops, the driving voltage rises, and ZVS is realized.

Based on the above design and simulation, we created a multi-module parallel redundant power supply, which consists of four power modules in parallel, as shown in Figure 18.

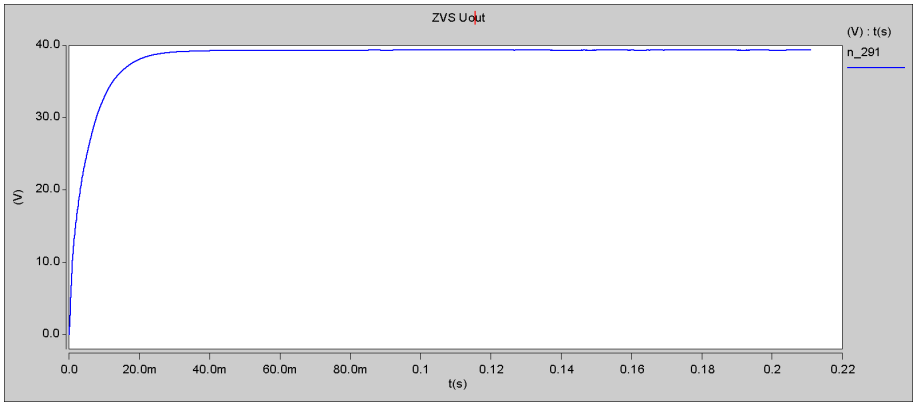


Figure 12. The output waveform of the power supply.

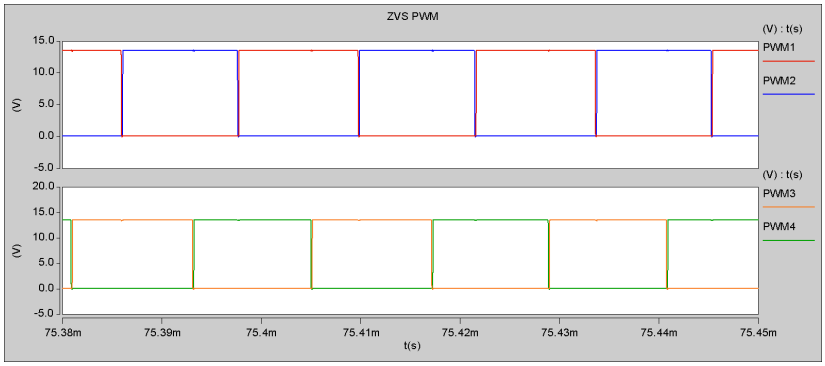


Figure 13. Four-phase PWM drive waveforms of A, B, C, and D.

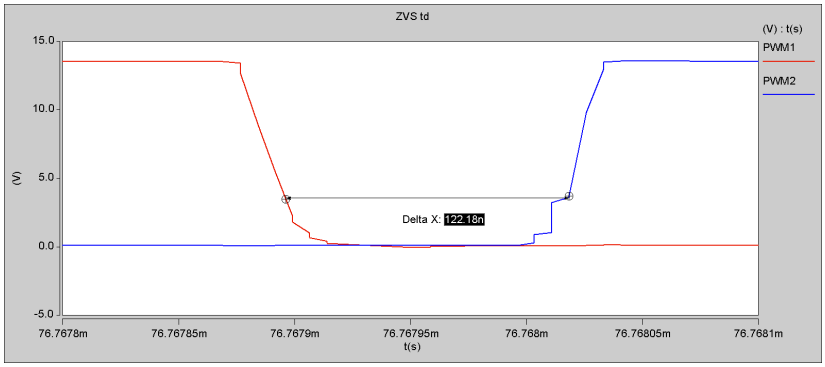


Figure 14. The dead time of phases A and B.

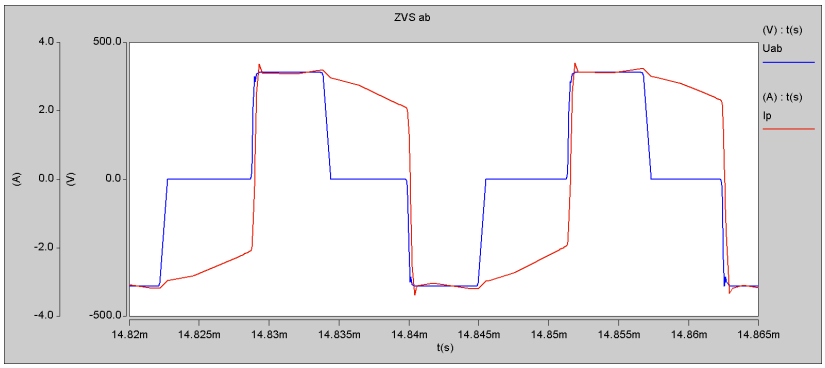


Figure 15. The voltage between the midpoints of the two legs of the H-bridge and the current waveform of the resonant inductor.

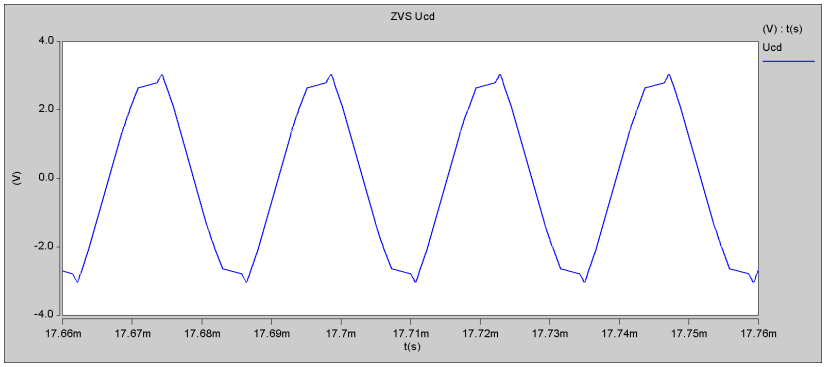


Figure 16. The voltage waveform of DC blocking capacitor.

The current source has fault tolerance, it can still operate normally after a module failure. Figure 19a shows the voltage difference at the midpoint of the H-bridge of the power module, which is consistent with the simulation results shown in Figure 15. Figure 19b shows the drain-source voltage and drive voltage of Q1. The drain-source voltage dropped to 0 before the driving voltage rises, which is consistent with the simulation results shown in Figure 17, so the ZVS is achieved.

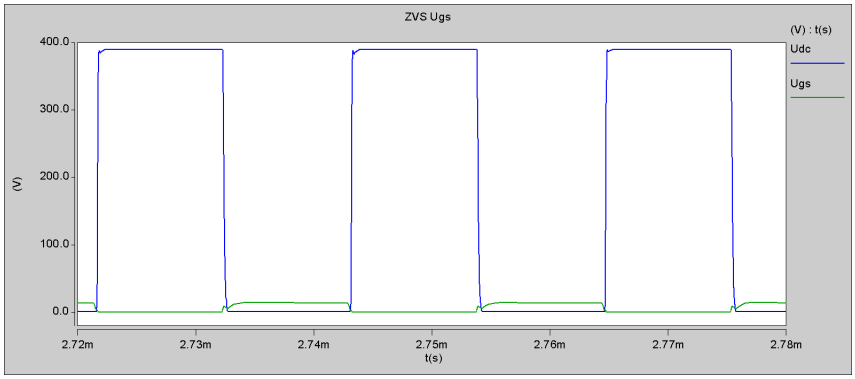


Figure 17. The drain-source voltage and driving voltage of transistor Q1.

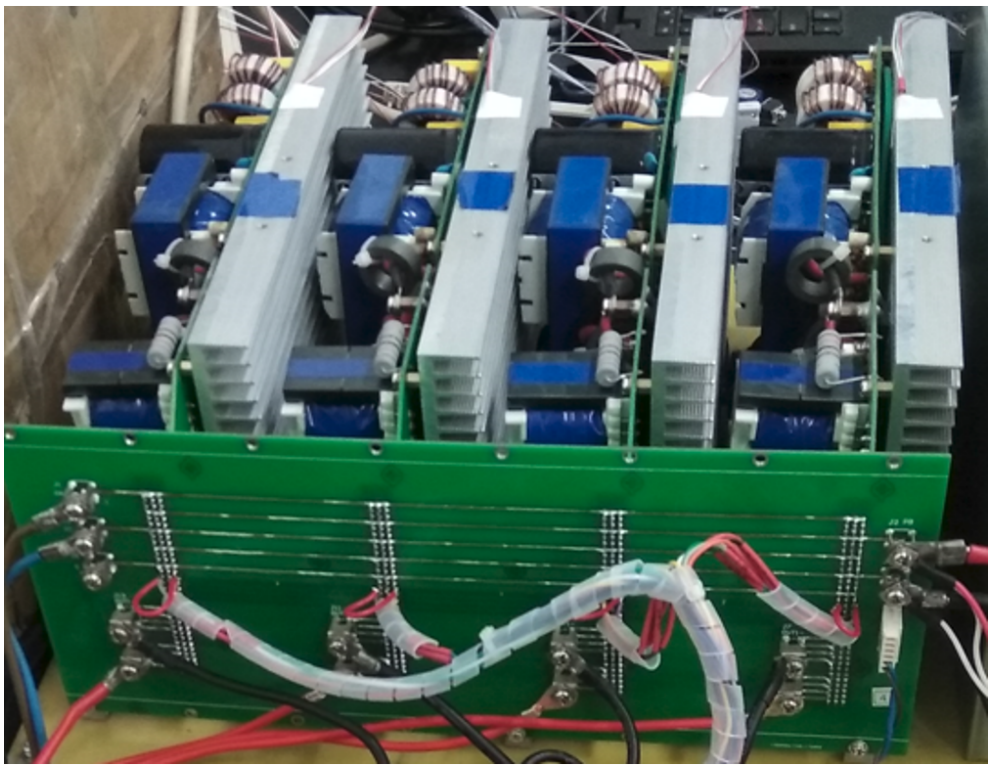
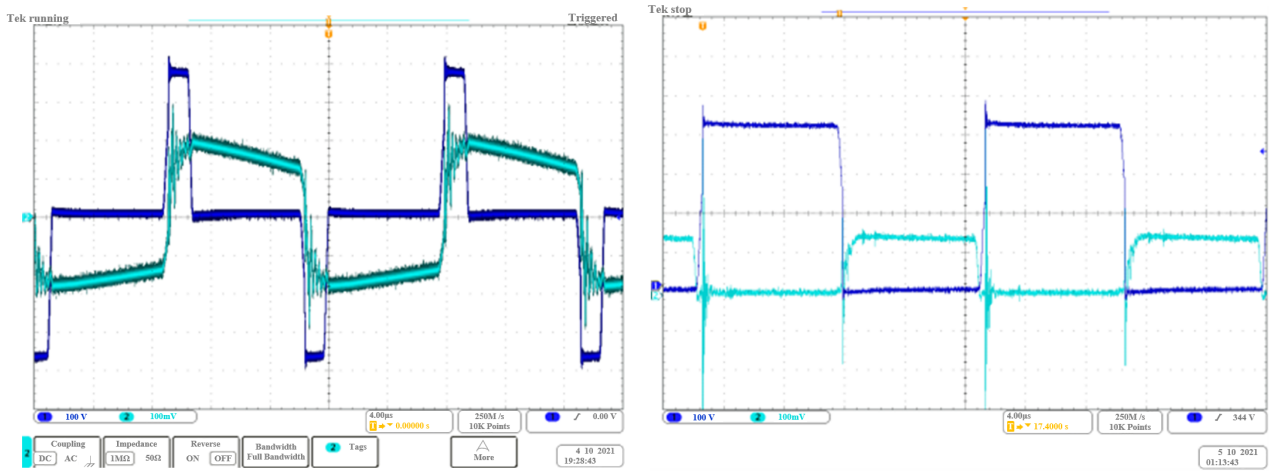


Figure 18. Photo of the 3 + 1 parallel redundant power supply.



(**a**) (**b**)

Figure 19. ZVS waveform of the power module. (**a**) The waveform of the voltage difference at the midpoint of the H-bridge. (**b**) The waveform of drain-source voltage and driving voltage of Q1.

4. Conclusions

This paper proposes a series of design schemes to improve the reliability of modular high-power current sources. We propose a reliability design scheme from two aspects of overall structure and module details. For the overall structure, the design of the $N + 1$ redundant structure and the selection of the number of modules are deeply analyzed; in terms of details, the PSFB with obvious consumption reduction and the derating design of the device is realized, and the working temperature of the module is reduced as much as possible. Power availability is a broad topic. Besides the presented solutions introduced in this article, many factors are also related, such as the design details of the SLAC proposed in the introduction section, as well as power supply cooling, layout, and human factors. The power supply reliability design and simulation method provided in this paper can provide useful theoretical and technical support for the reliability research of high-power power supplies.

Author Contributions: Conceptualization, Q.Z. and Y.X.; Formal analysis, Q.Z., Y.X. and Z.Z.; Funding acquisition, X.Q.; Investigation, Q.Z. and X.Q.; Methodology, Q.Z.; Project administration, Y.X.; Resources, Y.X. and X.Q.; Supervision, Y.X.; Validation, X.Q.; Writing—original draft, Q.Z.; Writing—review & editing, Z.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by National Natural Science Foundation of China grant number D5110220135.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Cepin, M.; Bris, R. *Safety and Reliability. Theory and Applications*; CRC Press: Boca Raton, FL, USA, 2017.
2. Stawowy, M.; Rosiński, A.; Siergiejczyk, M.; Perlicki, K. Quality and Reliability-Exploitation Modeling of Power Supply Systems. *Energies* **2021**, *14*, 2727. [CrossRef]
3. Mohamad, F.; Teh, J.; Lai, C.-M.; Chen, L.-R. Development of energy storage systems for power network reliability: A review. *Energies* **2018**, *11*, 2278. [CrossRef]
4. Li, C.; Zhang, Y.; Cao, Z.; Dewei, X. Single-phase single-stage isolated ZCS current-fed full-bridge converter for high-power AC/DC applications. *IEEE Trans. Power Electron.* **2016**, *32*, 6800–6812. [CrossRef]
5. Zhang, Z.; Mallik, A.; Khaligh, A. A high step-down isolated three-phase AC-DC converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *6*, 129–139. [CrossRef]
6. Chen, G.; Chen, L.; Deng, Y.; Wang, K.; Qing, X. Topology-reconfigurable fault-tolerant LLC converter with high reliability and low cost for more electric aircraft. *IEEE Trans. Power Electron.* **2018**, *34*, 2479–2493. [CrossRef]

7. Udris, D.; Bručas, D.; Pomarnacki, R. Reliability Improvement of Power Distribution System for UAV. *Electronics* **2019**, *8*, 636. [CrossRef]
8. Hayashiya, H.; Masuda, M.; Noda, Y.; Suzuki, K.; Suzuki, T. Reliability analysis of DC traction power supply system for electric railway. In Proceedings of the 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, Poland, 11–14 September 2017; pp. 1–6.
9. Sandelic, M.; Sangwongwanich, A.; Blaabjerg, F. Reliability evaluation of PV systems with integrated battery energy storage systems: DC-coupled and AC-coupled configurations. *Electronics* **2019**, *8*, 1059. [CrossRef]
10. Stawowy, M.; Rosiński, A.; Paś, J.; Klimczak, T. Method of Estimating Uncertainty as a Way to Evaluate Continuity Quality of Power Supply in Hospital Devices. *Energies* **2021**, *14*, 486. [CrossRef]
11. Mohamad, F.; Teh, J. Impacts of energy storage system on power system reliability: A systematic review. *Energies* **2018**, *11*, 1749. [CrossRef]
12. Maish, A. Defining requirements for improved photovoltaic system reliability. *Prog. Photovoltaics Res. Appl.* **1999**, *7*, 165–173. [CrossRef]
13. Zhang, W.; Xu, D.; Enjeti, P.N.; Li, H.; Hawke, J.T.; Krishnamoorthy, H.S. Survey on fault-tolerant techniques for power electronic converters. *IEEE Trans. Power Electron.* **2014**, *29*, 6319–6331. [CrossRef]
14. Kumar, G.K.; Elangovan, D. Review on fault-diagnosis and fault-tolerance for DC–DC converters. *Iet Power Electron.* **2020**, *13*, 1–13. [CrossRef]
15. Zhang, W.; Xu, D. Fault analysis and fault-tolerant design for parallel redundant inverter systems in case of IGBT short-circuit failures. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 2031–2041. [CrossRef]
16. Wang, H.; Pei, X.; Wu, Y.; Kang, Y. A general fault-tolerant operation strategy under switch fault for modular series–parallel DC–DC converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *9*, 872–884. [CrossRef]
17. Costa, L.; Buticchi, G.; Liserre, M. A fault-tolerant series-resonant DC–DC converter. *IEEE Trans. Power Electron.* **2016**, *32*, 900–905. [CrossRef]
18. Zhao, N.; Liu, J.; Shi, Y.; Yang, J.; Zhang, J.; You, X. Mode analysis and fault-tolerant method of open-circuit fault for a dual active-bridge DC–DC converter. *IEEE Trans. Ind. Electron.* **2019**, *67*, 6916–6926. [CrossRef]
19. Pei, X.; Nie, S.; Chen, Y.; Kang, Y. Open-circuit fault diagnosis and fault-tolerant strategies for full-bridge DC–DC converters. *IEEE Trans. Power Electron.* **2011**, *27*, 2550–2565. [CrossRef]
20. Costa, L.F.; Buticchi, G.; Liserre, M. A family of series-resonant DC–DC converter with fault-tolerance capability. *IEEE Trans. Ind. Appl.* **2017**, *54*, 335–344. [CrossRef]
21. Li, L.-L.; Wang, P.-C.; Wang, C.-H. Lifetime prediction model for electric vehicle IGBT modules under driving conditions. *J. Chin. Inst. Eng.* **2018**, *41*, 308–316. [CrossRef]
22. Andresen, M.; Ma, K.; Buticchi, G.; Falck, J.; Blaabjerg, F.; Liserre, M. Junction temperature control for more reliable power electronics. *IEEE Trans. Power Electron.* **2017**, *33*, 765–776. [CrossRef]
23. Wang, C.; He, Y.; Wang, C.; Li, L.; Wu, X. Multi-chip IGBT module failure monitoring based on module transconductance with temperature calibration. *Electronics* **2020**, *9*, 1559. [CrossRef]
24. Macnair, D. *Digitally Controlled High Availability Power Supply*; Technical Report; Office of Scientific Technical Information: Menlo Park, CA, USA, 2008.
25. Bellomo, P.; Macnair, D.; Menlo, S. *SLAC Next-Generation High Availability Power Supply*; Accelerator Reliability Workshop: Menlo Park, CA, USA, 2009.
26. Szott, M.; Wermiński, S.; Jarnut, M.; Kaniewski, J.; Benysek, G. Battery energy storage system for emergency supply and improved reliability of power networks. *Energies* **2021**, *14*, 720. [CrossRef]
27. Lüdeke, A. Accelerator Reliability Reporting at the Swiss Light Source. In Proceedings of the 5th International Particle Accelerator Conference (IPAC'14), Dresden, Germany, 15–20 June 2014; pp. 3819–3821.
28. Savio Abraham, D.; Verma, R.; Kanagaraj, L.; Giri Thulasi Raman, S.R.; Rajamanickam, N.; Chokkalingam, B.; Marimuthu Sekar, K.; Mihet-Popa, L. Electric vehicles charging stations' architectures, criteria, power converters, and control strategies in microgrids. *Electronics* **2021**, *10*, 1895. [CrossRef]
29. Arpaia, P.; Buzio, M.; Caspers, F.; Golluccio, G.; Oberson, D. European organization for nuclear research CERN-accelerators and technology sector. *Rev. Sci. Instrum.* **2012**, *83*, 013306. [CrossRef]
30. Vinogradov, A.; Bolshev, V.; Vinogradova, A.; Jasiński, M.; Sikorski, T.; Leonowicz, Z.; Goňo, R.; Jasińska, E. Analysis of the power supply restoration time after failures in power transmission lines. *Energies* **2020**, *13*, 2736. [CrossRef]
31. Pol, A.; Heuer, R.; Stamm, P. Inside CERN: European Organization for Nuclear Research; Lars Müller Publ.: Zurich, Switzerland, 2013.
32. Lam, B.; Bellomo, P.; De Lira, A.; MacNair, D. ILC-ATF2 dc-magnet power supplies. In Proceedings of the 2007 IEEE Particle Accelerator Conference (PAC), Albuquerque, NM, USA, 25–29 June 2007; pp. 569–571.
33. Selvaraj, R.; Desingu, K.; Chelliah, T.R.; Khare, D.; Bharatiraja, C. Fault tolerant operation of parallel-connected 3L-neutral-point clamped back-to-back converters serving to large hydro-generating units. *IEEE Trans. Ind. Appl.* **2018**, *54*, 5429–5443. [CrossRef]
34. Mukherjee, S.; Saha, S.S.; Chowdhury, S. Design of Duty-Ratio and Phase-Shift Control Circuits for MPPT of SPV Source using ZV-ZCS PSFB Converters. In Proceedings of the 2021 Devices for Integrated Circuit (DevIC), Nadia, India, 19–20 May 2021; pp. 555–559.

35. Jadli, U.; Mohd-Yasin, F.; Moghadam, H.A.; Pande, P.; Chaturvedi, M.; Dimitrijev, S. A Method for Selection of Power MOSFETs to Minimize Power Dissipation. *Electronics* **2021**, *10*, 2150. [CrossRef]
36. Naraharisetti, K.; Channegowda, J.; Green, P.B. Design and modeling of CCM average current control PFC AC-DC Boost converter. In Proceedings of the 2021 IEEE Green Technologies Conference (GreenTech), Denver, CO, USA, 7–9 June 2021; pp. 403–408.