Article

# A Two-Stage DC/DC Isolated High-Voltage Converter with Zero-Voltage Switching and Zero-Current Switching Applied in Electronic Power Conditioners 

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#### Abstract

This paper presents a two-stage DC/DC converter with high efficiency utilized in an electronic power conditioner (EPC), which is widely applicable in satellite communications, etc. The galvanically isolated converter contains two cascaded converters: a buck converter, which is a pre-regulator operating under a closed-loop condition, and a push-pull converter, which is intended to boost the input voltage, operating under an open-loop condition. In the push-pull converter, the power switches, including the main switches and the rectifier diodes, operate under zero-voltage switching (ZVS) and zero-current switching (ZCS) at both switch off and switch on, which minimizes the switching loss. Furthermore, all of the parasitic parameters, such as the parasitic capacitance, leakage inductance, and magnetizing inductance of the main transformer, are fully utilized. Therefore, the presented topology benefits from fewer semiconductors but higher efficiency. The proposed topology produces less EMI noise because of ZVS and ZCS processes whose fundamental switching frequency interference is relatively low. The presented converter achieves a wide bus voltage regulation range in a satellite because of the pre-regulation of the buck cell. The theoretical analysis is validated by a prototype and its experimental results. The maximum efficiency of the converter can be up to $94.5 \%$, and the high-voltage output is 7000 V .


Keywords: two-stage DC/DC converter; zero-voltage switching (ZVS); zero-current switching (ZCS); high efficiency

## 1. Introduction

Microwave signals are amplified using space traveling wave tube amplifiers [1] (STWTA) as an important component of satellite systems. Typically, a TWTA comprises a traveling wave tube [2] (TWT) and an electronic power conditioner [3] (EPC). An interaction between a beam wave and an electromagnetic wave contributes to the amplification of microwave power when a TWT is utilized. Additionally, the EPC converts the satellite bus voltage [4] (typically ranging from 30 to 100 V DC ) to the required electrode voltage (ranging from a few kV to a few hundred kV DC ) through high-frequency power converters. Since the primary power conversion is the most significant aspect of the EPC, it must be considered when designing the circuit [5].

Presently, the main power conversion is categorized into two major types: singlestage power conversion and two-stage power conversion. The greatest advantage of single-stage conversion is its simplicity, and it is used in applications such as phase-shifted full-bridges [6-8], asymmetric half-bridges [9-11], three-transistor push-pulls [12], and so on. However, all of these single-stage topologies suffer from the same issue: stringent input voltage and load quality requirements. The application of a single-stage power conversion cannot satisfy the requirements of satellites. Consequently, two-stage power converters are increasingly utilized in the EPC. There are two types of topologies that have
become dominant applications: boost and full-bridge [13], and buck and phase-shifted full-bridge [14]. In boost and full-bridge topologies, the control loop response time is very slow, and the surge current is high [15]. Furthermore, the complexity of the control systems of buck and phase-shifted full-bridge converters negatively impacts their reliability, and this topology cannot work in ZVS or ZCS when the load is not heavy [16]. Two other two-stage cascade transformations, flyback and asymmetrical half-bridge, and forward and push-pull, are rarely used due to their poor efficiency. In these two-stage topologies, forward and push-pull have the highest efficiency, which is $91.47 \%$ [17].

The statistics indicate that STWTAs consume $70 \%$ to $90 \%$ of DC consumption. Additionally, they contribute to $35 \%$ of the total weight in radar systems [18]. Therefore, power conversion topology must be continuously enhanced to meet the requirements of higher efficiency [19] and the miniaturization of on-board equipment.

Buck and push-pull, and boost and push-pull are two different topologies, as shown in Figure 1. Based on the system requirement, if EPC has some malfunctions or failures, it cannot affect other modules in the satellite. If in the fault mode, the power switch (the red one) in Figure 1a can be turned off and thus can prevent affecting the bus voltage in the satellite. However, in Figure 1b, the power switch (the red one), when turned off, cannot prevent affecting the bus voltage, and it must include an additional protective circuit. Moreover, if ZVS and ZCS need to be realized in a boost and push-pull topology, extra inductance and capacitance (the blue ones) need to be added to the circuit, which increases the complexity of the circuit.


Figure 1. The two different topologies of a two-stage converter: (a) The buck and push-pull topology, and (b) the boost and push-pull topology.

Motivated by the above analysis and practical application, this paper presents a twostage converter topology with a high efficiency: buck and push-pull, where the push-pull converter is implemented in ZVS and ZCS. The buck regulator is used to pre-regulate the voltage in hard switching.

In addition, the high-voltage output is achieved through a soft-switching push-pull converter. The block diagram of this two-stage converter is shown in Figure 2. Closed-loop feedback is applied in the buck regulator to provide stable voltage for the push-pull circuit, and the push-pull circuit works in an open-loop state with a high output voltage after a doubler rectifier circuit.

This two-stage DC/DC converter topology enjoys the following advantages:
(1) It makes full use of the parasitic capacitance and inductance that participate in the resonant switching, without adding additional components, in order to achieve soft switching and thereby increase efficiency.
(2) The power switches of the push-pull converter and the diodes of the second side of the rectifier can be operated to provide zero current and zero voltage both at the time of switching off and switching on, resulting in increased efficiency and reduced voltage and current limitations.
(3) Dual interleaved drivers are used in the buck circuit, so the magnetic reset process does not need to be considered for duty cycles that exceed $50 \%$, and the design of the drive
transformer is more compact than that of a single-drive method, resulting in a significantly broader range of applications.
(4) This topology produces less EMI noise due to the shapes of the current and voltage waveforms, which contain very low magnitudes of fundamental switching frequency interference.
(5) The cost is lower as a result of the low-current/voltage limitation (also a result of point 1), and it is simple to implement overload limitation without causing component damage.
(6) The control scheme can be simpler than full-bridge or other topologies if the switches in both the buck and push-pull operate on the same frequency.

This paper begins with Section 2, which examines operational modes. Section 3 introduces the key parameter utilized in the topology design. Section 4 presents the experimental results from the laboratory prototype. Section 5 compares buck and pushpull converters with other topologies and discusses potential future research enhancements. Section 6 concludes the paper.


Figure 2. The block diagram of the two-stage converter.

## 2. The Proposed Converter

### 2.1. Description of the Topology

This paper proposes a two-stage DC/DC converter consisting of a buck regulator and a push-pull converter. The schematic circuit is depicted in Figure 3.


Figure 3. The DC/DC converter circuit diagram.
$Q_{3}, Q_{4}, D_{1}, L_{b}$, and $C_{b}$ constitute the interleaved dual-driver buck regulator. They are power switches, the fly-wheel diode, inductance, and capacitance, respectively. Equivalent primary leakage inductance, $L_{p}$, helps achieve the soft-switching with $C_{b}$, as will be discussed later. The resonant frequency is $f=\frac{1}{2 \pi \sqrt{L_{p} C_{b}}}$. $Q_{1}$ and $Q_{2}$ are power switches used
in push-pull converter. The transformer, T, provides galvanic isolation between the input and output sides and is employed to generate high voltage together with voltage-doubler circuits, which include voltage-doubler rectifier diodes and capacitance: $D_{O 1}, D_{\mathrm{O} 2}, C_{O 1}$, and $C_{O 2}$. Winding capacitance, $C_{p 1}$ and $C_{p 2}$, cannot be ignored because the converter is applied in a high-voltage situation. $C_{Q 1}$ and $C_{Q 2}$ denote the sums of the parasitic output capacitance of the semiconductor and external parallel capacitance. $D_{Q 1}$ and $D_{Q 2}$ are body diodes.

The following considerations are made to make the analysis simpler:
(1) Assume that all components are ideal;
(2) Transformer turns ratio, $N$ :

$$
\begin{gather*}
N_{1}=N_{2}=\frac{N_{3}}{N}  \tag{1}\\
L_{m 1}=L_{m 2}=L_{m}=\frac{L_{m 3}}{N^{2}} \tag{2}
\end{gather*}
$$

where $L_{m}$ is much larger than $L_{p}$;
(3) The sum of semiconductor parasitic output capacitance and external parallel capacitance:

$$
\begin{equation*}
C_{Q 1}=C_{Q 2}=C_{Q} \tag{3}
\end{equation*}
$$

(4) Voltage-doubler rectifier capacitance

$$
\begin{equation*}
C_{O 1}=C_{O 2} \tag{4}
\end{equation*}
$$

and the voltage of both $C_{O 1}$ and $C_{O 2}$ are $\frac{U_{O}}{2}$.

### 2.2. Modes of Operation

Throughout the process of a completed switching cycle, from $t_{0} \sim t_{8}$, the converter operates in eight modes, as in the following exposition. The key waveforms are exhibited in Figure 4.


Figure 4. The key waveforms in a complete switching cycle.

Mode I [ $t_{0}, t_{1}$ ]: The equivalent circuit of mode I is depicted in Figure 5. The switch $Q_{2}$ turns off at the instant of $t_{0}$, the capacitance $C_{Q 2}$ starts to charge, and the voltage increases. On the other hand, $C_{Q 1}$ is discharging simultaneously. Furthermore, the charging capacity of $C_{Q 2}$ is equal to the discharging capacity of $C_{Q 1}$ due to the coupling effect and the balance of the transformer. There is no energy exchange in the transformer. The leakage inductance $L_{p}$ resonates with $C_{Q 1}$ and $C_{Q 2}$. The winding capacitance of transformer $C_{p 1}$ starts charging and $C_{p 2}$ discharges. In addition, $I_{C p 1}=I_{C p 2}$. When the voltage of $C_{p 1}$ reaches $-V_{b}, V_{C p 2}$ reaches $V_{b}$ and this mode comes to the end.


Figure 5. The equivalent circuit of mode I.
Since there is no energy exchange between the primary side and the secondary side in mode I, the voltage across $C_{b}$ can be considered constant, and the equivalent circuit of mode I can be depicted in Figure 6.


Figure 6. Approximated equivalent circuit for no energy exchanging between the primary side and secondary side.

Therefore:

$$
\left\{\begin{array}{l}
V-L_{m 1} \frac{d i_{1}}{d t}+M \frac{d i_{2}}{d t}-\frac{1}{C_{Q 1}} \int i_{1} d t=0  \tag{5}\\
V-L_{m 2} \frac{d i_{2}}{d t}-M \frac{d i_{1}}{d t}-\frac{1}{C_{Q 2}} \int i_{2} d t=0
\end{array}\right.
$$

As $L_{m 1}=L_{m 2}=L_{m}, C_{Q 1}=C_{Q 2}=C_{Q}$, neglecting the effect of the leakage inductance, it is $M=L_{m}$, so that yields:

$$
\begin{equation*}
i_{1}=-i_{2} \tag{6}
\end{equation*}
$$

Combining (5) and (6):

$$
\begin{equation*}
V-2 L_{m} \frac{d i_{1}}{d t}-\frac{1}{C_{Q}} \int i_{1} d t=0 \tag{7}
\end{equation*}
$$

The solution of (7) is:

$$
\begin{gather*}
i_{1}(t)=\frac{I_{m}}{\sqrt{2} \cos \psi} \cos (\omega t+\psi) \\
\omega=\frac{1}{\sqrt{2 L_{m} C_{Q}}}  \tag{8}\\
I_{m}=\frac{1}{2} \frac{V}{L_{m}} T_{O N}
\end{gather*}
$$

Mode II $\left[t_{1}, t_{2}\right]$ : The equivalent circuit of mode II is depicted in Figure 7. In this mode, the voltage of winding capacitance $C_{p 1}$ remains $-V_{b}$, and $V_{C p 2}$ remains $V_{b}$. $C_{Q 2}$ keeps charging, and the voltage increases. Since $C_{Q 1}$ is discharging, the voltage decreases as well. A small level of high-frequency oscillated current flows through the second-side rectifier diode $D_{O 2}$. When the voltage of $V_{Q 1}$ drops to 0 and $V_{Q 2}$ rises to $2 V_{b}, C_{Q 1}$ and $C_{Q 2}$ complete discharging and charging and mode II finishes.


Figure 7. Equivalent circuit of mode II.
Mode III $\left[t_{2}, t_{3}\right]$ : The equivalent circuit of mode III is depicted in Figure 8.When the resonance on the primary side of the transformer finishes, the current through $C_{Q 1}, C_{Q 2}$, $C_{p 1}$, and $C_{p 2}$ returns to 0 , but the voltage is still the same, respectively. $I_{Q 1}$ and $I_{L p}$ go to 0 gradually so that the MOSFET $Q_{1}$ operates in ZCS when it turns on. From the moment of $t_{2}$, the current through $D_{\mathrm{O} 2}$ returns to 0 , and $D_{\mathrm{O} 2}$ operates in ZCS in the stage of energy exchange between the primary and secondary sides.


Figure 8. Equivalent circuit of mode III.
Mode IV $\left[t_{3}, t_{4}\right]$ : As $V_{Q 1}$ had already been 0 at $t_{3}$, the MOSFET $Q_{1}$ turns on in ZVS. Mode IV is the major process that transfers energy from the primary side to the secondary side. No more current flows in $C_{Q 1}, C_{Q 2}, C_{p 1}$, or $C_{p 2}$, but the voltage on them is invariable. Energy transmits from the push-pull side to the high-voltage side through a high-frequency transformer on the coupling of magnetizing inductance $L_{m 1}$. The current in $Q_{1}$ increases gradually in sinusoidal form from 0 to the maximum (about 10 A ), then decreases to 0 later again, the current in $D_{\mathrm{O} 2}$ charges the voltage-doubling capacitance in the same form and synchronously offers energy for the load. In the current circumstance $t_{4}$, the MOSFET $Q_{1}$ operates in ZCS when it turns off, and mode IV comes to an end.

The equivalent circuit of Figure 9 can be depicted in Figure 10 during the time that switch $Q_{1}$ is on. Normally, the equivalent output capacitance, $C_{O}^{\prime}$, is much smaller than the
buck capacitance, $C_{b}$, so the main resonance can be located in the loop consisting of $C_{b}$ and leakage inductance, $L_{p}$. According to KCL,

$$
\begin{equation*}
I_{L b}=I_{C b}+I_{L p} \tag{9}
\end{equation*}
$$

Hence,

$$
\begin{equation*}
\frac{I_{L b}}{C_{b}}=\frac{I_{L p}}{C_{b}}+L_{P} \frac{d_{I_{L p}}^{2}}{d t^{2}} \tag{10}
\end{equation*}
$$

whose solution is:

$$
\begin{gather*}
I_{L p}(t)=I_{L b}-I_{L b 0} \cos (\omega t+\varphi)  \tag{11}\\
\omega=\frac{1}{\sqrt{L_{p} C_{b}}}
\end{gather*}
$$

According to KVL,

$$
\begin{equation*}
V_{C b}-V_{L p}=V_{L m 1} \tag{12}
\end{equation*}
$$

that is,

$$
\begin{equation*}
V_{C b}(t)-V_{L m 1}=L_{p} \frac{d i}{d t} \tag{13}
\end{equation*}
$$

Applying (11) into (13):

$$
\begin{gather*}
I_{L b}-I_{L b 0} \cos \varphi=0 \\
\frac{V_{C b}(t)-V_{L m 1}}{L_{p} I_{L b 0}}=\omega \sin \varphi \tag{14}
\end{gather*}
$$

whose solution is:

$$
\begin{gather*}
\operatorname{tg} \varphi=\frac{V_{C b}(t 3)-V_{L m 1}}{L_{p} I_{L L b} \omega}  \tag{15}\\
I_{L b 0}=\frac{I_{L b}}{\cos \varphi}
\end{gather*}
$$

Until the moment $t_{4}$, the first half of the switching cycle comes to an end, and the circuit turns into the second half of the cycle. Based on symmetry, modes V~VIII are in one-to-one correspondence with modes I~IV.


Figure 9. Equivalent circuit of mode IV.


Figure 10. When the switch $Q_{1}$ turns on, this circuit is equivalent to the circuit in Figure 9.

## 3. Key Parameter Design

Taking input voltage $V_{i n}=30 \mathrm{~V} \mathrm{DC}$, output voltage $V_{O}=7000 \mathrm{~V} \mathrm{DC}$, load power $P_{O}=130 \mathrm{~W}$, and switch frequency $f=100 \mathrm{kHz}$ as an example, the key parameter design of the circuit is as follows.

### 3.1. Buck Inductance, $L_{b}$

Buck inductance can be calculated as:

$$
\begin{equation*}
L_{b}=\frac{V_{b}(1-D)}{K_{i n d} I_{b} f} \tag{16}
\end{equation*}
$$

where $V_{b}$ is the voltage of buck output $(\mathrm{V})$, in this case, $V_{b}=22 \mathrm{~V} ; D$ is the duty cycle $(\%)$ in the interleaved dual-driver, $D=\frac{1}{2} \frac{V_{b}}{V_{\text {in }}}=36.67 \% ; K_{\text {ind }}$ is the ripple current rate, $K_{\text {ind }}=0.3$, generally; $I_{b}$ is the current of the buck output (A), and $I_{b}=\frac{P_{0}}{V_{b}}=5.91 \mathrm{~A}$. Hence, $L_{b}=78.6 \mathrm{uH}$.

### 3.2. Buck Capacitance, $C_{b}$

Buck capacitance can be calculated as:

$$
\begin{equation*}
C_{b}=\frac{1}{f^{2}} \frac{1}{4 \pi^{2} L_{p}}=4.2 \mathrm{uF} \tag{17}
\end{equation*}
$$

where $L_{p}=0.6 \mathrm{uH}$ is the leakage inductance of the transformer and $f=100 \mathrm{kHz}$ is the switching frequency.

### 3.3. Power Transformer Parameter

The number of turns on the primary side of the transformer is:

$$
\begin{equation*}
N_{p}=\frac{V_{i n}}{K_{f} f B_{W} A_{e}} \tag{18}
\end{equation*}
$$

where $K_{f}=4.0$ is the waveform factor of the square wave; $f=100 \mathrm{kHz}$ is the switching frequency; the type of magnetic core is TPW33-UYF36 series; $B_{w}=150 \mathrm{mT}$ is the magnetic flux density; and $A_{e}=130.98 \mathrm{~mm}^{2}$ is the effective cross areas of the core. Therefore, $N_{p}=4.16$. Taking an integer value, that is $N_{1}=N_{2}=5$.

The number of turns on the secondary side of the transformer can be calculated by

$$
\begin{equation*}
N_{s}=\frac{N_{p} V_{o}}{2 V_{i n}}=583.4 \tag{19}
\end{equation*}
$$

In this case, $N_{3}=584$.
The general design rule of the power transformer parameter is that the equivalent primary leakage inductance, $L_{p}$, and the winding capacitance of the transformer, $C_{p}$, should be suitable. The practical measurements of these parasitic parameters: $L_{p}=0.6 \mathrm{uH}$ and $C_{p}=9 \mathrm{nF}$. If $L_{p}$ is different from the design value, a switch frequency of $f=100 \mathrm{kHz}$ can be achieved by adjusting the value of the buck capacitance, $C_{b}$, according to $f=\frac{1}{2 \pi \sqrt{L_{p} C_{b}}}$. If the sum value of $C_{p}, C_{Q}$, and the external parallel capacitance is about $10 \mathrm{nF}, \mathrm{ZVS}$ and ZCS are realized in the two-stage converter.

### 3.4. Power Loss of Transformer

Allowable loss can be calculated as:

$$
\begin{align*}
P_{f e}=P_{\Sigma}-P_{c u}= & \left(\frac{P_{o}}{\eta}-P_{o}\right)-\left(P_{p c u}+P_{s c u}\right)=\left(\frac{P_{o}}{\eta}-P_{o}\right)-\left(I_{p}^{2} R_{p}+I_{o}^{2} R_{s}\right) \\
& =\left(\frac{P_{o}}{\eta}-P_{o}\right)-\left[\left(\frac{P_{o}}{V_{i n} \eta}\right)^{2}(M L T)\left(N_{p}\right) \frac{\mu \Omega}{\mathrm{cm}} 10^{-6}+\left(\frac{P_{o}}{U_{o}}\right)^{2}(M L T)\left(N_{s}\right) \frac{\mu \Omega}{\mathrm{cm}} 10^{-6}\right]=3.02 \mathrm{~W} \tag{20}
\end{align*}
$$

where $P_{\Sigma}$ is the total loss $(\mathrm{W}), P_{c u}$ is the total copper loss $(\mathrm{W}), P_{p c u}$ is the copper loss of the primary side $(\mathrm{W}), P_{s c u}$ is the copper loss of the secondary side $(\mathrm{W})$, and $M L T$ is the average length of a single turn (cm).

The actual loss can be calculated as:

$$
\begin{equation*}
P_{f e}^{\prime}=\frac{W}{k g} \times W_{t f e}=2.63 \mathrm{~W} \tag{21}
\end{equation*}
$$

where $W_{t f e}$ is the weight of allowable iron loss ( kg ).
Obviously,

$$
\begin{equation*}
P_{f e}^{\prime}<P_{f e} \tag{22}
\end{equation*}
$$

The loss in the unit area can be calculated as:

$$
\begin{equation*}
\Phi=\frac{P_{f e}^{\prime}+P_{c u}}{A_{s}}=0.025 \mathrm{~W} / \mathrm{cm}^{2} \tag{23}
\end{equation*}
$$

The temperature increase in the transformer is less than $20^{\circ} \mathrm{C}$ in this case. The coiling method of the transformer additionally obtains a smaller distributed capacitance in layer coiling mode than in slot coiling mode, which has just a couple of $n \mathrm{~F}$.

### 3.5. Interleaved Dual-Driver Isolated Transformer

Buck circuits use interleaved dual drivers that require the support of an isolated driver transformer. The leakage inductance and power loss are reduced as a result of the use of the RM5 series of ferrite magnet cores and the "hamburger" coiling method, in which the primary side coil is wrapped by two secondary side coils. The calculation of drive transformer turns is identical to that of power transformer turns.

$$
\begin{equation*}
N_{p}=N_{s 1}=N_{s 2}=54 \tag{24}
\end{equation*}
$$

## 4. Experimental Validation

As shown in Figure 11, a laboratory prototype of the EPC was fabricated to verify the ZVS and ZCS in the two-stage DC/DC converter, along with other characteristics. In the converter, there are four power switches: two switches are used in the buck regulator and another two switches are used in the push-pull circuit. The driver transformer is used to isolate the drive signals because the source electrodes of power switches in the buck circuit connect to the non-zero level. The inductances include one buck inductance and two filter inductances in input voltage. CPLD is used to generate control signals and control the sequence relationships.

Dual interleaved drivers are used in the buck circuit, and the driving frequency of the buck regulator is consistent with that of the push-pull circuit. The single-channel drive frequency is 45.2 kHz , and the equivalent switching frequency of the dual interleaved drivers is 90.4 kHz . The drive signals are applied to the power switches of the buck circuit through the drive chip and the isolated drive transformer. Table 1 outlines the parameters.

Table 1. Parameters of the converter.

| Parameter | Value |
| :---: | :---: |
| Input voltage, $V_{i n}$ | 30 V DC |
| Output voltage, | 7000 V DC |
| Rated power, $P_{O}$ | 130 W |
| Buck voltage, $V_{b}$ | 22 V |
| Buck inductance, $L_{b}$ | 75 uH |
| Buck capacitance, $C_{b}$ | 4.4 uF |
| Output capacitance, $C_{O}$ | 47 uF |
| Voltage-doubling rectifier capacitances, $C_{01}$ and $C_{02}$ | 2.2 uF |
| Power MOSFETs, $Q_{1}$ to $Q_{4}$ | IRFB4127 |
| Power diode, $D_{1}$ | DSA30C150 |



Figure 11. Experimental EPC in the laboratory.
Figure 12 shows that ZVS and ZCS can be realized in both the on and off states. The waveforms of both $V_{D S(Q 1)}$ and $V_{D S(Q 2)}$ are approximately trapezoidal, and $I_{Q 1}$ and $I_{Q 2}$ are sinusoidal. There is no voltage spike or overshooting current. The peak voltage of the switches:

$$
\begin{equation*}
V_{p-p}=2 V_{b}=46 \mathrm{~V} \tag{25}
\end{equation*}
$$



Figure 12. Steady-state waveforms of the converter.
The voltage stress is independent of the load. The peak current of the switches:

$$
\begin{equation*}
I_{p-p}=\frac{P_{o}}{V_{b}}\left(1+\frac{1}{\cos \left\{\tan ^{-1}\left[2 \pi f^{2}\left(\frac{T_{o f f}-T_{o n}}{2}\right)^{2}\right]\right\}}\right)=12.64 \mathrm{~A} \tag{26}
\end{equation*}
$$

where $f$ is the operating frequency of dual interleaved drivers, which is $90.4 \mathrm{kHz}, T_{\text {off }}$ is the off time of the switches, which is 14.9 us, while $T_{\text {on }}$ is the on time of the switches, which is 7.38 us.

In the same load condition ( 130 W ), the parasitic capacitance and leakage inductance are used to form the resonant tank. Moreover, another two-stage converter, boost and push-pull, can realize ZVS but cannot realize ZCS. The drain-source voltage also increases and reaches 70 V, as shown in Figure 13.


Figure 13. The waveform of another two-stage converter, boost and push-pull. The load is 130 W .
According to Figure 14, the buck voltage is about 22 V in the two-stage converter.

t ( $5 \mathrm{us} / \mathrm{div}$ )
Figure 14. The waveform of buck voltage, $V_{b}$.

The bus voltage in satellites always varies, but the target of high efficiency never changes. Figure 15 illustrates the variation in efficiency in different input voltages, where Figure 15a illustrates the efficiency when the output power is 130 W, while Figure 15b shows the efficiency when the output power is 75 W . The lower input voltage or the heavier load leads to a higher duty cycle for the buck converter. As a result, the efficiency of the DC/DC converter increases as well. The highest efficiency can be up to $95 \%$.


Figure 15. The efficiencies of the converter in different input voltages for different loads: (a) The efficiencies for 130 W ; (b) The efficiencies for 75 W .

Figure 16 shows the test result of the conducted emission of this two-stage converter in different switching conditions, where Figure 16a presents the test result when the converter worked in hard switching, while Figure 16b shows the result when the converter worked in soft switching. According to the test results of conducted emission, when the converter worked in ZVS and ZCS, the interference of conduction emission was smaller than that in hard switching.


Figure 16. The test result of conducted emission in different switching conditions: (a) The two-stage converter in hard switching; (b) The two-stage converter in soft switching.

## 5. Discussion

According to the experiment results, the buck and push-pull converter works in ZVS and ZCS in both the off and on states. Another two-stage converter, boost and push-pull,
can realize ZVS but not ZCS under the same load condition (130 W), and the drain-source voltage also increases.

Compared with a unipolar topology, this two-stage topology can operate steadily in ZVS and ZCS over a wider input voltage range from 25 V to 40 V . When the input voltage ranges from 24 V to 30 V , unipolar topologies, such as three-transistor push-pull, can realize ZVS and ZCS [12].

Another common two-stage converter is forward and push-pull. The forward and push-pull converter can realize ZCS or zero-current transition (ZCT) using resonant components on the secondary side of the transformer. ZCS causes high current stress, and its efficiency is low. ZCT operates in quasi-resonance mode, which may result in low current stress; the efficiency is relatively higher; and the maximum efficiency is $91.47 \%$ when operating at full load [17]. Compared with forward and push-pull, the buck and push-pull converter can achieve up to $94.5 \%$ efficiency.

However, the two-stage converter has many aspects that need to be improved. In subsequent work, the planar transformer will be considered for a further reduction in volume, and the lower ripple of the output voltage needs to be researched continuously.

## 6. Conclusions

In this paper, a two-stage DC/DC converter, buck and push-pull, was proposed. The proposed power converter was studied based on circuit analysis. In addition, a prototype was built, and the theoretical analysis was validated by the experimental results. The proposed two-stage converter enjoys the following advantages:
(1) All parasitic parameters, including the leakage inductance, magnetizing inductance, and parasitic capacitance, are fully utilized in the proposed two-stage power converter. Only an external resonant capacitance is required for the resonant tank. Therefore, fewer components are needed.
(2) In addition, all power switches, including the main switches and the rectifier diodes, operate under ZVS and ZCS. As a result, the switching loss is minimized, which contributes to the increase in the switching frequency and efficiency. Experimental results show that the efficiency can reach $94.5 \%$.
(3) Furthermore, the EMI issue is improved due to the soft switching advantages, which was validated by the experimental results.

In conclusion, a two-stage power converter was proposed, where the first stage is a buck converter and the second stage is a resonant push-pull converter. The working principles and the calculations of the main parameters were researched. The theoretical analysis was validated by a prototype. The experimental results show that the proposed topology is suitable for high-voltage, high-efficiency applications.

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## Nomenclature

The following is a list of symbols used in this paper and their meanings.
DC
Direct-current main
$Q_{1}$ to $Q_{4}$
$C_{Q 1}$ to $C_{Q 4}$
Power switches
The sum of parasitic output capacitance of semiconductor and external
parallel capacitance
$D_{Q 1}$ to $D_{Q 4} \quad$ Body diode
$D_{1} \quad$ Power diode of buck regulator
$L_{b} \quad$ Inductance of buck regulator
$C_{b} \quad$ Capacitance of buck regulator
T Transformer
$L_{p} \quad$ Equivalent primary leakage inductance of transformer
$I_{L p} \quad$ Current of equivalent primary leakage inductance
$C_{p 1}, C_{p 2}$
Winding capacitance of transformer
$L_{m 1}$ to $L_{m 3} \quad$ Magnetizing inductance
$N_{1}$ to $N_{3}$
$D_{01}, D_{02}$
Transformer turns
Voltage-doubling rectifier diode
$C_{01}, C_{02} \quad$ Voltage-doubling rectifier capacitance
$I_{c o 1}, I_{c o 2} \quad$ Current of voltage-doubling rectifier capacitance
$C_{0} \quad$ Output capacitance
$R_{o} \quad$ Output resistance
$V_{0} \quad$ Output voltage
$I_{Q 1}, I_{Q 2} \quad$ Commutated current of power switches in push-pull regulator
$V_{D S}\left(Q_{1}\right), V_{D S}\left(Q^{2}\right) \quad$ Drain-source voltage of power switches
$V_{G S}(Q 1) \quad$ Gate-source voltage of power switch

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