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A New High-Gain DC-DC Converter with Continuous Input Current for DC Microgrid Applications

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Abstract: The growth of renewable energy in the last two decades has led to the development of new power electronic converters. The DC microgrid can operate in standalone mode, or it can be grid-connected. A DC microgrid consists of various distributed generation (DG) units like solar PV arrays, fuel cells, ultracapacitors, and microturbines. The DC-DC converter plays an important role in boosting the output voltage in DC microgrids. DC-DC converters are needed to boost the output voltage so that a common voltage from different sources is available at the DC link. A conventional boost converter (CBC) suffers from the problem of limited voltage gain, and the stress across the switch is usually equal to the output voltage. The output from DG sources is low and requires high-gain boost converters to enhance the output voltage. In this paper, a new high-gain DC-DC converter with quadratic voltage gain and reduced voltage stress across switching devices was proposed. The proposed converter was an improvement over the CBC and quadratic boost converter (QBC). The converter utilized only two switched inductors, two capacitors, and two switches to achieve the gain. The converter was compared with other recently developed topologies in terms of stress, the number of passive components, and voltage stress across switching devices. The loss analysis also was done using the Piecewise Linear Electrical Circuit Simulation (PLCES). The experimental and theoretical analyses closely agreed with each other.

Keywords: voltage stress; distributed generation (DG); high gain; quadratic boost

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1. Introduction

In recent years, the development of electricity-generation systems with nonconventional energy sources has called for a new generation of high-gain DC-DC converters [1]. High-gain converters can be nonisolated or isolated. Transformerless topologies are becoming important in medium power applications up to 400–500 W due to their low cost and good efficiency. Conventional topologies of a DC-DC converter, like boost, SEPIC, and ZETA, have a simple structure, but their efficiency is low and for achieving high gain they need to be operated at high duty ratios, which leads to a substantial increase in the stress across the switching devices. Several topologies of high-gain DC-DC converters have been developed by researchers. Each of the configurations has its advantages and disadvantages. Usually, switched capacitors, voltage multiplier cells (VMCs), and switched inductors are used for increasing the gain. Common ground, isolation, and high efficiency are the key features that are available in isolated topologies [2] for high-power applications. High-gain

non-isolated converters can also be used in microgrid applications with a bidirectional power flow [3]. In [4], a new non-isolated switched-capacitor based new boost converter was proposed by the authors. The converter utilized two inductors and a single switch, but the gain was limited. The PV system mostly requires a step-up converter to enhance voltage by utilizing the MPPT tracking function. In [5], a new improved boost converter for renewable energy applications was proposed by the authors. In [6,7], a new high-gain boost and SEPIC converter with a continuous input current are proposed by the authors. Many techniques have been developed to enhance the gain with lower price and higher efficiency. A generalized structure of a high gain DC-DC converter with a single switch and switched inductors is proposed in [8]. The boost converter gain has been increased by using the quadratic boost technique with high component voltage stress [9]. Despite that, the output voltage was equal to the voltage stress. As a result, a higher rated switch was used to compensate for the voltage stress on the provided switch, making excessive conduction loss [10]. The quadratic boost converter can produce high voltage without extreme duty ratios. The conventional quadratic boost converter (CQBC) proposed in [11] had a single switch with a voltage stress equal to V_O. In [12], a voltage doubler circuit was introduced by the authors. With the help of diodes and switched capacitors, the voltage at the output could be increased significantly. In [13], a new DC-DC Luo converter having positive output voltage was introduced. Only switched capacitors and diodes were employed for increasing gain. Coupled inductor-based topologies are also popular to achieve very high gain. To achieve the desired gain, the coupled inductor's turn ratio is adjusted, but this results in higher input current ripple. The high-gain converters proposed in [14–17] addressed the problems associated with coupled inductor topologies. New boost converters with a voltage multiplier cell (VMC) were proposed by the authors in [18–20]. VMC can be incorporated with conventional converters like boost, SEPIC, and conventional quadratic boost (CQBC) to increase the gain. A VMC employing switched capacitors suffers from the problem of high charging current, which results in additional power losses. Moreover, the number of components also increases when a VMC is used, leading to an increase in the cost and decrease in the reliability of the converter. Another family of converters are interleaved boost converters. These converters produce high gain at smaller duty ratios. An interleaved converter needs several VMCs [21–24] at the output to increase the voltage. In [25], a three-port DC-DC converter suitable for solar PV applications was proposed by the authors. In [26], an extendable switched inductor based high-gain converter was proposed by authors. The converter in [26] had continuous input current and reduced stress across switches, but many inductors were used to achieve high gain. In [27], a new hybrid switched-capacitor high-gain converter for DC microgrids was proposed. In [28], a modified SEPIC converter was proposed for solar PV applications. In [29], a boost converter with a VMC was explained and discussed. However, the converter had many voltage-multiplier levels, but the converter still provided low voltage gain. A new high-gain converter with built-in transformers and a VMC was proposed in [30]. In [31], a non-isolated high-gain converter with switched capacitors and voltage doublers was proposed by the authors. In [32], a new QBC with a voltage doubler and a single switch was proposed by the authors. Some other recently developed high-gain converters have been proposed by authors in [33–35]. Although these converters have high gain, the number of passive components is high. The main novelty of the converter proposed in the current study is that it has a quadratic gain with only four passive elements. The other features of the converter are:

- Continuous input current;
- Quadratic voltage gain with reduced voltage stress across switches;
- High efficiency and easy control.

In subsequent sections, the workings of the proposed converter is discussed. Experimental results and efficiency of converter are reported in Sections 5 and 6. The conclusions are discussed in Section 7.

2. Structure and Working of the Proposed Converter

The circuit diagram of the proposed converter is shown in Figure 1. The control signal is the same for both the switches. Based on the control signal, there are two modes of operation; that is, switch-on mode of operation and switch-off mode of operation. The modes of operations can be explained as follows:

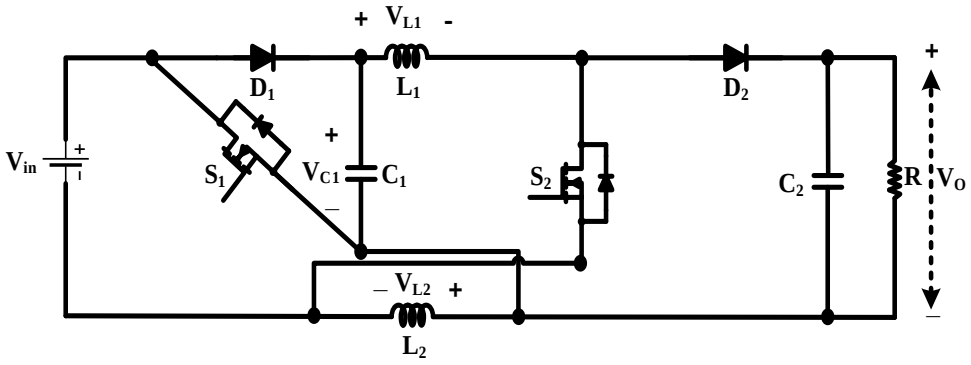


Figure 1. The proposed converter.

Mode 1: Both the switches are turned ON simultaneously, and hence diodes D_1 and D_2 are reverse-biased. The conduction diagram is given in Figure 2. In this operation mode, both the capacitors discharge and transfer their energy to the inductors and to the load, respectively, while both inductors store energy, and the inductor current subsequently increases linearly.

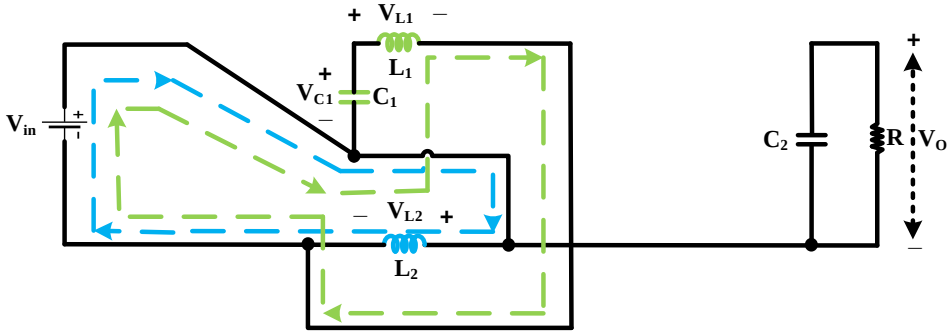


Figure 2. Conduction diagram for the first mode of operation.

The governing equations for the first mode are as follows:

$$V_{L1} = V_{in} + V_{C1} \tag{1}$$

$$V_{L2} = V_{in} \tag{2}$$

Mode 2: The switches are turned OFF, and both the diodes conduct. Both the capacitors are charged during this mode of operation, while the energy of both the inductors is transferred to the load as their current decreases. The conduction diagram is shown in Figure 3. The equations for this mode are as shown below:

$$V_{L1} = V_{C1} - V_O \tag{3}$$

$$V_{L2} = V_{in} - V_{C1} \tag{4}$$

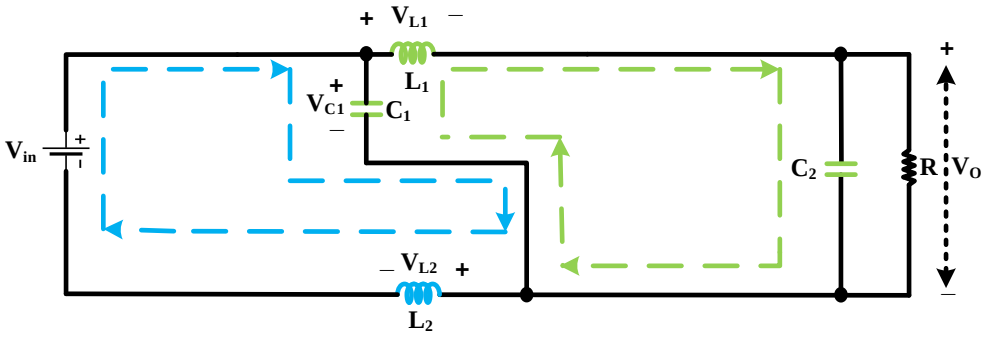


Figure 3. Conduction diagram for the second mode of operation.

Applying the principle of volt-sec balance in inductor L_2 and L_1:

$$\int_0^T V_{L2}(t) \cdot dt = 0 \tag{5}$$

$$V_{in} \times DT + (V_{in} - V_{C1}) \times (1 - D)T = 0 \tag{6}$$

$$V_{C1} = \frac{V_{in}}{1 - D} \tag{7}$$

$$\int_0^T V_{L1}(t) \cdot dt = 0 \tag{8}$$

$$(V_{in} + V_{C1}) \times DT + (V_{C1} - V_O) \times (1 - D)T = 0 \tag{9}$$

From Equations (7) and (9), the gain (M) is written as:

$$M = \frac{V_o}{V_{in}} = \frac{(1 + D - D^2)}{(1 - D)^2} \tag{10}$$

From Equation (10), it can be inferred that the voltage gain of the proposed converter is quadratic.

3. Design of Passive Components and Stress across Switches

3.1. Design of Inductors

Rewriting the equation of the first mode of operation in a differential form, we get:

$$L_1 \frac{dI_{L1}}{dt} = V_{in} + V_{C1}, \quad L_2 \frac{dI_{L2}}{dt} = V_{in} \tag{11}$$

$$\Delta I_{L1} = \frac{(V_{in} + V_{C1})DT}{L_1}, \quad \Delta I_{L2} = \frac{V_{in}DT}{L_2} \tag{12}$$

After combining Equations (7) and (12), we get:

$$\Delta I_{L1} = \frac{V_{in}(2 - D)DT}{(1 - D)L_1} \tag{13}$$

The average current through L_1 and L_2 are:

$$I_{L1} = \frac{V_O}{R(1 - D)}, \quad I_{L2} = \frac{V_O(2D - D^2)}{R(1 - D)^2} \tag{14}$$

The minimum current through the inductors are as follows:

$$(I_{L1})_{Min} = \frac{V_O}{R(1 - D)} - \frac{V_{in}(2 - D)DT}{2(1 - D)L_1} \tag{15}$$

$$(I_{L2})_{Min} = \frac{V_O(2D - D^2)}{R(1-D)^2} - \frac{V_{in}DT}{L_2} \tag{16}$$

For the continuous conduction operation mode, the minimum inductance required can be calculated as given:

$$L_1 \geq \frac{(2-D)D(1-D)^2R}{f_s(1+D-D^2)} \tag{17}$$

$$L_2 \geq \frac{D(1-D)^4R}{f_s(1+D-D^2)} \tag{18}$$

3.2. Design of Capacitor

The selection of a capacitor depends on the minimum permissible ripple in the voltage across the capacitor. The charge stored by the capacitor is as follows:

$$\Delta Q = C\Delta V_C \tag{19}$$

$$I_C\Delta T = C\Delta V_C \tag{20}$$

when the switch is ON, the current through each capacitor is as follows:

$$(I_{C1})_{ON} = \frac{Vo}{R(1-D)}, \ (I_{C2})_{ON} = \frac{Vo}{R} \tag{21}$$

After combining (20), (21), and (10), the value of capacitors can be calculated as follows:

$$C_1 = \frac{V_{in}(1+D-D^2)D}{R(1-D)^3\Delta V_{C1}f_s} \tag{22}$$

$$C_2 = \frac{V_{in}(1+D-D^2)D}{R(1-D)^2\Delta V_{C2}f_s} \tag{23}$$

3.3. Voltage Stress across Switches

The voltage stress across the various components is given by (24) and (25). It can be seen from (24) and (25) that stress across the switch S_1 and S_2 is less than V_O.

$$V_{S1} = \frac{V_{in}}{1-D} = \frac{V_O(1-D)}{(1+D-D^2)} \tag{24}$$

$$V_{S2} = \frac{V_{in}}{(1-D)^2} = \frac{V_O}{(1+D-D^2)} \tag{25}$$

The related waveforms during continuous conduction mode are shown in Figure 4.

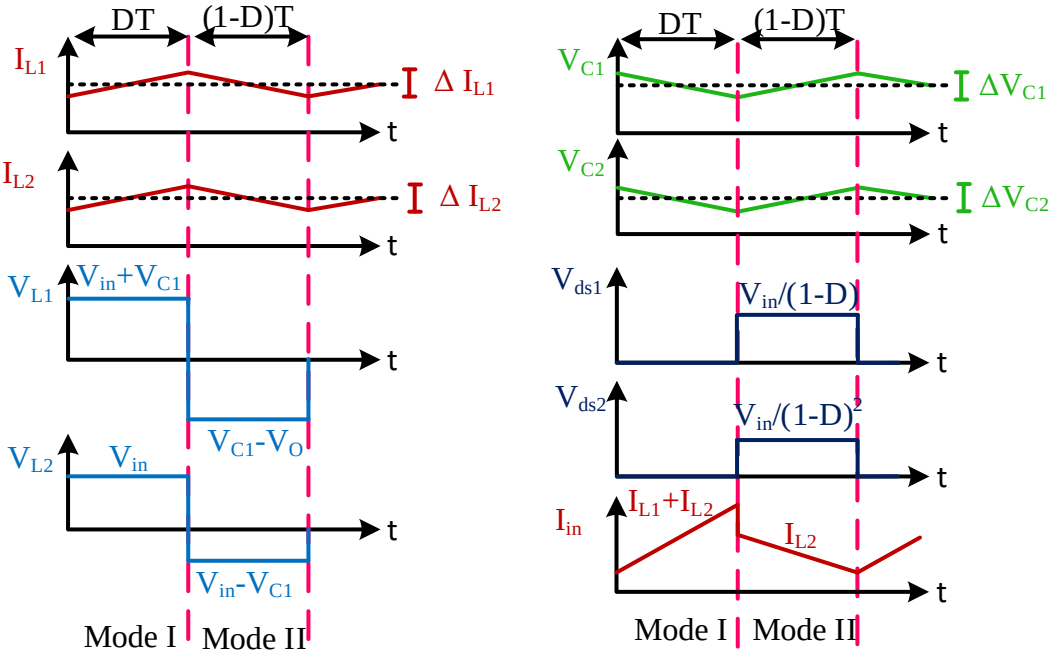


Figure 4. Related waveforms in CCM.

4. Comparison Assessment with Other Converters

In this section, the high-gain boost converter presented in this paper is compared. The comparison is shown in Table 1. The converter given in [4] had 2 inductors (L), 3 capacitors (C), and a single switch (S), but has lower gain than the presented converter. The converter given in [6] had a total number of 10 components with two inductors and 4 diodes, but its voltage gain was only 3.5 at a duty ratio of 0.5, whereas at D = 0.5, our proposed topology has a gain of 5.3. The modified buck-boost topology proposed in [7] had 4 inductors, 6 capacitors, and 3 diodes, but the substantial gain could be achieved only by operating it at high duty ratios. To obtain a gain of 15, the converter proposed in [7] needed to be run at 0.8 duty, whereas the converter presented here achieve a gain of more than 30 times at the same duty ratio. The switched inductor topology proposed in [9] employed a VMC made of diodes and an inductor for increasing the converter gain; 7 diodes and 4 inductors were utilized for increasing the converter gain, but the gain was still less than our proposed converter. The quadratic buck-boost converter proposed in [10] had the advantage of common ground, but the gain was not very high, and the input current was discontinuous, which made it unsuitable for solar PV applications. The conventional quadratic boost converter (CQBC) [11] also had two inductors, but its gain was low and the switch had voltage stress, which is equal to V_O. Similarly, the converter proposed in [28] had three inductors and three capacitors; still, the gain was limited and stress across the switch was high. As can be observed in Figure 5, our proposed high-gain structure has a gain of 8 times at D = 0.6. The gain rapidly increases from 0.7 to 0.8 duty ratio. Apart from higher gain, the converter utilizes only 8 components, and hence losses in the ON state and parasitic resistance would be low. Figure 6 gives the normalized voltage stress across the switch of the converter. It can be observed that the two switches of the converter had different voltage stresses across them. As compared with other structures, the switch S_1 had the lowest stress across it. The stress across switch S_2 was less than V_O but was higher than S_1. Further, it can be observed that the stress across S_2 also was less than in the converters proposed in [28] and the conventional quadratic boost converter (CQBC) proposed in [11].

Table 1. Comparison of the proposed converter with similar topologies.

Topology	Inductors	Capacitors	Switches	Diodes	Total Components	Voltage Gain (V_o/V_{in})	Normalized Voltage Stress (V_S/V_{in})
[4]	2	3	1	3	9	$\frac{1+D}{(1-D)}$	$\frac{1}{1-D}$
[6]	2	3	1	4	10	$\frac{3+D}{2(1-D)}$	$\frac{1}{1-D}$
[7]	4	6	1	3	14	$\frac{3D}{(1-D)}$	$\frac{1}{1-D}$
[9]	4	1	2	7	14	$\frac{1+3D}{(1-D)}$	$\frac{1+D}{1-D}$
[10]	2	2	1	3	8	$\frac{D(2-D)}{(1-D)^2}$	$\frac{2}{(1-D)}$
[11]	2	2	1	3	8	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$
[28]	3	3	1	3	9	$\frac{D}{(1-D)^2}$	$\frac{D}{(1-D)^2}$
Proposed	2	2	2	2	8	$\frac{1+D-D^2}{(1-D)^2}$	$S_1[\mathrm{P}] = \frac{1}{1-D}$ $S_2[\mathrm{P}] = \frac{1}{(1-D)^2}$

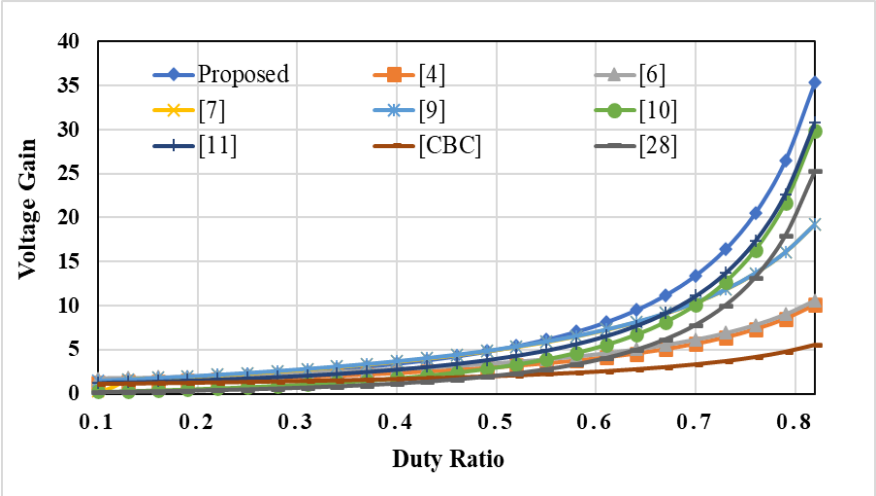


Figure 5. Comparision of the Voltage gain for different converters.

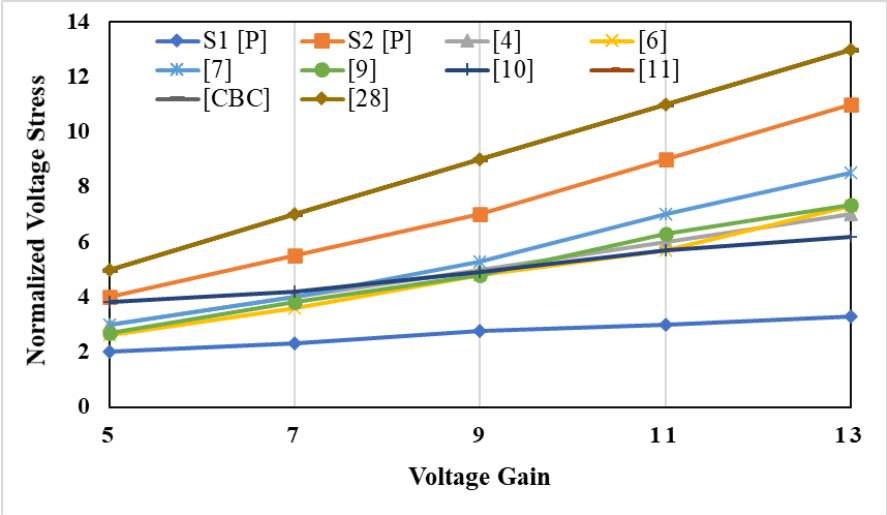


Figure 6. Comparison of stress across the switches.

5. Experimental Results

Table 2 shows the specifications of the presented converter. The simulation results were validated by running it on a hardware prototype. The working of the converter was tested by building a 150 W prototype as given in Figure 7. The prototype was operated at a 0.4 duty ratio. From Figure 8a, the output voltage V_O was equal to 80 V, which was proximate to the theoretical value. The voltage across the capacitor was found to be 40 V, which was half the V_O. The converter was operating in continuous conduction mode, as evident from the waveforms of the inductor currents shown in Figure 8b. The voltage stress across switch S_1 was found to be 40 V, and the stress across the switch S_2 was found to be 65 V, as observed in Figure 8c. The stress across both switches was less than V_O, which was an improvement over the other conventional topologies, thereby improving the efficiency. The converter had a continuous input current, which is its main advantage. The average input current I_{in} and output current I_O were found to be 1.5 A and 0.4 A, respectively. Furthermore, the input current had a very low voltage ripple, which eliminated the need for any input filter.

Table 2. Ratings of components.

Elements	Rating/Model
V_{in}	24 V, 10 V
P_o (max)	150 W
f_s	50 kHz
R (Load)	250 Ω, 300 Ω
Inductors	$L_1 = L_2 = 330$ µH, ESR = 0.2 Ω
Capacitors	$C_1 = C_2 = 33$ µF 200 V, ESR = 0.15 Ω
S_1 and S_2	SPW52N50C3
D_1 and D_2	SF8L60USM
Gate Drivers IC	TLP250H
Microcontroller	STM32 Nucleo H743ZI2

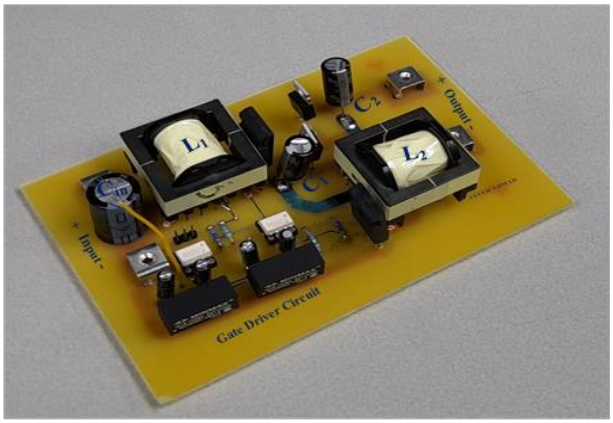
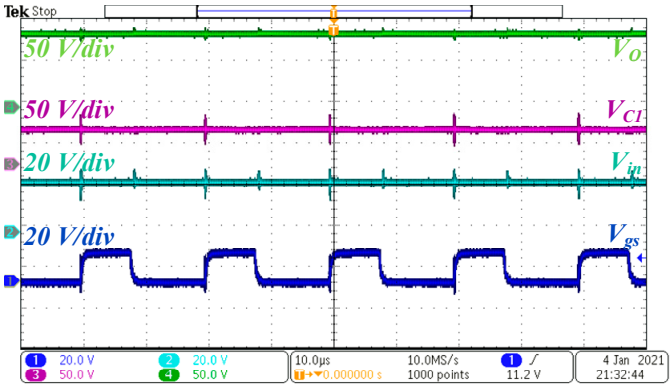
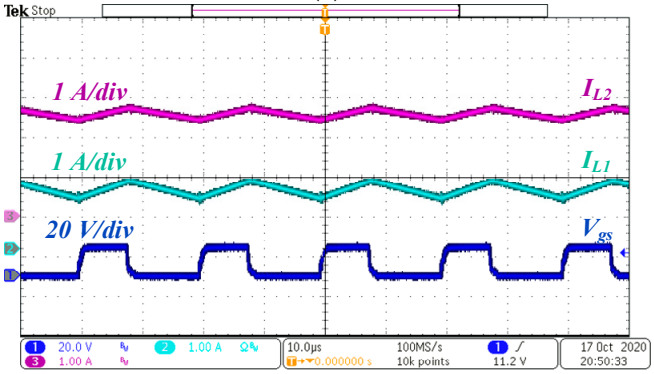


Figure 7. Prototype of the proposed converter.

Figure 9a shows the experimental results at a duty ratio of 0.65 and input voltage of 10 V, and it was found that the output voltage was almost 100 V, which also verified the calculated gain of 10 times. The voltage across the capacitor C_1 was 27 V, which was almost the same as that of the calculated value. The inductor currents and voltage across switches are shown in Figure 9b,c.



(**a**)



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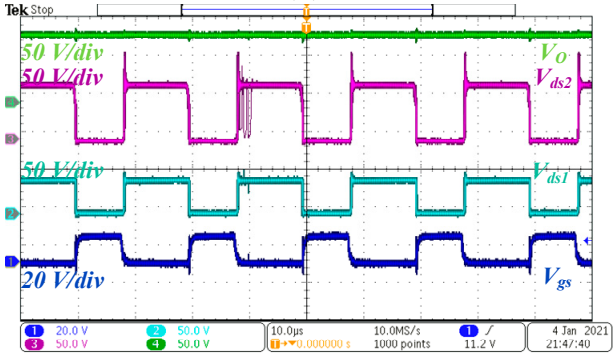
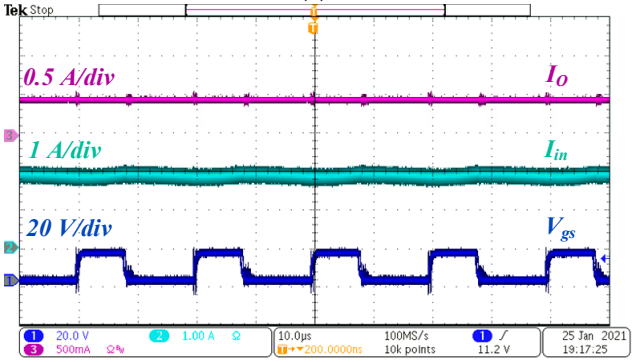


(**c**)



(**d**)

Figure 8. Experimental results at V_{in} = 24 V, D = 0.4. (**a**) V_O, V_{C1}, and V_{in}. (**b**) I_{L1} and I_{L2}. (**c**) V_O, V_{ds1}, and V_{ds2}. (**d**) I_o, I_{in}, and V_{gs}.

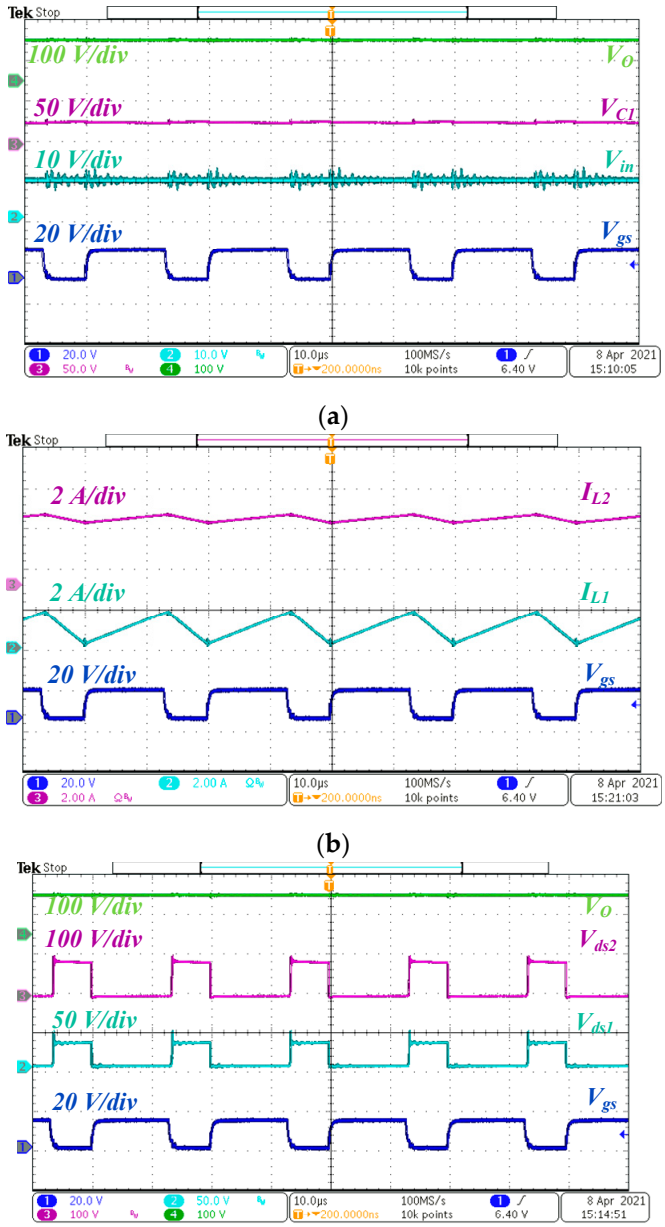


Figure 9. Experimental results at V_{in} = 10 V, D = 0.65. (**a**) V_O, V_{C1}, and V_{in}. (**b**) I_{L1} and I_{L2}. (**c**) V_O, V_{ds1}, V_{ds2}.

6. Efficiency Calculation

In this section, the power loss in different components of the converter is calculated. The power loss in the converter occurs because of parasitic resistances of inductor capacitors and ON-state resistance of switches and diodes.

Power loss in inductors: Neglecting the ripple in the current, the RMS and average current flowing in inductor can be assumed to be the same. The power loss due to parasitic resistance of inductors is as shown in (26):

$$P_{L1} = \frac{{V_O}^2 r_{L1}}{R^2(1-D)^2}, \qquad P_{L2} = \frac{{V_O}^2(2D-D^2)^2 r_{L2}}{R^2(1-D)^4} \tag{26}$$

where r_{L1} and r_{L2} are parasitic resistances of inductors.

Power loss in capacitors: Similarly, the loss in capacitors due to ESR is as given below:

$$P_{C1} = i^2_{C1_{RMS}}\, r_{C1}$$
$$P_{C1} = \frac{{V_O}^2 D r_{C1}}{R^2(1-D)^3} \tag{27}$$

$$P_{C2} = i^2_{C2_{RMS}}\, r_{C2}$$
$$P_{C2} = \frac{{V_O}^2 D r_{C2}}{R^2(1-D)} \tag{28}$$

Power loss in diodes: By knowing the RMS current, the average current of the total power loss across each diode is calculated as follows:

$$P_{D1} = V_D i_{D1_{avg}} + i^2_{D1_{RMS}}\, r_{D1}$$
$$P_{D1} = \frac{V_D V_O}{R(1-D)} + \frac{{V_O}^2 r_D}{R^2(1-D)^4} \tag{29}$$

$$P_{D1} = V_D i_{D1_{avg}} + i^2_{D1_{RMS}}\, r_{D1}$$
$$P_{D2} = \frac{V_D V_O}{R(1-D)} + \frac{{V_O}^2 r_D}{R^2(1-D)} \tag{30}$$

where V_D is the voltage drop across the diode.

Power loss in the switch: There are two types of switch losses: conduction loss ($P_{sw_{Cond}}$) and switching loss (P_{sw}). These losses can be calculated as follows:

$$P_{sw} = P_{sw_{Cond}} + P_{sw_{ON}} + P_{sw_{OFF}} \tag{31}$$

$$P_{sw_{Cond}} = {I^2}_{sw_{RMS}} r_{sw_{ON}} \tag{32}$$

where $r_{sw_{ON}}$ is ON-state resistance of MOSFET.

$$P_{sw1_{Cond}} = \frac{{V_O}^2 \left(2D - D^2\right)^2}{R^2(1-D)^4 D} r_{sw_{ON}} \tag{33}$$

$$P_{sw2_{Cond}} = \frac{{V_O}^2}{R^2(1-D)^2} r_{sw_{ON}} \tag{34}$$

$$P_{sw_{ON}} = \frac{I_{sw_{ON}} V_{DD}}{2} \times \frac{t_{ri} + t_{fv}}{2} \times f_s \tag{35}$$

$$P_{sw1_{ON}} = \frac{V_O\left(2D - D^2\right) V_{in}}{2R(1-D)^3} \times \frac{t_{ri} + t_{fv}}{2} \times f_s \tag{36}$$

$$P_{sw2_{ON}} = \frac{V_O V_{in}}{2R(1-D)^3} \times \frac{t_{ri} + t_{fv}}{2} \times f_s \tag{37}$$

$$P_{sw1_{OFF}} = \frac{V_O\left(2D - D^2\right) V_{in}}{2R(1-D)^3} \times \frac{t_{fi} + t_{rv}}{2} \times f_s \tag{38}$$

$$P_{sw2_{OFF}} = \frac{V_O V_{in}}{2R(1-D)^3} \times \frac{t_{fi} + t_{rv}}{2} \times f_s \tag{39}$$

where: $\frac{t_{ri}+t_{fv}}{2}$ is turn ON time;
$\frac{t_{fi}+t_{rv}}{2}$ is turn OFF time; and
f_s is switching frequency.

To find the actual output voltage equation, we can combine all the losses and apply the law of conservation of power. A simplified output voltage equation considering only inductor and capacitor losses is provided in (40):

$$V_O = \frac{\left[V_{in}(1-D)\left(1+D-D^2\right)\right]R(1-D)}{R(1-D)^4 + r_{L1}(1-D)^2 + r_{L2}(4D^2+D^2-4D^3) + r_{C1}D(1-D) + r_{C2}D(1-D)^3} \quad (40)$$

Equation (40) can be verified by using the values of parameters from Table 2. The value of V_O is found to be 82.1 V for V_{in} = 24 V and D = 0.4, which is very close to the experimental value of 80 V.

$$V_O = \frac{\left[24(1-0.4)\left(1+0.4-0.4^2\right)\right](300)(1-0.4)}{39+0.072+0.0272+0.036+0.013} = 82.1\ V \quad (41)$$

The bifurcation of losses in converter is shown in Figure 10. The total losses in the MOSFETs accounted for 40% of the total losses. The total losses in diodes were 31%. In Figure 11, efficiency of converter is plotted at different values of input voltages. At low input voltages, the peak efficiency was found to be low. This is because high current flows in the circuit for achieving the same output power, and hence more losses occurred in the converter. The converter efficiency was high if the input voltages were between 24 and 40 V. Usually, the output from the solar PV module is 24 V. Hence, the proposed converter may be applied for stepping-up the voltage with high efficiency in the power range of 200–300 W.

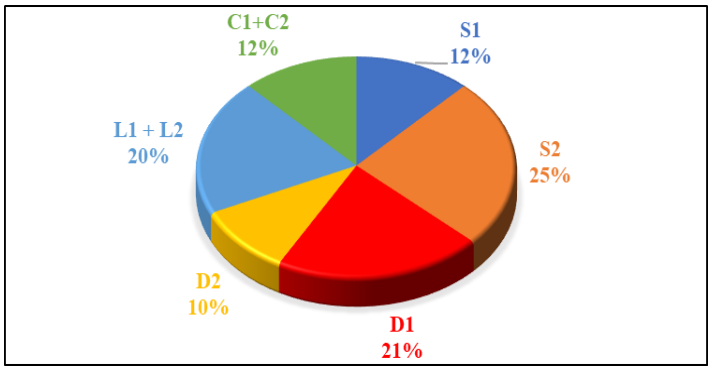


Figure 10. The breakup of losses of the proposed converter at 25 W output.

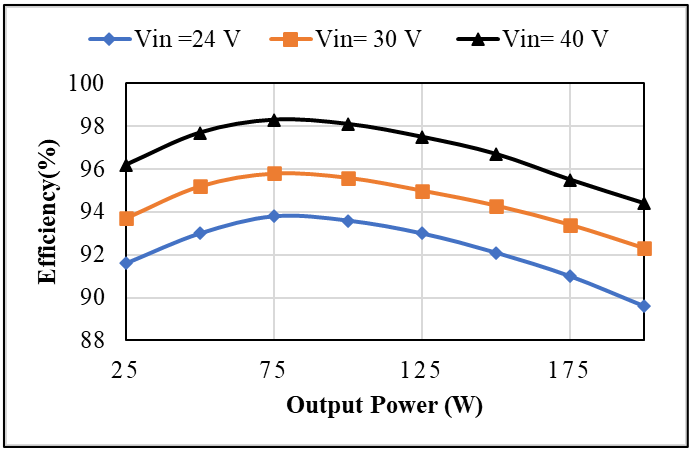


Figure 11. Efficiency of converter at different input voltages.

7. Conclusions

A new high-gain converter was proposed and analyzed. The proposed converter utilized only a total of eight components to achieve high quadratic voltage gain. Usually, converters that produce quadratic voltage gain utilize more than three inductors and several diodes. The converter has a continuous input current, which is its main feature as it increases the life of solar PV panels. A hardware prototype of 150 W was developed in laboratory. Experimental results validated the workings and performance of converter. The converter was superior to quadratic boost, conventional boost, and other high-gain converters in terms of gain and voltage stress across switch. The peak efficiency of the converter was found to be 93.7% for V_{in} = 24 V. The merits of converter make it worthy for renewable energy applications for an output power in the range of 200–300 W.

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