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Fault Simulations in a Multiterminal High Voltage DC Network with Modular Multilevel Converters Using Full-Bridge Submodules

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Abstract: The concept of high-voltage DC transmission using a multiterminal configuration is presently a central topic of research and investment due to rekindled interest in renewable energy resource integration. Moreover, great attention is given to fault analysis, which leads to the necessity of developing proper tools that enable proficient dynamic simulations. This paper leverages models and control system design techniques and demonstrates their appropriateness for scenarios in which faults are applied. Furthermore, this paper relies on full-bridge submodule topologies in order to underline the increase in resilience that such a configuration brings to the multiterminal DC network, after an unexpected disturbance. Therefore, strong focus is given to fault response, considering that converters use a full-bridge topology and that overhead power lines connect the terminals.

Keywords: full-bridge circuit; modular multilevel converters; high-voltage direct current transmission; multiterminal grid



Citation: Damian, I.-C.; Eremia, M.; Toma, L. Fault Simulations in a Multiterminal High Voltage DC Network with Modular Multilevel Converters Using Full-Bridge Submodules. *Energies* **2021**, *14*, 1653. <https://doi.org/10.3390/en14061653>

Academic Editor: Gianfranco Chicco

Received: 4 February 2021

Accepted: 11 March 2021

Published: 16 March 2021

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1. Introduction

Presently, there is a growing interest towards renewable sources and the integration of such sources in the power system. This interest is even more strongly underlined by the increasing number of electric vehicles, which leads to an increase in electricity demand. Since the goal of the electric vehicle industry is to provide a cleaner environment by reducing CO₂ emission, it is not acceptable to generate needed power from coal (or even gas) power plants. Therefore, investments in hydroelectric, solar and wind power plants is encouraged [1,2]. However, such plants are seldom near large electricity consumers. Besides investments in new power plants, additional investment is needed for transmission systems. Because of the significant distance between generation plants and large consumers, the best technical and economical solution is the use of high-voltage direct current transmission (HVDC), in a multiterminal layout.

Due to frequent routing restrictions (available construction space, terrain difficulties, etc.), a combination of overhead and underground power lines must be used. Such configurations result in exposure to environmental conditions (which can lead to sudden faults). In order to address this problem, there are three possible solutions [3–5].

The first considers the use of circuit breakers on the AC side of the converter to limit fault currents. This approach uses mature technology, but is not appropriate for multiterminal HVDC, because it leaves the entire DC network offline.

The second solution corresponds to the deployment of DC circuit breakers (DCCB). However, such a circuit breaker is extremely expensive, and the technology is not mature enough. There are three types of possible DC circuit breaker topologies: mechanical HVDC circuit breaker (with passive resonance or active resonance), hybrid DCCB and pure solid-state DCCB. Presently, the maximum voltage rating of a mechanical DCCB is 550 kV, and the maximum rating of hybrid DCCBs is 200 kV (in Zhoushan project [6]). There are

no solid-state DCCBs in commissioned HVDC projects, and all existing solutions are only experimental. The interrupt current rating is up to 5 kA.

The third solution proposes the use of modular multilevel converters (MMCs) which have full-bridge submodules. Such topologies have the inherent ability to limit fault currents. Therefore, these are preferred in configurations which make use of overhead lines, even though conduction losses are higher compared to the full-bridge MMC.

In the following paragraphs, this paper continues on the path established in [7,8], regarding the use of a straight-forward detailed equivalent model for MMC-HVDC converters, in conjunction with an efficient vector control approach, in order to evaluate the performance of converters with full-bridge circuits, during fault conditions. This analysis is centered around a multiterminal configuration, and it is motivated by an increased worldwide tendency to expand the concept of HVDC towards a grid/radial network structure. Finally, some simulations with fault conditions are shown (all simulations are generated in Matlab/Simulink).

2. Model of MMC-HVDC with Full-Bridge Submodules

An MMC-HVDC converter consists of a several submodules (SMs), connected in series, which form the upper or lower arm. The full-bridge submodule consists of several insulated gate bipolar transistors (IGBTs) with antiparallel diodes and a capacitor (Figure 1). This SM distinguishes itself from other topologies by the increased number of possible output voltage levels. These levels can be grouped in two categories: voltage levels which can be obtained during normal operation (0 and V_C), and a voltage level which can be used during fault conditions ($-V_C$).

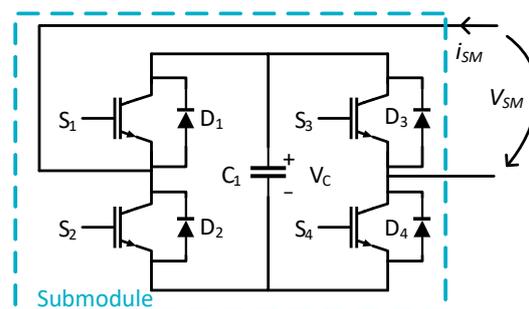


Figure 1. Representation of a full-bridge submodule [8].

There are multiple ways in which an MMC can be modelled. The most popular methods are the average value model (AVM) and the detailed equivalent model (DEM) [9,10]. For dynamic simulations, the most appropriate method is DEM, because it provides sufficient detail and access to individual submodules. This is important in the context of controller design, as well as for capacitor balancing.

DEM approaches converter modelling through a “one resistor, one voltage source” technique for every SM [10,11]: each IGBT with antiparallel diodes ($S_1 \dots S_4$ & $D_1 \dots D_4$) is replaced by a resistor ($R_1 \dots R_4$), and the capacitor (C_1) is modelled, using the Trapeze method, by a voltage source ($V_{c,eq}$) in series with a resistor (R_c). The IGBT equivalent resistances will have values depending on the state of the switches, with a high value in *off* state and a low value in *on* state.

Using the Thevenin technique, as well as star–delta conversions, it is possible to finally obtain a submodule equivalent resistance $R_{SM,eq}$ and an equivalent voltage source $V_{SM,eq}$, as detailed in [7,8].

Considering $R_{SM,eq}$ and $V_{SM,eq}$ for all submodules, as well as the multivalve current I_{MV} , with the help of the equivalent resistance R_{arm} in (1) and the equivalent voltage V_{eq} in (2), the converter voltage V_{MV} is defined as in (3).

$$R_{arm}(t) = \sum_{i=1}^{nrSM} R_{SMi,eq}(t) \quad (1)$$

$$V_{eq}(t - \Delta T) = \sum_{i=1}^{nrSM} V_{SMi,eq}(t - \Delta T) \quad (2)$$

$$V_{MV}(t) = R_{arm}(t)I_{MV}(t) + V_{eq}(t - \Delta T) \quad (3)$$

3. Converter Control System Design

Each converter in a multiterminal network can have various modes of operation, but at least one converter station should control the DC voltage. There is also a possibility to control the DC voltage using multiple converters, with voltage droop control or voltage margin control, and it is more appropriate to multiterminal networks that have more than three converters [12] (this will not be applied in the case study section).

There are two main approaches to converter control: direct control or vector control. The latter is preferred, due to a more streamlined approach to controller tuning. As such, using Clarke and Park transformation, a system consisting of two axes is obtained. Moreover, it is possible to independently control parameters such as active and reactive power due to this separation on two axes [13], using the direct and quadrature currents.

In order to develop the vector control loops, it is necessary to use a simplified converter model, which is shown in Figure 2.

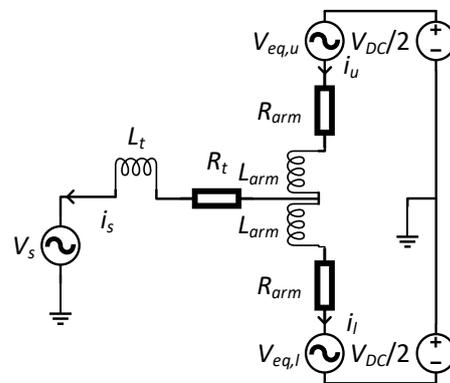


Figure 2. One-phase representation of a simplified converter model [7].

L_{arm} represents the arm inductor, R_t represents the transformer resistance and L_t represents the transformer inductance. V_s is the AC network equivalent voltage and V_{DC} represents the DC network equivalent voltage. Nevertheless, i_u is the upper arm current, i_l is the lower arm current and i_s is the AC network current.

Of use in this paper are three outer control loops (active power, reactive power and DC voltage) and two inner current control loops. A summary of the control layer, with connection to the model layer, is shown in Figure 3.

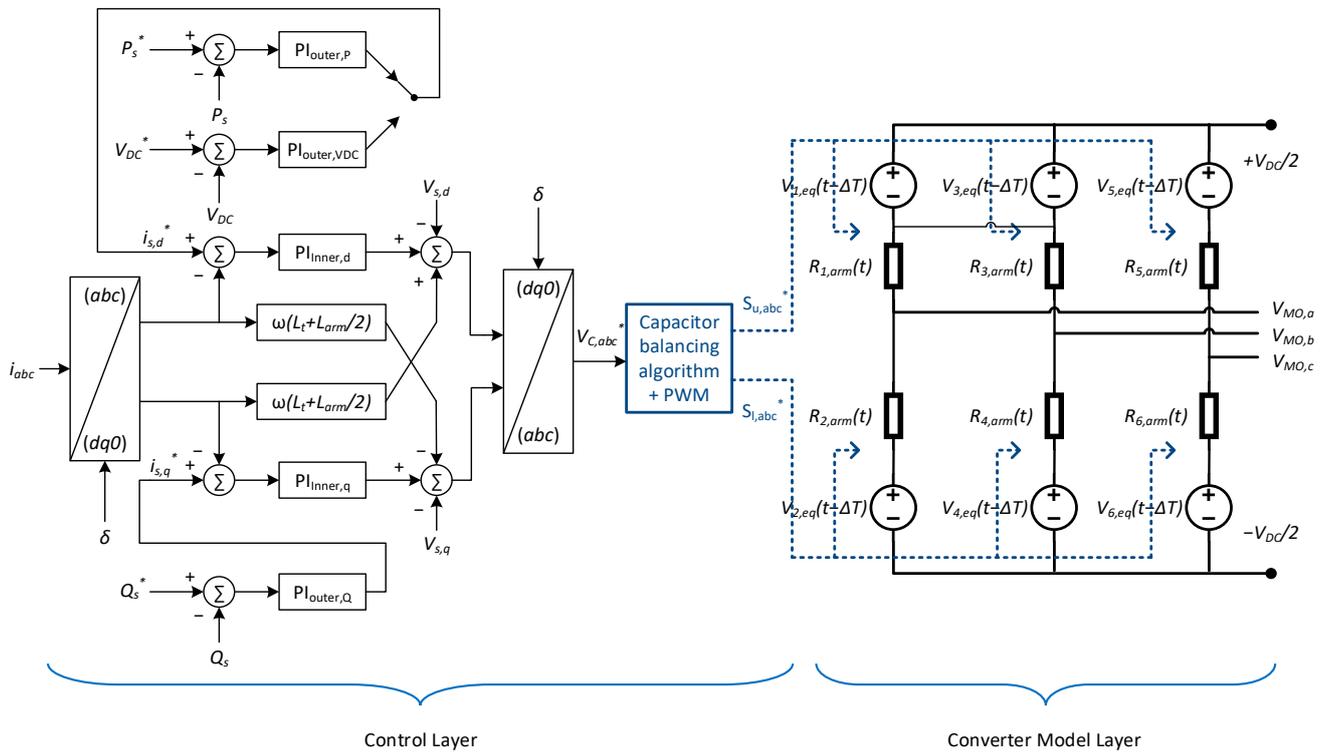


Figure 3. Interaction between the control layer and the converter model layer.

By applying the modulus optimum criterion in the tuning process of all these loops, with the consideration that there should be a delay for the outer control loops in order to ensure stable operation, it is possible to identify the proportional integral (PI) parameters for the second-order transfer function coefficients [7,8,14–16].

In this paper, the modulus optimum criterion is also applied for the DC voltage loop, which is in contrast with other approaches [13,16] that use the symmetrical optimum criterion. More specifically, this methodology is possible due to the fact that, for MMC-HVDC, there are no DC side capacitor filters, and the large majority of capacitors are located within the SMs.

The inner current control loops are designed using the circuit equations that result from the simplified converter model in Figure 2. Furthermore, the active and reactive power loops are based on the instantaneous power theory [17]. The DC voltage loop is based on the active power flow equality between the AC region and the DC region of the converter. This design theory is extensively reasoned in previous work [7,8,17].

The inner current controller proportional coefficient $k_{p,d}$ and integral coefficient $k_{i,d}$, on the direct axis are shown in (4) and (5). The coefficient values associated to the quadrature axis can be determined using the same equations.

$$k_{p,d} = \frac{-\left(\frac{L_{arm}}{2} + L_t\right)}{2T_{delay}} \tag{4}$$

$$k_{i,d} = \frac{-\left(\frac{R_{arm}}{2} + R_t\right)}{2T_{delay}} \tag{5}$$

T_{delay} signifies the delay introduced by the pulse width modulation as well as the capacitor balancing controllers.

Next, the outer active and reactive power controller proportional coefficients ($k_{p,P}$ and $k_{p,Q}$) and integral coefficients ($k_{i,P}$ and $k_{i,Q}$) can be defined as in (6) and (7).

$$k_{p,P} = k_{p,Q} = 0 \quad (6)$$

$$k_{i,P} = -k_{i,Q} = \frac{1}{3v_d T_{eq}} \quad (7)$$

T_{eq} is an intentionally induced delay that ensures the fact that during tuning process, the outer loop controller is slower than the inner loop controller.

Regarding the DC voltage control loop, using the same parameter tuning technique, it is possible to identify the proportional coefficient $k_{p,VDC}$ and integral coefficient $k_{i,VDC}$, as in (8) and (9).

$$k_{p,VDC} = 0; \quad (8)$$

$$k_{i,VDC} = \frac{I_{DC}}{3v_d T_{eq}} \quad (9)$$

4. Case Study

The proposed network consists of three terminal MMC-HVDC, with full-bridge sub-modules (Figure 4).

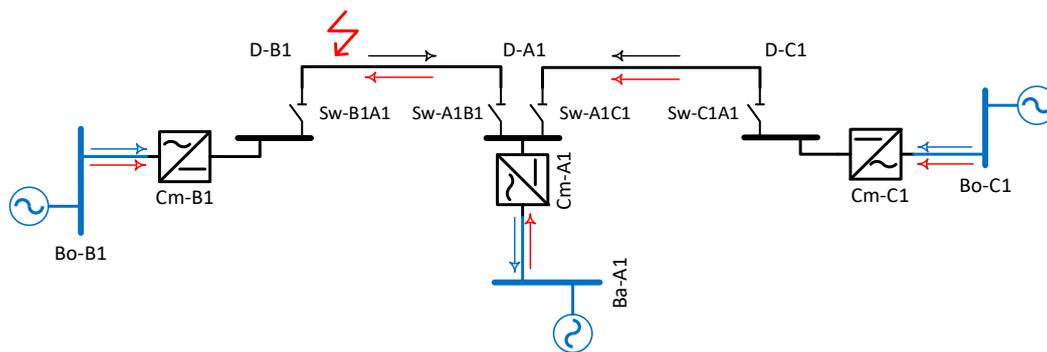


Figure 4. Multiterminal high-voltage direct current transmission (HVDC) network.

There are two rectifier stations, $Cm-C1$ and $Cm-B1$, connected to off-shore wind power plants. However, the design of the two converter allows bi-directional power flow. Furthermore, there is one inverter station, $Cm-A1$, which is also bi-directional. The rated DC voltage is ± 200 kV.

Between the three converters, overhead power lines are used, each with a length of 200 km. Line parameters are shown in Table 1.

Table 1. DC line data [9].

Line Data	r_0 (Ω/km)	l_0 (mH/km)	c_0 ($\mu\text{F}/\text{km}$)	g_0 ($\mu\text{S}/\text{km}$)	Max. Current (A)
Overhead line ± 200 kV	0.0133	0.8273	0.0139	-	3000

All converters use a modular multilevel structure, which leads to low harmonic content. Therefore, filters are omitted in the simulation. Furthermore, the converters contain full-bridge submodules and are able to command mechanical switches, which are located at the end of the DC lines: $Sw-B1A1$, $Sw-A1B1$, $Sw-A1C1$, $Sw-C1A1$.

All converter nominal values are presented in Table 2 and are based on parameters recommended by Cigre Working Group B4 [9]. Moreover, all PI coefficients, which have been calculated using (4)–(9) are introduced in Table 3.

Table 2. Converter data.

Equipment	Data	A1	C1	B1
Converter	Rated power	800 MVA	800 MVA	600 MVA
	Arm reactance	59 mH	59 mH	59 mH
Converter transformer	Leakage reactance	79 mH	79 mH	79 mH
	Resistance	0.363 Ω	0.363 Ω	0.363 Ω
	Primary rated voltage	380 kV	145 kV	145 kV
	Secondary rated voltage	220 kV	220 kV	220 kV
Submodules	Number/half arm	200	200	200
	Individual capacitance	10 mF	10 mF	10 mF
	IGBT conduction resistance	0.00136 Ω	0.00136 Ω	0.00136 Ω

Table 3. Control loop PI coefficients.

Type of Loop	Coefficient	Value
Inner control loop	$k_{p,d} = k_{p,q}$	−108.5
	$k_{i,d} = k_{i,q}$	−499.1
Active power control loop	$k_{p,P}$	0
	$k_{i,P}$	0.001515
Reactive power control loop	$k_{p,Q}$	0
	$k_{i,Q}$	−0.001515
DC voltage control loop	$k_{p,VDC}$	0
	$k_{i,VDC}$	6.061

Because the detailed equivalent model provides access at a submodule level, it is possible to effectively include pulse-width-modulation blocks inside the simulation, in order to determine the number of SMs that need to be bypassed/inserted. In the analyzed configuration, a carrier-based modulation is used: the phase-shifted carrier technique.

The two rectifier stations are in active power and reactive power control mode. Moreover, the inverter station controls the DC voltage and the reactive power. The initial setpoint values are:

- *Cm-A1* (inverter): DC voltage, $V_{DC}^* = \pm 200$ kV; Reactive power, $Q_S^* = 0$ Mvar.
- *Cm-C1* (rectifier 1): Active power, $P_S^* = -320$ MW; Reactive power, $Q_S^* = 0$ Mvar.
- *Cm-B1* (rectifier 2): Active power, $P_S^* = -280$ MW; Reactive power, $Q_S^* = 100$ Mvar.

Negative active power values signify rectifier operation and positive values signify inverter operation.

At $t = 0.4$ s, the active power setpoints of both rectifiers are increased to the following values:

- *Cm-C1* (rectifier 1): Active power, $P_S^* = -380$ MW.
- *Cm-B1* (rectifier 2): Active power, $P_S^* = -350$ MW.

At $t = 0.6$ s, there is a pole-to-ground fault (on positive pole) on the line between *Cm-A1* and *Cm-B1*, at half the line distance. The fault resistance is 50 Ω . The direction of the fault currents is represented in red, in Figure 4. Figure 5 shows power values for all converters, as measured on the AC side. In this first scenario, no fault-handling capabilities are used (only the reaction of the PI control system is considered). As can be seen, at time $t = 0.4$ s the active power setpoint change leads to a fast response of the control system. The small power ripple which can be seen on all graphics is the result of the non-optimal dimensioning of converter capacitors and the arm reactor.

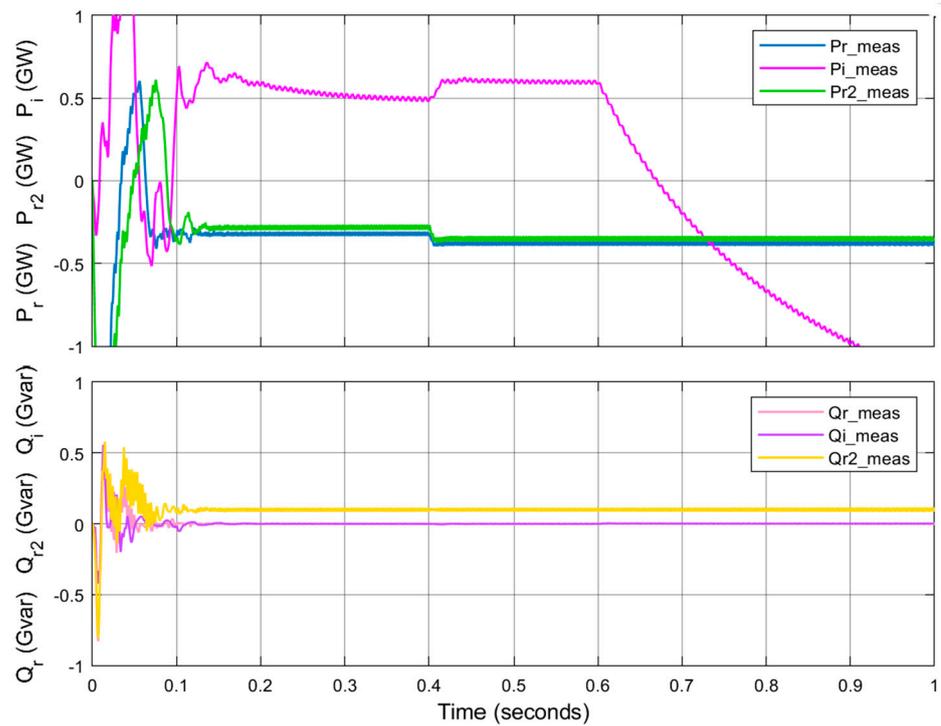


Figure 5. Measured powers for all converters in Scenario 1.

At $t = 0.6$ s, the fault initially discharges all submodule capacitors from the inverter. Next, there is a reversal of power as measured on the AC side of the inverter; the AC system now feeds the fault. As can be observed, this reverse power reaches values of over 1.5 GW, which can definitely destroy the submodules.

The pole currents, as measured on the DC side of the inverter, are shown in Figure 6 (where $I_{DC,ui2}$ represents the positive pole current, and $I_{DC,li2}$ represents the negative pole current).

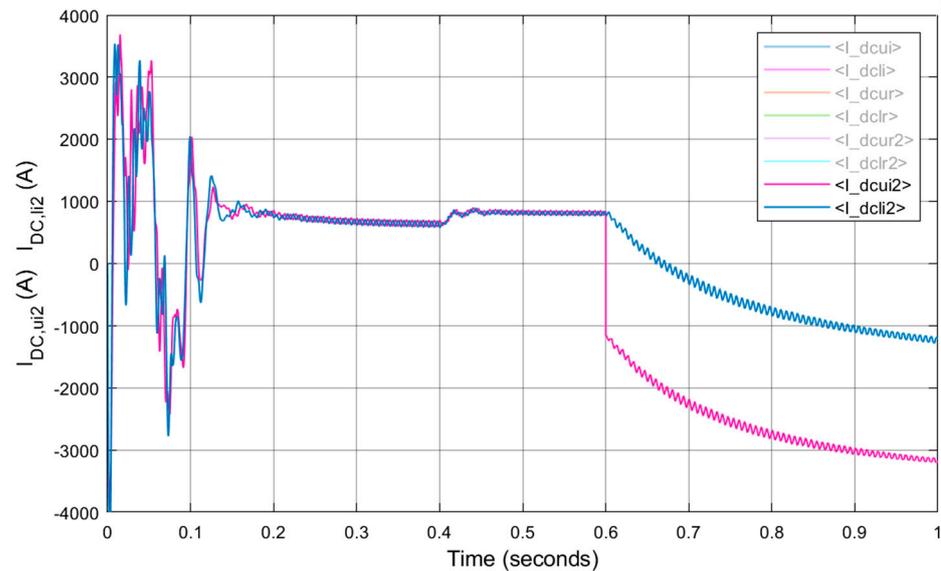


Figure 6. Positive and negative pole currents, as measured on the DC side of the inverter, in Scenario 1.

All oscillations which can be seen at the beginning of the simulation ($0 \dots 0.1$ s) should be disregarded, due to being the result of initial value model stabilization.

In the second scenario, all converters enter fault-handling mode: the inverter detects a sudden current increase, and it commands all submodules to output a negative voltage. In the simulation, the control loops are never switched off.

When the current reaches zero, a mechanical switch opens on the DC side of converters *Cm-A1* and *Cm-B1*. While the mechanical switches are open, *Cm-B1* remains offline. After the fault is cleared, all converters switch back on, using previous setpoints. This change is illustrated in Figure 7. After the fault, the inverter needs about 0.3 s to recover to the initial active power value, and less than 0.1 s to recoup to the initial reactive power value.

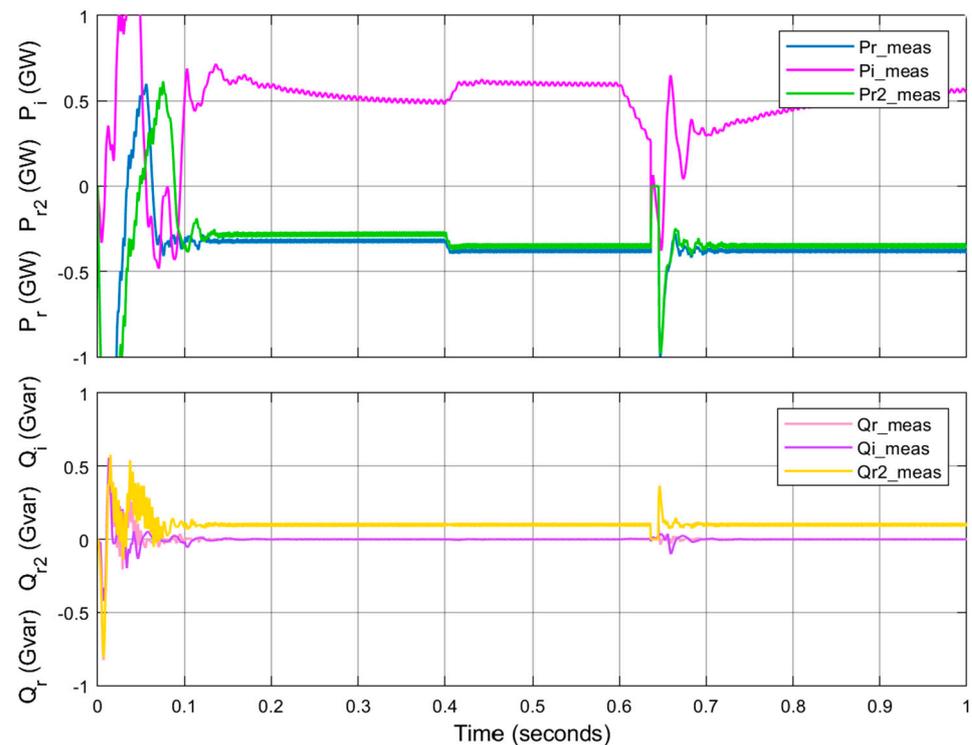


Figure 7. Measured powers for all converters in Scenario 2.

5. Discussion

The three-terminal HVDC network, which has been shown in the case study, offers great flexibility during or after faults, because it implements a fault-handling configuration at a terminal level, while also making use of simple mechanical switches at the end of the lines. In this manner, if there is a fault on any of the overhead lines, it is possible to quickly respond and, if the fault is not permanent, to recover the system to the initial state in less than 0.3 s after the fault has been eliminated. Moreover, if the fault is permanent, it is possible to isolate the affected zone and to ensure partial operation of the network.

An additional aspect which favors the configuration presented in the case study relates to the initial cost as well as to the availability of technology. More specifically, even though a submodule with a full-bridge configuration is more expensive compared to half-bridge, this cost disadvantage is compensated by much simpler protection equipment. As such, a mechanical switch is preferred over a DC circuit breaker, due to the fact that DC circuit breakers are still in early development stages, have restrictive voltage and current ratings and require a high investment cost.

Another aspect that is observable in the simulations relates to the significant energy that is stored inside the SM capacitors. This energy, which is the first that flows towards the faulted zone, ensures a reaction buffer. Therefore, electrical parameters (AC voltages, active and reactive powers) change at a slower rate, which permits fault mitigation without severely affecting the operation of connected HVAC systems.

6. Conclusions

The scope of this paper was to bring forward an approach that enables dynamic simulations of faults and to present a multiterminal HVDC network configuration that provides high flexibility during and after faults.

One aspect, which was promoted in the paper, related to the use of detailed equivalent models, which enable access at a submodule level and allow for changes to be made regarding IGBT conduction/blocking internal resistance. Moreover, such models permit measurements of capacitor voltages, thus paving the way for the implementation of various capacitor balancing techniques, in conjunction with pulse-width modulation.

A second aspect that was endorsed in this paper was the flexibility of vector control, together with a straight-forward approach to controller tuning, that is the modulus optimum criterion. In contrast to other papers, tuning was done exclusively using modulus optimum, without the need to increase controller complexity as compared with symmetrical optimum.

Furthermore, a heavy focus was given to the aspect of fault handling in a multiterminal HVDC network that uses converters with full-bridge submodules in conjunction with mechanical switches at the end of the HVDC lines. Advantages of this proposed configuration were consequently underlined, giving arguments related to operational capabilities as well as cost restrictions.

Nevertheless, in order to validate all proposed ideas, several simulations were performed. All the simulations approach realistic conditions regarding converter control and response during fault conditions. These simulations underlined the potential regarding the use of full-bridge submodules inside of MMC-HVDC converters that are deployed in a multiterminal configuration.

Author Contributions: Conceptualization, I.-C.D. and M.E.; methodology, I.-C.D., M.E. and L.T.; software, I.-C.D.; validation, M.E. and L.T.; formal analysis, I.-C.D., M.E. and L.T.; investigation, I.-C.D.; resources, I.-C.D.; data curation, M.E. and L.T.; writing—original draft preparation, I.-C.D.; writing—review and editing, I.-C.D.; visualization, I.-C.D.; supervision, M.E. and L.T. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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