



Article Multivariable Deadbeat Control of Power Electronics Converters with Fast Dynamic Response and Fixed Switching Frequency

Jaime A. Rohten ^{1,*,†}, David N. Dewar ^{2,†}, Pericle Zanchetta ^{2,3,†}, Andrea Formentini ^{2,†}, Javier A. Muñoz ^{4,†}, Carlos R. Baier ^{4,†} and José J. Silva ^{5,†}

- ¹ Department of Electrical and Electronic Engineering, Universidad Del Bío-Bío, Avenida Collao 1202, 4051381 Concepción, Chile
- ² Department of Electrical and Electronic Engineering, University Park, University of Nottingham, Nottingham NG7 2RD, UK; David.Dewar@nottingham.ac.uk (D.N.D.); Pericle.Zanchetta@nottingham.ac.uk or pericle.zanchetta@unipv.it (P.Z.); Andrea.Formentini@nottingham.ac.uk (A.F.)
- ³ Department of Electrical Computer and Biomedical Engineering, University of Pavia, Via A. Ferrata 5, 27100 Pavia, Italy
- ⁴ Department of Electrical Engineering, Universidad de Talca, Camino Los Niches Km. 1, 3340000 Curicó, Chile; jamunoz@utalca.cl (J.A.M.); cbaier@utalca.cl (C.R.B.)
- ⁵ Department of Electrical Engineering, Universidad de Concepción, Victor Lamas 1290, 4070386 Concepción, Chile; jsilvac@udec.cl
- * Correspondence: jrohten@ubiobio.cl
- + These authors contributed equally to this work.

Abstract: Power converters have turned into a critical and every-day solution for electric power systems. In fact, the incorporation of renewable energies has led towards the constant improvement of power converter topologies and their controls. In this context, over the last 10 years, model predictive control (MPC) is positioned as one the most studied and promising alternatives for power converter control. In voltage source inverters (VSI), MPC has only been applied in the inner current control loop, accelerating and improving its dynamic response, but as mentioned, has been limited only to the current control loop. The fastest of the MPC techniques is the Deadbeat (DB) control, and in this paper, it is proposed to employ DB control on the entire system, therefore accelerating the time response not only for the current loops, but also for voltage loops. At the same time, this avoids overshoots and overpower in order to protect the power converter, leading to the fastest dynamic response according to VSI capabilities. For renewable energies, fast-dynamics entails fast maximum power tracking and therefore, maximizes energy harvesting, or in other words, reduces the losses due to the control dynamics. Thus, this paper gives a clear procedure and key points for designing a DB control for all the variables based on a mathematical model, which is corroborated by simulations and the experimental results.

Keywords: model predictive control; soft deadbeat algorithm; power converters; energy management

1. Introduction

Predictive control has been gaining increasing interest over the past ten years, in both research and industrial environments in the control of power electronics systems. The predictive control family includes trajectory-based and hysteresis-based control strategies, Model Predictive Control (MPC), and Deadbeat (DB) control. MPC is a strong and refined way to regulate the system dynamics subject to physical constraints [1]. It uses a mathematical model to estimate the evolution of system state variables in the future for several different control actions. The optimal control action is then selected by minimization of a cost function. Conventionally, the minimization of cost function needs to be performed at each sample time [1,2], resulting in a computationally demanding procedure to be



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/). computed in real time. Hence, more recent solutions involve the MPC problem being reformulated as a multi-parametric algorithm solved offline for all valid states, entailing a lookup table for the optimal solution depending upon the current actual value [3–7]. Due to there being an intrinsic finite set of valid states of power converter that can be applied, an MPC variation, appropriately named Finite Control Set MPC (FCS-MPC), has started to be widely employed [8–10]. In this strategy, several system state predictions are made for a finite series of control actions. The action which results in the minimization of a performance cost function is considered optimal and is thus applied to the converter. Thanks to the numerous benefits it can provide, such as the absence of a modulation technique, fast dynamic response, and easy enclosure of the system nonlinearities and constraints, this method has been successfully applied to several different power converter topologies, such as shunt active filters [11,12], matrix converters [13,14], and drive systems [15]. However, applying a single vector at each sampling time entails a variable switching frequency, increasing the nondeterministic ripple on the output voltages and currents, and hindering the passive filter design.

The lack of a modulator has its drawbacks, even considering the transient time performance of the system. For instance, under steady-state conditions when high controller bandwidth is not mandatory, large current ripples are induced due to the limited set of available control actions. In order to overcome this issue, fixed switching frequency MPC algorithms have been researched and published in the past few years [16–21]. Although they improve the steady state performance, in terms of the state variables ripple, they fail to achieve the same steady state performance of a classical pulse width modulation (PWM) or Space Vector Modulator (SVM).

Deadbeat control is of particular interest because of its fast dynamic performance, which is able to impose zero error with respect the references in a short finite time, speeding up the transient response. Compared to FCS-MPC, DB mixes fast dynamic performance together with a constant switching frequency and minimum steady state distortion thanks to the presence of a modulator. Because of these reasons, the DB controller is more frequently chosen over other controllers in power converter applications such as Uninterruptible Power Supplies (UPS) [22–24], PWM rectifiers, active filter controls [25,26], motor drive controls [27–30], and paralleled converter configurations [31]. Some other techniques also accelerate the dynamic behavior, where one of the most known methods is sliding mode control, which is capable of managing the inner loops with fast dynamic response, as shown in [32]. In fact, the time response can be specified considering a given initial condition; however, this technique has also been included for the inner control loop (current or power control loop).

In all previous applications, DB control has been used to control a single variable (most commonly, the control of currents) or more variables at the same time, linking all controlled terms through a linear relationship. To the author's knowledge, no work has appeared in the literature using DB control for the full control of all variables in a power converter. Thus, this paper innovates in the application of developing a DB controller which manages all the control variables for a given power converter. All variables are, therefore, provided with the advantages of this fast-dynamic control, as well as avoiding overshoot, which is typical in these kinds of applications [33–35].

This paper therefore proposes a multivariable DB control for power electronics converters in order to regulate all system variables in a single predictive loop, from ac currents, to the *dc* voltage, and the active and reactive powers, [35–38]. As a case study, the full control of a standard three-phase grid connected converter has been chosen to demonstrate the proposed control approach and to validate its performance. Complementary to that presented in the literature [15,22,24,25,28,30,31,33–35,39,40], this multivariable DB control is designed to maximize all the dynamic responses and to ensure an excellent steady state behavior, whilst still maintaining the system variables within clear limits, to ensure the proper operation of the converter [41]. Fast-dynamics are of particular interest for renewable energies because they can reach the maximum power point faster and therefore,

maximize the harvesting energy; in general, faster control on the power converter gives a degree of freedom for users when needed.

The final algorithm shall be shown to be simple and easy to implement and does not necessitate major computational requirements. Finally, the simulations and experimental results show the effectiveness and feasibility of the proposed control algorithm, corroborating the theoretical development.

2. System Modelling

2.1. Continuous Static Reference Frame Model

Considering the power converter diagram illustrated in Figure 1, modeling in the *abc* reference frame results in the following expression:

$$\mathbf{v_s}^{abc} = L_s \frac{d\mathbf{i_s}^{abc}}{dt} + R_s \mathbf{i_s}^{abc} + \mathbf{v_o}^{abc}$$
(1)



Figure 1. Power Converter System.

Meanwhile, on the *dc* link side:

$$C_{dc}\frac{dv^{dc}}{dt} = i_s{}^{dc} - i_L{}^{dc}$$
⁽²⁾

where *Ls* and *Rs* are the inductor and resistor at the converter *ac* side and C_{dc} is the capacitor at the *dc* side. Furthermore, the power converter voltage related to the switches' states is:

v

$$\mathbf{r}_{\mathbf{o}}^{abc} = \mathbf{s}^{abc} v^{dc} \tag{3}$$

The *dc* side current is given by:

$$i_s^{dc} = \left\langle \mathbf{s}^{abc}, \mathbf{i}_{\mathbf{s}}^{abc} \right\rangle$$
 (4)

where $\langle \cdot, \cdot \rangle$ denotes the dot product and s^{abc} represent the converter switching functions The model can then be expressed in the $\alpha\beta$ reference frame as:

$$\mathbf{v_s}^{\alpha\beta} = L_s \frac{d\mathbf{i_s}^{\alpha\beta}}{dt} + R_s \mathbf{i_s}^{\alpha\beta} + \mathbf{s}^{\alpha\beta} v^{dc}$$
(5)

$$C_{dc}\frac{dv^{dc}}{dt} = \left\langle \mathbf{s}^{\alpha\beta}, \mathbf{i}_{\mathbf{s}}^{\alpha\beta} \right\rangle - i_{L}^{dc}$$
(6)

2.2. Discrete Static Reference Frame Model

The implementation of predictive control is tied to a discrete representation of the model, leading to the definition of the future values of the variables in a discrete way and as a function of system dynamics and parameters. The Forward Euler Approximation is one of the most employed discretization methods to find the equivalent model. Using this approximation, the power converter model can be defined in discrete time as:

$$\mathbf{v_s}^{\alpha\beta}(k) = L_s \frac{\mathbf{i_s}^{\alpha\beta}(k+1) - \mathbf{i_s}^{\alpha\beta}(k)}{T_s} + R_s \mathbf{i_s}^{\alpha\beta}(k) + \mathbf{v_o}^{\alpha\beta}(k)$$
(7)

$$C_{dc}\frac{v^{dc}(k+1) - v^{dc}(k)}{T_s} = \left\langle \mathbf{s}^{\alpha\beta}(k), \mathbf{i}_s^{\alpha\beta}(k) \right\rangle - i_L^{dc}(k)$$
(8)

3. Predictive Control Strategy

Once the power converter behavior is described by discrete equations, further predictions may be performed in order to gain knowledge about the future values of the state variables as a function of the past and present states of the system.

3.1. Power Converter Voltage

Considering the converter voltage $\mathbf{v_o}^{abc}$, as the control actuating variable, it can be generated as a function of the desired future value of the currents. Together, the source currents $\mathbf{i_s}^{abc}$ and voltages $\mathbf{v_s}^{abc}$ provide the total power consumption, which in turn sets the power factor and the amount of active power drained by the load.

From Equation (7), the converter input voltage is computed as a function of the input current and its one time step future prediction $\mathbf{i_s}^{\alpha\beta}(k+1)$, the parameters of the filter, and the sampling time T_s :

$$\mathbf{v_o}^{\alpha\beta}(k) = \mathbf{v_s}^{\alpha\beta}(k) - L_s \frac{\mathbf{i_s}^{\alpha\beta}(k+1) - \mathbf{i_s}^{\alpha\beta}(k)}{T_s} - R_s \mathbf{i_s}^{\alpha\beta}(k)$$
(9)

where $\mathbf{i_s}^{\alpha\beta}(k+1)$ is the power converter current reference, $\mathbf{v_s}^{\alpha\beta}(k)$ the supply voltage, and $\mathbf{v_o}^{\alpha\beta}(k)$ the converter injected voltage; Rs and Ls are the filter parameters. However, due to processing delays, the voltage $\mathbf{v_o}^{\alpha\beta}$ cannot be calculated and applied at the same time *k*. Therefore, time delay compensation is mandatory. Subsequently, the voltage in Equation (9) is to be expressed as:

$$\mathbf{v_o}^{\alpha\beta}(k+1) = \mathbf{v_s}^{\alpha\beta}(k+1) - L_s \frac{\mathbf{i_s}^{\alpha\beta}(k+2) - \mathbf{i_s}^{\alpha\beta}(k+1)}{T_s} - R_s \mathbf{i_s}^{\alpha\beta}(k+1)$$
(10)

where the known variables $\mathbf{i_s}^{\alpha\beta}(k+1)$, $\mathbf{v_s}^{\alpha\beta}(k+1)$ can be estimated by using the following procedure.

The supply voltage obeys a rotating trajectory which can be predicted under the assumption of low amplitude and low frequency variation such that:

$$\hat{\vec{v}}_{s}^{\alpha\beta}(k+1) = e^{j2\pi f T_{s}} \hat{\vec{v}}_{s}^{\alpha\beta}(k) \approx \hat{\vec{v}}_{s}^{\alpha\beta}(k+1)$$
(11)

where the phasor $\hat{\vec{v}}_s^{\alpha\beta}(k+1)$ is obtained as a function of the source frequency *f* and *T*_s, thus the estimation of the source voltage is found to be

$$\hat{\mathbf{v}}_{\mathbf{s}}^{\alpha\beta}(k+1) = \begin{bmatrix} v_s^{\alpha}(k)\cos(\omega T_s) - v_s^{\beta}(k)\sin(\omega T_s) \\ v_s^{\alpha}(k)\sin(\omega T_s) + v_s^{\beta}(k)\cos(\omega T_s) \end{bmatrix}$$
(12)

Additionally, the current at time k + 1 can be expressed from Equation (7) as:

$$\hat{\mathbf{i}}_{\mathbf{s}}^{\alpha\beta}(k+1) = \left(1 - \frac{T_s R_s}{L_s}\right) \mathbf{i}_{\mathbf{s}}^{\alpha\beta}(k) + \left(\frac{T_s}{L_s}\right) \left(\mathbf{v}_{\mathbf{s}}^{\alpha\beta}(k) - \mathbf{v}_{\mathbf{o}}^{\alpha\beta}(k)\right)$$
(13)

3.2. Current References as a Function of the Power Reference

Active and reactive power, drawn by the converter from the grid, are chosen as targets for the deadbeat control. These power components can be managed by controlling the currents $\mathbf{i_s}^{abc}$ and the voltages $\mathbf{v_s}^{abc}$. In fact, the power consumed by the topology is given by:

$$\vec{s}_{pq}(k) = p_s(k) + jq_s(k) = \vec{v}_s^{\alpha\beta}(k)\vec{i}_s^{\ast\alpha\beta}(k)$$
(14)

where:

$$\vec{v}_s^{\alpha\beta}(k) = v_s^{\alpha}(k) + jv_s^{\beta}(k) \tag{15}$$

$$\stackrel{\rightarrow}{i}_{s}{}^{*\alpha\beta}(k) = i_{s}{}^{\alpha}(k) - ji_{s}{}^{\beta}(k)$$
(16)

Therefore, the current references can be set to meet the power reference $\vec{s}_{pq}^{ref}(k) = p_s^{ref}(k) + jq_s^{ref}(k)$ by using the following expressions:

$$i_{s}^{\alpha, ref}(k) = \frac{1}{\left|\vec{v}_{s}^{\alpha\beta}(k)\right|^{2}} \operatorname{Re}\left\{\vec{v}_{s}^{\alpha\beta}(k)\vec{s}_{pq}^{*ref}(k)\right\}$$
(17)

$$i_{s}{}^{\beta, ref}(k) = \frac{1}{\left|\vec{v}_{s}{}^{\alpha\beta}(k)\right|^{2}} \operatorname{Im}\left\{\vec{v}_{s}{}^{\alpha\beta}(k)\vec{s}_{pq}^{*ref}(k)\right\}$$
(18)

From Equation (10) it can be seen that the current reference needs to be forwarded by two sample periods. Therefore, Equations (17) and (18) need to also be computed two steps ahead, by replacing k by k + 2, as follows

$$i_{s}^{\alpha, ref}(k+2) = \frac{\operatorname{Re}\left\{\hat{\vec{v}}_{s}^{\alpha\beta}(k+2)\hat{\vec{s}}_{pq}^{ref}(k+2)\right\}}{\left|\hat{\vec{v}}_{s}^{\alpha\beta}(k+2)\right|^{2}}$$
(19)

$$i_{s}^{\beta, ref}(k) = \frac{\operatorname{Im}\left\{\stackrel{\widehat{v}_{s}}{v}^{\alpha\beta}(k+2)\stackrel{\rightarrow}{s}^{*}_{pq}^{ref}(k+2)\right\}}{\left|\stackrel{\widehat{v}_{s}}{v}^{\alpha\beta}(k+2)\right|^{2}}$$
(20)

where the estimation of the voltage $v_s^{abc}(k + 2)$ can be found by assuming the frequency and amplitude as constant, as was mentioned in Equation (11), to find:

$$\hat{\mathbf{v}}_{\mathbf{s}}^{\alpha\beta}(k+2) = \begin{bmatrix} v_s^{\alpha}(k)\cos(2\omega T_s) - v_s^{\beta}(k)\sin(2\omega T_s) \\ v_s^{\alpha}(k)\sin(2\omega T_s) + v_s^{\beta}(k)\cos(2\omega T_s) \end{bmatrix}$$
(21)

3.3. Power Reference Calculation

The power reference is set in terms of active and reactive powers. The active power consumed by the power converter can be separated into three main parts:

<u>*dc*</u> load power consumption: This contribution represents what the power converter is supplying to the *dc* loads through the current i_L^{dc} . The related *dc* power is computed as:

$$p_L(k) = v^{dc}(k)i_L{}^{dc}(k)$$
(22)

- <u>ac inductive filter losses</u>: The filter included on the *ac* side has natural losses, associated to *R_s*, due to the non-ideality of the inductance, and can be calculated as:

$$p_{RL}(k) = \operatorname{Re}\left\{ \left(\vec{v}_s^{\alpha\beta}(k) - \vec{v}_o^{\alpha\beta}(k) \right)^{\overrightarrow{i}_s^{\alpha\beta}}(k) \right\} = \left| \vec{i}_s^{\alpha\beta}(k) \right|^2 R_s$$
(23)

- Power supplied to the *dc* capacitor: The *dc* link capacitor C_{dc} is charged/discharged in order to maintain the *dc* voltage to its reference. Therefore, this power is regulated by the *dc* voltage control. The energy on the *dc* capacitor at time *t* is given by:

$$e_{C_{dc}}(t) = \frac{1}{2} C_{dc} \left(v^{dc}(t) \right)^2$$
(24)

where the power can be found from Equation (24) deriving with respect to time as:

$$p_{C_{dc}}(t) = \frac{1}{2} C_{dc} \frac{d\left(v^{dc}(t)\right)^2}{dt}$$
(25)

Applying the Euler Approximation, the discretization of Equation (25) is given by:

$$p_{C_{dc}}(k) = \frac{1}{2} C_{dc} \frac{\left(v^{dc}(k+1)\right)^2 - \left(v^{dc}(k)\right)^2}{T_s}$$
(26)

Therefore, the total amount of active power required by the power converter from the source, which represents the active power reference, is given by:

$$p_s^{ref}(k) = p_L(k) + p_{RL}(k) + p_{C_{dc}}(k)$$
(27)

However, the power reference is required to be at time k + 2, therefore all the terms in Equation (27) need to be considered two steps ahead; Equations (22), (23) and (26) therefore need to be recalculated at the sampling instant k + 2.

In order for Equation (22) to be approximated two steps ahead, $v^{dc}(k + 2)$ is required. An estimation of this voltage at k + 1 can be found solving Equation (8) as:

$$\hat{v}^{dc}(k+1) = v^{dc}(k) + \frac{T_s}{C_{dc}} \left(\left\langle \mathbf{s}^{\alpha\beta}(k), \mathbf{i}_{\mathbf{s}}^{\alpha\beta}(k) \right\rangle - i_L^{dc}(k) \right)$$
(28)

The voltage $v^{dc}(k + 2)$ cannot be estimated from Equation (28) because this voltage would be based on the unknown switching states $\mathbf{s}^{\alpha\beta}$ at time (k + 1), i.e., $\mathbf{s}^{\alpha\beta}(k + 1)$. Thus, the estimation of the voltage $v^{dc}(k + 2)$ is obtained by interpolation as:

$$\hat{v}^{dc}(k+2) = \hat{v}^{dc}(k+1) + \Delta v^{dc}(k+1)$$
(29)

with $\Delta v^{dc}(k+1) = \hat{v}^{dc}(k+1) - v^{dc}(k)$.

On the other hand, as the current $i_L{}^{dc}$ is considered as a disturbance and changes as a function of the load requirements, the estimation turns into a difficult task considering this as an uncertain future value. Therefore,

$$i_L{}^{dc}(k+2) \approx i_L{}^{dc}(k+1) \approx i_L{}^{dc}(k)$$
(30)

Which, under any change on $i_L{}^{dc}$, will influence the control as a delay of two steps at most, with:

$$p_L(k+2) = \left(2\hat{v}^{dc}(k+1) + v^{dc}(k)\right)i_L{}^{dc}(k)$$
(31)

The power losses in Equation (23) are negligible when compared with the other power terms because R_s is close to zero. The prediction $\mathbf{i_s}^{\alpha\beta}(k + 1)$ can therefore be found by using Equation (13) and the current $\mathbf{i_s}^{\alpha\beta}(k + 2)$ can be found similarly as performed for

the *dc* link voltage at time (k + 2) in Equation (29), where the interpolation can now define $p_{RL}(k + 2)$ to be:

$$p_{RL}(k+2) = \left| \stackrel{\stackrel{\wedge}{i}{}_{s}}{}^{\alpha\beta}(k+2) \right|^{2} R_{s}$$
(32)

where:

$$\hat{\vec{i}}_{s}^{\alpha\beta}(k+2) = 2\left(1 - \frac{T_{s}R_{s}}{L_{s}}\right)\hat{\vec{i}}_{s}^{\alpha\beta}(k) + 2\left(\frac{T_{s}}{L_{s}}\right)\left(\vec{\vec{v}}_{s}^{\alpha\beta}(k) - \vec{\vec{v}}_{o}^{\alpha\beta}(k)\right) - \hat{\vec{i}}_{s}^{\alpha\beta}(k)$$
(33)

Finally, the power related to the *dc* capacitor, which is also forwarded two steps ahead in Equation (26), needs two additional terms: (*i*) the voltage at k + 3 which is set as the voltage reference, and (*ii*) the voltage at k + 2, shown in Equation (29), where the final expression for this power is:

$$p_{C_{dc}}(k+2) = \frac{1}{2} \frac{C_{dc}}{T_s} \left(v^{dc,ref}(k+3) \right)^2 - \frac{1}{2} \frac{T_s}{C_{dc}} \left[\frac{C_{dc}}{T_s} \left(v^{dc}(k) \right)^2 + \left\langle \mathbf{s}^{\alpha\beta}(k), \mathbf{i}_{\mathbf{s}}^{\alpha\beta}(k) \right\rangle - i_L^{dc}(k) \right]^2$$
(34)

On the other hand, the total reactive power reference can be imposed as:

$$q_s^{ref}(k+2) = \tan\left(\theta^{ref}\right) p_s^{ref}(k+2) \tag{35}$$

where θ^{ref} is the angle between the voltage and the current (capacitive or inductive) and may be defined by the power factor (*pf*) as:

$$\theta^{ref} = \pm \arccos(pf) \tag{36}$$

where the sign depends on whether an inductive or capacitive reactive power reference is imposed.

4. Multivariable Fast-Dynamic Deadbeat Control

The proposed power converter control is fast enough to reach the reference, theoretically, in three steps for the *dc* voltage and two steps for the current control. However, finalizing the *dc* voltage transients in three steps may demand an enormous amount of power in a short time, which cannot be achieved due to the power rating of the converter, the maximum current rating, and the natural saturation of the $\mathbf{v_o}^{abc}$ due to the finite value of the *dc* link voltage v^{dc} .

Particularly, the power associated to the *dc* voltage in Equation (26) (or Equation (34) which is defined in k + 2) may take an even larger value, due to the presence of noise on the sensing circuits. This is because the voltage is squared and divided by the sampling time T_s , which can be tens of microseconds. This operation may cause an excessive increase in the power demanded by the control, which can be beyond the rated values of the converter, and therefore, generate an inflated power reference, only due to the presence of noise.

Thus, two new conditions have been introduced to overcome these issues: (*i*) a noise rejection parameter and (*ii*) a maximum power limitation. The gain k_{Cdc} shall be introduced to reduce the noise effect on the power reference, altering Equation (34) to be:

$$p_{C_{dc}}(k+2) = \frac{1}{2} \frac{C_{dc}}{T_s} k_{Cdc} \left(v^{dc,ref}(k+3) \right)^2 - \frac{k_{Cdc}}{2} \frac{T_s}{C_{dc}} \left[\frac{C_{dc}}{T_s} \left(v^{dc}(k) \right)^2 + \left\langle \mathbf{s}^{\alpha\beta}(k), \mathbf{i}_{\mathbf{s}}^{\alpha\beta}(k) \right\rangle - i_L^{dc}(k) \right]^2$$
(37)

leading to the final expression for active power reference as shown in Equation (38).

$$p_{s}^{ref}(k+2) = \frac{1}{2} \frac{C_{dc}}{T_{s}} k_{Cdc} \left(v^{dc,ref}(k+3) \right)^{2} - \frac{1}{2} \frac{T_{s}}{C_{dc}} k_{Cdc} \left[\frac{C_{dc}}{T_{s}} \left(v^{dc}(k) \right)^{2} + \left\langle \mathbf{s}^{\alpha\beta}(k), \mathbf{i}_{\mathbf{s}}^{\alpha\beta}(k) \right\rangle - i_{L}^{dc}(k) \right]^{2} + \cdots$$

$$\left(\hat{v}^{dc}(k+1) + \Delta v^{dc}(k+1) \right) i_{L}^{dc}(k) + \left| 2 \left(1 - \frac{T_{s}R_{s}}{L_{s}} \right) \overrightarrow{i}_{s}^{\alpha\beta}(k) + 2 \left(\frac{T_{s}}{L_{s}} \right) \left(\overrightarrow{v}_{s}^{\alpha\beta}(k) - \overrightarrow{v}_{o}^{\alpha\beta}(k) \right) - \overrightarrow{i}_{s}^{\alpha\beta}(k) \right|^{2} R_{s}$$

$$(38)$$

This new parameter can be observed to introduce a delay in the active power in relation to the capacitor response; in other words, this parameter increases the time response of this *dc* voltage control by transforming Equation (26) into:

$$p_{C_{dc}}(k) = \frac{1}{2} C_{dc} \frac{\left(v^{dc}(k+1)\right)^2 - \left(v^{dc}(k)\right)^2}{T_s} \frac{1}{T_m}$$
(39)

where $T_m > 1$ represents the times in which the response is delayed; to speed up computations in the controller, this term is transformed into k_{Cdc} as follows:

$$k_{Cdc} = \frac{1}{T_m} \tag{40}$$

On the other hand, the total amount of power in Equation (27) is limited by adding a restriction according the power converter maximum power, which is turned into the following function in the control algorithm:

$$if\left(\left|p_{s}^{ref}(k+2)\right| > P_{\max}\right)$$

then:
$$p_{s}^{ref}(k+2) = sign\left(p_{s}^{ref}(k+2)\right)P_{\max}$$
(41)

where P_{max} represents the maximum rated power the converter.

The whole control scheme is shown in Figure 2, where the three active power terms are generated to give the total amount of consumed power and the reactive power as a function of the desired angle between the current and voltage.



Figure 2. Converter control algorithm.

5. Simulation and Experimental Results

The proposed control algorithm has been tested both by means of computer simulations and experimentally using a 2 kW three-phase voltage source rectifier prototype feeding a *dc* load, as in Figure 1. Key waveforms are presented to illustrate the control performance both in steady state and in transient conditions due to *ac* current and *dc* voltage reference changes, and the resultant regulation of active and reactive power. Table 1 reports the system parameters of the experimental prototype, which have also been used in the simulation tests, employing the space vector modulation technique to synthetize the power converter voltage.

Parameters	Value	
v_s (grid nominal voltage value)	230 V, rms	
<i>v^{dc}</i> (<i>dc</i> link nominal voltage)	700 V	
R_s (filter resistance)	$0.4 \ \Omega$	
L_s (filter inductance)	4.75 mH	
C_{dc} (dc link capacitor)	2.2 mF	
f_s (grid frequency)	50 Hz	
T_s (controller sampling time)	50 µs	
f_{sw} (switching frequency)	20 kHz	
T_m (controller parameter)	25 p.u.	

5.1. Simulative Results

The proposed controller is simulated using MATLAB 2019 with PowerGui-Simulink tools, obtaining the results illustrated in Figure 3, where the power converter control, as expected, has the fastest possible response, limited only by the maximum power set by the user. The first column of Figure 3 shows the performance considering 5 kW as the maximum power the converter can bear; meanwhile, the second column of Figure 3 shows the response with 10 kW as the maximum permitted power. Figure 3 (a.1,2—first row) shows the *dc* link voltage response, where the voltage in Figure 3 (a.2) reaches the reference faster since the maximum power is double when compared with Figure 3 (a.1). Figure 3 (b.1,2-second row) shows the reactive power capabilities, where in both cases the angles between the voltage and current are imposed to be equal, although the amplitude in Figure 3 (b.2) is higher since the allowable power is higher with respect to Figure 3 (b.1). Figure 3 (c.1) shows the $\alpha\beta$ current when the power is limited at 5 kW and Figure 3 (c.2) shows the $\alpha\beta$ current when the power is limited at 10 kW. The last graphics—Figure 3 (d.1) for 5 kW limitation and Figure 3 (d.2) for 10 kW limitation—show the power control response, where the difference in the limitation of the power is clearly expressed, which changes the rapidness of each control. Thus, Figure 3 illustrates that the higher the power limitation is (Equation (41)), the faster the dynamic that is obtained.

5.2. Response under Model Uncertainties

The systems parameters can change in the course of time as well as the real parameters not being 100% accurate, leading to parametric uncertainty. Thus, the proposed controller was tested using parametric values, slightly adjusted with respect to the real parametric value, to highlight the uncertainty of the system.

Figure 4 shows the results considering model uncertainties. For all four tests, shown in Figure 4, a load increase of 100% is applied between 0.15 and 0.25 s, where the *dc* resistance goes from 250 to 125 Ω .

Figure 4 (a–d.1) show the system behavior when the inductances L_s are reduced to 50% from their original value, i.e., L_s changes from 4.75 to 2.375 mH, whilst the controller still considers L_s = 4.75 mH. The results show the control has good performance, despite the high noise presented due to the reduced inductance not being capable of properly mitigating the switching effects.



Figure 3. Simulated Results, (**a**) *dc* voltage and reference, (**b**) v_s^{α} voltage and i_s^{α} current, (**c**) $\mathbf{i_s}^{\alpha\beta}$ currents, (**d**) active p_s and reactive q_s power; (**1**) $p_s \max = 5$ kW, (**2**) $p_s \max = 10$ kW.



Figure 4. Model uncertainties, (**a**) *dc* voltage and reference, (**b**) v_s^{α} voltage and i_s^{α} current, (**c**) $\mathbf{i_s}^{\alpha\beta}$ currents, (**d**) active p_s and reactive q_s power, with (**1**) inductances decrease to 50%, (**2**) inductances increase to 200%, (**3**) resistances decrease to 50%, (**4**) resistances increase to 200%.

Figure 4 (a–d.2) show the increase in inductances L_s to 9.5 mH (twice the original value), whilst the control always considers $L_s = 4.75$ mH. The noise in this case is low because the filter is enlarged. The results show the control can cope with variation of this type and keep stability and reference tracking.

Figure 4 (a–d.3) and (a–d.4) show system performance against a variation on the resistance R_s of 50% and 200% from the original value, respectively. In both cases, the controller considers the original resistance value of $R_s = 0.4 \Omega$. In both cases, the effectiveness of the proposed control strategy even under parametric uncertainty is demonstrated, keeping the rapidness of the *dc* link voltage and regulating the current in order to keep the phase shift between the voltage and current close to zero. In addition, in all cases, there is no overshoot on the *dc* link voltage response, being one of the most distinguished advantages of the proposal.

The parameters can be chosen carefully because a larger L_s inductor implies a reduction in noise in the current but also makes the control slower; therefore, the inductor can be selected by a procedure related to the allowed current ripple, the nominal current, and the switching frequency as reported in [42]. On the other hand, the capacitor affects the dcvoltage dynamic, where larger capacitors help to maintain the voltage under disturbances as voltage sags/swells or changes on the current drained i_L^{dc} [43,44]. In Figure 5, there are results including different parameters in order to test the power converter control under different inductances and capacitors values, where, in this case, the control has the correct parameters into the algorithm. Figure 5(1) shows the results where the inductance increases its values to 200% with respect to the nominal value listed in Table 1, where the noise in the current shows a moderate reduction but the power control shows a slower dynamic. In Figure 5 (2), the inductances are reduced to 50% with respect to the nominal value and the noise is higher but not as high as the noise shown in Figure 4 (1), because the controller has the correct parameter in the algorithm and therefore, the prediction error is reduced. When the capacitor is increased (Figure 5 (3)) or decreased (Figure 5 (4)), the dcvoltage dynamic changes notoriously; therefore, this greatly increases its rapidness for the low C_{dc} value. However, the higher the value of the capacitor, the more effective rejection to disturbances achieved. Thus, there is an equilibrium that does not allow the capacitor to be reduced; in fact, if some imbalance appears, then the capacitor should be large enough to reduce the second order harmonic in the v_{dc} which causes a third harmonic in the ac currents. Another interesting case is the H-Bridge topology, which is noted to include a second order voltage and which is mostly reduced by enlarging the dc capacitor [45].

5.3. Experimental Tests

The control algorithm has been experimentally tested using a proof-of-concept 2 kW prototype setup shown in Figure 6, to validate the theoretical control design on a real power converter. Results are illustrated in Figure 7, where four main tests have been performed.

Figure 7a,b show a *dc* voltage step response. Firstly, a *dc* voltage step is applied with a unity power factor (Figure 7a); then, it is also imposed with a 0.7 (*inductive*) power factor (Figure 7b). The results of these tests are obtained considering the maximum power rating of the converter as 2 kW. The results show a very fast dynamic with no overshoot, as expected from the designed controller and simulation results; the total transient time for the voltage step from 250 up to 270 V is about 70 ms.

Figure 7c illustrates the power factor control; the currents go from an inductive power factor of 0.7 to a unity power factor at 125 ms, and from the figure, the dynamics are almost instantaneous, about 100μ s, as expected from a current DB control which needs two steps to reach the current reference, if no over-modulation is required.

Figure 7d presents a load impact test, from a power value close to zero up to 1.35 kW. The results show fast-dynamics and the good performance of this power converter control algorithm, where the current i_s^{abc} is always maintained within certain boundaries that ensure not to exceed the maximum power, yet the power reference is reached in the shortest time, related to the current time response, i.e., about 100µs without over-modulation. In

effect, the theoretical development says the voltage reference can be attained in three sample times; however, due to the amount of power required for this action, the time is enlarged to avoid damage to the power converter components. Therefore, the *dc* link voltage is reached in the shortest possible transient time to avoid exceeding the power converter limits.

The implementation was performed on a TMS320F6713 DSP using the uCube controller described in [46], with a total algorithm execution time of 20µs, which entails a minimum computational burden. This means that the proposed algorithm results in a very interesting choice with direct application in high-performance control systems. The proposed method also presents an additional advantage of a fast model-based control, which, however, employs a fixed switching frequency, with consequent simplification in measurements and filters design.



Figure 5. Different parameters, (**a**) *dc* voltage and reference, (**b**) v_s^{α} voltage and i_s^{α} current, (**c**) $\mathbf{i_s}^{\alpha\beta}$ currents, (**d**) active p_s and reactive q_s power, (**e**) load current i_L^{dc} , with (**1**) inductances increase to 200%, (**2**) inductances decrease to 50%, (**3**) capacitor increases to 200%, (**4**) capacitor decreases to 50%.



Figure 6. Experimental Setup.



Figure 7. Experimental Results, (**a**) *dc* voltage step up with unitary power factor, (**b**) *dc* voltage step up with power factor of 0.7(*inductive*), (**c**) change on the power factor, (**d**) load step up from 0 (A) to 4.7 (A).

6. Conclusions

Predictive control has proved to be an interesting alternative for power converter controls. Within the predictive control family, deadbeat control is used for its fast dynamics, simplicity of implementation (once a system model is known), and for the possibility of being used in conjunction with a modulator, ensuring high steady state quality of the con-

trolled signals and constant switching frequency. This work has proposed a multivariable DB control approach capable of controlling more than one converter variable, on both converter sides, in a single feedback loop. This approach retains the DB control feature of ensuring the fastest possible control action for all controlled variables, whilst still taking into account the variables' nature, their intrinsic dynamics, and the circuit power limitation. Furthermore, the maximum power can be set easily and therefore, protect the power converter's switches, filters, and circuit in general. The proposed strategy has also been tested under model uncertainty scenarios, demonstrating robustness and control effectiveness. In addition, the algorithm has low computational cost, obtaining a high performance with minimum digital effort and permits simple modulation techniques to be employed, such as SPWM, which facilitates filtering design. The theory has been corroborated by use of simulations and experimental results to highlight the feasibility of the proposed strategy and its capacity to be included in industrial implementations.

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