



Article Fabrication of Silicon Nanowire Metal-Oxide-Semiconductor Capacitors with Al₂O₃/TiO₂/Al₂O₃ Stacked Dielectric Films for the Application to Energy Storage Devices

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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). **Abstract:** Silicon nanowire (SiNW) metal-oxide-semiconductor (MOS) capacitors with Al₂O₃/TiO₂/Al₂O₃ (ATA) stacked dielectric films were fabricated by metal-assisted chemical etching (MACE) and atomic layer deposition (ALD). High-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) images revealed that SiNWs were conformally coated with ATA although the cross-sectional shapes of MACE-SiNWs were non-uniform and sharp spikes can be seen locally. The dielectric capacitance density of 5.9 μ F/cm² at V = -4 V of the perfect accumulation region was achieved due to the combination of the large surface area of the SiNW array and the high dielectric constant of ATA. The capacitance changed exponentially with the voltage at V < -4.3 V and the capacitance of 84 μ F/cm² was successfully achieved at V = -10 V. It was revealed that not only 3D structure and high-*k* material but also local nanostructure of SiNWs and stacked dielectric layers could contribute to the considerable high capacitance.

Keywords: silicon nanowire; energy storage device; metal assisted chemical etching; atomic layer deposition

1. Introduction

Electrostatic capacitors have attractive characteristics for the application in energy storage devices. Electrostatic capacitors have considerably higher power densities than batteries and electrochemical capacitors because of their short charge/discharge time (<1 μ s) [1]. Moreover, electrostatic capacitors have high mechanical and thermal stabilities [1]. Since electrolyte solution is not necessary for electrostatic capacitors, there are much lower risks of fire and explosion compared to Li ion batteries and so on. However, electrostatic capacitors. These characteristics limit the application to large-scale energy storage devices, for example, energy storage devices for renewable energies such as photovoltaic systems [2] and for vehicles [3,4]. In the case of capacitors, it is necessary to achieve high capacitance density for high energy density. Three-dimensional (3D) structuring is one of the methods to achieve high capacitance density. The capacitance density of an electrostatic capacitor with 3D structures with respect to its imprint area is given by the following equation.

$$C = \varepsilon_r \varepsilon_0 \frac{S}{tA'},\tag{1}$$

Here, ε_r is the relative dielectric constant of the dielectric layer, ε_0 is the permittivity of the vacuum, *S* is the electrode surface area, *A* is the top view area occupied by the device,

and *t* is the dielectric layer thickness [5]. Thus, capacitors with 3D structures have high capacitance density because of the high *S*/*A* ratio.

There are several approaches to implement 3D structure into capacitors as summarized in Table 1. Banerjee et al. adopted anodic aluminum oxide (AAO) template to fabricate a 3D capacitor structure [6]. TiN/Al₂O₃/TiN stack layers were deposited on AAO templates with a pore depth of 10 μ m and a pore diameter of 50 nm by atomic layer deposition (ALD). Further, 100 μ F/cm² was achieved by the metal/insulator/metal (MIM) capacitor. Silicon nanowires (SiNWs) are also one of the 3D structures with a considerably high S/A ratio. There are some reports of metal-oxide-semiconductor (MOS) capacitors using SiNWs. Morel et al. achieved the capacitance density of 18 μ F/cm² using SiNWs and 10-nm-thickalumina (Al_2O_3) deposited by atomic layer deposition (ALD) as a dielectric material [7]. However, this method to prepare SiNWs needs a chemical vapor deposition (CVD) process using copper catalysts, which is a vacuum process and requires a high temperature (above \sim 400 °C) [7]. Moreover, it is difficult to control the length and diameter of SiNWs using this CVD process, which means less controllability on the capacitance density. We adopted a metal-assisted chemical etching method (MACE) [8–10] to fabricate SiNWs for a SiNW MOS capacitor. The MACE process is simple and SiNWs can be obtained at room temperature in a large area. The diameter of SiNWs prepared by MACE can be controlled using silica nanoparticles as etching masks [11]. If the length, diameter, dielectric film thickness, and dielectric material can be designed as intended, it is possible for higher capacitance density to be achieved with good controllability. A SiNW MOS capacitor has the potential of an easy fabrication process, good controllability, and higher capacitance density. A SiNW MOS capacitor with the SiNW length of 2.4 μ m and Al₂O₃ thickness of 10 nm, fabricated by MACE achieved the maximum capacitance of 4.1 μ F/cm² [5]. However, there are no reports about a 3D MIM or MOS capacitor with a dielectric layer with a higher dielectric constant than Al_2O_3 as shown in Table 1. It is expected that a MOS capacitor with a high-k material and a 3D structure has a higher capacitance density. Titania (TiO_2) is one of the high-k materials, which is easily prepared by ALD [12-14]. The relative dielectric constant of TiO₂ ranges from 16 to 100 [13,15], which depends on the type of crystals. However, its relatively less narrow bandgap (~3.3 eV [16–18]) compared to other oxides causes high leakage current density. Thus, TiO_2 combined with Al_2O_3 has been studied to overcome the problem. The preparation of $Al_2O_3/TiO_2/Al_2O_3$ (ATA) [19–21], Al-doped TiO_2 [20,22], $(Al_2O_3)_x(TiO_2)_y$ [23], nanolaminated Al_2O_3 -TiO_2 [24,25], and $AlO_x/TiO_x/ZnO_x$ [26] has been reported. Woo et al. fabricated flat MIM capacitors with ATA as an insulator and achieved 2.13 μ F/cm² at 1 MHz [19]. In this study, we implemented a SiNW template into a MOS capacitor with ATA as an insulator (Figure 1), and measured device characteristics. As a result, it was found that an increase of capacitance versus voltage and considerable high capacitance of 84 μ F/cm² at -10 V and 1 MHz can be achieved using SiNW MOS capacitors with ATA. It was revealed that not only 3D structure and high-k material but also the local nanostructure of SiNWs and stacked dielectric layers could contribute to the considerably high capacitance density.

Table 1. Comparison of capacitance density and leakage current density of each capacitor with the literature. 3D structures such as ZnO nanorod (ZnO-NR), porous Si (P-Si), Si trench (Si-TR), anodic aluminum oxide (AAO), and SiNW were used as a template. Part of the data was read from the figure in each reference using a software.

Туре	Template	Insulator	Capacitance Density (µF/cm²)	Leakage Current Density (A/cm ²)	Electrode Area (cm ²)	Ref.
MIM	ZnO-NR	Al ₂ O ₃ (10 nm)	$6.3 imes 10^{-3}$ (10 kHz)	$7.16 imes 10^{-3}\ (1 ext{ V})$	0.25	[27]
MOS	P-Si	Al ₂ O ₃ (50 nm)	2.5 (10 kHz)	$5.27 imes 10^{-5}$ (1 V)	$\begin{array}{c} 1.13 \times 10^{-2} \\ 1.33 \times 10^{-2} \end{array}$	[28]
MIM	Si-TR	Al ₂ O ₃ (9~10 nm)	3.62 (200 Hz)	3×10^{-9} (1 V)	$3.3 imes 10^{-3}$	[29]

Туре	Template	Insulator	Capacitance Density (µF/cm ²)	Leakage Current Density (A/cm ²)	Electrode Area (cm ²)	Ref.
MIM	AAO	Al ₂ O ₃ (10 nm)	3.7 (200 kHz)	$1.7 imes 10^{-7}\(1\ { m V})$	$1.0 imes 10^{-4}$	[30]
MOS	SiNW	Al ₂ O ₃ (10 nm)	4.1 (1 kHz)	$1.49 imes 10^{-9} \ (-1 ext{ V})$	$2.5 imes 10^{-5}$	[5]
MOS	SiNW	Al ₂ O ₃ (10 nm)	18 (1 kHz)	$4.0 imes 10^{-6}\ (1 ext{ V})$	$1 imes 10^{-4}$	[7]
MIM	AAO	Al ₂ O ₃ (7 nm)	26.2 ± 1.5 (20 Hz)	$4.3 imes 10^{-10}\ (0.7\ { m V})$	-	[31]
MIM	AAO	Al ₂ O ₃ (6.6 nm)	100 (20 Hz and DC)	$6.63 imes 10^{-10} \ (1 ext{ V})$	$1.27 imes 10^{-4}$	[6]
MIM	Flat	Al ₂ O ₃ (6 nm)/ TiO ₂ (20 nm)/ Al ₂ O ₃ (6 nm)	2.13 (1 V, 1 MHz)	$4.71 imes 10^{-13}$ (1 V)	$6 imes 10^{-6}$	[19]
MIM	Flat	Anatase TiO ₂ (4 nm)/ Al ₂ O ₃ (1.25 nm)/ Rutile TiO ₂ (4 nm)	4.26 (-1 V, 1 MHz)	$9.41 imes 10^{-5}$ (-1 V)	$3.53 imes 10^{-4}$	[25]
MOS	Flat	$(TiO_2)_x$ (2.5 nm)/ (Al ₂ O ₃) _y (2.5 nm)	6.96 (1 V, 1 MHz)	$5.31 imes 10^{-6}$ (1 V)	7.85×10^{-5}	[23]
MOS	SiNW	Al ₂ O ₃ (3.6 nm)/ TiO ₂ (15.2 nm)/Al ₂ O ₃ (3.7 nm)	0.99 (-1 V, 1 MHz) 5.9 (-4 V, 1 MHz) 84 (-10 V, 1 MHz)	$\begin{array}{c} 3.81 \times 10^{-4} \\ (-1 \text{ V}) \\ 7.45 \times 10^{-1} \\ (-4 \text{ V}) \end{array}$	1.96×10^{-3}	This study





Figure 1. Schematic diagram of a fabricated SiNW MOS capacitor. The insulator consists of an $Al_2O_3(3.6 \text{ nm})/TiO_2(15.2 \text{ nm})/Al_2O_3(3.7 \text{ nm})$ stacked structure.

2. Materials and Methods

p-type Czochralski-silicon (Si) (100) wafers, which have a $525 \pm 25 \,\mu\text{m}$ thickness and resistivity of 2–5 Ω ·cm, were used. SiNWs were prepared on the Si wafers by the MACE method. The Si wafers were dipped into the AgNO₃ and HF mixed solution (AgNO₃: HF: $H_2O = 120$ mg: 10 mL: 40 mL) for 50 seconds to deposit Ag nanoparticles. After that, the Si wafers with the Ag nanoparticles were dipped into the H₂O₂ and HF mixed solution (H_2O_2 : HF: $H_2O = 0.7$ mL: 10 mL: 40 mL) to etch Si using the Ag nanoparticles as catalysts. The etching duration was set to 1.5 and 15 minutes, which corresponds to the SiNW length of 1 and 8 μ m. The samples were immersed in HNO₃ for 10 minutes and HF (5%) for 1 minute to remove Ag residues for three successive cycles. Before the dielectric thin film deposition on SiNWs, the samples were cleaned by dipping in a piranha solution at 120~140 °C for 15 minutes and an HF (5%) solution at room temperature for 1 minute. The stacked dielectric films of $Al_2O_3(3.5 \text{ nm})/\text{Ti}O_2(16 \text{ nm})/Al_2O_3(3.5 \text{ nm})$ (ATA) were deposited on SiNWs and a flat Si substrate by ALD (Arradiance, GEMSTAR-6) at 200 °C. $Al(CH_3)_3$ (trimethyl-aluminum: TMA) and $Ti(N(CH_3)_2)_4$ (tetrakis(dimethylamino)titanium: TDMAT) were used as precursors for Al_2O_3 and TiO_2 , respectively. H_2O was also used as an oxidizer. The number of ALD cycles was set to make the total thickness of the ATA dielectric films ~23 nm. Al was deposited on surfaces covered with dielectric films by the vacuum evaporation method as surface electrodes. The size of the electrodes was 0.5 mm ϕ . InGa was pasted on the back surface as a back electrode. The structure and dielectric film of the samples were characterized by scanning electron microscopy (SEM: JEOL, JSM-7001FA), energy dispersive X-ray spectrometry (EDS), Fourier transform infrared spectroscopy (FT-IR: Bruker, ALPHA), and high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM: JEOL, JEM-ARM200F). Capacitance density and leakage current density characteristics were measured using an LCR meter (HP, 4248A) and an electrometer (Keithley, 6517B/J), respectively. The capacitance density was measured at the ac applied voltage of 10 mV and a frequency of 1 MHz.

3. Results and Discussion

Figure 2a shows a cross-sectional scanning electron microscopy (SEM) image of an SiNW array of MACE for a duration of 15 minutes after ATA deposition. It was found that SiNWs were embedded in a dielectric material and the length of SiNWs is around 8 μ m. The energy-dispersive X-ray spectroscopy (EDS) mappings of Al K, Ti K, and O K signals are shown in Figure 2b–d, respectively. From these EDS mappings, signals from Al, Ti, and O atoms were detected through the whole parts of the SiNWs. FT-IR spectra for ATA/SiNW samples with different lengths of SiNWs are shown in Figure S1. The FT-IR spectra showed two broad bands between 1000–700 cm⁻¹ and 700–400 cm⁻¹ and the absorbance of the broad bands was increased with increasing the length of SiNWs. According to the previous papers, the bands are attributed to vibrations characteristic of Al₂O₃ [32] and amorphous TiO₂ [33,34]. If TiO₂ was crystallized, a strong TiO₂ anatase band at 435 cm⁻¹, TiO₂ is amorphous.

Figure 3 shows HAADF-STEM images of ATA/SiNWs cut into round slices. From Figure 3a, it was found that the SiNWs had random shapes, and each SiNW had relatively flat-face parts and sharp spikes. Regardless of such a non-uniform shape, the whole surface of SiNWs is successfully coated with ATA. This is because enough exposures of precursors were set as mentioned below. Figure 3b showed that the ATA film consisted of triple layers (Al₂O₃/TiO₂/Al₂O₃). From the TEM image, each thickness of ATA was Al₂O₃(3.6 nm)/TiO₂(15.2 nm)/Al₂O₃(3.7 nm). The ALD method provides uniform coatings inside holes and trenches with very high aspect ratios, using suitable pairs of reactants supplied in alternating doses of vapor [35]. In the experiment, the exposures of Al(CH₃)₃ (trimethyl-aluminum: TMA) and Ti(N(CH₃)₂)₄ (tetrakis(dimethylamino)titanium: TD-MAT), which are precursors for Al₂O₃ and TiO₂, respectively, were set as 2.0 × 10⁵ and 4.4 × 10⁴ Langmuir (1 Langmuir = 1.33×10^{-4} Pa·s = 1.0×10^{-6} Torr·s), respectively. According to a kinetic model introduced by Gordon et al. [36], the exposure required to

conformally coat a hole with a certain aspect ratio *a* is given by the depth of a hole/diameter of a hole.

$$(Pt)_{\min} = S_C \sqrt{2\pi m k_B T} \left(1 + \frac{19}{4}a + \frac{3}{2}a^2 \right), \tag{2}$$







Figure 3. Round-sliced HAADF-STEM images of a SiNW array coated with ATA, (**a**) \times 160,000, (**b**) \times 1,600,000. Each thickness of ATA was Al₂O₃(3.6 nm)/TiO₂(15.2 nm)/Al₂O₃(3.7 nm).

In this equation, S_C is the saturated coverage of the reactant molecule per unit surface area (molecules/m²), *m* (kg) is the mass of the reactant molecules, k_B is the Boltzmann constant, and *T* (K) is the sample temperature. When the aspect ratio was assumed to be $a = \text{Depth}(8 \,\mu\text{m})/\text{Diameter}(0.1 \,\mu\text{m}) = 80$, the (*Pt*)_{min} for TMA and TDMAT were

estimated to be 2.8×10^4 and 1.4×10^4 Langmuir, respectively. The exposures used in this experiment are large enough compared to the $(Pt)_{min}$. Therefore, conformally coated SiNWs were successfully obtained. The cross-sectional SEM images of ATA/SiNWs after Al deposition are shown in Figure S2. It was found that ATA/SiNWs were not perfectly covered with Al. Al electrodes were localized on the surface from the top to the middle of SiNWs. To charge electrons fully in the SiNW MOS capacitor, the perfectly covered Al electrode is preferable. Therefore, it is possible to enhance the capacitance density further by improving the coverage of Al electrodes. The length of SiNWs can be controlled by the duration of MACE. To increase the surface area of the SiNW array, longer SiNW is preferable. However, Al flakes can be found only until the middle of SiNWs. Therefore, in this study, 1 and 8 μ m were adopted for the lengths of SiNWs.

Figure 4a shows capacitance-voltage (*C*-*V*) characteristics of MOS capacitors using a flat Si and a SiNW with L = 1 and 8 µm. The *C*-*V* curve of the flat capacitor has typical MOS characteristics. Assuming that there are few fixed charges in the ATA film in the flat MOS capacitor, the flat band voltage (V_{FB}) of -0.87 V should be obtained, which comes from the work function difference between Al and Si ($\phi_{\text{MS}} = 0.87$ eV [37]). However, the V_{FB} from Figure 4a was estimated to be -2.05 V, suggesting that there are fixed charges in the ATA film. The fixed charge density (Q_{f}) can be calculated by the following equation,

$$Q_{\rm f} = \frac{C_{ox}}{qA} (\phi_{\rm MS} + V_{\rm FB}), \tag{3}$$

where C_{ox} is the measured dielectric capacitance at accumulation, *q* is the elementary charge, and *A* is the area of electrodes. The positive fixed charge density of the flat MOS capacitor was calculated to be 5.1×10^{12} cm⁻². These positive fixed charges seem to mainly come from dipoles induced by cation intermixing near the TiO₂/Al₂O₃ interface [38]. Zhang et al. reported that local intermixing of TiO₂ and Al₂O₃ in the annealed dielectric is suggested by the grading of the composition profile over a distance of ~1 nm with respect to the nominal interface positions. When titanium atoms are incorporated in aluminum sites in Al₂O₃, they act as electron donors (Ti_{A1}⁺), whereas Al in TiO₂ are expected to be incorporated as acceptors occupying the Ti site (Al_{Ti}⁻). Many of the Ti_{A1} species in Al₂O₃ are expected to be in a positive charge state, whereas the Al_{Ti} defects in TiO₂ are predicted to occur in the negative charge state. That is why dipoles are generated near the TiO₂/Al₂O₃ interfaces. Since the thickness of Al₂O₃ is very thin, with a value of 3.6 nm, the positive charges influence the depletion layer in p-type Si, and the flat band voltage was shifted.

At the inversion region (V = 1 V), the depletion layer capacities (C_d) of flat and SiNW MOS capacitors are 2.8×10^{-2} and $2.7 \times 10^{-2} \,\mu\text{F/cm}^2$, respectively. On the other hand, in the accumulation region ($V < V_{FB}$), C_d disappears and only C_{ox} can be measured shown in Figure S3. The capacitance density at the accumulation region (V = -5 V) of 0.7 μ F/cm² was achieved by the flat MOS capacitor using ATA. In the case of the SiNW MOS capacitor, two regions with a gradual slope can be seen in both L = 1 and 8 μ m. This suggests that there are two kinds of parts with and without dipoles in ATA. In the case of $L = 8 \mu m$, region 1 in the range of -1 V < V < -0.5 V represents the capacitance derived from the accumulation in the part without any dipoles, which means few fixed charges exist in an insulator. In fact, the $V_{\rm FB} = -0.25$ V at the part without any dipoles is much less than $V_{\rm FB} = -2.05$ V of the flat MOS capacitor with dipoles. On the other hand, region 2 in the range of -4 V < V < -3.5 V represents the capacitance derived from the accumulation in the part with the dipoles. The flat band voltage of the second region is around -1.9 V, which is comparable to $V_{\text{FB}} = -2.05$ V of the flat MOS capacitor. The capacitance in the range of -4 V < V < -3.5 V is a plateau, suggesting that charging was completely finished in all the parts with and without dipoles. The capacitance densities of SiNW MOS capacitors with 1 and 8 μ m were 3.2 and 5.9 μ F/cm² at -4 V. In this range, it can be regarded as a perfect accumulation region and this capacitance value was 4.6 and 8.4 times higher than that of the flat MOS capacitor using ATA, respectively. This is the effect of the 3D template. The higher capacitance density mainly comes from the larger surface area of a SiNW array

than the flat Si substrate. In the case of a single Al_2O_3 with a thickness of 25 nm, as shown in Figure S4, the capacitance densities of flat and SiNW MOS capacitors with $L = 1 \mu m$ were 0.31 and 0.55 μ F/cm², respectively. Therefore, by inserting a TiO₂ layer, capacitance densities of flat and SiNW MOS capacitors were 2.3 and 5.8 times enhanced, respectively. It suggests that the SiNW structure and ATA causes the capacitance density to be enhanced synergistically. The dielectric constant of a single Al_2O_3 and ATA is estimated at 8.8 and 19.8, respectively. Therefore, by inserting a TiO₂ layer, the dielectric constant was enhanced 2.25 times. In the case of a single TiO₂ layer, the *C-V* measurement was not successful due to a too-large leakage current.



Figure 4. (a) *C*-*V* characteristics, (b) *J*-*V* characteristics of SiNW MOS capacitors (blue and red solid line) and flat MOS capacitors (black solid line). The vertical axis shows the absolute value of leakage current density. (c) *J*-*V* characteristics of SiNW MOS capacitors fitted by the Fowler–Nordheim tunneling equation.

The parts without dipoles are attributed to the shape of SiNWs. As shown in the HAADF-STEM images of Figure 3a, several sharp spikes can be seen. At the sharp spikes, two different TiO_2/Al_2O_3 interfaces are close and intersect each other. That is why the cancellation of dipoles was caused. The dependence of the capacitance on the voltage can be observed at V < -4.3 V even though the depletion region seems to perfectly disappear (Region 3). Such a dependence is often observed on some capacitors using high-*k* films. The detailed investigation is written below.

Figure 4b shows the leakage current density-voltage (*J-V*) of the flat and SiNW MOS capacitors using ATA. The vertical axis shows the absolute value of leakage current density. The SiNW MOS capacitor shows a higher leakage current density than the flat MOS capacitor in the whole applied voltage. One possible reason is the area used in this calculation. The leakage current density was obtained by dividing the measured leakage current by a top view area of the device, indicating that the leakage current density of SiNW MOS capacitors is overestimated. Ideally, the increasing rates of capacitance density and leakage current density by implementing a 3D structure should be equal. However, the increasing rate of capacitance density was 8.4 times. On the other hand, the leakage current density of the SiNW MOS capacitor. Therefore, other effects should be considered. The Al₂O₃ layers in the ATA are not sufficiently thick to prevent tunneling current. Under the application of a high electric field, the barrier of Al₂O₃ has a triangular shape. Tunneling through the triangular barrier can be characterized as Fowler–Nordheim (F-N) tunneling [39]. The F-N current density is given by the following equation.

$$J \propto E^2 \exp\left[\frac{-4\sqrt{2m_e}(q\phi_{ox})^{3/2}}{3\hbar qE}\right],\tag{4}$$

Here, *E* is the net electric field applied to a barrier oxide layer, m_e is an effective mass in a barrier material, *q* is an elementary charge, ϕ_{ox} is a barrier height, and \hbar is a Dirac constant. Since under high voltage biases, the barrier thickness is reduced, the tunneling current density was increased according to Equation (4). The dashed line in Figure 4c shows fitted curves. $m_e = 0.2m_0$ was used as an effective mass in Al₂O₃ [40]. Assuming that $E = V/d_{ox}$ can be applied and $d_{ox} = 3.7$ nm, the barrier heights ($q\phi_{ox}$) are estimated at 0.36 and 1.1 eV, respectively. These values are lower than the conduction band offset between TiO₂ and Al₂O₃. The details are discussed in the last paragraph. The leakage current density of the SiNW MOS capacitor with $L = 1 \mu m$ is larger than that of $L = 8 \mu m$. This is due to the difference of the existence of the non-coverage area of an Al electrode.

Schmitz et al. reported the RF capacitance-voltage characterization of MOSFETs with high leakage dielectrics [41]. This can be understood conceptually by considering a simple three-element equivalent circuit for the leaky MOS capacitor as shown in Figure S5. The capacitance *C* is connected in parallel with a differential conductance *g* derived from the leakage current. *R* is an external resistance. A capacitance measurement is only straightforward when the capacitance is large enough (typically at least 1 pF), and the quality factor (Q_f) is larger than unity. To obtain the $Q_f > 1$, the minimum measurement frequency can be expressed as

$$f_{\min} = \frac{1 - \sqrt{1 - 4gR(1 + gR)}}{4\pi RC} \approx \frac{g}{2\pi C'},$$
(5)

From a linear fitting in the range of -4 to -1 V in Figure 4b, conductance in the SiNW MOS capacitor with the length of 8 µm is estimated roughly at 3.3 mS. For a $S = \pi (0.025)^2$ cm² MOS capacitor, typical values are C = 5.9 µF/cm² × S = 12 nF, g = 3.3 mS, and $R = 10 \Omega$ leading to $f_{min} = 49$ kHz. We tried to conduct *C-V* measurement at 50 kHz as shown in Figure S6. The capacitance density was decreased by increasing the absolute value of the applied voltage due to the tunnel leakage current [42]. Since we conducted the

C-V measurement at 1 MHz, the influence of the leakage current on the *C-V* measurement can be ignored in this measurement.

To conduct a more detailed investigation of capacitance characteristics at V < -4.3 V (Region 3) of the SiNW MOS capacitor using ATA, the *C*-*V* characteristics in the range of -10 V < V < -4 V was measured as shown in Figure 5. The exponential increase with decreasing voltage can be observed at V < -6 V. The considerable high capacitance density of 84 μ F/cm² can be obtained at V = -10 V. The combination of the local nanostructure in SiNWs and the interface of the stacked dielectric layers could contribute to a capacitance density 120 times higher compared to the flat capacitor with ATA.



Figure 5. *C*-*V* characteristics of the SiNW MOS capacitor using ATA ($L = 8 \mu m$) in the high voltage region (-10 V < V < -4 V). The solid line shows an experimental curve, and the dashed line shows theoretical capacitance density represented by (10).

To understand this behavior, an equivalent circuit of the MOS capacitor with ATA was assumed as shown in Figure 6a. Not only C_{ox} but also the capacitance element at the interface of TiO₂/Al₂O₃ (C_i) was considered. The total impedance observed was measured as an equivalent-series RC combination as indicated in Figure 6b in this experiment. By equating the circuits (a) and (b), it can be shown that

$$R = R_i + \frac{R_{ox}}{1 + \omega^2 R_{ox}^2 C_i^2},$$
(6)

$$\frac{1}{\omega C} = \frac{1}{\omega C_i} + \frac{\omega R_{ox}^2 C_{ox}}{1 + \omega^2 R_{ox}^2 C_{ox}^2},\tag{7}$$

(a)

(b)



Figure 6. (a) Equivalent circuit depicting the interface impedance (C_i, R_i) in series with the oxide capacitance (C_{ox}, R_{ox}) . (b) Total observed capacitance *C* and resistance *R* in terms of an equivalent series circuit.

From Equation (7), the total capacitance density can be represented as

$$C = \frac{C_i (1 + \omega^2 R_{ox}^2 C_{ox}^2)}{1 + \omega^2 (R_{ox}^2 C_{ox} C_i + R_{ox}^2 C_{ox}^2)},$$
(8)

When C_i is much larger than C_{ox} and $\omega^2 R_{ox}^2 C_{ox} C_i \gg 1$, Equation (9) can be obtained.

$$C \simeq C_{ox} + \frac{1}{\omega^2 R_{ox}^2 C_{ox}},\tag{9}$$

Figure 7 shows the capacitance–frequency characteristics of the SiNW MOS capacitor with ATA ($L = 8 \mu m$) at V = -5 V. From Equation (8), $C_{ox} = 5.0 \mu F/cm^2$, $C_i = 3.9 \times 10^3 \mu F/cm^2$, and $R_{ox} = 4.1 \times 10^{-7} M\Omega \cdot cm^2$ were obtained. C_i is much larger than C_{ox} . In general, the capacitance density of an electric double layer is ~20 $\mu F/cm^2$. If the length, diameter, and filling ratio are 8 μm , 100 nm, and 0.5, the surface area is about 160 times compared with a flat substrate. If such an electric double layer exists at the interface in the ATA, $3.9 \times 10^3 \mu F/cm^2$ can be realized. From the R_{ox} value, $g_{ox} = 4.8 mS$ can be obtained, which is comparable with that of 3.3 mS from Figure 4c. Assuming that the electric field is uniform at $E = V/d_{ox}$ and R_{ox} is determined by Equation (4), the relationship between *C* and *V* can be obtained as follows.

$$C \propto V^2 \exp\left(-\frac{8\sqrt{2m_e}(q\phi_{ox})^{3/2}d_{ox}}{3\hbar q(-V)}\right) + C_{ox},\tag{10}$$



Figure 7. Capacitance–frequency characteristics of SiNW MOS capacitor with ATA ($L = 8 \mu m$) at V = -5 V. The solid line shows an experimental curve, and the dashed line shows theoretical capacitance density represented by the Equation (8).

By fitting Equation (10) and the *C*-*V* characteristics as shown in Figure 5, $q\phi_{ox} = 1.1 \text{ eV}$ was obtained. This value corresponds to that obtained from Figure 4c. To discuss the height of the barrier for tunneling, the calculated MOS band diagram at V = -5 V is shown in Figure 8. These simulation results were obtained using the TCAD software Silvaco Atlas. Since, under a large bias, the voltage high electric field is applied to the Al₂O₃ layer on the p-type Si side, the barrier of Al₂O₃ has a triangular shape. Therefore, F-N tunneling occurs at the interface. The holes are supplied from the p-type Si into the interface between TiO₂/Al₂O₃ on the metal side. It is believed that this is the origin of the *C_i*. In this case, the hole barrier height at the Al₂O₃/p-type Si interface is 2.37 eV, which is larger than the obtained value of 1.1 eV. One possibility is the non-uniform electric field distribution. In this calculation of the barrier height, a uniform electric field of E = V/d_{ox} was assumed. However, at local sharp spikes of SiNWs seen in Figure 3a, the electric field is concentrated, leading to high leakage current according to Equation (4). Therefore,

 $q\phi_{ox}$ was underestimated. Another reason for the lower barrier height is defects in Al₂O₃. As mentioned before, cation intermixing forms positive and negative charge states in Al₂O₃ [38]. The positive charge states are located at a higher level by 3.5 eV from the top of the valence band in Al₂O₃. It is possible that positive charge states assist hole tunneling, leading to the underestimation of the barrier height.



Figure 8. Calculated MOS band diagram at V = -5 V. These simulation results were obtained using the TCAD software Silvaco Atlas. The work function of Al electrode was assumed at 4.20 eV. The electron affinities of Al₂O₃ and TiO₂ were taken to be 1.4 [43] and 4.0 eV [44], respectively. The bandgaps of Al₂O₃ and TiO₂ were taken to be 6.4 [43] and 3.2 eV [45], respectively.

If this model is true, the interface charging phenomenon at TiO_2/Al_2O_3 is very important. Since this charging can be obtained under a DC bias, it is acceptable to charge electricity from renewable energy. It should be studied further. Apparently, from Figure 5, the capacitance density seems to increase until C_i by increasing the absolute value of the applied voltage. However, if the leakage at the TiO_2/Al_2O_3 interface on the metal side becomes remarkable due to tunneling, the capacitance density could be decreased. To realize a high capacitance density close to C_i , further investigation including device design is necessary.

4. Conclusions

SiNW MOS capacitors with ATA stacked dielectric films were fabricated by MACE and ALD. HAADF-STEM images revealed that although the cross-sectional shapes of MACE-SiNWs are non-uniform and sharp spikes can be seen locally, SiNWs were conformally coated with ATA. Each thickness of ATA was Al₂O₃(3.6 nm)/TiO₂(15.2 nm)/Al₂O₃(3.7 nm). The dielectric capacitance density of 5.9 μ F/cm² at V = -4 V of the perfect accumulation region was achieved due to the combination of the large surface area of the SiNW array and the high dielectric constant of ATA. The capacitance changed exponentially with voltage at V < -4.3 V and the maximum capacitance of 84 μ F/cm² was successfully achieved at V = -10 V. Not only 3D structure and high-*k* dielectrics, but also the combination of local nanostructure in SiNWs and the interface of the stacked dielectric layers, could contribute to a capacitance density 120 times higher compared to the flat capacitor with ATA. It was found that ATA/SiNWs were not perfectly covered with the Al electrode. Therefore, it is possible to enhance the capacitance density further by improving the coverage of the Al electrodes.

Supplementary Materials: The following are available online at https://www.mdpi.com/article/10 .3390/en14154538/s1, Figure S1: FT-IR spectra of SiNW arrays and a flat Si wafer coated by ATA. Two pronounced bands are attributed to IR absorption by Si–O₂ complexes (at ~1107 cm⁻¹) and by Si lattice phonons (at ~610 cm⁻¹), respectively. An Al₂O₃ broad band (500~1000 cm⁻¹) can be seen. If TiO₂ was crystallized, strong TiO₂ anatase band at 435 cm⁻¹ could be observed. However, since there is no strong band at 435 cm⁻¹, TiO₂ is amorphous, Figure S2. Cross-sectional SEM image of a SiNW MOS capacitor after Al evaporation. Flakes of Al crystals can be seen from the top to middle of SiNWs. Since Al electrodes were deposited by thermal evaporation, SiNWs were not perfectly coated with Al, Figure S3. Energy band diagram and equivalent circuit of a MOS capacitor in the range of V < 0, Figure S4. *C-V* characteristics of (Dashed line) a flat MOS capacitor and (Solid line) a SiNW MOS capacitor using 25-nm-thick Al₂O₃ as an insulator. The length of SiNWs is 1.0 µm, Figure S5. Equivalent circuit approximation of a leaky MOS capacitor, Figure S6. *C-V* characteristics of the SiNW MOS capacitor with the length of 8 µm measured at 50 kHz.

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