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Design and Implementation of Improved High Step-Down DC-DC Converter for Electric Vehicles

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Abstract: An improved high step-down DC-DC converter for charging the batteries in an electric vehicle application is proposed in this paper. It adopts the topology of the conventional full-bridge converter, which has a coupled inductor current-doubler rectifier as the secondary side of the transformer. In addition, four power switches are driven using a phase-shifting technique. The proposed converter can achieve a high step-down voltage with low-voltage stress on the rectifier diodes. In addition, the coupled inductor current-doubler rectifier of the secondary side can reduce the ripple current and losses of the secondary side to achieve high efficiency. Furthermore, the proposed converter can overcome the drawbacks of the conventional full-bridge converter, such as switching loss caused by high switching frequency, duty-cycle loss, voltage stress, and numerous components, and can increase the efficiency with the soft-switching technique. A 600 W laboratory prototype of the proposed converter was manufactured. The results of the experiments performed with the prototype proved the effectiveness and validated the use of the proposed converter for better charging of electric vehicles.

Keywords: high step-down DC-DC converter; current-doubler rectifier; coupled inductor; phase-shift full-bridge; battery charger; electric vehicles; zero voltage switching

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1. Introduction

While the first and second industrial revolutions resulted in the improvement of mechanical and electrical technologies, the third industrial revolution has brought about the use of various electronic devices in people's everyday lives.

Various types of electronic devices have been developed over the years, based on improvements such as miniaturization and high efficiency, and the operating voltage of devices has been gradually decreasing; notably, the operating voltage of microprocessors has decreased from 5 V to 3.3 V. In some cases, operating voltage has dropped below 1 V, but current has gradually increased, and is expected to exceed 100 A in the future. Therefore, a point-of-load DC-DC converter with independent voltage distribution uses 5 V or 12 V as the main input voltage to reduce distribution loss. Based on these tendencies, an isolated DC-DC converter with high output current, high step-down voltage ratio, and high efficiency is usually required, as shown in the shaded area of Figure 1 [1].

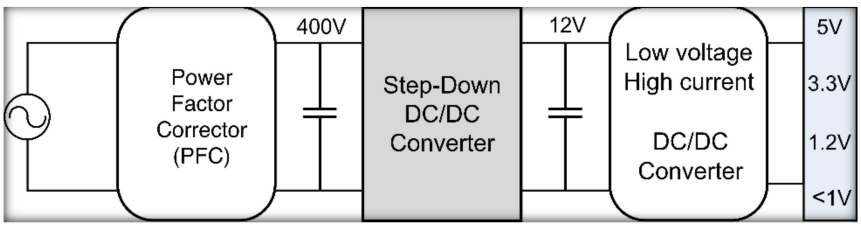

Figure 1. Distributed power conversion system.

In addition, global warming and the depletion of natural resources have become global issues in recent decades, resulting in the need to regulate carbon dioxide emissions; accordingly, various eco-friendly vehicles such as hybrid electric vehicles (HEV), plug-in HEVs (PHEV), mild HEVs (MHEV), and battery electric vehicles (BEV) have been developed. These vehicles, except for MHEV, necessarily require a rechargeable battery system as a power source for the electric traction system [2,3].

With the continued development of these systems, the importance of batteries in various electrical vehicles (xEVs) is increasing steadily. Among them, HEVs and PHEVs typically require a high-voltage battery to be charged from a public line via the AC–DC converter to drive the vehicle's electric motor; in addition, most of the vehicle's electronic equipment requires a low-voltage battery to be charged. In order to meet the requirements of low ripple current and high efficiency, a high-voltage battery, named as the battery charger, requires an AC-DC converter with a power factor corrector (PFC) circuit and an isolated DC-DC converter; this system is called an on-board charger (OBC) [4–9].

In addition, the low-voltage battery is charged from the high-voltage battery through a low-voltage DC-DC converter (LDC) to drive most of the vehicle's electronic equipment, such as lights, wipers, and audio [10,11]. The overall electric traction system of HEV and PHEV is shown in Figure 2.

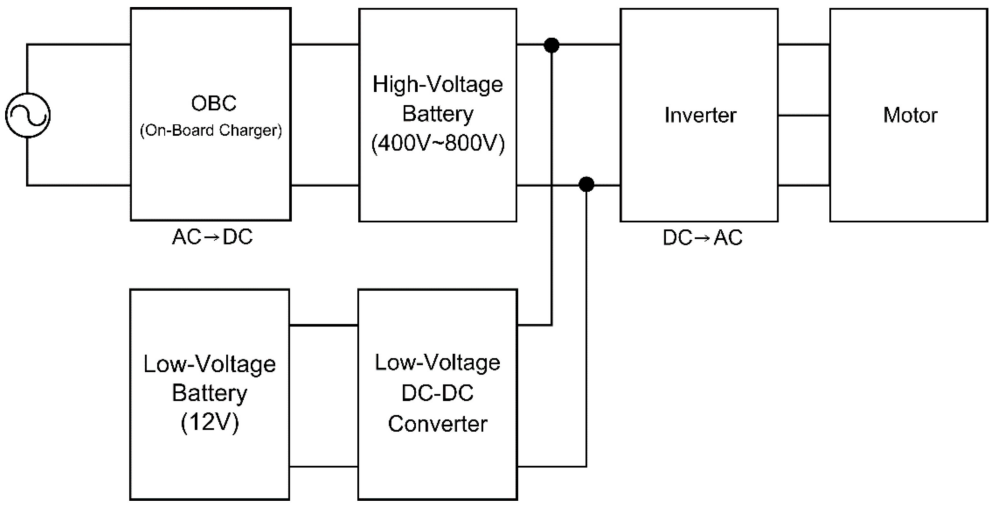

Figure 2. Power conversion system of xEVs.

Research into improving the efficiency and durability of the OBC and LDC has been actively conducted, and improvements in system weight, volume, and cost have been emphasized [12]. Moreover, the capacity of the OBC and LDC in HEVs and PHEVs is increasing in proportion to the capacities of high-voltage and low-voltage batteries. High power density and high efficiency are most essential to this system. In particular, a high switching frequency is required to achieve the high power density of the LDC, and the elements and circuit design should be selected appropriately to achieve high efficiency and reduce loss [13–15].

The LDC has two important roles in charging the low-voltage battery (auxiliary battery). First, the low-voltage battery, charged from the high-voltage battery and LDC, supplies a low voltage of 12 V to the electric field system of the EVs. Second, the LDC supplies high voltage during the initial operating phase of the EVs [10,16]. Therefore, the LDC is the most essential component in the power train of the EVs to charge the low-voltage battery, and various topologies have been developed based on it. A phase-shift full-bridge (PSFB) converter is a commonly used topology for low output voltage, high output current, and high efficiency, and it has been widely researched for medium- or high-power applications requiring isolation [17–19]. The PSFB has a very simple structure and can perform a zero-voltage-switching (ZVS) operation with constant frequency pulse-

width modulation (PWM), and without auxiliary components or complex control circuit. Nevertheless, it has limitations such as a high step-down voltage conversion, which necessitates a low duty ratio of the power switch or high turns ratio of the transformer. High turns ratio will increase the voltage stress of components such as the power switch [20]. In addition, the large external resonant inductor induces a very large circulating current, which flows through the primary winding of the transformer and the power switch during the reflux period. Therefore, the conduction loss of the power switch and copper loss of the transformer are of serious concern; in addition, reverse recovery losses occur. Several researchers have attempted to overcome these problems of the conventional PSFB converter [19,21–27]. In addition to the numerous studies on improvement of the primary side circuit, various secondary-side circuits for rectification have been considered in recent years; the secondary-side rectification circuits were introduced in [28–31]. Many researchers have adopted various techniques such as the conventional bridge rectifier, the center-tapped rectifier, and the current-doubler rectifier (CDR) as secondary rectification methods for the PSFB. The CDR method has proven suitable as a secondary side rectification method for a high-output-current application in many studies [32,33].

In this paper, a PSFB with a coupled inductor current-doubler rectifier (CICDR) is proposed as an LDC for EVs. The circuit design is illustrated in Figure 3. The proposed rectification method is the same as in the conventional CDR method, but the turns ratio of the coupled inductor can be adjusted to expand the range of the duty ratio, thereby reducing the current stress of the transformer and power switch and the output current ripple. Further, the voltage stress of the rectification diode can be reduced even in high-frequency operations and, consequently, the reverse recovery loss can be reduced.

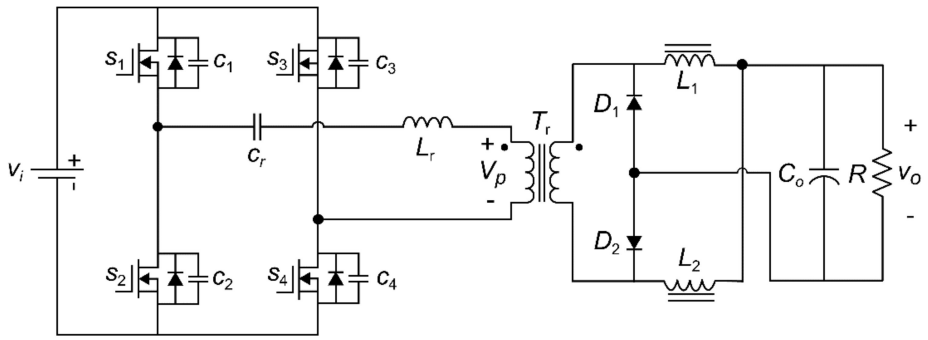

Figure 3. Proposed converter with CICDR.

Section 2 describes and proves the operating principle of the proposed converter. Section 3 describes the steady-state operation analysis and characteristics of the proposed converter.

The design considerations of the proposed converter are presented in Section 4, and Section 5 describes the experimental results obtained with a 600 W laboratory prototype of the proposed converter to verify its feasibility. Finally, the conclusion is presented in Section 6.

2. Derivation and Operating Principles of the Proposed Converter

2.1. Circuit Derivation

The derivation of the CDR method is based on the conventional voltage-doubler rectifier circuit shown in Figure 4a. Based on the concept of duality, nodes are used in place of the meshes of the voltage-doubler and inductors replace conductors; a current-doubler rectifier is formed with no change in diodes, as depicted in Figure 4b. Based on the secondary rectification method presented above, this paper proposes the CICDR method for the secondary side; the electrical schematic diagram is shown in Figure 4c. Figure 5 presents the winding arrangement of the CICDR. The two freewheeling diodes and the output capacitor C_o are the same as in the conventional CDR, but the output filter inductor

combines two filter inductors and the winding is located on the outer leg of the E-Type single core. Finally, the coupled inductor functions as a transformer, and the currents i_{Lo1} and i_{Lo2} generate magnetic flux in the winding direction, which is added to the center leg. The turns ratio of the two windings is assumed as one. The electrical characteristics are presented in Figure 6.

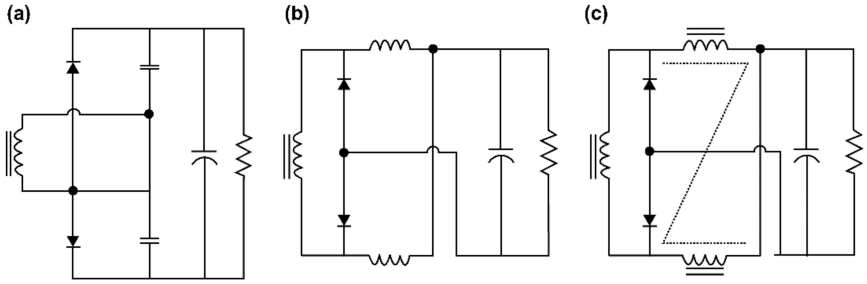

Figure 4. Development of the proposed CICDR: (**a**) voltage-doubler rectifier; (**b**) current-doubler rectifier; (**c**) electrical schematic of the proposed CICDR.

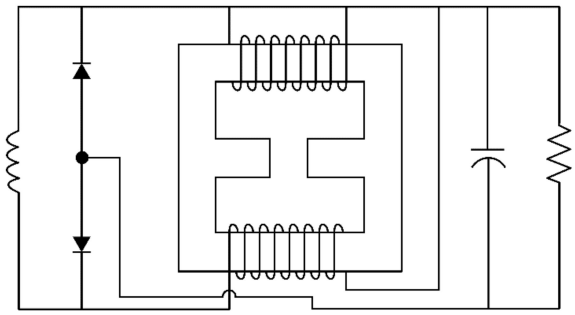

Figure 5. Winding arrangement of the proposed CICDR.

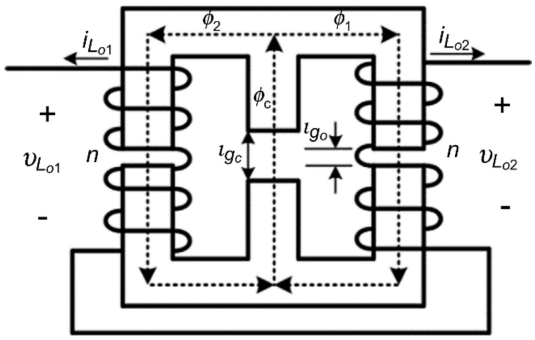

Figure 6. Coupled inductor.

2.2. Analysis of Operating States of Modes

To analyze the operation of the proposed converter, the following assumptions are made:

- The switching devices are ideal MOSFETs except for the internal body diodes and parasitic capacitors.
- The transformer ideally operates according to the turns on the primary and secondary sides, i.e., N_p and N_s, respectively.
- The output filter inductors have the same magnitude, i.e., $L_1 = L_2$, and the output current ripples are the same, i.e., $\Delta i_{L1} = \Delta i_{L2}$.
- The output filter capacitor C_o is large enough to be treated as a voltage source with output voltage V_o.

Figure 7 shows the key waveforms of the proposed converter. v_p, v_s denotes the voltage across the resonant inductor and the primary winding of the transformer and the voltage of the secondary side of the transformer, respectively, and i_p denotes the primary side current of the transformer. i_{L1} and i_{L2} denote the currents of the coupled inductor, D_{eff} and D_{loss} denote the effective duty cycle and duty cycle loss, respectively, and i_o denotes the output current. From Figure 7, the proposed converter has six modes during a half cycle, and the other half cycle has symmetrical operation. Figure 8 shows the equivalent circuits for twelve operation modes. Additionally, the other symbols stated in all equations are as follows:

v_i—Input voltage
v_o—Output voltage
v_{C1}, v_{C2}, v_{C3}, v_{C4}—voltage of the switch capacitor
i_i—Input current
i_o—Output current
n—Turns ratio of the transformer
L_k—Leakage inductance of the transformer
C_{oss}—Output capacitance of the switch
f_s—Switching frequency

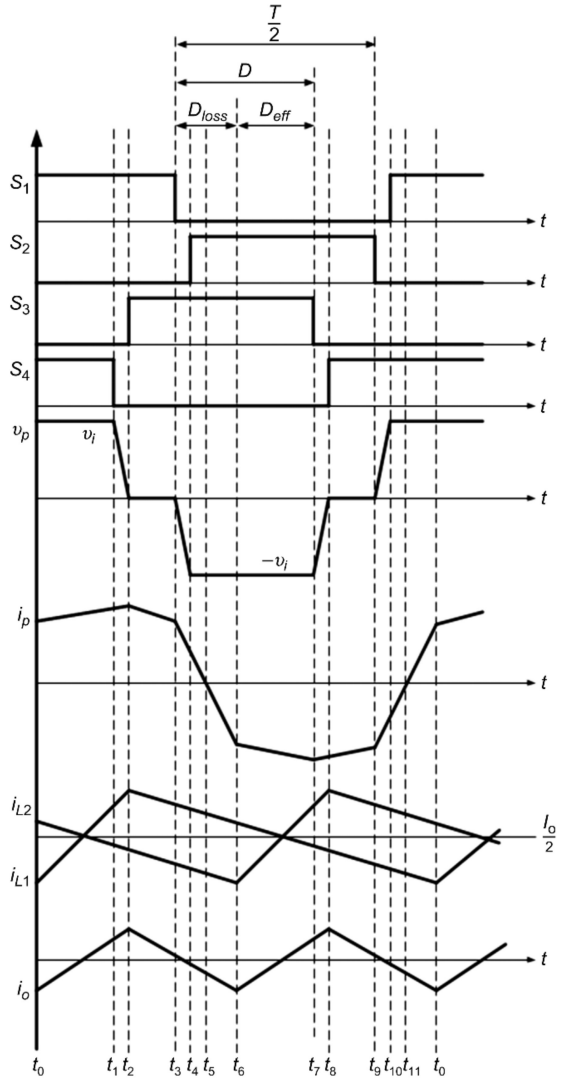

Figure 7. Key waveforms of the proposed converter.

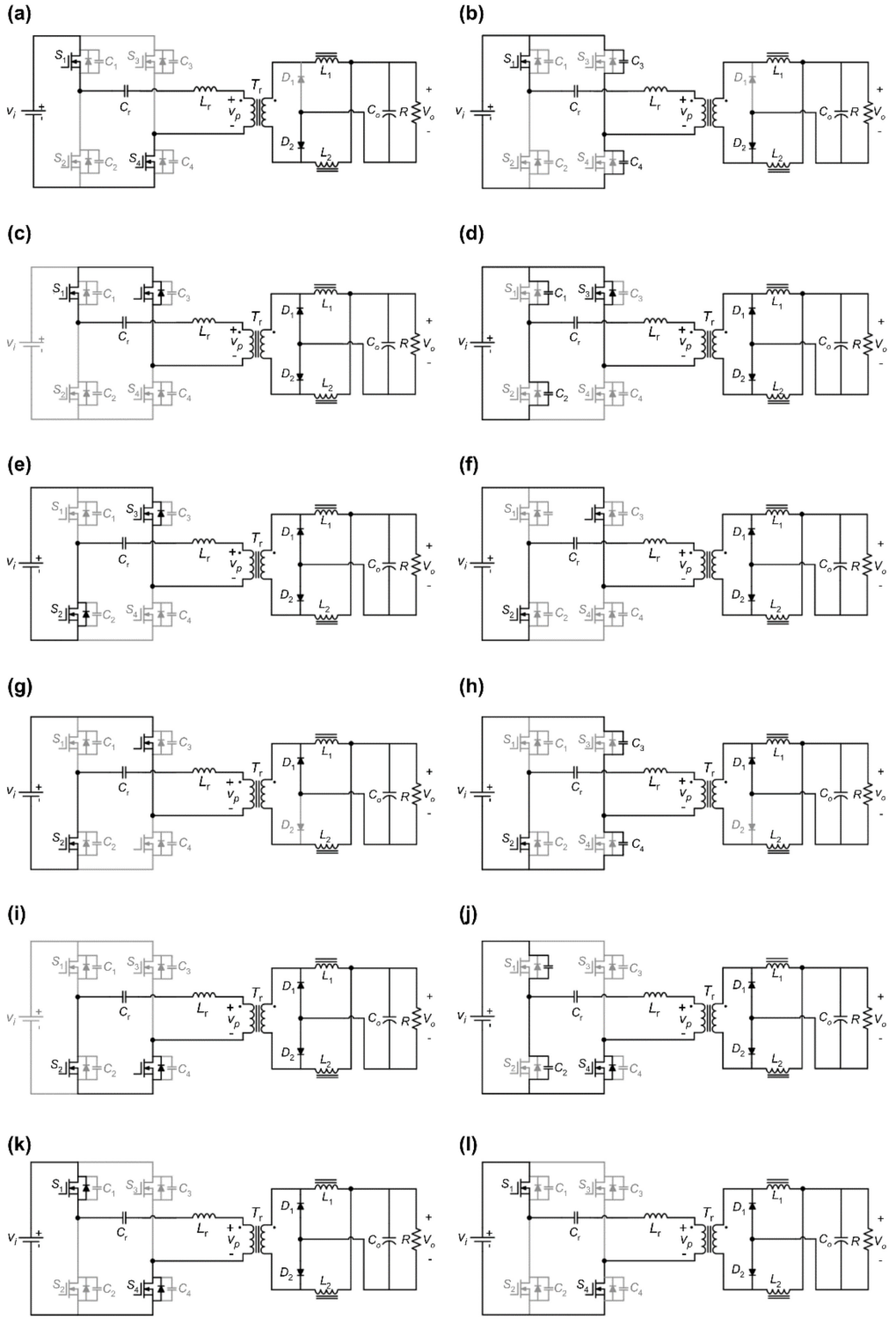

Figure 8. Equivalent circuits of the operating modes. (**a**) *Mode* 1 ($t_0 \leq t < t_1$) (**b**) *Mode* 2 ($t_1 \leq t < t_2$) (**c**) *Mode* 3 ($t_2 \leq t < t_3$) (**d**) *Mode* 4 ($t_3 \leq t < t_4$) (**e**) *Mode* 5 ($t_4 \leq t < t_5$) (**f**) *Mode 6* ($t_5 \leq t < t_6$) (**g**) *Mode* 7 ($t_6 \leq t < t_7$) (**h**) *Mode* 8 ($t_7 \leq t < t_8$) (**i**) *Mode* 9 ($t_8 \leq t < t_9$) (**j**) *Mode* 10 ($t_9 \leq t < t_{10}$) (**k**) *Mode* 11 ($t_{10} \leq t < t_{11}$) (**l**) *Mode 12* ($t_{11} \leq t < t_{12}$).

Mode 1 [$t_0 \leq t < t_1$]: Figure 8a shows the equivalent circuit of this mode. In this mode, switches S_1 and S_4 are turned on, and transformer primary side voltage v_p equals input voltage v_i. The input energy is transferred to the secondary side through switches S_1, S_4, and the transformer. The energy from the primary side is transferred to the output through

filter inductor L_1, filter capacitor C_o, and diode D_2. Thus, inductor current i_{L1} increases. In this mode, inductor current i_{L2} has to flow through filter inductor L_2 and filter capacitor C_o; therefore, diode D_1 is turned off. This mode ends when switch S_4 is turned off. The primary voltage, output current, and filter inductor currents are expressed as follows.

$$v_p = v_i, \tag{1}$$

$$i_o(t) = i_{L1}(t) + i_{L2}(t), \tag{2}$$

$$i_{L1}(t) = \frac{nv_i - v_o}{L_1}(t - t_0) + i_{L1}(t_0), \tag{3}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(\mathrm{t} - t_o) + i_{L2}(t_o). \tag{4}$$

Mode 2 [$t_1 \leq t < t_2$]: Figure 8b shows the equivalent circuit of this mode, where $C_{eq} = C_3 + C_4 = 2C_{oss}$, ($C_{oss} = C_1 = C_2 = C_3 = C_4$). At time $t = t_1$, switch S_4 is turned off, capacitor C_4 for switch S_4 is charged from 0 V to v_i, and capacitor C_3 for switch S_3 is discharged from v_i to 0 V. Capacitor voltage v_{C4} for capacitor C_4 increases linearly because the capacitances for switches S_3 and S_4 are very small. Capacitor voltages v_{C3}, v_{C4} are given as follows.

$$v_{C3}(t) = \frac{-ni_{L1}(t_1)}{2C_{oss}}(t - t_1) + v_i, \tag{5}$$

$$v_{C4}(t) = \frac{ni_{L1}(t_1)}{2C_{oss}}(t - t_1). \tag{6}$$

At time $t = t_2$, the capacitor voltage v_{C4} is equal to input voltage v_i. The transformer primary side voltage and current, secondary side voltage and current, and output current are expressed as follows.

$$v_p(t) = v_i - v_{c4}(t), \tag{7}$$

$$i_p(t) = ni_{L1}(t), \tag{8}$$

$$i_o(t) = i_{L1}(t) + i_{L2}(t), \tag{9}$$

$$i_{L1}(t) = \frac{nv_i - v_o}{L_1}(t - t_1) + i_{L1}(t_1), \tag{10}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(t - t_1) + i_{L2}(t_1). \tag{11}$$

The time interval from t_1 to t_2 is given as

$$\Delta t_{12} = \frac{v_i}{ni_{L1}(t_1)} \cdot 2C_{oss}. \tag{12}$$

The time interval Δt_{12} is very small, and the primary side current of the transformer is nearly constant because the voltage associated with the leakage inductance converges to zero.

$$v_{L_k} = L_k \times \frac{d(ni_{L1})}{dt} \approx 0. \tag{13}$$

Mode 3 [$t_2 \leq t < t_3$]: Figure 8c shows the equivalent circuit of this mode. At time $t = t_2$, capacitor C_3 is discharged to zero voltage when switch S_3 is turned on. Therefore, switch S_3 is turned on under the ZVS condition. In this mode, a delay time t_d is necessary between the turning off of switch S_4 and the turning on of switch S_3, and it has to be longer than time interval Δt_{12}. The required delay time is given as

$$t_d = \frac{v_i \cdot 4C_{oss}}{ni_{L1}(t_1)}. \tag{14}$$

In this mode, the transformer's primary and secondary side voltages of the transformer equal 0 V, i.e., $v_p = v_{s,drop} = 0$ V, $v_s = 0$ V, where ($v_{s,drop}$ = forward voltage drop of the power switch).

Both diodes D_1 and D_2 are turned on. The primary side current and secondary side current of the transformer are expressed as follows.

$$i_p(t) = \left[\frac{v_{s,drop}}{r} + i_p(t_2)\right] e^{-\frac{r}{L_k}(t-t_2)} - \frac{v_{s,drop}}{r}, \tag{15}$$

$$i_{L1}(t) = -\frac{v_o}{L_1}(t - t_2) + i_{L1}(t_2), \tag{16}$$

$$i_{L2}(t) = -\frac{v_o}{L_2}(t - t_2) + i_{L2}(t_2), \tag{17}$$

where r is the equivalent series resistor for the leakage inductor L_k. This mode is ended when switch S_1 is turned off.

Mode 4 [$t_3 \leq t < t_4$]: Figure 8d shows the equivalent circuit of this mode. At time $t = t_3$, switch S_1 is turned off because the energy stored in the leakage inductor is discharged through capacitor C_1 of switch S_1. Thus, capacitor C_1 is charged from 0 V to v_i and capacitor C_2 is discharged from v_i to 0 V. The capacitor voltages v_{C1}, v_{C2} are expressed as follows.

$$v_{C1}(t) = \frac{i_p(t_3)}{2C_{oss}}(t - t_3), \tag{18}$$

$$v_{C2}(t) = \frac{-i_p(t_3)}{2C_{oss}}(t - t_3) + v_i. \tag{19}$$

The transformer primary side voltage and current, and the secondary side voltage and current, are expressed as follows.

$$v_p(t) = -v_{C1}(t), \tag{20}$$

$$i_p(t) = \left[\frac{v_{C1}(t)}{r} + i_p(t_3)\right] e^{-\frac{r}{L_k}(t-t_3)}, \tag{21}$$

$$i_{L1}(t) = \frac{-v_o}{L_1}(t - t_3) + i_{L1}(t_3), \tag{22}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(t - t_3) + i_{L2}(t_3), \tag{23}$$

This mode is ended when capacitor voltage v_{C1} equals input voltage v_i. The time interval from t_3 to t_4 is given as

$$\Delta t_{34} = 2C_{oss} \cdot \frac{v_i}{i_p(t_3)}. \tag{24}$$

Mode 5 [$t_4 \leq t < t_5$]: Figure 8e shows the equivalent circuit of mode 5. The operation of this mode is very similar to that of mode 3, except for switch S_2 being turned on under the ZVS condition. At time $t = t_4$, capacitor C_2 is discharged to zero voltage for switch S_2 to be turned on. Therefore, switch S_2 is turned on under the ZVS condition. The transformer primary side voltage v_p equals $-v_i$ to decrease primary side current i_p. For ensuring the ZVS operation, a delay time t_d is needed between the turning off of switch S_1 and the turning on of switch S_2. The required delay time is given as

$$t_d = 2\Delta t_{34} = \frac{4C_{oss}}{n i_{L1}(t_3)}. \tag{25}$$

The voltages and currents of the transformer primary side and secondary side are expressed as follows.

$$v_p = -v_i, \tag{26}$$

$$i_p(t) = \frac{-v_i}{L_k}(t - t_4) + i_p(t_4), \tag{27}$$

$$i_{L1}(t) = -\frac{v_o}{L_1}(t - t_4) + i_{L1}(t_4), \tag{28}$$

$$i_{L2}(t) = -\frac{v_o}{L_2}(t - t_4) + i_{L2}(t_4). \tag{29}$$

This mode ends when the transformer primary side current i_p equals zero.

Mode 6 [$t_5 \leq t < t_6$]: Figure 8f shows the equivalent circuit of this mode. The operation of this mode is very similar to that of mode 5, except that the transformer primary side current i_p is negative and flows through switches S_2 and S_3. The voltages and currents of the transformer primary and secondary sides are expressed as follows.

$$v_p = -v_i, \tag{30}$$

$$i_p(t) = \frac{-v_i}{L_k}(t - t_5), \tag{31}$$

$$i_{L1}(t) = -\frac{v_o}{L_1}(t - t_5) + i_{L1}(t_5), \tag{32}$$

$$i_{L2}(t) = -\frac{v_o}{L_2}(t - t_5) + i_{L2}(t_5). \tag{33}$$

This mode ends when the transformer primary side current i_p equals ni_{L2}.

Mode 7 [$t_6 \leq t < t_7$]: Figure 8g shows the equivalent circuit of this mode. In this mode, switches S_2, S_3 are turned on and the transformer primary side voltage v_p equals $-v_i$. The input energy is transferred to the secondary side through switches S_2, S_3, and the transformer. The energy from the primary side is transferred to the output through filter inductor L_2, filter capacitor C_o, and diode D_1. In this mode, inductor current i_{L1} has to flow through filter inductor L_2 and filter capacitor C_o; therefore, diode D_2 is turned off. This mode ends when switch S_3 is turned off. The output current and filter inductor currents are expressed as follows.

$$i_o(t) = i_{L1}(t) + i_{L2}(t), \tag{34}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(\mathrm{t} - t_6) + i_{L2}(t_6). \tag{35}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(\mathrm{t} - t_6) + i_{L2}(t_6). \tag{36}$$

Mode 8 [$t_7 \leq t < t_8$]: Figure 8h shows the equivalent circuit of this mode. At $t = t_7$, switch S_3 is turned off. Capacitor C_3 for switch S_3 is charged from 0 V to v_i, and capacitor C_4 for switch S_4 is discharged from v_i to 0 V. Capacitor voltage v_{C3} for capacitor C_3 increases linearly because the capacitance of the switches S_3 and S_4 is very small. Capacitor voltages v_{C3}, v_{C4} are given as follows.

$$v_{C3}(t) = \frac{ni_{L1}(t_7)}{2C_{oss}}(t - t_7), \tag{37}$$

$$v_{C4}(t) = \frac{-ni_{L1}(t_7)}{2C_{oss}}(t - t_7) + v_i. \tag{38}$$

At time $t = t_8$, capacitor voltage v_{C3} equals input voltage v_i. The transformer primary side voltage and current, secondary side voltage and current, and output current are expressed as follows.

$$v_p = v_i - v_{C3}(t), \tag{39}$$

$$i_p(t) = ni_{L2}(t), \tag{40}$$

$$i_o(t) = i_{L1}(t) + i_{L2}(t), \tag{41}$$

$$i_{L1}(t) = \frac{nv_i - v_o}{L_1}(t - t_7) + i_{L1}(t_7), \tag{42}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(t - t_7) + i_{L2}(t_7). \tag{43}$$

The time interval from t_7 to t_8 is given as

$$\Delta t_{78} = 2C_{oss} \cdot \frac{v_i}{ni_{L2}(t_7)}. \tag{44}$$

Mode 9 [$t_8 \leq t < t_9$]: Figure 8i shows the equivalent circuit of this mode. At time $t = t_9$, capacitor C_4 for switch S_4 is discharged to zero voltage for turning on switch S_4. Therefore, switch S_4 is turned on under the ZVS condition. To ensure the ZVS operation, a delay time t_d is needed between the turning off of switch S_3 and the turning on of switch S_4, and it has to be longer than time interval Δt_{78}. The required delay time is given as

$$t_d = 2\Delta t_{78} = \frac{4C_{oss} \cdot v_i}{ni_{L2}(t_7)}. \tag{45}$$

In this mode, the transformer primary and secondary side voltages equal 0 V, i.e., $v_p = v_{s,drop} = 0$ V, $v_s = 0$ V.

Both diodes D_1 and D_2 are turned on. The primary and secondary side currents of the transformer are expressed as follows:

$$i_p(t) = \left[i_p(t_8) + \frac{v_{s,drop}}{r} \right] e^{-\frac{r}{L_k}(t - t_8)} - \frac{v_{s,drop}}{r}, \tag{46}$$

$$i_{L1}(t) = \frac{-v_o}{L_1}(t - t_8) + i_{L1}(t_8), \tag{47}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(t - t_8) + i_{L2}(t_8), \tag{48}$$

where r is the equivalent series resistor for the leakage inductor L_k. This mode ends when switch S_2 is turned off.

Mode 10 [$t_9 \leq t < t_{10}$]: Figure 8j shows the equivalent circuit of this mode. At time $t = t_9$, switch S_2 is turned off because the energy stored in the leakage inductor is discharged through capacitor C_2 of switch S_2. Thus, capacitor C_2 is charged from 0 V to v_i and capacitor C_1 is discharged from v_i to 0 V. Capacitor voltages v_{C1}, v_{C2} are expressed as

$$v_{C1}(t) = v_i - \frac{i_p(t_9)}{2C_{oss}}(t - t_9), \tag{49}$$

$$v_{C2}(t) = \frac{i_p(t_9)}{2C_{oss}}(t - t_9). \tag{50}$$

The transformer primary side voltage and current, and the secondary side voltage current, are expressed as follows.

$$v_p(t) = -v_{C2}(t), \tag{51}$$

$$i_p(t) = \left[i_p(t_9) + \frac{v_{C2}(t)}{r} \right] e^{-\frac{r}{L_k}(t - t_9)}, \tag{52}$$

$$i_{L1}(t) = \frac{-v_o}{L_1}(t - t_9) + i_{L1}(t_9), \tag{53}$$

$$i_{L2}(t) = \frac{-v_o}{L_2}(t - t_9) + i_{L2}(t_9). \tag{54}$$

This mode ends when capacitor voltage v_{C2} equals input voltage v_i. The time interval from t_9 to t_{10} is given as

$$\Delta t_{9\ 10} = 2C_{oss} \cdot \frac{v_i}{i_p(t_9)}. \tag{55}$$

Mode 11 [$t_{10} \leq t < t_{11}$]: Figure 8k shows the equivalent circuit of this mode. At time $t = t_{10}$, capacitor C_1 is discharged to zero voltage for switch S_1 to be turned on. Thus, switch S_1 is turned on under the ZVS condition. Transformer primary side voltage v_p equals v_{in} to increase primary side current i_p. To ensure the ZVS operation, a delay time t_d is needed between the turning off of switch S_2 and the turning on of switch S_1. The required delay time is expressed as follows.

$$t_d = 2\Delta t_{9\ 10} = \frac{v_i \cdot 4C_{oss}}{n i_{L2}(t_9)}. \tag{56}$$

The transformer primary side voltage and current, and the secondary side voltage and current, are expressed as follows.

$$v_p = v_i, \tag{57}$$

$$i_p(t) = \frac{v_i}{L_k}(t - t_{10}) + i_p(t_{10}), \tag{58}$$

$$i_{L1}(t) = -\frac{v_o}{L_1}(t - t_{10}) + i_{L1}(t_{10}), \tag{59}$$

$$i_{L2}(t) = -\frac{v_o}{L_2}(t - t_{10}) + i_{L2}(t_{10}). \tag{60}$$

This mode is ended when the primary side current i_p equals 0 A.

Mode 12 [$t_{11} \leq t < t_0$]: Figure 8l shows the equivalent circuit of this mode. The operation of this mode is very similar to that of mode 11, except that the transformer primary side current i_p is positive and flows through switches S_1 and S_4. This mode ends when primary side current i_p equals $-ni_{L1}$. The voltage and current of the transformer are expressed as follows.

$$v_p = v_i, \tag{61}$$

$$i_p(t) = \frac{v_i}{L_k}(t - t_{11}), \tag{62}$$

$$i_{L1}(t) = -\frac{v_o}{L_1}(t - t_{11}) + i_{L1}(t_{11}), \tag{63}$$

$$i_{L2}(t) = -\frac{v_o}{L_2}(t - t_{11}) + i_{L2}(t_{11}). \tag{64}$$

The operation of the proposed converter is analyzed through *mode 1–12*. It is confirmed that the waveforms of the primary side voltage and current in modes 1–6 are symmetrical to those in modes 7–12. In addition, by analyzing the operation, it is confirmed that one period is shaped by twelve modes and four switches are turned on and turned off under the ZVS condition.

3. Characteristics of the Proposed Converter

3.1. Voltage Gain and Effective Duty Cycle

In Figures 7 and 8, a time shift occurs between S_1 and S_3 for achieving zero voltage at time $t_2 - t_3$, $t_8 - t_9$. Moreover, based on the operation analysis in Section 2, rectification and freewheeling are performed when the two diodes are conducted during the time intervals $t_3 - t_6$ and $t_9 - t_0$.

The input energy is never transferred to the output. Therefore, the effective duty cycle is smaller than the designed duty cycle, as shown in Figure 9. The effective duty cycle is expressed as

$$D_{eff} = \frac{v_o}{nv_i} = \frac{n'^2 v_o}{v_s} \tag{65}$$

where n' is the turns ratio of the coupled inductor as the transformer.

The designed duty cycle D is expressed as

$$D = D_{eff} + D_{loss}, \tag{66}$$

where D is the duty cycle of the switch ($D < 0.5$) and D_{loss} is the duty cycle loss during the time intervals $t_3 - t_6$ and $t_9 - t_0$. The duty cycle loss has to be much smaller than the effective duty cycle and is expressed as $D_{loss} = 2f_s(t_6 - t_3) = 2f_s(t_0 - t_9)$, where f_s is the switching frequency of the switches.

The relationship curve between duty ratio D and voltage gain v_o/v_s is illustrated in Figure 10a, and the comparison curve of voltage gain between the conventional CDR and CICDR is illustrated in Figure 10b and voltage gain v_o/v_s for different values of turns ratio n; (**b**) Comparison curve between the conventional CDR and the proposed CICDR.

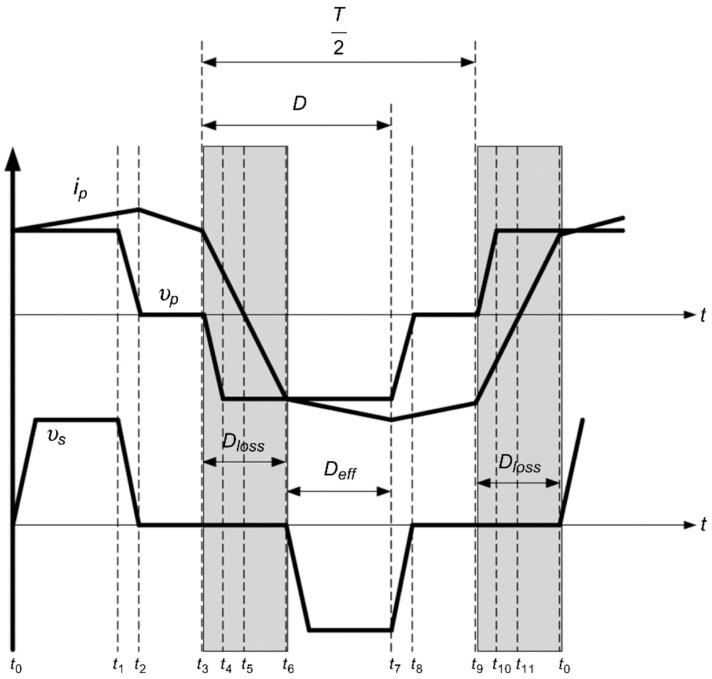

Figure 9. Key waveforms of transformer and illustration of duty cycle.

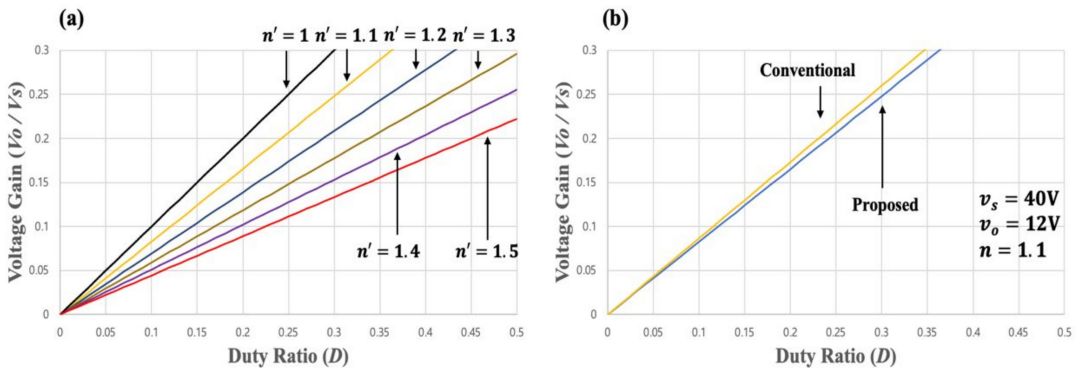

Figure 10. (**a**) Relationship curve between duty ratio D and voltage gain v_o/v_s for different values of turns ratio n; (**b**) Comparison curve between the conventional CDR and the proposed CICDR.

3.2. Voltage Stress

In modes 1 and 2, diode D_1 is in the off state, whereas diode D_2 is conducting. On the contrary, in modes 7 and 8, diode D_2 is in the off state, whereas diode D_1 is conducting. Thus, the voltage stress of the rectifier diode at the transformer secondary side can be expressed as

$$V_{D1} = V_{D2} = \frac{V_s}{n}. \tag{67}$$

For illustrating the voltage stress of the proposed converter, Figure 11 shows the relationship curve between the voltage stress and the turns ratio n.

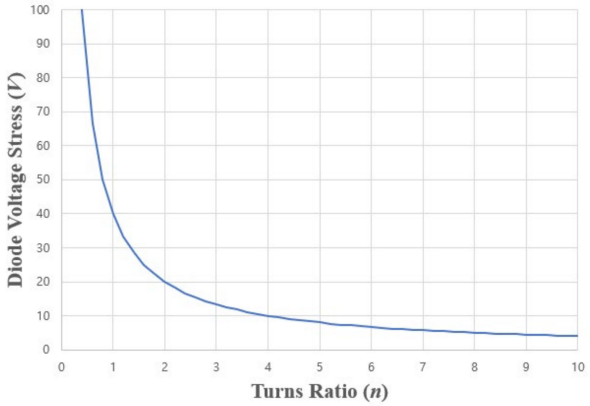

Figure 11. Relationship curve between diode voltage stress and turns ratio n.

3.3. Resonant Capacitance

The resonant capacitance depends upon the output capacitance C_{oss} of the two MOSFETs and the parasitic capacitance of the primary side, $C_{tmr,p}$, for high switching frequency f_s. Thus, the resonant capacitance is expressed as

$$C_r = 2C_{oss} + C_{tmr,p}. \tag{68}$$

In addition, the energy stored at the resonant capacitance can be expressed as

$$E_{C_r} = \frac{1}{2}\left(2C_{oss} + C_{tmr,p}\right)v_i^2. \tag{69}$$

3.4. Resonant Inductance

The leakage inductance on the primary side of the transformer functions as the resonant inductance. Resonant inductance can be determined by resonant frequency ω_r (or delay time t_d), and the resonant capacitance.

The resonant frequency, the delay time for ensuring the ZVS operation, and resonant inductance are expressed as follows.

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}, \tag{70}$$

$$t_d = \frac{\pi\sqrt{L_r C_r}}{2}, \tag{71}$$

$$L_r = \frac{1}{\omega_r^2 C_r} = \frac{1}{\left(\frac{\pi}{2t_d}\right)^2\left(2C_{oss} + C_{tmr,p}\right)}. \tag{72}$$

The energy stored in the resonant inductance is expressed as

$$E_{L_r} = \frac{1}{2}L_r i_p^2. \tag{73}$$

To ensure ZVS operation, the energy stored in the resonant inductance should be much larger than that stored in the resonant capacitance.

4. Design Considerations

To verify the proposed converter, a 600 W prototype converter with the proposed rectification method was designed and built. The hardware system parameters are as follows:

(1) Input voltage range V_i: 360–400 V;
(2) Output voltage V_o: 12 V;
(3) Rated output power P_o: 600 W;
(4) Switching frequency f_s: 100 kHz;
(5) Maximum output current I_o: 50 A;
(6) Output filter ripple voltage Δv_o: 0.12 V;
(7) Output filter ripple current Δi_L: 9 A.

4.1. Design of the Isolation Transformer

The TDK ETD 39/20/13 core with $B_{max} = 200$ mT, $A_e = 1.25$ cm^2 is used in the isolation transformer for minimizing the core loss. In addition, the maximum duty cycle is 0.4 for maximum efficiency. By Faraday's law, the transformer primary winding is determined as

$$N_p = \frac{v_{i(\min)} D_{max}}{B_{max} A_e f_s} = 46.08. \tag{74}$$

Thus, 46 turns are chosen for this design. Therefore, the secondary side voltage and number of winding turns are determined as follows.

$$V_s = \frac{V_o}{n} = \frac{n\prime^2 V_o}{D} = 40 \text{ V}, \tag{75}$$

$$N_s = N_p \frac{V_s}{V_{p(\min)}} = 4. \tag{76}$$

From Equations (74)–(76), the magnetizing inductance is calculated as

$$L_m = v_{i(min)} \frac{\Delta t}{\Delta i_L \frac{N_s}{N_P}} = 192 \text{ μH}. \tag{77}$$

4.2. Selection of the Filter Coupled Inductors and Capacitor

For lower leakage inductance, lower power loss, and high step-down voltage gain, the turns ratio n' is determined as 1.15. Thus, filter-coupled inductance $L = L_1 = L_2$ is calculated as

$$L = L_1 = L_2 = \frac{D(v_s - v_o)}{\Delta i_L f_s} = 8 \text{ μH}. \tag{78}$$

The filter capacitance is usually related to output ripple voltage Δv_o, which has to be less than 1% of rated output voltage V_o.

Thus, filter capacitance is calculated as

$$C_o = \frac{I_o D_{max}}{0.01 V_o f_s} = 1680 \text{ μF}. \tag{79}$$

4.3. Selection of the Rectifier Diodes and Power Switches

When rectifier diodes D_1 or D_2 are conducting, the maximum current flowing through the diode is $I_{o(max)} = i_{D(max)} = 50$ A. Therefore, Vishay V60100C Dual High-Voltage Trench is used in this design.

In addition, Vishay IRFP460A MOSFETs with output parasitic capacitance $C_{oss} = 870$ pF are used as the active power switches for this design. Therefore, the resonant

capacitance is approximated as 3.5 nF. Based on Equations (70) and (72), the resonant inductor L_r is approximately 5.5 μH.

5. Experimental Verification

Based on the design considerations, a 600 W laboratory prototype of the proposed converter, shown in Figure 12, was manufactured for verifying the theoretical analysis and effectiveness of the converter. Additionally, Figure 13 shows the designed block diagram of the proposed converter. A digital signal processing (DSP) controller was used to generate the PWM for a MOSFET gate. The DSP control was realized using the TMS320F28335 chip, which has a C28X Core 32-bit FPU and is capable of high-speed processing of decimal data with a processing capability of 150 MHz. Additionally, the ADC circuit was capable of sampling at 12.5 MSPS with 16 channels, and the analog input signal range was 0 to 3 V.

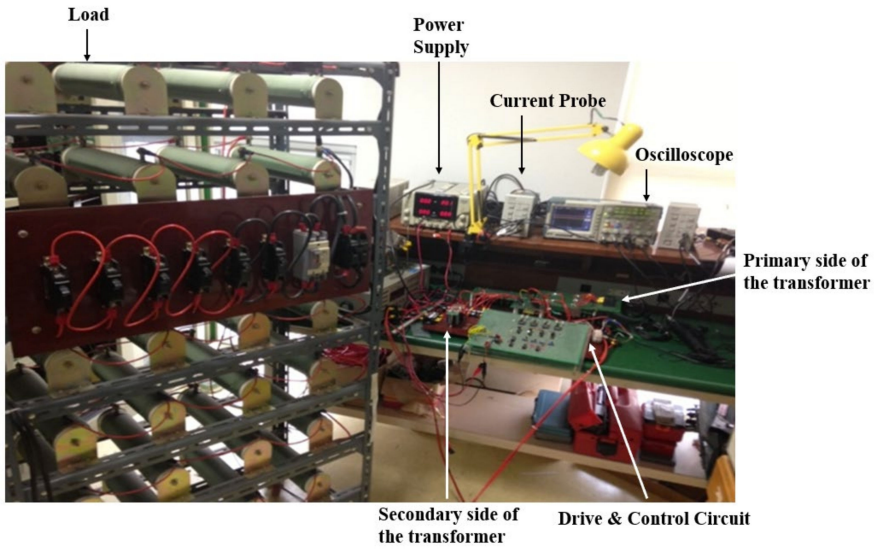

Figure 12. Laboratory prototype (600 W) of the proposed converter.

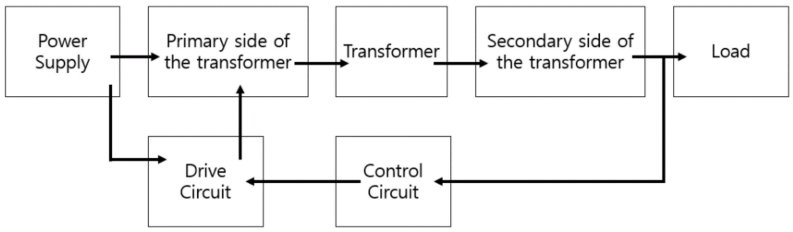

Figure 13. The designed block diagram of the proposed converter.

Figure 14 shows gate-source voltage v_{GS} waveforms of switches S_1, S_2, S_3, and S_4. Based on the design considerations, four switches were shifted to control the power transferred from the primary side of the transformer to the secondary side. Figure 15a shows the voltage and current waveforms of switch S_1 under the half-load condition. The measured voltage and current waveforms of switch S_2 under the full-load condition are shown in Figure 15b. Operation of the switches under the ZVS condition is verified through Figure 15c. In addition, Figure 16a,b shows the primary side voltage and current of the transformer under the half- and full-load conditions, respectively. The current waveforms of the filter inductor with CICDR for the half- and full-load conditions are shown in Figure 17a,b. The fact that CDR is suitable for high output current has already been verified through various experiments conducted in recent years. Figure 18 shows the calculated efficiency of the proposed converter, along with the input power and output power under various load conditions.

The efficiencies of various conventional converters are shown in Figure 15. A comparison with conventional converters such as hard switching, center-tapped, and CDR shows that the proposed converter with CICDR is much better than those with low-voltage and high current, and it has a lower loss.

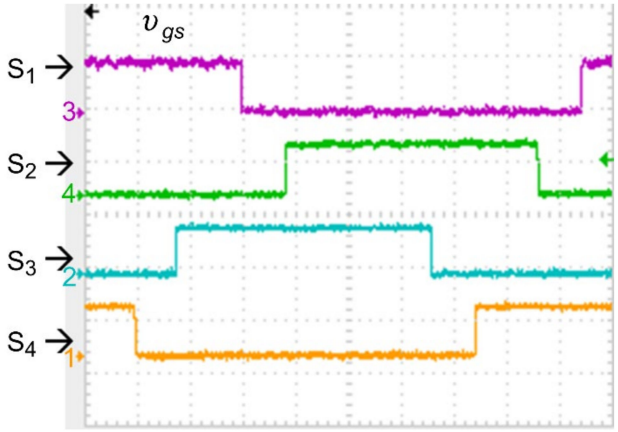

Figure 14. Waveforms of gate-source voltage, v_{GS}, of the switch.

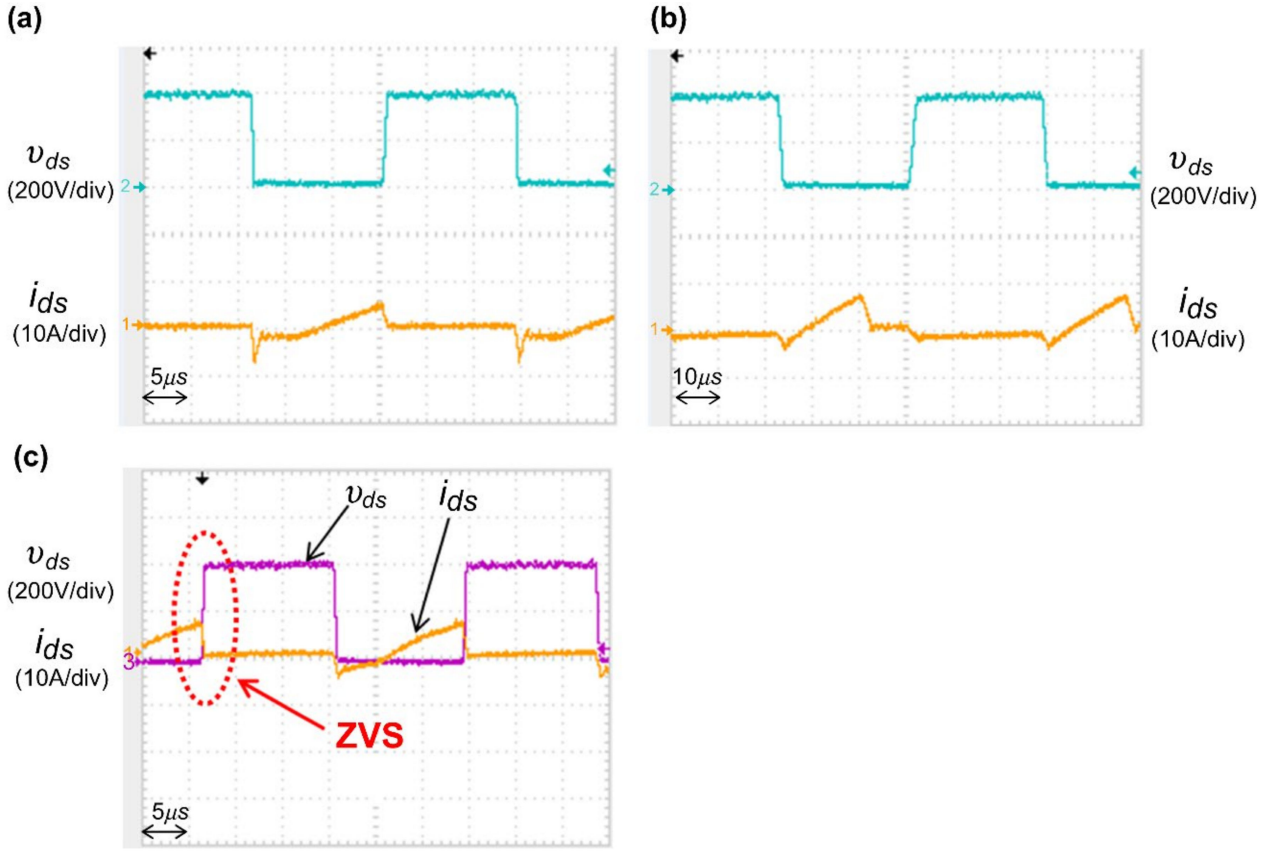

Figure 15. Waveforms of drain-source voltage and current, v_{GS}, i_{ds}, of switch S_1: (**a**) half-load condition; (**b**) full-load condition; (**c**) ZVS operation.

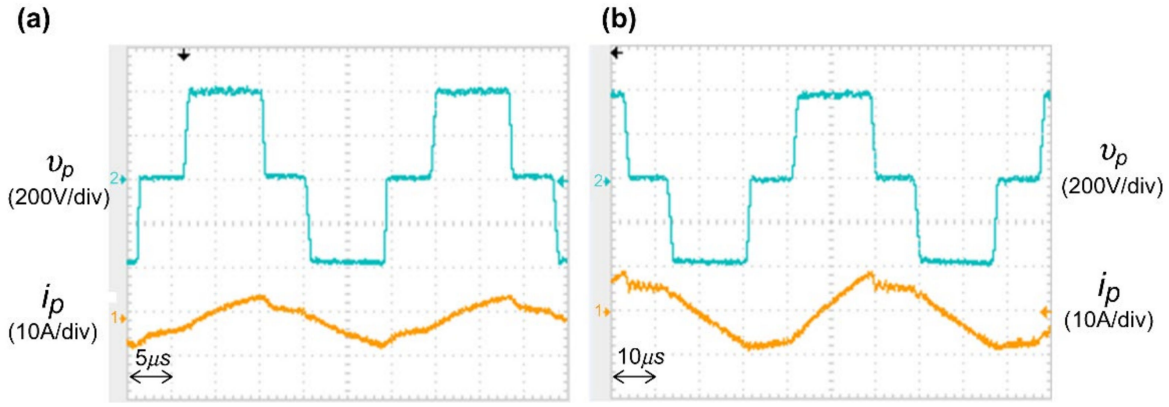

Figure 16. Waveforms of the primary side voltage and currents, v_p, i_p, of the transformer: (**a**) half-load condition; (**b**) full-load condition.

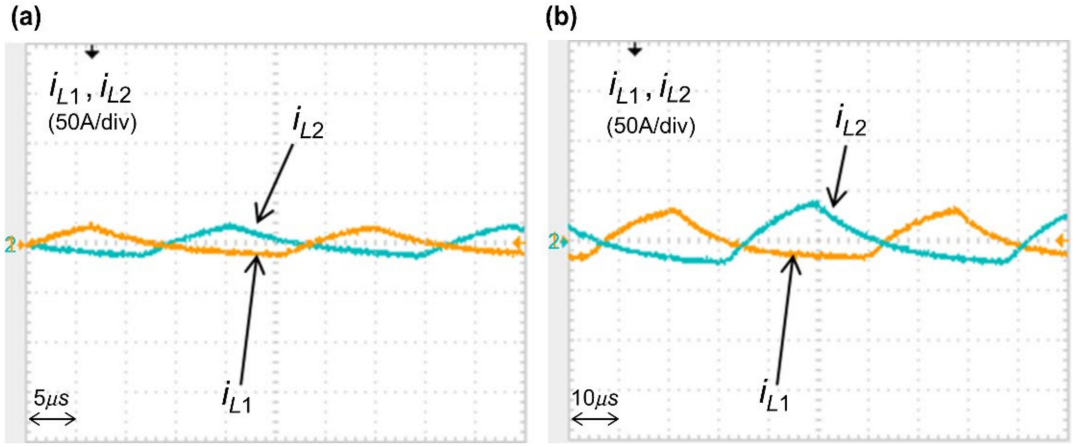

Figure 17. Waveforms of the primary side voltage and currents, v_p, i_p, of the transformer: (**a**) half-load condition; (**b**) full-load condition.

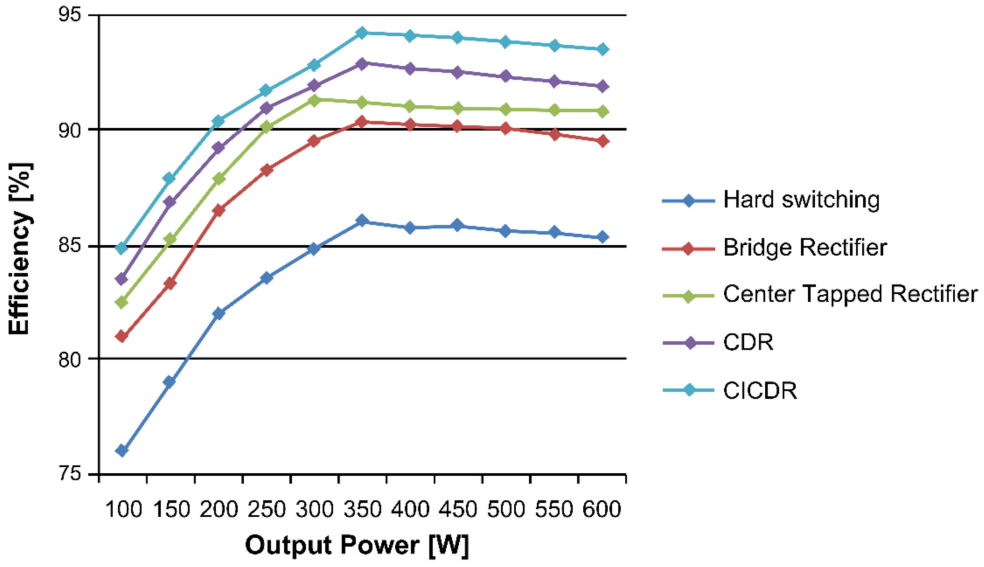

Figure 18. Efficiency comparison between proposed converter and conventional converters.

6. Conclusions

In this paper, an improved high step-down DC-DC converter with CICDR for EVs has been proposed. Its topology is based on the conventional phase-shift full-bridge converter. In addition, the proposed converter achieves high efficiency based on the soft-switching technique with the phase-shifting technique. Furthermore, a current-doubler rectifier with a coupled inductor is adopted to reduce various losses, extend the duty range, and ensure ZVS operation and high efficiency. The effectiveness and validity of the proposed converter for low-voltage battery charging in EVs was experimentally verified. The experimental results showed that the proposed converter with CICDR can achieve high efficiency under various load conditions when compared with the conventional converter. The characteristics of the proposed converter are summarized as follows:

1. The CICDR rectification method can achieve high output current and high step-down voltage gain for EVs;
2. The voltage stress of the rectifier diode is low. Consequently, the losses of the rectifier diode can be reduced and high efficiency can be obtained;
3. The leakage energy can turn on the switch under the ZVS condition. This reduces conduction loss and improves efficiency.

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